Active Electrode IC for EEG and Electrical Impedance Tomography with Continuous monitoring of contact impedance

Active Electrode IC for EEG and Electrical Impedance Tomography with Continuous Monitoring of Contact Impedance

Marco Guermandi, Roberto Cardu, Eleonora Franchi Scarselli, *Member, IEEE*, and Roberto Guerrieri, *Member, IEEE*

***Abstract*—The IC presented integrates the front-end for EEG and Electrical Impedance Tomography (EIT) acquisition on the electrode, together with electrode-skin contact impedance monitoring and EIT current generation, so as to improve signal quality and integration of the two techniques for brain imaging applications. The electrode size is less than 2 cm^2 and only 4 wires connect the electrode to the back-end. The readout circuit is based on a Differential Difference Amplifier and performs single-ended amplification and frequency division multiplexing of the three signals that are sent to the back-end on a single wire which also provides power supply. Since the system's CMRR is a function of each electrode's gain accuracy, an analysis is performed on how this is influenced by mismatches in passive and active components. The circuit is fabricated in 0.35 μm CMOS process and occupies 4 mm^2, the readout circuit consumes 360 μW, the input referred noise for bipolar EEG signal acquisition is 0.56 μV_{RMS} between 0.5 and 100 Hz and almost halves if only EEG signal is acquired.**

I. Introduction

Neuroimaging is a discipline which deals with the ability to image the structure and/or functionality of the central nervous system (CNS). Among the techniques currently used to provide functional maps of CNS activity in clinical practice or at research level we may mention Positron Emission Tomography (PET), Functional Magnetic Resonance Imaging (fMRI) [1], Electro- and Magneto-Encephalography (EEG and MEG) [2] and Diffuse Optical Tomography (DOT, also known as NIRS) [3]. The first two techniques provide the highest level of spatial accuracy at the price of rather low temporal resolution (one scan every few seconds). Moreover, the expensive and voluminous hardware limits use of them to hospital settings while patient discomfort hampers several possible applications, for example in sleep research or epileptic focus localization which require long-term monitoring. By contrast, the other techniques trade spatial accuracy for compactness, movability and ease of use. In particular, the localization of EEG signal sources is a fairly well established method of providing functional maps of brain activity [2] and one which guarantees good levels of portability and comfort for the patient. It is true that EEG source localization suffers from a lower spatial resolution than fMRI and PET; however images can be acquired at a much higher sampling rate, allowing analysis of phenomena occurring at time intervals of fractions of seconds. A diagnostic system based on EEG source localization could therefore be ideal for settings such as doctors' surgeries, the home or ambulances, provided an improvement in spatial accuracy can be achieved. Since EEG source localization relies on the ability to reconstruct current dipole locations inside the patient's head volume by measuring the voltages generated on its surface, a high density system is required so as to optimize the localization accuracy [4]. EEG source localization algorithms rely heavily on the availability of an accurate, patient-specific head model able to describe the electrical behavior of the domain [5]. To this end, if one could obtain structural information, say, from a one-off MRI scan, that would significantly increase the reconstruction quality. However this would still not provide direct information about the conductivity of the various tissues or regions which are in practice commonly guessed by simply assigning a single, time-invariant conductivity value to each of the few tissues into which the head volume is usually segmented. To overcome these limitations, it has been proposed that local, time-dependent conductivity information be provided by Electrical Impedance Tomography (EIT) [6][7] a relatively new imaging technique which allows one to estimate the conductivity distribution inside a body by injecting small AC currents at frequencies ranging from a few KHz to a few MHz on the surface and measuring the resulting voltage on the same surface. Applications range from lung monitoring [8] to personalized monitoring systems [9]. Although this is not the designed target application for the ASIC presented, EIT is allegedly able to directly image brain activity by measuring conductivity variations in cerebral regions due, for example, to modifications in blood perfusion, akin to the BOLD signal detected by fMRI [10]. Recently, ASICs have been specifically designed for EIT measurements [8][11] but not for being directly integrated on the electrode.

A common source of EEG signal quality degradation is the contact impedance which exists at the interface between the electrode metal surface and the patient's skin. A high value of contact impedance leads to a potential divider effect at the input of the remote amplifier which causes a reduction in CMRR; it also increases the noise generated at the metal-skin interface and augments the effect of interference coupling through capacitive effects to the cables, or artifacts due to cable movement, microphony and the piezoelectric effect [12].

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This can be particularly troublesome when performing an EEG on an epileptic patient since artifacts can be incorrectly interpreted as seizures. Contact impedance is minimized in clinical EEG protocols by removing superficial skin layers by abrasion and inserting a conductive gel or paste in-between the two surfaces. Extensive skin preparation is not suitable for high density systems and out-of-hospital settings in view of the long preparation time, infection risks and significant level of training required by the person placing the electrodes [13].

This paper presents an IC enabling one to integrate the

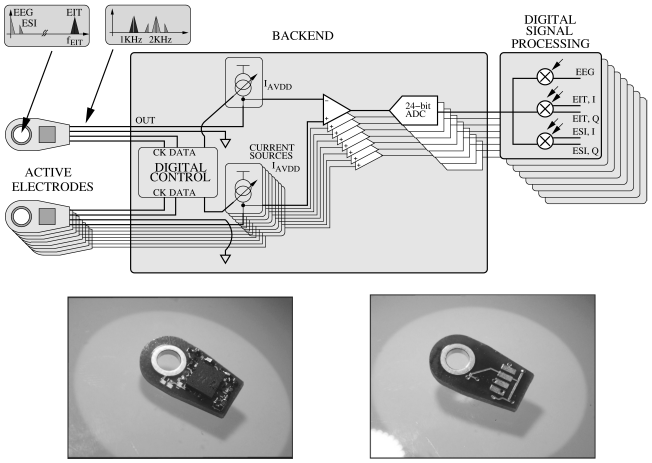


Fig. 1. On the top, the test system for the active-electrode characterization. On the bottom, pictures of the top and bottom side of the electrode before cable soldering and sealing with resin.

front-end for EEG and EIT acquisition on the electrode, together with electrode-skin contact impedance monitoring (ESI) and EIT current generation. The main purpose is to provide a system which enables the user to gather conductivity information on the head tissues from EIT measurements, so as to improve EEG source localization. The IC is designed to acquire EEG and EIT signals (plus the electrode contact impedance) at the same time so as to have the best possible integration between the two techniques. This overcomes the common limitations associated with using two separate systems for EEG and EIT. It directly performs signal preconditioning on the electrode, much like active-electrodes reported in the literature [14][15] which improve EEG signal extraction quality by placing a high input impedance, low output impedance and low noise amplifier directly on the electrode, so as to be less prone to issues originating from contact impedance. The active-electrode is also designed to down-convert the EIT output voltage to a lower frequency, so as to relax back-end bandwidth specifications, and synthesize EIT input current. Another design feature is the ability to continuously monitor ESI, which can provide information on the signal quality and a possible need to replace or reposition an electrode [16][17]. The active-electrode area is small enough to be compatible with high-density integration; moreover, since EEG, EIT and ESI signals share the same output line, the wire number is minimized and only one acquisition channel is required by each electrode. A different implementation of this active-electrode able to jointly extract EEG, EIT and ESI was presented in [16]. As compared to that, the present solution improves performance by reducing power consumption by a factor of almost three, whilst still achieving lower noise. This is obtained thanks to a different architecture in the readout circuit which is now based on a single Differential Difference Amplifier (DDA) rather than three operational amplifiers. Moreover, the digital interface is extended so that an EIT current waveform is obtained by direct synthesis, storing the 8-bit waveform samples in an on-chip memory, which gives a much larger degree of freedom in choosing EIT current waveforms than with square wave alone. To our knowledge, this work and [16] are the first and only attempts to integrate EEG, EIT and ESI on an active-electrode. An overview of the active-electrodes and of the full system in which they are integrated is presented in Section II; Section III presents the integrated circuit and the single blocks composing it; while Section IV shows measurement results, both from an electrical characterization stand-point and from some simple functional testing in acquisition of EEG, EIT and contact impedance. Conclusions are drawn in Section V.

II. An EEG system based on active-electrodes

In order to understand the design requirements for the active-electrodes, the test system developed for electrode characterization is introduced in Fig. 1. Each active-electrode can be configured at any time between i) EEG/ESI readout, ii) EIT potential and EEG/ESI readout and iii) EIT current injection.

A. Active-electrode specifications and characteristics

Specifications for EEG signal quality are derived from the International Federation of Clinical Neurophysiology (IFCN)'s standards which are commonly adopted in clinical practice [18]. Preamplifier input impedances should be higher than 100 MΩ, the Common Mode Rejection Ratio (CMRR) of the system must be at least 110 dB and additional noise introduced in the recording should be less than 0.5 μV root-mean-square at any frequency from 0.5 to 100 Hz including 50$-$60 Hz.
Unlike EEG, EIT is currently not included in standard clinical practice and is only being used in research settings, so no widely accepted standard exists to define the minimum requirements in terms of signal quality. Concerning maximum noise value, the choice was to adopt the same level as for EEG signals. The maximum instantaneous value of EIT injected current was deliberately limited to 127 μA. This value is well within the limits prescribed by IEC-60601 technical standards for medical electrical equipment since injected current frequency is limited to values higher than 16 KHz [19]. Common mode rejection of an EIT system is not required to remove interference coupling from the mains as happens with EEG signal acquisition, but mainly to prevent the measurement from being affected by the common mode signal introduced by the voltage drop which may be caused by unmatched EIT currents flowing to ground [20]. In general, values in the order of 60 to 70 dB are commonly found in systems reported in the literature [21] and are therefore used as the specification. Common injection frequencies for EIT range from a few KHz to MHz [6][21]. In this system, the maximum

injection frequency is limited to 256 KHz, since working at higher frequency generally requires extensive and continuous calibration to compensate for different behavior among the full set of electrodes. This is unrealistic in a system which is designed to be easy to use and set up.

In order to support high-density system integration, the electrode PCB (see the pictures in Fig. 1) occupies less than 2 cm^2 and places the IC on the top side together with a few external components; soldered onto the bottom side are the wires connecting the electrode to the back-end. Both sides are then covered with resin in order to seal the electronics. The PCB has a 5 mm diameter hole whose walls are gold-plated; this is used for direct contact with the patient's skin, achieved by placing the PCB on the scalp and filling the hole with conductive gel. This electrode size allows for a high-density system with up to 300 channels approx. for an average-size head. For such a high number of channels, cable lightness and compactness are of major importance; hence, the number of signals needed to connect each electrode to the back-end was minimized to 4, namely the output signal (OUT), ground and two digital programming signals (CK, DATA). The electrode is connected to the back-end by means of a 1 m four-core cable terminating in a four-pole touch-proof connector.

A dedicated power line is not foreseen; the power supply for the analog part is provided by the output line itself, which is DC biased by a programmable external current source whose value can be increased when the electrode is acting as an EIT current source in order to provide this additional current only when requested. The output line is shared among EEG, EIT and ESI signals by placing them at different frequency bands. It should be noted that none of the three signals is transferred at baseband. The first reason for this is that in this way most noise and interference which can couple to the ground and output signal through the cables (e.g. 50-60 Hz network interference) do not affect the readout voltages. Moreover, every signal is located above the flicker noise corner frequency of the circuits on the electrode and at the back-end, somewhat as is done in standard chopper amplifiers [15], where the best trade-off between noise and power consumption can be obtained. A third reason relates to the gain accuracy and CMRR and will become clear in Sec. II-B.

Each electrode performs single-ended amplification. This is desirable since it avoids sending back the reference signal to each electrode, which would lead to an increased number of wires. The difference between each signal and the reference one is performed at the back-end. The main drawback of this solution is the limit it poses on the CMRR of the system, which is limited by the mismatch between the single-ended gains of the two electrodes' ICs, as discussed in Sec.II-B. The final down-conversion to baseband (with quadrature signals for ESI and EIT) and separation of the three signals is not performed until after analog-to-digital-conversion, so as to relax noise level specifications at the back-end as well.

B. Common Mode Rejection Ratio analysis for single-ended amplification

Referring to Fig. 2, let us consider two active-electrodes based on a non-inverting integrated amplifier in which, to obtain the highest achievable gain accuracy and avoid complex and expensive trimming procedures, the gain value is fixed by a capacitance ratio ($G = 1 + C_1/C_2$). Resistor R is inserted only for DC biasing of the inverting node and its effect may be considered negligible at the frequency in question. The difference of the two output signals will be:

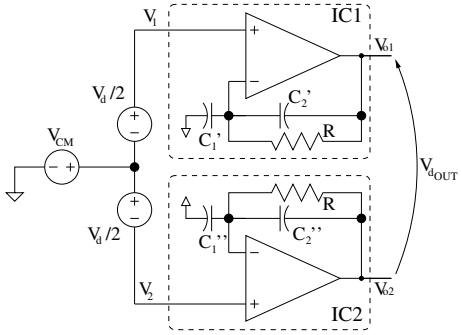


Fig. 2. Sample circuit for computing CMRR reduction due to mismatches in the gain of the amplifiers of two active-electrodes ($G_1 = 1 + C_1'/C_2'$ and $G_2 = 1 + C_1''/C_2''$).

$$V_{d_{OUT}} = \frac{G_1 + G_2}{2} \cdot V_d + (G_1 - G_2) \cdot V_{CM} = G_D \cdot V_d + G_{CM} \cdot V_{CM} \tag{1}$$

which gives a CMRR of

$$CMRR = \frac{G_D}{G_{CM}} = \frac{G_1 + G_2}{2 \cdot (G_1 - G_2)} \tag{2}$$

hence limited by the mismatch between gains G_1 and G_2 of the two amplifiers. The main sources of gain mismatch are the limited gain of the OpAmp and the mismatch in active and passive components within the same IC [22].

We now focus on mismatches on capacitors, while other causes will be discussed in Sec. III-B once the active element topology is introduced. A simple model for integrated capacitors describes the standard deviation σ of the ratio between the capacitance mismatch ΔC and its desired value C as

$$\sigma\left(\frac{\Delta C}{C}\right) \approx \frac{A_c}{\sqrt{WL}} = \frac{\epsilon_c}{\sqrt{C}} \tag{3}$$

where $\epsilon_c = A_c \cdot \sqrt{C_a}$ is a process-dependent parameter (it can be roughly estimated to be in the range of 10^{-10} for the process used) and C_a the capacitance per unit area. The worst case scenario for the mismatch between the gain of two different ICs G_1 and G_2 will be:

$$\begin{aligned} G_1 &= 1 + \frac{C_1 - \Delta C_1}{C_2 + \Delta C_2} \\ G_2 &= 1 + \frac{C_1 + \Delta C_1}{C_2 - \Delta C_2} \end{aligned} \tag{4}$$

where ΔC_1 and ΔC_2 are the absolute value of the maximum deviation which is expected on capacitance values C_1 and C_2. Common mode and differential gain will therefore be given by:

$$\begin{aligned} G_{CM} &= 2\frac{C_2 \Delta C_1 + C_1 \Delta C_2}{C_2^2 - \Delta C_2^2} \\ G_D &= 1 + \frac{C_2 C_1 + \Delta C_2 \Delta C_1}{C_2^2 - \Delta C_2^2} \end{aligned} \tag{5}$$

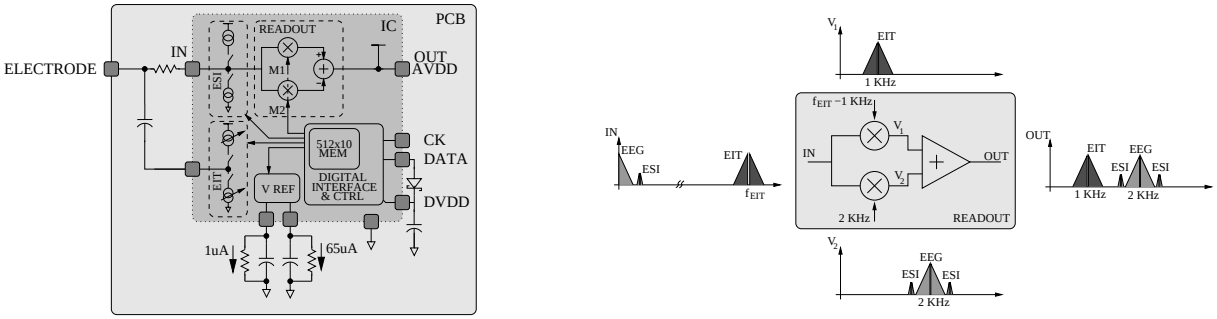


Fig. 3. On the left, scheme of the active-electrode's IC and PCB. On the right, frequency plan for multiplexing the three signals on the same output line.

The CMRR will be:

$$\begin{aligned} CMRR &= \frac{C_1C_2+\Delta C_1\Delta C_2+C_2^2-\Delta C_2^2}{2\cdot(C_2\Delta C_1+C_1\Delta C_2)} \\ &\approx \frac{C_2C_1+C_2^2}{2\cdot(C_2\Delta C_1+C_1\Delta C_2)} \end{aligned} \quad (6)$$

having assumed that $C_{1,2} >> \Delta C_{1,2}$. Now, substituting $C_1 = (G-1)\cdot C_2$ and considering a $\pm 3\sigma$ deviation for the capacitance values which, from (3), gives $\Delta C_2 = 3\epsilon_c\sqrt{C_2}$ and $\Delta C_1 = 3\epsilon_c\sqrt{(G-1)\cdot C_2}$, one gets

$$\begin{aligned} CMRR &= \frac{\sqrt{C_2}}{6\epsilon_c}\cdot\frac{G}{G-1+\sqrt{(G-1)}} \\ &= \frac{\sqrt{C_T}}{6\epsilon_c}\cdot\frac{\sqrt{G}}{G-1+\sqrt{(G-1)}} \end{aligned} \quad (7)$$

where, since capacitance size is generally limited by area occupation constraints, the CMRR is expressed as a function of the total capacitance $C_T = C_1 + C_2 = G\cdot C_2$.

From (7), one can observe how the CMRR is not only affected by process-dependent parameter ϵ_c and the sizing of capacitances C_T, but also decreases as the differential gain increases. For the standard CMOS 0.35μm process used in this design, a reasonable area occupation in the order of 0.5 mm^2 for the passive components yields a total capacitance value of about 200 pF. Limiting the differential gain to a value of 10, the maximum achievable CMRR is computed from (7) to be about 70 dB. One additional reason for limiting the differential gain is that the addition of the EIT signal on each electrode easily leads to high amplitude signals up to some tens of mV on the electrodes near those injecting currents. Moreover, it should be pointed out that single-ended amplification is prone to reduction in CMRR performance due to non-linear behavior which might arise for large output swings. IFCN standards prescribe a CMRR of at least 110 dB for the acquisition of an EEG signal. Driven Right Leg (DRL) loops are commonly used in EEG systems [12][23] in order to increase the CMRR by 30 to 40 dB and can be implemented to satisfy the specification. It should be pointed out that, since the DRL loop bandwidth needs to be limited to a few hundred Hz so as to guarantee stability, it does not increase the CMRR at EIT frequencies.

When using capacitive passives to set the gain of the amplifier, one should bear in mind that an additional resistive path needs to be added in parallel in order to set the DC voltage of internal nodes (resistor R in Fig. 2). In high-CMRR differential amplifiers for neural recording applications [15][16][24] it is common to substitute standard resistors by so-called MOS-bipolar pseudoresistor elements which, for small voltages across the device, can achieve an incremental resistance in excess of 10^{10} Ω. This value would not be high enough to guarantee the required gain accuracy and CMRR at the lowest limit of the standard EEG band (0.5 Hz), while it is sufficient in the frequency bands where EEG signals are up-converted and EIT signals down-converted prior to amplification.

III. The active-electrode IC

A. Architecture

The main blocks composing the active-electrode's IC are shown in Fig. 3 while table III-A summarizes some main characteristics of IC programming in the different working modalities. A current limiting resistor is placed on the input signal path to guarantee patient safety. For the same reason, but in order to allow a higher AC current value for EIT injection, the EIT current source is connected to the electrode through a de-coupling capacitor. The input stage of the readout section consists of two input mixers. In normal operation, the mixers run at f_{EIT} - 1 KHz and 2 KHz for respectively down-converting the EIT signal around 1 KHz and up-converting the EEG signal. The two signals are then subtracted by a differential amplifier based on a DDA. If only the EEG signal is required, the mixers are driven in counter-phase by 1 KHz square wave. Since the EEG signal already drops below system noise level at frequencies higher than a few hundred Hz and EIT is a slowly modulated signal related to either the head structure or the metabolism, there is no risk of the two signals overlapping in normal conditions. High-frequency content in EEG signals might be associated with large artifacts due to electrode movement which can lead to overlapping. However, it should be noted that EIT is by itself very sensitive to this sort of artifact [6] which should in any case be minimized.

The digital portion of the IC is mainly comprised of an input interface which acquires programming data from the back-end, some registers for storing configuration bits and a 512x10 bit Sequential Access Memory (SAM), which stores the samples for direct synthesis of the EIT current waveform (8 bit digital word) plus digital signals M1 and M2 which control the mixers for input signal down- and up-conversion. The memory can be read at a frequency ranging from 2 KHz (if only the EEG signal is acquired and the highest frequency signals required are M1 and M2 which are 1 KHz square wave) to 512 KHz

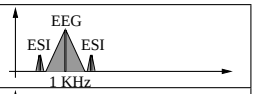
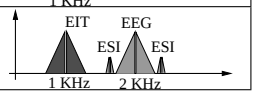
Config	f_{CK}	f_{M1}	f_{M2}	f_{EIT} (inj. current)	I_{AVDD}	OUT Spectrum
EEG Readout	2 KHz	1 KHz	1 KHz	-	120 μA	
EEG+EIT Readout	32 to 512 KHz	f_{EIT} - 1 KHz	2 KHz	-	120 μA	
EIT Injection	32 to 512 KHz	-	-	16 KHz to $f_{CK}/2$	380 μA	

TABLE I
SUMMARY OF IC'S MAIN CHARACTERISTICS FOR DIFFERENT CONFIGURATIONS

(memory cycled every 1 ms). In order to minimize coupling of digital noise to the analog circuits, digital power is separated from the analog power supply and is derived from rectification of the DATA signal by means of a low-threshold (30 mV) Shottky diode and a 1 nF capacitance. An internal bandgap reference voltage provides the required reference currents. Two different bias currents are foreseen; a 1 μA current which is used as the reference current for the analog readout circuit and a higher accuracy 65 μA branch which is turned on only when the electrode is acting as an EIT current source.

Electrode-Skin contact impedance monitoring is performed

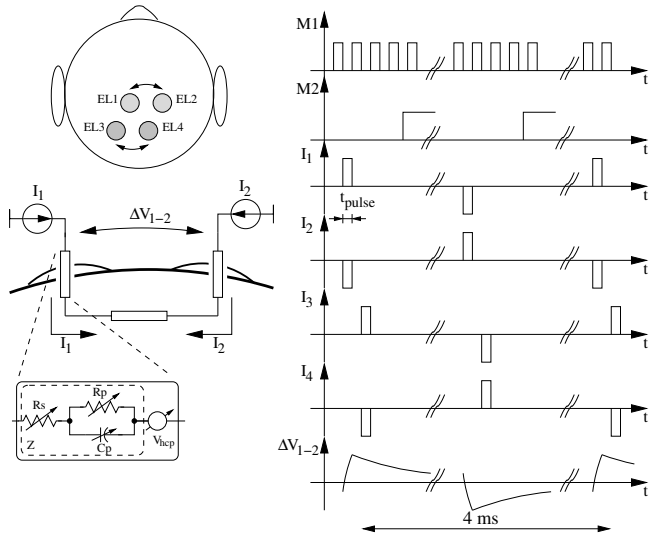


Fig. 4. Working principle, circuit model and timing of electrode-skin contact impedance measurement. Current sources are only turned on when the input is disconnected from the DDA by the input mixers.

at the same time as the EEG/EIT readout and simultaneously on all electrodes. The monitoring is based on injecting a very small AC test current between adjacent electrodes and measuring the differential voltage at the injection frequency across the two electrodes (see Fig. 4). This will be given by the sum of the two contact impedances plus the contribution of tissue impedance. The default value of the injection frequency is chosen to be 250 Hz, which is close to the EEG frequency range in order to have a good estimate for its low frequency value without overlapping the EEG signal. Test current is injected in small pulses of 1 μA with a very low duty-cycle and only when both signals controlling the input mixers (M1 and M2) are set to zero, so that the electrode is disconnected from the readout circuit. This happens for one fourth of the time due to the 50% duty-cycle of M1 and M2 and does not require modification in the readout circuit behavior. Nevertheless, since the electrode-skin contact impedance has a significant reactive component at 250 Hz, the differential signal ΔV_{1-2} generated by the current injection is still up-converted to around 2 KHz by M2, together with the baseband EEG signal. Higher-order harmonics of the differential signal are markedly attenuated before being up-converted in their turn. The shape of the injected current is chosen for two reasons. The first is to minimize the effect of current injection on the readout of EIT and EEG signals. The second is that, since at the injection frequency the tissue's electrical behavior is generally resistive rather than reactive [26], the portion of the voltage drop associated with tissue impedance is not up-converted. This is especially important when simultaneously scanning a high number of electrodes since, even though tissue impedance is generally at least two orders of magnitude lower than contact impedance, the aggregate effect of multiple injections on every electrode could easily affect the contact impedance measurement.

B. Readout section circuit design

The readout section is based on a DDA (see Fig. 5), which was first introduced in [27]. It is basically an extension of a standard operational amplifier with two differential inputs. Using this block to design an instrumentation amplifier allows both inputs to show a high-impedance, without the need for either two additional buffers at the inputs (such as in [16]) or three-OpAmp structures. In what follows, since we are interested in having a good closed loop gain accuracy to match CMRR specifications (see (2)), we will perform a gain variation analysis due to parasitic capacitances and process mismatches. Characterization of the block in terms of noise, DC gain and frequency behavior can be readily derived from that of the OpAmp topology on which it is based, so it will not be carried out here.

Going on to consider parasitic capacitances and assuming an infinite gain for the DDA, the ratio between output and input differential voltage for the AC coupled differential amplifier shown in Fig. 5(b) will be:

$$\frac{v_o}{v_1 - v_2} = \left[1 + \frac{C_1 + \alpha \cdot (C_1 + C_2) + C_{in}}{C_2}\right] \cdot \frac{C_0}{C_0(1+\alpha) + C_{in}} \tag{8}$$

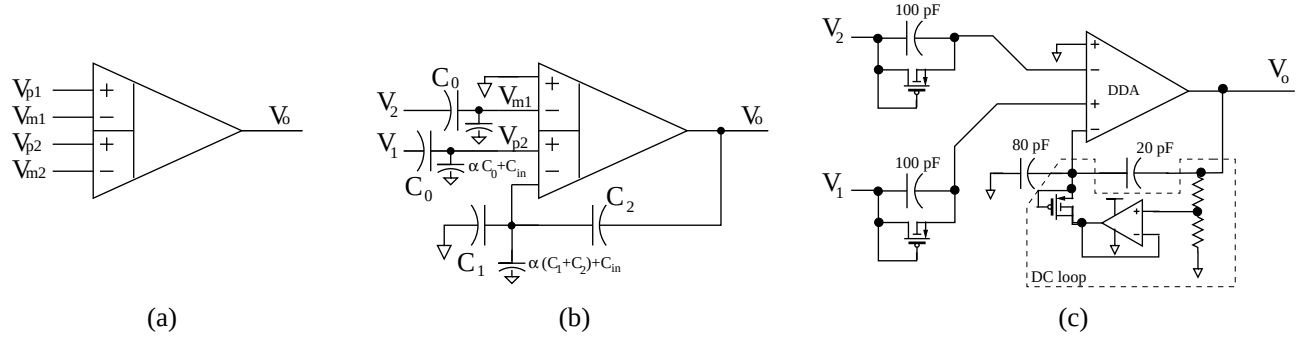


Fig. 5. (a) DDA symbol and (b) differential amplifier based on DDA. Capacitance C_0 is added to cancel parasitic effects at DDA input nodes. (c) Implementation of the differential amplifier in the active-electrode's IC.

where α is the ratio between the parasitic capacitance associated with the top-plate of each capacitor and the capacitance itself, while C_{in} is the input capacitance of the DDA. Neglecting non-idealities ($\alpha = 0$, $C_{in} = 0$), the equation reduces to $\frac{v_o}{v_1 - v_2} = 1 + \frac{C_1}{C_2}$ which is the same as for a non-inverting configuration of a standard operational amplifier. From (8), it can easily be seen that the deviation of gain from the expected value due to parasitic effects is canceled when $C_0 = C_1 + C_2$. Based on (7), which is still valid even if the OpAmp is substituted by a DDA, the gain of the differential amplifier has been limited to 5, with capacitance values of $C_1 = 80$ pF, $C_2 = 20$ pF and $C_0 = 100$ pF, targeting a CMRR of at least 70 dB. This leads to a conversion gain from the electrode to the IC ouput of $10/\pi$. This value is high enough to significantly relax the trade off between noise and power in the following stages in the back-end. We can consider the overall noise in EEG acquisition to be due to the sum of that of two active-electrodes ($v_{n,AE}$) plus that of the differential amplifier in the back-end ($v_{n,BE}$, see Fig. 1), namely $v_n = \sqrt{2 \cdot v_{n,AE}^2 + (\pi/10 \cdot v_{n,BE})^2}$. The overall noise budget is $0.5\mu V_{RMS}$; if we allow the differential amplifier to have an input-referred noise of up to $0.5\mu V_{RMS}$, the input-referred noise level for each of the active-electrodes can be computed to be $0.34\mu V_{RMS}$. If we assume a conservative value of 10 for the noise efficiency factor (NEF, [24]) of the differential amplifier in the back-end, we can expect its current consumption to be approximately 27 μA. As will be made clearer later in the paper, this value is less than one-fourth of the current consumption of a single active-electrode.

Fig. 5(c) shows the actual implementation of the differential amplifier where MOS pseudo-resistors are added for DC biasing of the input nodes. Since the input stage of the DDA is based on p-channel MOS differential pairs, the DC gain was fixed to 2 by means of a DC loop with a low-power (4 μA current consumption) active element, so that the output DC voltage will be twice that of the input. Fixing the patient's common mode to 1.5 V, the DC value of the electrode output will be 3 V; this guarantees that the differential couples of the DDA will operate correctly. The complete DDA is depicted in Fig. 6. The first stage is composed of two differential couples, whose output currents are summed on the output node and are followed by a common source stage. A third stage, a common drain, is needed to shift the output voltage since it is also used as V_{DD} of the analog circuits and of the DDA itself.

Unlike what happens in an OpAmp-based differential amplifier, mismatch in the transconductances of the differential couples in the proposed circuit is an issue since it can alter gain accuracy (as will be demonstrated in what follows), degrading the CMRR as discussed in Sec. II. The output voltage of the DDA-based differential amplifier is:

$$v_o = A_{v1} \cdot v_{p1} + A_{v2} \cdot v_{m1} + A_{v3} \cdot v_{p2} + A_{v4} \cdot v_o \frac{C_2}{C_1 + C_2} \quad (9)$$

where A_{vi} is the DDA open-loop DC gain from each of the four inputs to the output. The closed loop DC gain from each of the three inputs to the output will be:

$$\begin{aligned} A_{CL,i} = \left.\frac{v_o}{v_i}\right|_{v_j=0, j\neq i} &= \frac{A_{vi} \cdot (C_1+C_2)}{C_1 + C_2 - C_2 A_{v4}} \\ &= -\frac{A_{vi}}{A_{v4}} \cdot \frac{(C_1+C_2)}{C_2 - \frac{C_1+C_2}{A_{v4}}} \end{aligned} \quad (10)$$

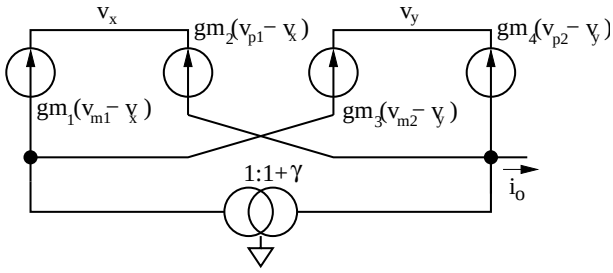


Fig. 7. Small signal model of DDA first stage. γ represents the mismatch between current mirror input and output currents.

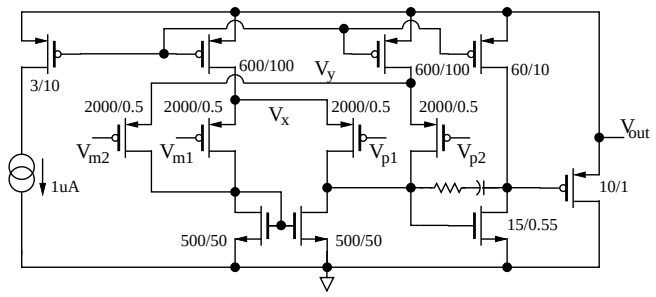


Fig. 6. Schematic and transistor sizing of the DDA. Power supply voltage is fixed by the output itself, which is DC biased by an external current source.

for $v_{i,j} = v_{p1}, v_{m1}, v_{p2}$. Linearizing the DDA first stage (see Fig. 7), neglecting output conductances and assuming each transconductance to have a different value due to mismatch, the transconductances from each input to the output current will be:

$$\begin{aligned} Gm_1 &= \frac{i_o}{v_{p1}}\Big|_{v_{m1}=v_{m2}=v_{p2}=0} = -\frac{gm_1 gm_2(2+\gamma)}{gm_1+gm_2} \\ Gm_2 &= \frac{i_o}{v_{m1}}\Big|_{v_{p1}=v_{m2}=v_{p2}=0} = \frac{gm_1 gm_2(2+\gamma)}{gm_1+gm_2} \\ Gm_3 &= \frac{i_o}{v_{p2}}\Big|_{v_{m1}=v_{p1}=v_{m2}=0} = -\frac{gm_3 gm_4(2+\gamma)}{gm_3+gm_4} \\ Gm_4 &= \frac{i_o}{v_{m2}}\Big|_{v_{m1}=v_{p1}=v_{p2}=0} = \frac{gm_3 gm_4(2+\gamma)}{gm_3+gm_4} \end{aligned} \tag{11}$$

where γ models the current mirror mismatch. Now, assuming that the DDA output voltage is given by $v_o = i_o \cdot (-R_o)$ where $-R_o$ represents the product of the output resistance at the first stage and the gain of the following stages, it is $A_{vi} = -G_{m_i} \cdot R_o$. Combining this with (11) and substituting in (10), one gets:

$$\begin{aligned} A_{CL,1} &= \frac{v_o}{v_{p1}}|_{v_{m1}=v_{p2}=0} \\ &= \frac{C_1+C_2}{C_2-\frac{C_1+C_2}{A_{v4}}} \cdot \frac{(gm_1 gm_2)(gm_3+gm_4)}{(gm_1+gm_2)(gm_3 gm_4)} \\ A_{CL,2} &= \frac{v_o}{v_{m1}}|_{v_{p1}=v_{p2}=0} \\ &= -\frac{C_1+C_2}{C_2-\frac{C_1+C_2}{A_{v4}}} \cdot \frac{(gm_1 gm_2)(gm_3+gm_4)}{(gm_1+gm_2)(gm_3 gm_4)} \\ A_{CL,3} &= \frac{v_o}{v_{p2}}|_{v_{m1}=v_{p1}=0} = \frac{C_1+C_2}{C_2-\frac{C_1+C_2}{A_{v4}}} \end{aligned} \tag{12}$$

As defined in (2), the CMRR is related to a mismatch between the gains of different ICs. From (12), one can observe how gain accuracy is not influenced, at first order, by mismatches in the current mirror. On the other hand, since there can be a significant spread in A_{v4} among different ICs due to process variations in MOS parameters, A_{v4} accuracy can not be high enough to guarantee a good match in $A_{CL,i}$ between different electrodes. Hence, the only way to guarantee a high CMRR for the system is to have a high open loop gain $\|A_{v,4}\|$ so that $\left\|\frac{C_1+C_2}{A_{v4}}\right\| << C_2$, just as would happen for an OpAmp based amplifier. To this end, the gain-bandwidth product of the DDA was fixed to 7 MHz, in order to guarantee a closed loop gain accuracy of more than 70 dB in the signal bandwidth. It should also be pointed out how, while the gain $A_{CL,3}$ from the input sharing the differential couple with the feedback voltage (v_{p2}, connected to v_1) is not affected by mismatches in the active elements, the other two gains ($A_{CL,1}$ from input v_{p1} and $A_{CL,2}$ from input v_{m1} which is connected to v_2) are. In the design under consideration (see Fig.5), this means that while one channel (i.e. v_1, whose gain is $A_{CL,3}$) has a CMRR which is, at first order, limited only by passive component mismatches, the other channel's CMRR (i.e. v_2, whose gain is $A_{CL,2}$) also degrades through mismatches in the active elements. Since the EIT signal differs from the EEG in that its CMRR is not increased by the DRL loop as discussed in Sec. II, the EIT signal is amplified through the first channel which ensures the best performance. Assuming a maximum transconductance deviation of $\pm\Delta g_m$ from the average value g_m, a little algebra enables the maximum and minimum values of $A_{CL,1,2}$ to be computed respectively as:

$$\begin{aligned} max(A_{CL,1,2}) &= \frac{(gm+\Delta gm)}{(gm-\Delta gm)}\frac{C_1+C_2}{C_2} \\ min(A_{CL,1,2}) &= \frac{(gm-\Delta gm)}{(gm+\Delta gm)}\frac{C_1+C_2}{C_2} \end{aligned} \tag{13}$$

which, when combined, provide the maximum variation in closed loop gain:

$$\frac{\Delta A_{CL,1,2}}{A_{CL,1,2}} = \frac{4gm\Delta gm}{gm^2-\Delta gm^2} \approx 4\frac{\Delta gm}{gm} \tag{14}$$

Following this result, careful design went into coherently sizing the current sources and differential couple MOS transistors in order to provide the required accuracy. Final tuning was based on MonteCarlo simulation and careful layouting was carried out on differential pairs, current sources and capacitances so as to minimize mismatches. Simulations show how the chosen component sizing leads to an accuracy which is limited by the mismatches in current sources and capacitors, hence mainly by the chip area which is available.

C. EIT and ESI current sources

127 positive and 127 negative current sources like the one depicted in Fig. 8(a) are grouped in 7 blocks of 64, 32, 16, 8, 4, 2 and 1 source respectively, each controlled by one of the 7 UP and 7 DOWN signals coming from the digital section of the IC. An 8-bit binary word is stored in the internal memory and contains 512 samples of output current. The output current lies between -127 and +127 μA, and is controlled in steps of 1 μA. Since the memory can be read at a frequency up to 512 KHz, the maximum representable frequency content is 256 KHz (without considering higher order harmonics). The EIT signal is down-converted in the input mixer by multiplication by a square wave at frequency f_{M1}, where f_{M1} is a submultiple of the memory clock. The synthesized current is normally chosen to be a digitized sinusoidal wave at $f_{EIT} = f_{M1} + 1$ KHz. More complex current waveforms can be used to simultaneously apply multiple current patterns adopting frequency-division or code-division multiplexing [25]. The reference current is fixed to 65 μA, which is equal to 65 times the current generated by the single current source. This reference current and the sizing of current source transistors were chosen so as to guarantee that the maximum absolute error in the generated current was below 1 μA. In order to have a high-speed turn on and off of each current source, the drain voltage of the transistors was kept equal to the average voltage of the current source output. In this way the parasitic capacitance on the drain node, which has a high value due to large transistor sizing for current accuracy and low flicker noise, is always kept approx. at the output voltage. This is achieved by the feedback loop in Fig. 8(a), which is based on a low-power operation amplifier (4μA bias current) and an off-chip capacitor. The output node of the current source is AC coupled to the electrode by means of a 100 nF off-chip capacitor. This is done to prevent DC current from flowing through the patient whenever the clock signal is stopped due to, for example, cable interruption or a failure in the back-end driving circuit. Current consumption of the block responsible for EIT current injection is 260 μA, which is required only when the IC is

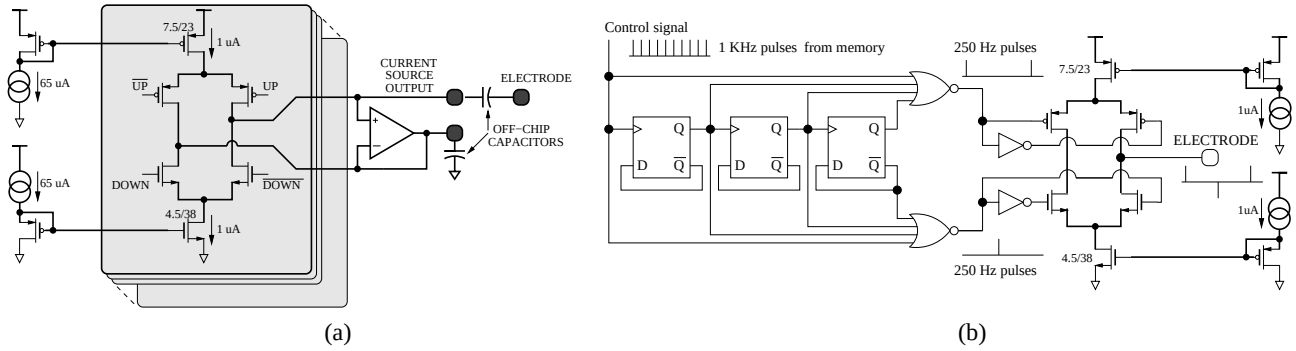


Fig. 8. (a) EIT current sources. Bias current is derived from a high accuracy reference current. (b) Diagram of ESI control logic and current sources. The input signal is the LSB of the EIT current source control word (ESI is only preformed when the electrode is programmed for EEG/EIT readout, not for EIT injection). Since memory is looped every 1 ms, the sequential circuit reduces the pulse frequency by a factor of 4 to produce a 250 Hz signal.

effectively programmed to deliver current to the electrode. For ESI measurement, the injected current waveform is determined from one bit of the digital word stored in the memory. Since the memory is cycled every 1 ms during normal operation with a simultaneous EEG/EIT signal readout, in order to be able to inject ESI current at lower frequencies alternate positive and negative pulses are generated once every four pulses detected on the input signal by the digital circuit depicted in Fig. 8(b). The current source is a replica of one branch used for EIT.

D. Digital section

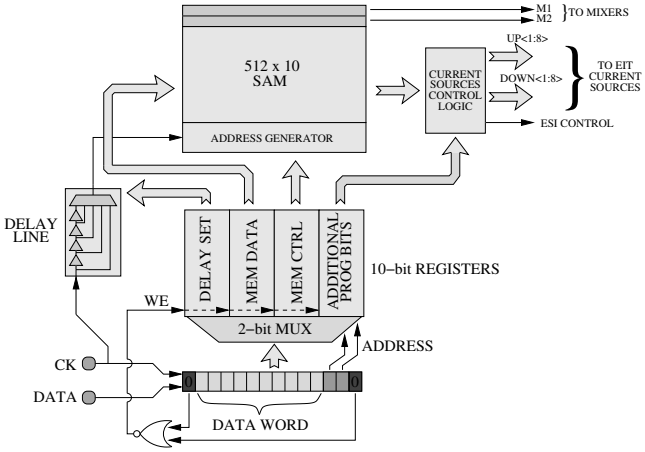


Fig. 9. Digital portion of the IC. This comprises a programmable delay line for the clock signal and a serial interface for writing programming words on four 10-bit registers. The sequential access memory contains samples of EIT current waveform for direct synthesis and input mixer control signals M1 and M2.

The digital section of the IC is depicted in Fig. 9. The core is the 512x10 bit SAM which is sequentially addressed in both reading and writing phases. During normal operation, words stored in memory are read sequentially to determine the instantaneous value of the EIT injected current and the value of signals M1 and M2 which drive the input mixer of the readout circuit. The time instant at which current sources and mixers switch can be modified by acting on the programmable delay line, which is provided in order to compensate for the different timing at which clock edges occur on different electrodes due to variability in line driver capability and load (i.e. cable capacitance). Depending on process corners, power supply and temperature, the steps by which the delay can be modified are comprised between approximately 500 ps and 1 ns, for an overall delay which lies between 16 and 32 ns.

An input interface is designed to store the electrode programming data on four 10-bit registers. Data are written by means of one serial data signal and one clock signal. The digital interface first converts the serial data stream into a parallel 14-bit word. The input shift-register continuously samples the data signal; to identify that a new word is ready to be written on one of the four internal registers, the first and last bits of the shift register need to be equal to zero. The register on which to write the new word is determined by two address bits, while the remaining ten bits provide the word to be written. The first register allows one to provide the programmable delay in the clock signal. The second register contains the data word to be written in the memory during write phases, while the third and fourth contain the configuration bits for memory read/write operations and additional configuration bits. Complete writing of the SAM requires less than 35 ms.

IV. IC Measurements

A. Electrical characterization

The IC is fabricated in 0.35 μm standard CMOS technology, 3.3 V supply voltage. The die (see Fig. 10) is 2x2 mm^2 in size and is encapsulated in a 5 by 5 mm^2 QFN plastic package. Performance values in terms of input referred noise are given in Fig. 11 for simultaneous acquisition of EEG and EIT signals. Since each electrode performs single-ended amplification, in order to evaluate noise at the input of the back-end ADC (see Fig. 1), the test setup is composed of an input DC signal connected to two ICs whose outputs are subtracted by an instrumentation amplifier for medical applications. The flicker noise corner frequency is around 200 Hz, so that EEG and EIT signals are both effectively placed in regions of the spectrum where thermal noise dominates. The upper-left graph of Fig. 11 shows noise spectral density, with M2 running at 2 KHz for EEG signal up-conversion. The input referred noise is 0.56 μV_{RMS} for the EEG signal integrated between 0.5

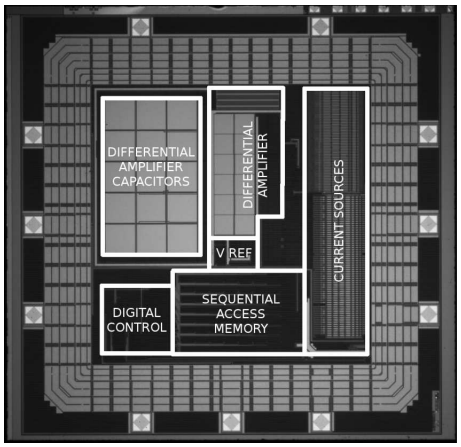


Fig. 10. Die photograph. The IC area is 4 mm^2.

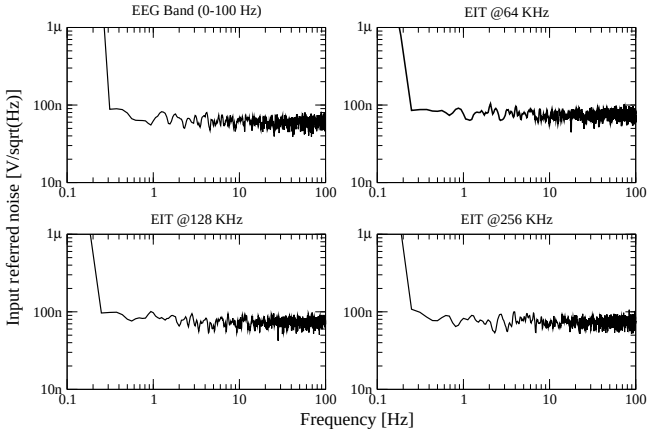


Fig. 11. Input referred noise for the acquisition of EEG (upper-left graph) and EIT signals (remaining three graphs, for different injection frequencies), once down-converted to base-band.

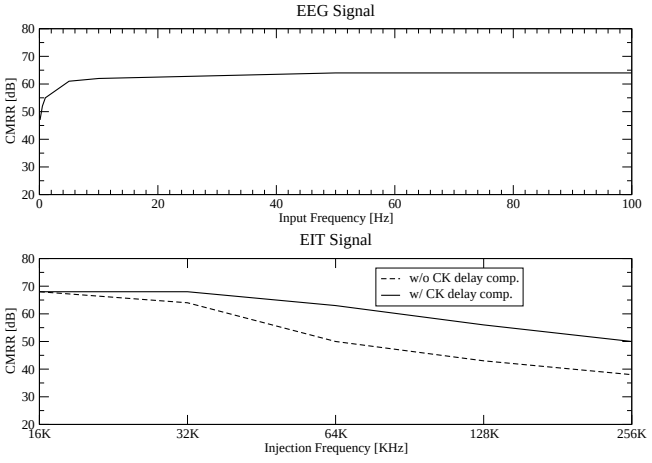


Fig. 12. Common Mode Rejection Ratio for the readout of EEG and EIT signals. For EIT, CMRR degrades as frequency increases. Calibration of clock delay line partially compensates the effect, improving the CMRR value.

and 100 Hz. The other three graphs show the equivalent input noise for EIT signal at different injection frequencies; it can be seen that the noise level is slightly higher than for EEG. If only one signal type is required (either EEG or EIT), M1 and M2 are driven in counter-phase, doubling the output signal and therefore approximately halving the input referred noise level to 0.28 μV_{RMS} for EEG signal acquisition.

CMRR measured performances are presented in Fig. 12 by measuring the output voltage mismatch of two active-electrodes with the same sinusoidal input signal of 50 mV peak-to-peak amplitude. This is a reasonable value for 50-60 Hz common mode signals once reduction of them due to DRL implementation is taken into account [23]. The CMRR is characterized for every combination of electrodes among a set of 8; results are presented for the worst case. The EEG channel is characterized by a slightly lower CMRR than the expected 70 dB, being about 64 dB at 50-60 Hz. At very low frequency, the CMRR degrades due to the presence of pseudo-resistors in parallel with the capacitances which set the amplifier gain. As expected from what was said in Sec. III-B, the EIT channel is characterized by a better CMRR at low frequency (68 dB for a 16 KHz input signal). This value degrades with increasing frequency down to less than 40 dB at 256 KHz. This is mainly due to the time delay between clock signals reaching different electrodes. After calibration is performed by programming the delay line in the digital section, CMRR is restored to 60 dB at 64 KHz and increased to 50 dB at 256 KHz.

A comparison between performances of the IC presented and other active-electrode's ICs reported in the literature is presented in Table II though for EEG signal readout only, since only [16] performs joint EEG-EIT signal readout and current injection. One should notice how the noise efficiency factor (NEF, [24]) is in-line with that reported in [15] (which however is not able to measure EIT or ESI) and almost one third of that in [16], due to the use of one DDA instead of multiple OpAmps. By contrast, the NEF value is quite high when compared to low-power differential instrumentation amplifiers such as [24] due to the decision not to take the reference signal to every electrode, as well as the need to be able to acquire EEG and high frequency EIT simultaneously. The CMRR for this work is similar to that of [16] and higher than that of the other active-electrode solution [15] in the absence of feedback techniques. However this value is high enough to be increased by DRL to similar or higher levels [12][23].

	[24]	[15]	[16]	This Work
Current $[\mu A]$	16	11	330	120
Z_{in} @ 50Hz $[\Omega]$	-	10 G	>100 M	>100 M
CMRR $[dB]$	83	52 (+30)	63	64
Noise $[\mu V_{rms}]$ (Band)	2.2 (0.025- -7200 Hz)	0.8 (0.5- -100 Hz)	0.45 (0.5- -100 Hz)	0.28 (0.5- -100 Hz)
NEF	4	12.3	31.8	12.5
Active-electrode	No	Yes	Yes	Yes

TABLE II
COMPARISON OF EEG READOUT PERFORMANCES AS COMPARED TO PREVIOUS WORK REPORTED IN THE LITERATURE. IN BRACKETS IN [15], THE CMRR IMPROVEMENT DUE TO FEEDBACK TECHNIQUES.

EIT characterization is shown in Fig. 13(a) by injecting a 64 KHz current with variable amplitude into a resistive load R_{LOAD} of either 150 Ω or 1050 Ω, with $R_{EL} = 500$ Ω (see Fig. 13(d)). A second IC down-converts the voltage across the resistor testing linearity and frequency behavior of both current injection and signal conditioning stages. Deviations from expected values were confined below 0.5% in every condition tested. Fig. 13(b) shows a similar test, considering a variable contact impedance R_{EL}. Even when increasing to values significantly higher than standard contact impedance value at EIT frequencies, the injected current is only slightly modified. The mismatch in currents injected by two different ICs is measured in Fig. 13(c) as a function of amplitude, with an injection frequency of 64 KHz. The mismatch is confined below 1% and 1 μA.

ESI measurement accuracy is reported in Fig. 14. The test is performed by injecting the current on known impedances. As expected and discussed in Sec. III-A, the error in the computed impedance increases when the load is mainly resistive (though always remaining lower than 20%) while, for more common values of the parameters (R_s, R_p and C_p in Fig. 4), the error is lower than 10%.

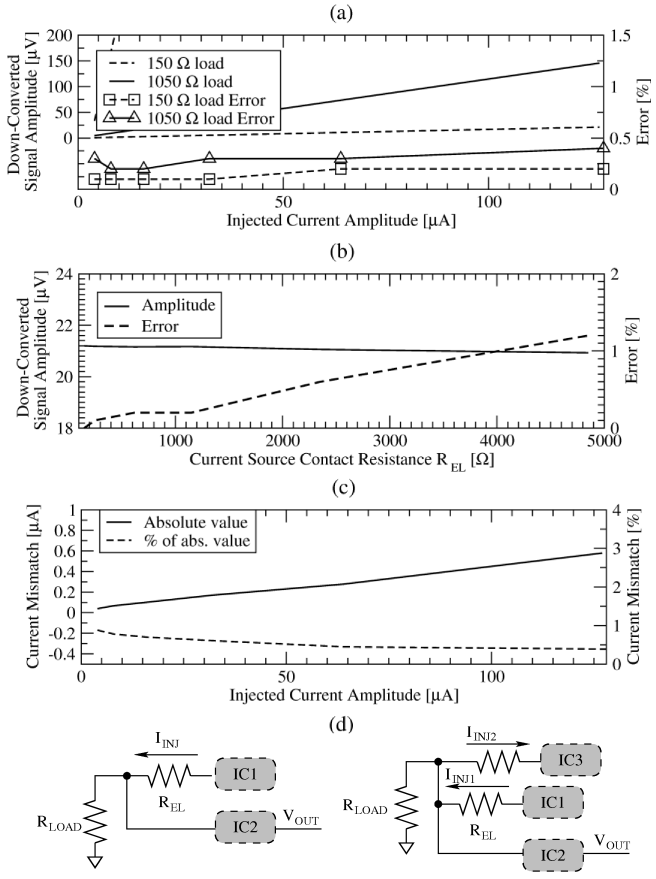


Fig. 13. Testing of EIT current generation and voltage down-conversion. IC1 (and IC3 where needed) generates the high frequency current, IC2 down-converts the voltage produced on a test resistor. (a) shows the linearity of both operation for increasing current amplitude with two different R_{LOAD} and $R_{EL} = 500\Omega$. (b) shows how upon increasing R_{EL} to values significantly higher than standard contact impedance at EIT frequencies, injected current is not modified significantly. (c) shows the mismatch between two opposite currents injected on the same node. The test setup is depicted in (d)-left for (a) and (b), and (d)-right for (c).

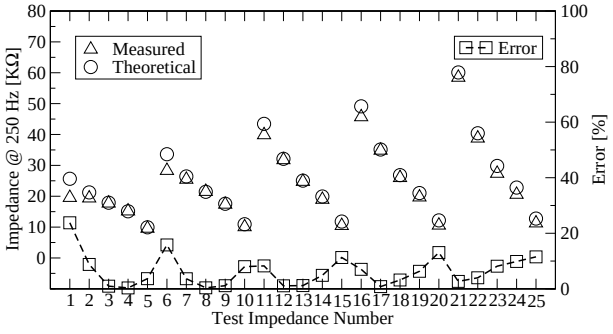


Fig. 14. ESI characterization by measurement of 25 known test impedances like the one in Fig. 4, with R_s=1 KΩ, 30 $K\Omega < R_p <$ 120 $K\Omega$, 10 $nF < C_p <$ 90 nF [28]. For common values of the three parameters ($R_s \approx 1$ $K\Omega$, $R_p \approx 50$ $K\Omega$, $C_p \approx 30$ nF for the series of two Ag/AgCl electrodes without skin abrasion, corresponding to test impedance number 8) the error is lower than 10%.

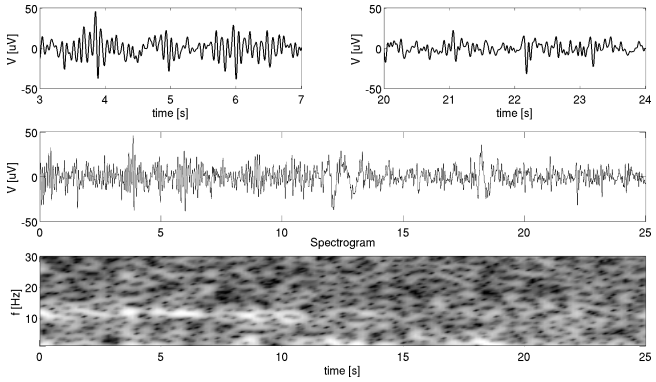


Fig. 15. The EEG signal is acquired in the right occipital position O_2, with reference on Fp_z. Alpha waves in the 8-13 Hz range are visible when the subject has his eyes closed in the first half of recording (lighter tones correspond to higher power spectral density in the short time Fourier transform graph).

is lower than 10%.

B. Functional characterization

Fig. 15 shows the functionality in the acquisition of EEG signals. One EEG channel is shown, acquired in the occipital region of the right hemisphere; alpha waves in the 8-13 Hz range are visible when the subject has his eyes closed in the first half of recording. Fig. 16 shows a simple test for simultaneous EEG and ESI measurement. During EEG acquisition in the resting state, the electrode cable is intentionally pulled so that the contact impedance increases, as attested by measurement. Due to worsening quality of the contact impedance, the EEG signal acquired on the electrode decreases significantly towards the end of the recording.

EIT is tested by using the resistive phantom depicted in Fig. 17(a). A resistive network with six different resistor values represents the scalp, skull and gray-white matter layers; two resistors in the outermost layers have different values to simulate variations in layer thickness. A 127 μA, 64 KHz current is injected between the third and ninth electrodes while 7 electrodes readout the output voltage. A 2 KΩ resistor is inserted in series with the electrode input in order to simulate

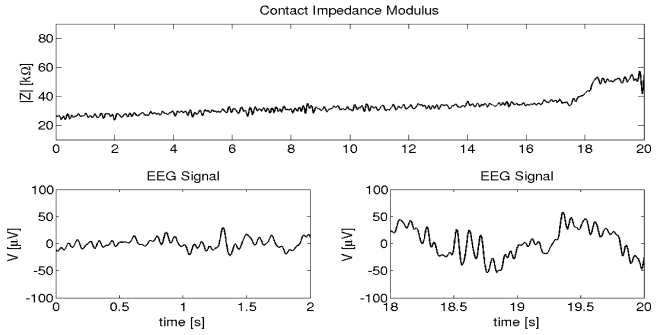


Fig. 16. The EEG signal acquired in O_2, with reference on Fp_z. Contact impedance is measured between O_1 and O_2 and increases during measurement since the electrode cable is being pulled, worsening contact quality. A sharp increase is visible close to the end of the recording. The EEG signal is of good quality at the beginning of the recording, while at the end, the bad contact quality gives rise to low frequency oscillations which make the signal quality unacceptable.

the contact impedance. Reconstruction is performed through a simple Newton-Raphson non-linear solver. Fig. 17(b) shows the relative errors in the reconstruction of resistor values, which are confined below 10%. In a second step, R_6 is increased by 10% and EIT signal acquisition is performed again. The difference between the two reconstruction solutions is computed and normalized to each resistor value, in order to estimate the relative variation in resistances. Fig. 17(c) shows the deviation with respect to the expected solution (10% for the inner layer, 0 for the others), normalized to each resistor value. For differential reconstruction, the error is confined below 4%. Additionally, an EIT real impedance map reconstruction is performed in a two-dimensional test phantom of known properties where a 35 mm diameter object with 0.7 S/m conductivity is placed inside a tank filled with 1 S/m saline solution. A 128 μA_{pp} current at 16 KHz is injected between opposite electrodes, while 10 different electrodes read out voltages at a frame rate of 10 Hz. Accuracy of reconstruction depends not only on the active-electrode properties but on density and position as well and on the EIT inverse problem solver. Since optimization of this lies outside the scope of this work, we adopted a simple one-step Gauss-Newton solver with Tikhonov regularization [6]. It can be seen that the system correctly identifies areas where resistivity increases.

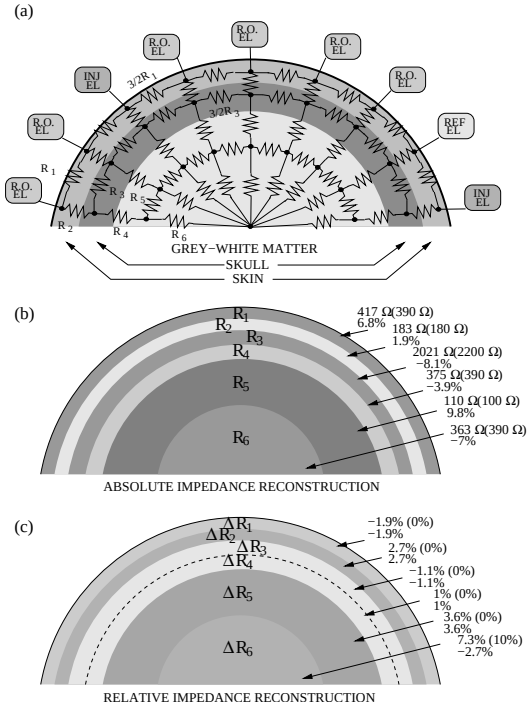


Fig. 17. (a) EIT is validated on a test phantom based on a resistor mesh (R_1=390 Ω, R_2=180 Ω, R_3=2200 Ω, R_4=390 Ω, R_5=100 Ω, R_6=390 Ω). Two electrodes are used for current injection (*INJ EL*), 6 plus the reference one for voltage readout(*R.O. EL* and *REF EL* respectively). The six reconstructed resistance value are shown in (b), showing the expected values (in brackets) and relative error. In (c), reconstructed variations are shown with respect to the previous solution, when increasing R_6 by 10% of its value.

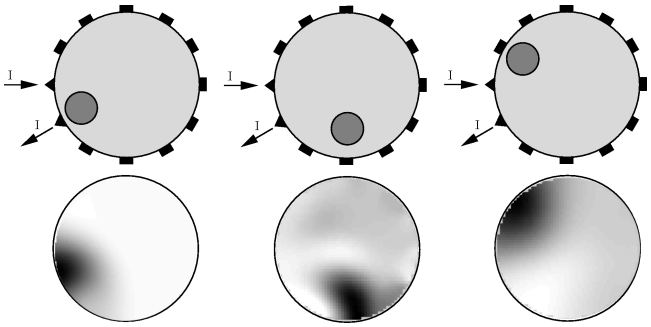


Fig. 18. Impedance map reconstruction of an 18 cm diameter cylindrical tank, 1 cm high, filled with a 1 S/m saline solution and a moving object with 0.7 S/m conductivity. Dark tones correctly identify regions where resistivity increases.

V. Conclusions

Neuroimaging techniques can be roughly divided into two groups; the first one (comprising fMRI and PET) is characterized by high spatial resolution, low temporal resolution and bulky and expensive hardware. This hampers both applicability outside hospital settings and possible applications. By contrast, EEG source localization is characterized by high portability, low cost and the ability to reconstruct rapidly varying signals. Unfortunately EEG based imaging suffers from low spatial resolution, which can be improved by using high density systems and improving the knowledge of the electrical characteristics of the head tissues, which can be provided by EIT.

The IC presented here allows one to integrate EEG and EIT techniques on the same active-electrode of a high density system, each electrode being able to be programmed at any time between EIT current injection and EEG/EIT voltage readout. During voltage readout, the electrode can also be used to continuously monitor the metal-skin contact impedance in order to evaluate signal quality and the possible need to reposition an electrode. With respect to the solution presented in [16], performance in terms of power consumption and noise has been significantly improved with similar CMRR. The noise level for EEG signal acquisition integrated on the 0.5 to 100 Hz bandwidth is 0.56 μV_{rms} when acquired at the same time as EIT, while it is halved when only EEG is acquired. Current consumption of the readout portion of the IC is 120 μA, with a noise efficiency factor for standalone EEG signal acquisition

of 12.5, which is in line with that reported in the literature for EEG-only active-electrodes [15].

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