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Hardware-Algorithms Co-design and Implementation of an Analog-to-Information Converter for Biosignals based on Compressed Sensing

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***Abstract*—We report the design and implementation of an Analog-to-Information Converter (AIC) based on Compressed Sensing (CS). The system is realized in a CMOS 180 *nm* technology and targets the acquisition of bio-signals with Nyquist frequency up to 100 kHz. To maximize performance and reduce hardware complexity, we co-design hardware together with acquisition and reconstruction algorithms. The resulting AIC outperforms previously proposed solutions mainly thanks to two key features. First, we adopt a novel method to deal with saturations in the computation of CS measurements. This allows no loss in performance even when 60% of measurements saturate. Second, the system is able to adapt itself to the energy distribution of the input by exploiting the so-called *rakeness* to maximize the amount of information contained in the measurements.**

With this approach, the 16 measurement channels integrated into a single device are expected to allow the acquisition and the correct reconstruction of most biomedical signals. As a case study, measurements on real electrocardiograms (ECGs) and electromyograms (EMGs) show signals that these can be reconstructed without any noticeable degradation with a compression rate, respectively, of 8 and 10.

***Index Terms*—Compressed Sensing, Analog-to-Information Converter (AIC), Rakeness, Smart saturation checking, Biomedical signals.**

I. Introduction

MINIATURIZED body area network nodes have recently attracted increasing attention as the possible vehicle to continuously and remotely measure biomedical signals, which is a fundamental step to provide the ubiquitous, long-term and real-time monitoring required by the patients and to enable faster coordination with medical personnel [1]. Such vision of continuous and distributed healthcare requires the research community to develop resource-efficient bio-sensing nodes [2], for which bio-signal acquisition performed via application-specific Analog-to-Digital Converters (ADC) is certainly a fundamental step. This is one of the reasons why, in recent years, increasing attention has been paid to ADCs exploiting input signal (statistical) features to reduce the amount of required resources (hardware, time, energy, etc.) with respect to standard, general purpose Nyquist-rate converters [3], [4].

In this paper we consider a different approach to signal acquisition which is based on the implementation of an Analog-to-Information Converter (AIC) relying on the paradigm of *Compressed Sensing* (CS) [5]–[9], that reduces the number of necessary measurements relative to those required by classical ADCs based on the Shannon-Wittaker sampling theorem [10].

More specifically, CS theory relates the number of required measurements with the *actual information* carried by the signal which is often not related to its *bandwidth*. To this aim, CS exploits a feature, known as *sparsity*, which is possessed by a large category of signals and which requires that the signal of interest can be expressed as the linear combination of only a few waveforms in a suitable basis.

Under this assumption, the input signal can be acquired in a way similar to common digital compression algorithms.

More precisely, in the standard digital compression approach of Fig. 1(a) the input signal is first sampled and converted into digital words at Nyquist rate, then a proper DSP or finite-state machine ensures data compression by means of a suitable lossless or lossy compression algorithm. The process is useful to save energy (memory) in data transmission (data storage). The original signal can be easily restored by means of the proper decompression algorithm.

In the CS approach of Fig. 1(b), the analog input signal is first processed by a proper analog front-end (the CS encoder), that generates a small number of measurements which are sampled and converted by an ADC at an operating rate much smaller than the Nyquist one. The input signal is then recovered (we say *reconstructed*) by means of a proper CS decoding algorithm.

The main difference between the two approaches is that, in the scheme of Fig. 1 (a), the compression algorithm is either, in the large majority of cases, the one with the highest complexity

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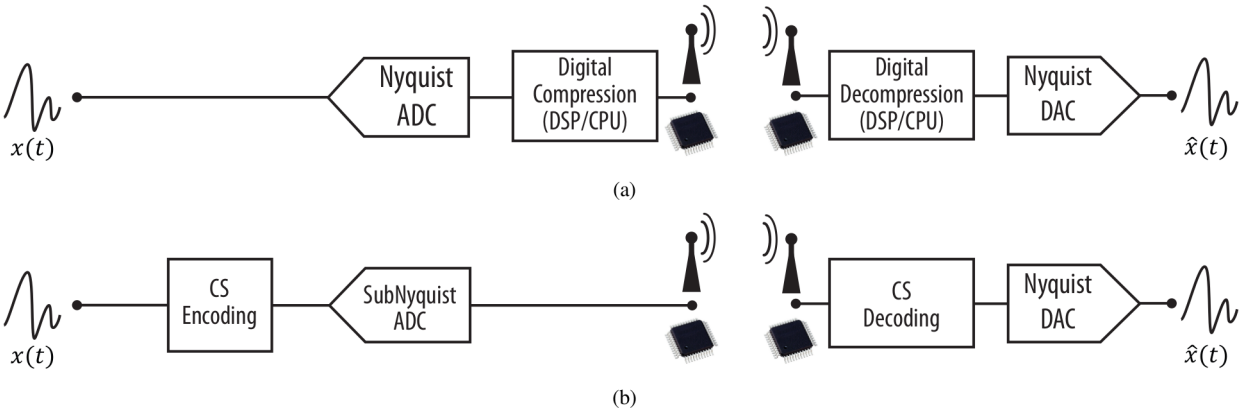


Fig. 1. Basic block diagrams for compression/decompression systems: (a) in the conventional approach the input signal is sampled and converted into digital words at Nyquist rate, then compressed by any choice of lossless or lossy algorithms. The input signal can be recovered from the compressed representation by the proper digital decompression algorithm; (b) in the CS approach the input signal is first elaborated by the (analog) CS encoder, then sampled and converted into digital words at a sub-Nyquist rate. The CS decoder ensures the input signal reconstruction from these values.

(and so with the need for a more complex hardware and higher energy requirements), while decompression is much simpler, or the required resources are evenly distributed between compression and decompression stages. On the contrary, the scheme of Fig. 1 (b) can be implemented in an asymmetric-resources scenario where the CS encoder is based on a very simple and extremely low-power hardware, while most of the complexity and energy requirements are transferred to the decoding stage. As a consequence, while case (a) is preferred when a single compression unit is used by many receivers, case (b) finds a natural application when multiple encoders communicate with a single data aggregator. This happens, for example, in the already mentioned body area networks for medical telemetry [1], [11], where a heterogeneous set of highly energy-efficient, small form factor bio-sensor nodes transmits data to a single monitoring station [12]. Performance in this scenario is boosted, since all biomedical signals posses the sparsity property, allowing the CS approach to achieve very large compression factors [9], [13]–[15].

As far as integrated prototypes are concerned, a few CS-based solutions have been proposed so far in the literature [16]–[21]. Most of them are based on the Random Modulation Pre-Integration (RMPI) architecture, which was shown to be the most versatile in terms of capability to acquire signals that are sparse regardless of their basis [8].

Interestingly, these prototypes target considerably different applications, ranging from RF systems to very-low-frequency biomedical circuits, and the CS approach shows different advantages in each case.

More specifically, in a RF scenario, the main advantage is to obtain a system capable to acquire a signal characterized by a Nyquist frequency much larger than the one at which the implemented ADC is operating. In other words, one can amply relax the system requirements and still be able to correctly process the RF input signals. For instance, the circuits in [18] and [19], both implemented in $90\,\mathrm{nm}$ CMOS technology, process, respectively, multitone BPSK signals up to $500\,\mathrm{kHz}$ and radar pulse signals up to $2\,\mathrm{GHz}$, with a power consumption of only $55\,\mathrm{mW}$ and $506\,\mathrm{mW}$ (without considering the final Nyquist ADC, that was not embedded in either circuits).

As far as biomedical signals acquisition is concerned, CS is exploited to design body area sensor network nodes with the architecture of Fig. 1(b), that is capable of lowering the power consumption with respect to the classical approach of Fig. 1(a). For example, the work in [20] is a $0.18\,\mu\mathrm{m}$ circuit for cortical signal recording, which includes an LNA front end, a $20\,\mathrm{kS/s}$ 10-bit ADC based on Successive Approximation Register (SAR), with an overall power consumption of $168\,\mu\mathrm{W}$. The circuit has been designed with tight area and power density constraints to fit implantable sensor requirements, and both the hardware architecture and also the adopted CS technique are strongly specialized, so the prototype can work only on this particular setting (i.e., multi-lead EEG signals). As another example, the prototype in [21] is an ultra-low power AIC for ECG recording, which adopts very specific solutions capable of lowering circuit energy requirements, but strongly limiting the bandwidth of the input signal to less than $1\,\mathrm{kHz}$. The circuit is designed in $0.12\,\mu\mathrm{m}$ technology, and embeds a $200\,\mathrm{S/s}$ SAR-based 10-bit ADC, with a power consumption as low as $1.8\,\mu\mathrm{W}$.

In this paper, we present an integrated AIC that, despite targeting biomedical signals acquisition, can be used also with a generic waveform with Nyquist frequency ranging from fractions of a Hz to a hundred of kHz. The circuit has been designed and fabricated in $180\,\mathrm{nm}$ CMOS technology and it is based on a 16-channel RMPI architecture, with a power consumption of about $27\,\mu\mathrm{W}$ per channel. The circuit also includes a shared 11-bit SAR based ADC.

Differently from all the aforementioned prototypes, the main innovative aspect of our circuit is not represented by the existence of ad-hoc solutions that increase performance on a very specific setting, but by the design based on a joint hardware-algorithms optimization. This allows us to increase system performance without any cost in terms of hardware complexity or computational power spent by decoding. Two important breakthroughs in the CS paradigm have been exploited towards this optimization. The first one is the so-called *rakeness*-based

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CS approach [22] that, roughly speaking, increases the CS performances by exploiting the fact that bio-signals are not only sparse, but also *localized*, i.e. that most of their energy is concentrated in a given region of the signal space (e.g. in a specific frequency range). This allows us to use a very limited number of RMPI channels to achieve an accurate reconstruction of the original signals, while, usually, a much larger channel quantity is used [21]. In fact, experimental measurements show that the 16 channels embedded into one of our integrated circuit prototypes suffice to process almost all biomedical signals of interest.

The second innovative feature is the addition to the prototype of the *smart saturation checking* capability [23]. With this approach, a minimal cost in terms of hardware complexity makes it possible to retrieve information also from RMPI channels in which the internal integrator exhibits saturation. Measurements highlight that the designed AIC can correctly reconstruct the original signal without any performance loss in presence of a *weak* saturation, i.e., when the input signal amplitude is slightly larger than the expected level and a few RMPI channels are corrupted by saturation. Furthermore, a weak saturation can even lead to a performance improvement due to the increase in the allowed input signal amplitude. Measurements also show that, in presence of a *stronger* saturation (when about 60% of the channels saturate) we are still capable to accurately reconstruct the signal with a minimal performance loss.

A final contribution of this work is the development of a suitable *testing technique* for a CS-based AIC, a territory which is basically uncharted in the literature.

The rest of the paper is organized as follows. In Section II we recall the basic concepts and notation for CS including a brief description of the rakeness approach, while in Section III we detail the architecture of the proposed circuit, with emphasis on the non-standard adopted solutions. Then, in Section IV, we present circuit measurement results, using both our testing techniques based on artificially created sparse signals, as well as real electrocardiograms (ECGs) and electromyograms (EMGs). In particular, circuit measurements on the latter ones shows the capability to get compression factors as high as 8–10. In Section V conclusions are finally drawn.

II. Compressed Sensing Fundamentals

The entire CS theory is developed on signals $x(t)$ defined in a window $0 \leq t < T_W$. This is not a limitation, since it is always possible to slice any signal of interest over adjacent time windows of length T_W, process them independently and then get the output signal by joining all elaborated slices.

The main assumption in the CS approach is that signals to be acquired are sparse. More precisely, given an orthonormal basis $[\psi_1(t), \psi_2(t), \ldots, \psi_N(t)]$, $0 \leq t < T_W$, any possible instance $x(t)$ of a sparse signal can be written as

$$x(t) = \sum_{i=1}^{N} \alpha_i \, \psi_i(t)$$

where the *sparse representation* vector $\alpha = \{\alpha_1, \ldots, \alpha_N\}$ has only $K \ll N$ non-vanishing terms: in this case the signal is said to be K-sparse.

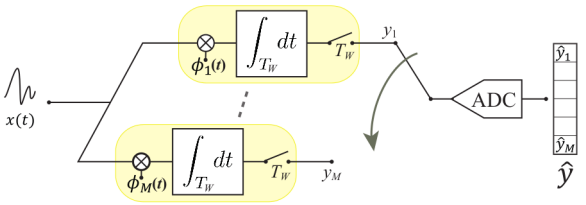


Fig. 2. Basic block diagram of the RMPI architecture with a shared ADC.

The CS approach aims at *sensing* $x(t)$ in a *compressed* way, i.e., by using only M measurements instead of N that would be required by the classical Nyquist-rate sampling, with $K < M < N$. The measurement vector $y = \{y_1, \ldots, y_M\}$ is obtained by projecting $x(t)$ over a set of sensing functions $\phi_j(t)$, $j = 1, \ldots, M$, i.e., $y_j = \langle \phi_j(t), x(t) \rangle_{T_W} = \int_{T_W} \phi_j(t) x(t) dt$, where $\langle \cdot, \cdot \rangle_{T_W}$ stands for inner product on the time window T_W.

Despite other solutions are possible [15], [17], the most common architecture of an AIC is the RMPI [24] shown in Fig. 2. Here, $x(t)$ is independently processed by M different channels to compute at the same time the M inner products. In the j-th channel, $x(t)$ is first multiplied with the j-th sensing function, and then integrated over a time window T_W. The resulting values y_j can be converted into digital form by a shared sub-Nyquist ADC, whose rate is M/T_W conversions per time unit, that is much smaller with respect to the Nyquist rate $1/T = N/T_W$.

In the case of a discrete-time input signal any realization in a time window of length $T_W = NT$ is expressed by a vector $x = \{x_1, x_2, \ldots, x_N\} \in \mathbb{R}^N$, where the x_i for $i = 1, \ldots, N$ represent the equivalent Nyquist-rate samples. In this case, the orthonormal sparsity basis can be written as a matrix $\Psi \in \mathbb{R}^{N \times N}$, whose columns are the basis vectors, such that $x = \Psi\alpha$. The M measurements are still obtained by means of the inner product between x and a set of M sensing vectors $\phi_j \in \mathbb{R}^N$, i.e.,

$$y_j = \langle \phi_j, x \rangle_N = \sum_{i=1}^{N} \phi_{j,i} x_i \tag{1}$$

where with $\phi_{j,i}$ we indicate the i-th element of the j-th vector. By defining the sensing matrix $\Phi \in \mathbb{R}^{M \times N}$ whose M rows are the vectors ϕ_j, one can express the measurements vector y as $y = \Phi x = \Phi\Psi\alpha$ or, more realistically, $\hat{y} = \Phi\Psi\alpha + \nu$ where ν represents non-idealities such as system noise and ADC quantization.

Since our aim is to develop a switched-capacitor (SC) architecture, as shown in Section III, in this paper we will concentrate only on the discrete-time case.

The CS decoder estimates α (and so x) from $\hat{y}$ under the assumption that Ψ and Φ are known. Since $M < N$, this is a linear ill-posed problem. To overcome this impasse, CS theory [6] relies on the solution $\hat{\alpha}$ of the convex minimization problem

$$\begin{aligned} \hat{\alpha} &= \arg\min_{\alpha} \|\alpha\|_1 \\ \text{s.t. } &\|\Phi\Psi\hat{\alpha} - \hat{y}\|_2 \leq \varepsilon \end{aligned} \tag{2}$$

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where $\|\cdot\|_1 = \sum|\cdot|$ and $\|\cdot\|_2 = \sqrt{\sum \cdot^2}$ stand respectively for the l_1 and l_2 norms, and ε bounds the effects of ν. The input signal can be reconstructed as $\hat{x} = \Psi\hat{\alpha}$ [5].

The quality of the reconstruction is guaranteed by the Restricted Isometry Property (RIP) [25] of the matrix $\Phi \cdot \Psi$, ensuring that the sensing stage is able to preserve as much as possible the l_2-norm of α also with $M < N$. The CS theory guarantees that, for all possible sparsity matrices Ψ (i.e. for any sparsity basis), the RIP is always satisfied for $\Phi \cdot \Psi$ by adopting Φ composed of a collection of *independent and identically distributed* (i.i.d.) random variables with either Gaussian or sub-Gaussian distribution. In this situation the reconstruction is guaranteed with high probability by adopting

$$M \geq M_{\min} = CK \log\left(\frac{N}{K}\right) \tag{3}$$

where C is a constant typically set around 4.

In the following, among the many algorithms and tools that have been proposed to solve problem (2) under the assumption (3), we will use the so-called SPGL-1 [26], that belongs to the class of iterative convex solvers for it.

Having a physical implementation of an AIC in mind, the most convenient way to ensure RIP is to generate $\phi_{j,i}$ as *binary antipodal* random variables, where the two possible values $+1$ and -1 occur with the same probability. This relaxes the product operations required to compute the inner products (1) into much simpler sign inversion operations, and allows a straightforward hardware implementation. With this approach, no reduction in terms of CS performance with respect to the Gaussian case has been observed [8].

In order to increase the performance of our prototype, we also rely on the possibility to optimize the sensing matrix Φ. More specifically, we adopt the recently introduced *rakeness* approach to CS [22]. This technique differs from others ones presented in the literature [27]–[29] where optimized sensing matrices are obtained by a proper specialization of Φ on an specific sparsity matrix without taking advantage of the input signal statistical features. Moreover, none of the approaches in [27]–[29] is capable to generate binary antipodal matrices, with the need, in principle, to implement of a complex and expensive full analog multiplier.

Conversely, the rakeness approach allows to obtain antipodal sensing matrices, optimized thanks to the exploitation of additional assumptions on the class of signals to acquire. More precisely, rakeness requires input vectors x that are not only sparse but also *localized*, i.e. their energy content is not uniformly distributed in the whole signal domain (as it almost always happens when dealing with real world signals [30]). The idea is to choose the sensing vectors ϕ_j to increase the average energy collected when the input signal is projected onto the sensing matrix, preserving at same time the RIP of the corresponding operator $\Phi \cdot \Psi$. The latter constraint guarantees that the sensing stage is not critically tuned on typical instances, so that outliers instances of the input class of signals can still be reconstruct.

More formally, let us model ϕ_j and x as realizations of two independent stochastic processes $\underline{\phi}$ and $\underline{x}$ whose $N \times N$ correlation matrices are given by $C^{\underline{\phi}}$ and $C^{\underline{x}}$. We define *rakeness* as the quantity

$$\rho(\underline{\phi}, \underline{x}) = \mathbf{E}_{\underline{\phi},\underline{x}}\left[\left|\langle\phi_j, x\rangle_N\right|^2\right] = \sum_{i=1}^{N}\sum_{j=1}^{N} {C^{\phi}}_{i,j} {C^{x}}_{i,j}$$

where $\mathbf{E}_{\underline{\phi},\underline{x}}$ stands for the expectation with respect to both $\underline{\phi}$ and $\underline{x}$. In other words, ρ is the expected value of the energy of the j-th measurement y_j, so that maximizing ρ implies the maximization of the energy collected (i.e., "*raked*") by the generic sensing vector ϕ_j. Imposing the constraint that the ϕ_j are random enough, the maximization of ρ is mapped into the following optimization problem:

$$\begin{aligned} \max_{C^{\phi}} \quad & \sum_{i=1}^{N}\sum_{j=1}^{N} {C^{\phi}}_{i,j} {C^{x}}_{i,j} \\ \text{s.t.} \quad & \sum_{i=1}^{N} {C^{\phi}}_{i,i} = e \\ & \sum_{i=1}^{N}\sum_{j=1}^{N} \left({C^{\phi}}_{i,j}\right)^2 \leq \tau e^2 \end{aligned} \tag{4}$$

where e is the energy of each sampling vector[1], while τe^2 is an upper bound[2] of the randomness of the process $\underline{\phi}$. The optimization problem (4) has been analytically solved in [22]. Its solution is given by a correlation matrix C^{ϕ}, that identifies the stochastic process to be used for generating sensing vectors.

While the generation of a random vector with a prescribed correlation is quite easy, the generation of binary antipodal vectors given C^{ϕ} is a substantially more complex task. To this aim, many different approaches have been proposed in the literature (see, e.g., [31]–[34]). Probably the simplest one relies on thresholding of Gaussian random vectors [34], [35]. Although not completely general[3] this approach is very simple, and can be specialized to our case as follows. Let us first compute the $N \times N$ matrix C^G defined as

$$C^G = \sin\left(\frac{\pi}{2} C^{\phi}\right)$$

when equality is meant componentwise. Then, let us generate M Gaussian vectors with zero mean and covariance matrix C^G. The ϕ_j are simply obtained by computing the sign of the elements of these Gaussian vectors. This approach is suitable for offline generation of the Φ, that can be easily stored in a local memory. When hardware constraints make it unfeasible to use local storage, online generation of a stream of antipodal symbols with a given correlation profile is possible using a so-called linear probability feedback generator [31], [32].

As a final remark, exploiting the rakeness approach means increasing the quality of the reconstructed signal for a given value of $M_{\min}$, or, *vice versa*, to decrease $M_{\min}$ guaranteeing the same reconstructed signal quality [22]. The latter scenario is particularly important since it allows us to reduce circuit

[1]For antipodal sampling sequences it is always $e = N$.

[2]Tuning of τ on a proper range is not critical, since it does not appreciably alter the overall system performance [30].

[3]The method does not guarantee that a process can be generated for each feasible correlation matrix C^{Φ}; however the method almost always succeeds in real cases.

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TABLE I
DESIGN PERFORMANCE SUMMARY FOR EACH CHANNEL OF THE SWITCHED CAPACITOR RMPI ARCHITECTURE.

RMPI performance	
capacitors value	$C_S = 5\,\text{pF}$, $C_F^I = C_F^{II} = 40\,\text{pF}$
gain	$g = -1/8$
area	$850 \times 280\,\mu\text{m}^2$
step-response settling time	$3\,\mu\text{s}$
data retention	$\approx 1\,\text{s}$
Op-amp performance	
architecture	class-A telescopic cascode
power consumption	$27\,\mu\text{W}$ ($15\,\mu\text{A}$@$1.8\,\text{V}$)
A_d	98 dB
GBW	480 kHz
V_{off}	$< 0.4\,\text{mV}$ (1)
CMR	[0.39 V, 1.58 V]

(1) Estimated from MonteCarlo simulations.

complexity: as it will be shown in the examples of Sec. IV-D, with the rakeness approach we are able to accurately reconstruct many different ECG signals (including waveforms presenting irregularities as motion artifacts or arrhythmia) by using only $M = 16$ measurements. Relying on a standard CS approach (i.e. using random i.i.d. sequences) values as large as $M = 64$ are required [21].

III. AIC PROTOTYPE ARCHITECTURE

Starting from the block diagram of Fig. 2, we have designed a 16-channel RMPI-based AIC prototype. The core of the proposed circuit is a low-power fully-differential SC integrator shown in the dashed box of Fig. 3 that implements a binary antipodal modulation, where multiplication with the $\phi_{j,i}$ is achieved by means of simple switches that swap the differential input signal pair (see the "modulator" block in Fig. 3).

In the following we describe the circuit behavior with emphasis on non-conventional solutions we adopted to cope with some hardware-related CS issues, in particular:

- time continuity for correct processing of all signal slices;
- saturation of the SC integrators;
- data corruption due to leakage currents.

We will address each of them, respectively, in Sec. III-A, III-B and III-C. The performances of each RMPI channel are summarized in Table I.

To allow a monolithic design, we also embed a low-power SAR based ADC in our prototype. It is based on a fully differential architecture, with two differential capacitive array dividers, and can operate at a rate up to $200\,\text{kS/s}$. The architecture of the SAR is detailed in Section III-D.

A. Switched Capacitor RMPI with time continuity

The architecture of a single RMPI channel (including the output buffer that is shared between all 16 channels) is detailed in Fig. 3. Basically, it can be described as a standard fully-differential SC integrator, with differential input signal voltage $V_x^D = V_x^+ - V_x^-$ and common mode voltage V_{CM}, and regulated by the two non-overlapping clock signals PHI_1 and PHI_2 of period T. The main differences with respect to a standard SC integrator can be summarized in two additional switches at the input stage to select whether the signal to be integrated is V_x^D or $-V_x^D$, and two couples of feedback capacitors C_F^I and C_F^{II} with same value $C_F^I = C_F^{II} = C_F$.

The latter capacitors are used to solve the problem of ensuring continuity between successive windows of the input signal. Referring to Fig. 2, this issue can be described as follows. Let us assume that all M RMPI channels are processing the same slice. At the end of the time window, the M integrations are complete and the measurements are available. However, before processing a new signal window, the accumulated values have to be converted by the ADC and, after that, integrators must be reset to eliminate the charge accumulated in the feedback capacitors. Yet, either these two operations (i.e., ADC sampling and charge removal) are performed in a negligible time, or the same hardware cannot be used to process the successive slice of the input signal. To solve this impasse, one can rely on two couples of capacitors C_F^I and C_F^{II} to be connected to the op-amp by means of two switches couples controlled by the signals WND^I and WND^{II} as shown in Fig. 3.

To explain the behavior in more detail, let us refer to the control signals shown in Fig. 4 and assume that WND^I is high, so C_F^I is connected to the op-amp. The behavior of the circuit is the same as a standard SC integrator, where each integration step is divided in a sampling phase (PHI_1 high, PHI_2 low) and an evaluation phase (PHI_2 high, PHI_1 low). Let us consider the j-th RMPI channel and the i-th sampling phase. In order to achieve the multiplication between the input signal and $\phi_{j,i} \in \{+1, -1\}$, we exploit two additional pairs of MOS switches (as in Fig. 3) controlled by signals $\text{PHI}_{1\text{A}}^{(j)}$ and $\text{PHI}_{1\text{B}}^{(j)}$. When $\phi_{j,i} = 1$ then $\text{PHI}_{1\text{A}}^{(j)}$ is high and V_x^D charges C_S. Otherwise, when $\phi_{j,i} = -1$ then $\text{PHI}_{1\text{B}}^{(j)}$ is high and C_S is charged by $-V_x^D$. At the end of the sampling phase the charge stored on C_S, assuming a 50% duty cycle, is $Q_S = \frac{C_S}{2}\,\phi_{j,i}\,V_x^D(iT - T/2)$.

Then, in the evaluation phase PHI_1, $\text{PHI}_{1\text{A}}^{(j)}$ and $\text{PHI}_{1\text{B}}^{(j)}$ are reset and PHI_2 is set, and Q_S is moved to C_F^I. At the end of this transient, the differential op-amp output voltage $V_o^D = V_o^+ - V_o^-$ is

$$\begin{aligned} V_o^D(iT) &= -\frac{C_S}{C_F}\sum_{k=1}^{i}\phi_{j,k}\,V_x^D\left(kT - \frac{T}{2}\right) \\ &= g\sum_{k=1}^{i}\phi_{j,k}\,V_x^D\left(kT - \frac{T}{2}\right) \end{aligned} \tag{5}$$

where $g = -C_S/C_F$ is the gain of the integrator. After the N-th step the integration is complete and the op-amp output differential voltage represents the desired measurement

$$V_{y_j} = V_o^D(NT) = g\sum_{i=1}^{N}\phi_{j,i}\,V_x^D\left(iT - \frac{T}{2}\right) \tag{6}$$

The only remarkable difference between (1) and (6) is the integrator gain g. The choice of g in our prototype is discussed in Sec. III-B, while that of C_S and C_F is explained in Sec. III-C.

At the same instant when a time window ends and the successive one begins, WND^I goes low and WND^{II} high.

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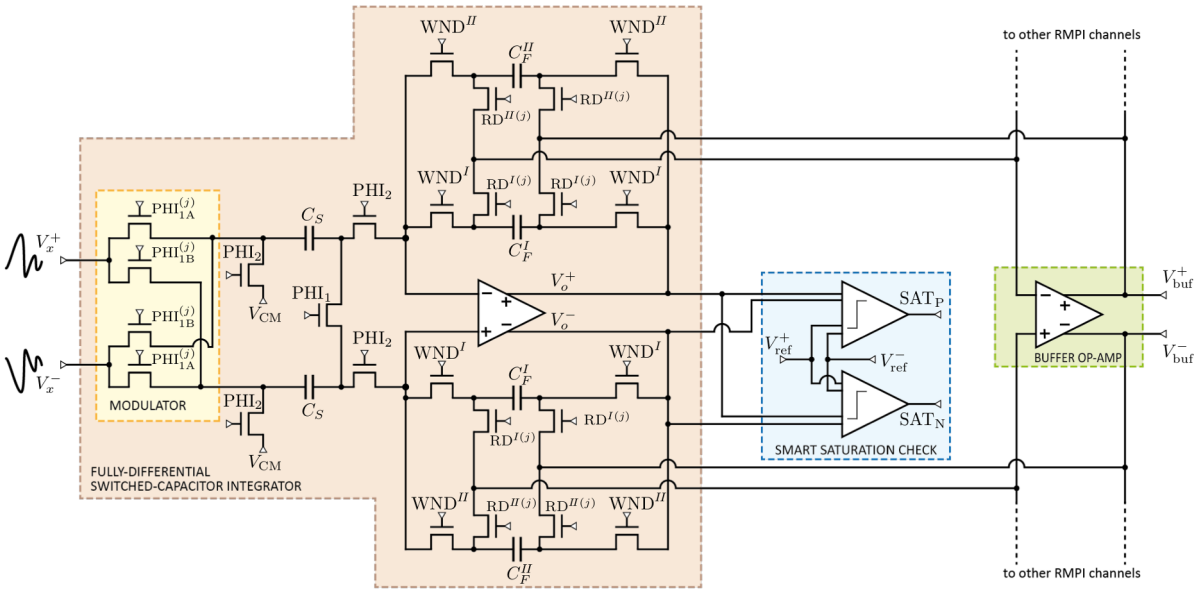


Fig. 3. Detailed architecture of the switched capacitor circuits implementing a single RMPI channel in the designed prototype, including the buffer shared between all RMPI channels.

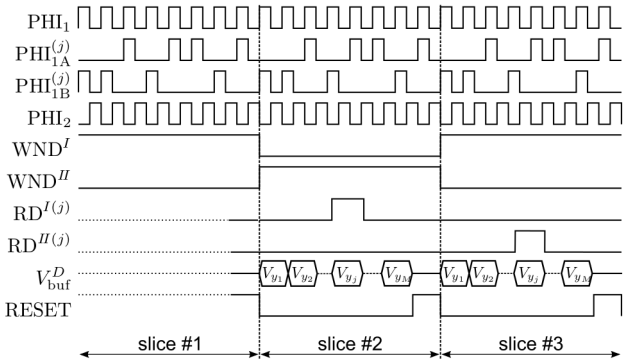


Fig. 4. Timing diagram for signals controlling the behavior of the j-th RMPI channel.

The capacitors C_F^I are therefore disconnected from the op-amp and they hold the sampled V_{y_j} value, while both C_F^{II} (assumed uncharged) are connected and a new integration can start immediately. Then, the C_F^I from all stages are sequentially connected to the buffer op-amp (signal $\mathrm{RD}^{I(j)}$ set), thus either charging the internal ADC input buffer or making the measurements externally available as a differential voltage signal. After that, a RESET signal (not shown in Fig. 3 for the sake of simplicity) is provided, and the C_F^I are completely discharged, making them ready to be used in a new integration process.

The advantage of this approach is to ensures time continuity at a small cost in terms of area requirement, but at no cost in terms of power. In fact, we need only a replication of the C_F and a few additional small switches, but no active devices such as amplifiers or active sample/hold circuits.

B. Smart Saturation Checking

In the designed prototype we set the integrator gain $g = -1/8$. This choice is actually a trade-off involving many other circuit design parameters. In fact, as shown in detail in [23], the central limit theorem can be applied to the sum in (6) so that, for large N (as in the biomedical signals case) the V_{y_j} can be approximated with a zero-mean Gaussian random variable. As a consequence, V_{y_j} may assume very large values, but the majority of the observed cases are located around the mean value $V_{y_j} = 0$. Furthermore, since the V_{y_j} are proportional to g, their standard deviation is proportional to $|g|$. Assuming that the back-end ADC is linear and that its conversion range is fixed, setting a low $|g|$ would prevent large V_{y_j} occurrences, so that all measurements would be converted correctly. Yet, in most cases the V_{y_j} would span only a range of few ADC bits, with very poor performance in terms of signal-to-quantization noise ratio. Conversely, increasing $|g|$ will also increase the ADC conversion performance, but many V_{y_j} may fall outside the ADC conversion range, i.e., we have to deal with *saturated measurements*.

The situation must be even more carefully addressed when rakeness-based CS is considered. Aiming to maximize ρ, the rakeness approach also does so for the standard deviation of the V_{y_j} thus increasing the probability of saturation events to occur. The value of $|g|$ must therefore be further reduced with respect to the standard CS case.

In order to mitigate all the aforementioned constraints on the choice of g, we have embedded in our design a smart saturation checking capability by adding two comparators for each RMPI channel (see Fig. 3). This is the second important step in our joint hardware-algorithms optimization of the AIC architecture. More specifically, these comparators are used to check if the intermediate accumulated voltage $V_o^D(iT)$ in (5) goes above or below the two threshold levels V_{ref}^D and $-V_{\mathrm{ref}}^D$ (with $V_{\mathrm{ref}}^D = V_{\mathrm{ref}}^+ - V_{\mathrm{ref}}^-$), as suggested in [23]. In such case, a flag signal (either $\mathrm{SAT_P}$ or $\mathrm{SAT_N}$) is generated, to indicated the instant in which the channel saturated.

The advantage of this approach is twofold and it is explained

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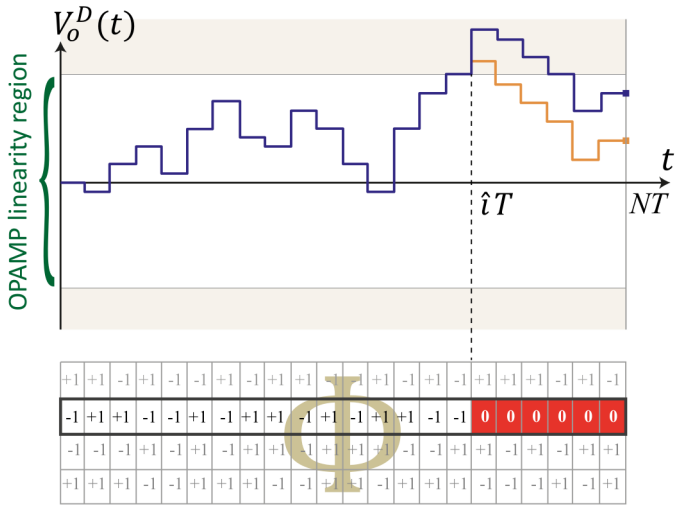


Fig. 5. Saturation of the op-amp may result in an actual $V_o^D(t)$ (light line in the top plot) completely different from the ideal expected one (dark line), ending in *corrupted* measurements. The information that $V_o^D(\hat{\imath}T) \approx \pm V_{\text{ref}}^D$ can be exploited in the reconstruction algorithm by zero-padding all $\phi_{j,i}$ terms with $\hat{\imath} \leq i \leq N$ and by assuming that the integrator output is $\pm V_{\text{ref}}^D$.

in details in [23]. Here, it is enough to say that the first positive feature of this approach is the ability to detect and avoid *corrupted* measurements. The main problem here is not that the measurement $V_{y_j} = V_o^D(NT)$ may fall outside of the conversion range of the ADC [36]. This event in fact can be easily detected, as these measurements are automatically converted either to the maximum or minimum digital value, and can be ignored by the reconstruction algorithm. The problem occurs when, conversely, $V_o^D(iT)$ reaches the op-amp saturation level at a time step $\hat{\imath} < N$: in this case, the final value $V_o^D(NT)$ is irreparably corrupted, as in the example of Fig. 5. Note that, depending on the values of $\phi_{j,i}$ and V_x^D for time steps between $\hat{\imath}$ and N, the $V_o^D(NT)$ may actually fall in the ADC conversion range as in Fig. 5. Of course, simply examining $V_o^D(NT)$ is not useful for detecting these events.

To highlight the second positive feature, we can recall that the philosophy underlying the entire CS framework is to recover a signal with the lowest possible amount of information, so M is usually not far from its lower bound in (3). With this assumption, discarding even a single measurement may lead to an insufficient quantity of information to correctly reconstruct the signal. Our idea is to recover some amount of information by replacing the corrupted j-th measurement with the last reliable knowledge we have on the j-th channel before its state is corrupted, i.e., $V_o^D(\hat{\imath}T) \approx \pm V_{\text{ref}}^D$. This can be easily fed in any reconstruction algorithm: to match (6) with the saturation information it is enough to set to zero in the reconstruction algorithm all terms in the $\phi_{j,i}$ with $\hat{\imath} < i \leq N$ as illustrated in Fig. 5, and to assume that the integrator output is $V_{y_j} = \pm V_{\text{ref}}^D$. When $\hat{\imath}$ is large, only a few terms in the $\phi_{j,i}$ are zeroed, and this ensures to the reconstruction algorithm almost the same quantity of information of an unsaturated measurement. Of course, if multiple saturation events are detected on the same channel, only the first one can be used, since the time position of the following ones may be corrupted.

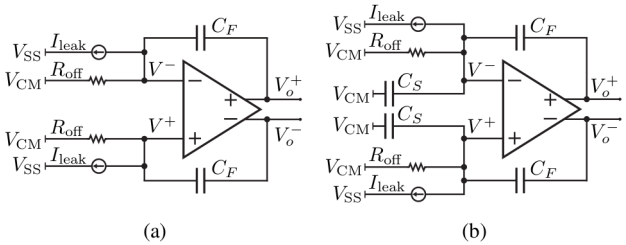


Fig. 6. Simplified equivalent SC circuit model for computing the effects of leakage currents. (a): Sampling phase; (b): evaluation phase.

Note that the overhead in terms of area and power consumption for applying this strategy is very limited, since only two comparators are required, that have been implemented as dynamic ones and without any particular speed or accuracy requirement. Moreover, as shown in the example of Sec. IV-B it is possible to achieve accurate signal reconstruction even in presence of more than 60% in saturated measurements.

C. Leakage effects

As already mentioned, all biomedical signals exhibit the sparsity property and can therefore be acquired using CS. Yet this happens only when the integration time NT is long enough, sometimes up to a few seconds [14], [37]. Consequently, using an AIC not specifically designed to work with very long NT may result in poor performance.

For instance, referring to the proposed architecture, if NT is very long, then the charge accumulated into either the C_F^I or the C_F^{II} may be corrupted by leakage currents. This issue must be taken into account in the design phase of the circuit.

To model the leakage on each RMPI channel we can use the simplified equivalent circuit of Fig. 6(a) for the sampling phase, and of Fig. 6(b) for the evaluation phase. The quantities R_{off} and I_{leak} are used to model, respectively, the source/drain current of all MOS switches in the off state, and the source/bulk and drain/bulk junctions inverse current, and have been computed according to the parameters of the CMOS technology exploited in our implementation. Additionally, the op-amp is modeled as an ideal amplifier with a limited differential gain A_d and a non-zero offset V_{off}, such that $V_o^D = A_d(V^+ - V^- - V_{\text{off}})$.

The evolution of the two circuits is simply studied, resulting in negative exponential voltage drops, as analyzed in [38]. More specifically, there is a common mode drop at the op-amp inputs, and a differential drop at the op-amp outputs. In both phases, the input common mode drop is fast, with a final voltage level equal to $V_{CM} - R_{\text{off}} I_{\text{leak}}$ which (for typical value of R_{off} and I_{leak}) is always in the op-amp common mode range; this issue is therefore not critical. On the contrary, the differential output drop is very slow (the associated time constant is $\approx A_d C_F R_{\text{off}}$) and the drop is linearly increasing with V_{off}.

The above observations have been exploited for determining the values of C_S and C_F. Aiming at an integration time of $NT \approx 1\,\text{s}$ (that is enough for all biomedical signals of interest) we carefully designed the op-amp to get a very high A_d and a very low V_{off}. Furthermore, we adopted minimum size NMOS

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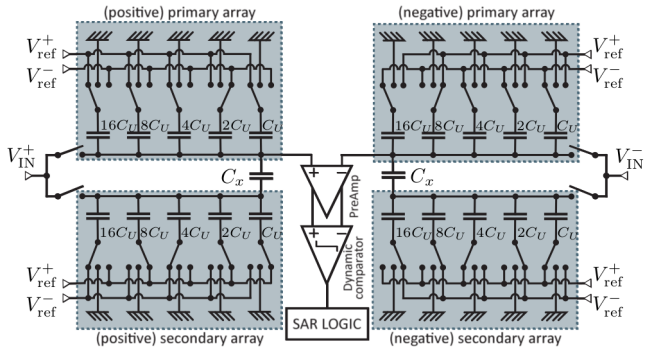


Fig. 7. Basic architecture of the SAR ADC.

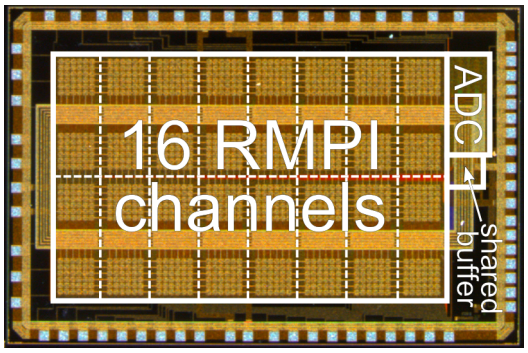


Fig. 8. Microphotograph of the designed integrated circuit.

switches, thus reducing the impact of both $R_{\rm off}$ and of $I_{\rm leak}$. According to the obtained values and to the developed model, and without applying any digital compensation technique [38], the differential voltage dropout is comparable to the ADC less significant bit (LSB) for a $NT = 1\,\mathrm{s}$ when $C_F \approx 40\,\mathrm{pF}$. To get $g = -1/8$, we set $C_S = 5\,\mathrm{pF}$ and $C_F = 40\,\mathrm{pF}$.

D. SAR ADC

The designed ADC is a standard 11-bit fully differential SAR converter [39]. The schematic is depicted in Fig. 7, and it is based on two couples of split capacitor arrays (a main couple and a secondary couple) with unit capacitance $C_U = 470\,\mathrm{fF}$, that scale the sampled voltage by means of charge redistribution to obtain successive approximations of the conversion. Due to the differential architecture, the first bit is obtained by a direct comparison between the differential pair generating the input signal, while other 5 bits are achieved by switching the main array, and 5 additional bits by switching the secondary one. Main and secondary arrays are connected together by a capacitance $C_x = C_U$ as in [40]. The comparator is based on a dynamic clocked architecture, and it is driven by a very small and low-power static preamplifier to decouple the comparator from the two arrays, thus increasing performance.

IV. Circuit Measurements

The circuit described in Sec. III has been designed and fabricated in Texas Instruments $180\,\mathrm{nm}$ $1.8\,\mathrm{V}$ CMOS technology. The microphotograph of the circuit is depicted in Fig. 8. The total circuit size is $2.3 \times 3.7\,\mathrm{mm}^2$.

TABLE II
SAR-based ADC performance summary.

Parameter	Value
Area	$320 \times 770\,\mu\mathrm{m}^2$
power consumption ($100\,\mathrm{kS/s}$) @$1.8\,\mathrm{V}$	$10.08\,\mu\mathrm{W}$
Dynamic Range ($100\,\mathrm{kS/s}$, $f_{\rm in} = 100\,\mathrm{Hz}$)	$64.2\,\mathrm{dB}$
ENOB	$8.99\,\mathrm{bit}$
INL	$< 3.4\,\mathrm{LSB}$
max. conversion speed	$200\,\mathrm{kS/s}$
Figure of Merit ($100\,\mathrm{kS/s}$)	$198\,\mathrm{fJ/c.-l.}$

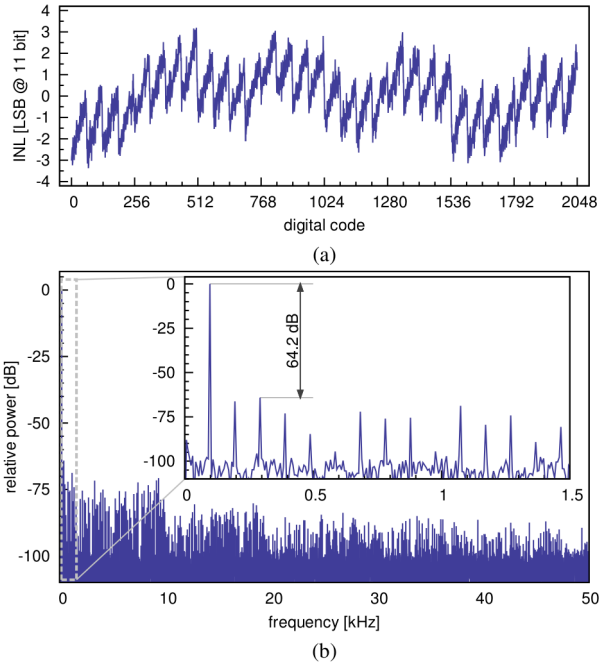


Fig. 9. Performance of the the SAR-based ADC. (a): Integral non-linearity; (b): spurious free dynamic range.

The designed integrated circuit possesses 16 RMPI channels and the $11\,\mathrm{bit}$ SAR ADC. The digital control logic (excluding that of the SAR) has not been embedded for maximum versatility, and all the measurements presented here have been obtained by controlling the designed circuit with a Xilinx Spartan 3E FPGA. The FPGA embeds the sensing matrix Φ in a memory-block, and also controls an external digital-to-analog converter that is used to generate the reference voltages and the differential input test signal.

This experimental measurements section is divided into two parts. The first one is dedicated to measuring the circuit performance with some suitable test signals. This is particularly important, since, as AICs have only been introduced recently, no standard testing procedure has been established yet. We here propose an approach based on three steps:

- first (Sec. IV-A), we measure performance of the SAR converter in the standard way;
- second (Sec. IV-B), by using two different suitable and artificially created sparse signals we show the overall CS system performance in terms of reconstruction signal-to-noise ratio (SNR), defined as

$$\mathrm{SNR_{dB}} = 20 \log \left(\frac{\|x\|_2}{\|x - \hat{x}\|_2} \right)$$

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This allows us to determine the quality of the basic functionality of the RMPI architecture, i.e., its ability to accurately acquire very simple sparse signals.
Due to the complexity of a CS system, it will not be easy to evaluate if the measured performance is aligned with the expected one. To this aim, in all examples we compute also the reconstruction SNR of an ideal RMPI system followed by an 11 bit ADC as a benchmark upper bound value. By comparing the ideal and the measured SNR, it is possible to estimate the loss due to disturbances and circuit nonidealities. This is actually equivalent to the comparison of the ideal and measured dynamic range in ADC testing when computing the effective number of bits.
We also provide the SNR of the actual measurements V_{y_j} with respect to the ideal expected ones (we define this as measurements SNR), and the evaluation of the maximum and minimum operating frequency;

- third (Sec. IV-C), the same sparse signals are used to test the system in presence of saturation events by increasing their amplitude. This allows to determine the AIC performance in presence of an increasing level of saturation and to guarantee the correct functionality of the AIC even when such events are present.

In the second part of the Section (Sec. IV-D) we test the behavior of the AIC by using real ECGs and EMGs taken from the PhysioNet database [41].

A. SAR ADC

The performance of the ADC is summarized in Table II. The integral non-linearity (INL) is within 3.4 LSB at 11 bit resolution – see Fig. 9(a) –, the spurious free dynamic range is measured as 64.2 dB – see Fig. 9(b) – and the effective number of bits (ENOB) is evaluated in approximately 9 bits. With a measured power consumption of 10.08 μW at 100 kS/s, the ADC figure of merit (defined as energy required per conversion per effective number of levels) is 198 fJ/conversion-level [42].

B. AIC, synthetic sparse signal tests

To properly determine all the features of the proposed AIC, we refer to two different settings based on two suitably synthesized sparse test signals.

In the first case, we have considered an input signal which is sparse in the basis of the normalized unit pulses, i.e.:

$$x(t) = \sum_{i=1}^{N} \alpha_i \, \mathrm{u}\,(t/T - i) \tag{7}$$

where $\mathrm{u}(t) = 1, \ 0 < t < 1$ and 0 elsewhere. Furthermore, we set $N = 20$ and a sparsity level $K = 2$, i.e. only 10% of the α_i are non zero. Using (3), the minimum number of measurements required for an accurate signal reconstruction in this setting is $M_{\min} = 8$. Accordingly, we enable only the first 8 RMPI channels of the designed circuit.

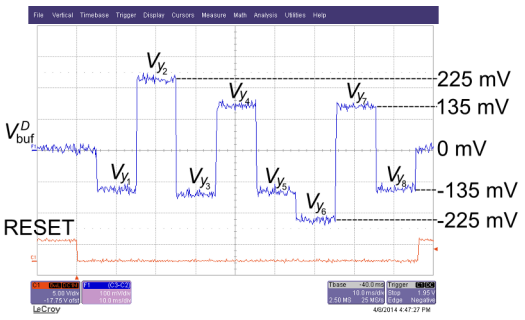


Fig. 10. Differential internal buffer output voltage (top trace) for the example of Sec. IV-B, showing the 8 measurements serially output by the multiplexer, and distributed according the 4 possible cases computed in (9). The bottom trace is the RESET signal.

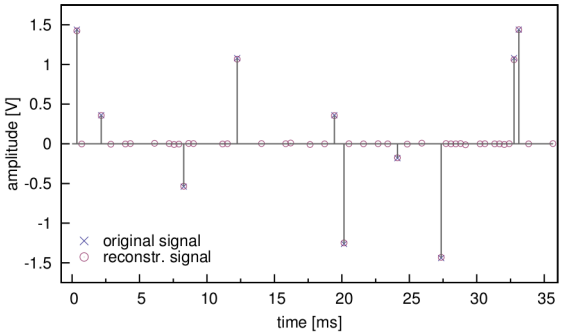


Fig. 11. Example of reconstruction of a signal with $N = 20$, $K = 2$ and $M = 8$ sparse on the canonical basis, 5 time windows with $NT = 7.2$ ms are plotted. Steps with non-vanishing amplitude are highlighted with a marker.

As an example, given the input signal sparse representation with

$$\begin{aligned} \alpha_2 &= 1.44\,\mathrm{V} \\ \alpha_7 &= 0.36\,\mathrm{V} \\ \alpha_i &= 0, \quad i \neq 2, i \neq 7 \end{aligned} \tag{8}$$

then the j-th measurement depends only on $\phi_{j,2}$ and $\phi_{j,7}$, and more precisely, accordingly to (6)

$$V_{y_j} = \begin{cases} -225\,\mathrm{mV} & \phi_{j,2} = 1 \text{ and } \phi_{\mathrm{j},7} = 1 \\ -135\,\mathrm{mV} & \phi_{j,2} = 1 \text{ and } \phi_{\mathrm{j},7} = -1 \\ 135\,\mathrm{mV} & \phi_{j,2} = -1 \text{ and } \phi_{\mathrm{j},7} = 1 \\ 225\,\mathrm{mV} & \phi_{j,2} = -1 \text{ and } \phi_{\mathrm{j},7} = -1 \end{cases} \tag{9}$$

The differential output $V^D_{\mathrm{buf}} = V^+_{\mathrm{buf}} - V^-_{\mathrm{buf}}$ of the internal buffer (see Fig. 3) for this example has been made externally available, and is shown in Fig 10. In the figure one can clearly identify the 8 measurements serially appearing at the output the multiplexer, each one having one of the possible values identified in (9).

In this example, an ideal RMPI system will reconstruct the input signal with a SNR of 49.0 dB. By using the designed prototype with $T = 360\,\mu$s, i.e., with a SC frequency equal to $f_s = 1/T = 2.78$ kHz, we get an average measurements SNR equal to 39.6 dB, and an average reconstruction SNR equal to 37.7 dB. An example showing both the input signal and the reconstructed signal over 5 consecutive time windows is depicted in Fig. 11.

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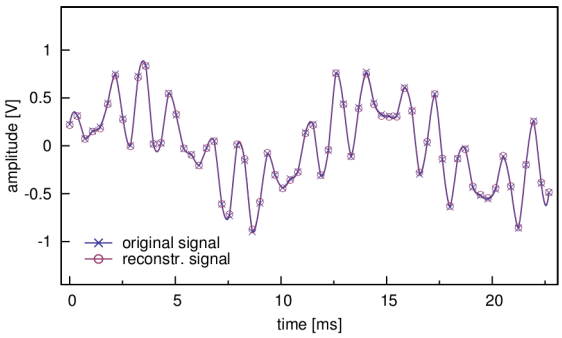


Fig. 12. Example of reconstruction of a signal with $N = 64$, $K = 3$ and $M = 16$ sparse on the Fourier basis, a single time windows with $NT = 23\,\mathrm{ms}$ is plotted. Actual sampling points are highlighted with a marker.

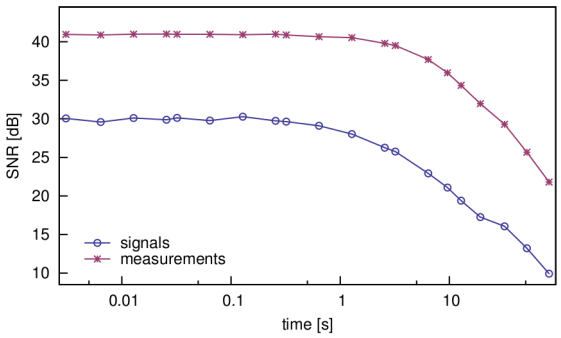


Fig. 13. Measurements SNR and reconstruction SNR for the Fourier sparse signal with $N = 64$, $K = 3$ and $M = 16$, for different time window lengths $T_W = NT$.

The second case is more complex and deals with a synthetic signal sparse in the Fourier basis, i.e.,

$$x(t) = \sum_{i=1}^{N/2-1} \alpha_i \sin(i\,t) + \sum_{i=N/2}^{N} \alpha_i \cos((N-i)t) \qquad (10)$$

For this setup, we set $N = 64$ and $K = 3$. In this case, to ensure accurate reconstruction we get from (3) that $M_{\min} = 16$; as such we use all channels of the RMPI prototype. With this setting system level simulations of an ideal system achieve a reconstruction SNR of $47.9\,\mathrm{dB}$. In the designed prototype, with $T = 360\,\mu\mathrm{s}$ (i.e. $f_s = 2.78\,\mathrm{kHz}$) measurements indicate an average SNR of $40.9\,\mathrm{dB}$ for actual V_{y_j}, and a reconstruction SNR of $30.0\,\mathrm{dB}$. The input and the reconstructed signal for this example in a single time window have been depicted in Fig. 12.

The latter setting has been also used for testing the behavior of the circuit at different clock speed. In particular, the maximum working speed for the designed circuit has been measured in approximately $f_s = 125\,\mathrm{kHz}$. For any clock speed below this limit, the measurements SNR is approximately constant around $41\,\mathrm{dB}$, and the reconstruction SNR is about $30\,\mathrm{dB}$.

The lower bound in speed is set by constraints imposed by the leakage currents as described in Sec. III-C. Performance for different f_s is shown in Fig. 13. In the figure we have plotted both measurements SNR (top plot) and reconstruction SNR (bottom plot) as functions of the integration window length $NT = N/f_s$, that is the actual parameter determining the voltage drop due to leakage. We can see that performance is constant up to NT in the order of magnitude of the second. If we define the maximum integration time as the NT where we have a $3\,\mathrm{dB}$ reconstruction SNR loss, we have $NT < 1.6\,\mathrm{s}$. This validates the developed leakage model, and ensures that the designed circuit can be correctly employed for the acquisition of biomedical signals.

A performance summary of all examples considered in this section can be found in Table III.

TABLE III
PERFORMANCE SUMMARY FOR TESTS BASED ON SYNTHETIC SIGNALS.

	canonical basis	Fourier basis
setting	$N = 20$, $K = 2$	$N = 64$, $K = 3$
frequency	$f_s = 2.78\,\mathrm{kHz}$	$f_s = 2.78\,\mathrm{kHz}$
time window length	$NT = 7.2\,\mathrm{ms}$	$NT = 23\,\mathrm{ms}$
measurements	$M = 8$	$M = 16$
theoretical rec. SNR	$< 49.0\,\mathrm{dB}$	$< 47.9\,\mathrm{dB}$
power consumption	$251\,\mu\mathrm{W}$	$495\,\mu\mathrm{W}$
measurements SNR	$39.6\,\mathrm{dB}$	$40.9\,\mathrm{dB}$
reconstruction SNR	$37.7\,\mathrm{dB}$	$30.0\,\mathrm{dB}$
max. working frequency	–	$f_s < 125\,\mathrm{kHz}$
max. time windows length	–	$NT < 1.6\,\mathrm{s}$

C. Saturation Checking Test

In this section we present results achieved with the same parameters of the Fourier-basis example of Sec. IV-B, and using the same input signal depicted in Fig. 12 but scaled by a factor $0 < s \leq 2$. For $s \leq 1$ none of the 16 used RMPI channels reaches final or intermediate saturation. Furthermore, for $s = 1$ the measurements V_{y_j} exploit almost all the ADC conversion range to maximize the signal-to-quantization noise. For values larger than $s = 1$, some saturation events are observed. Results are shown in Fig. 14.

For very low values of s we can observe a low performance, mainly due to the low V_{y_i} energy (that is actually scaled with s) and the associated low signal-to-quantization noise ratio. As s increases, the measurements SNR and consequently the reconstruction SNR increases.

For $s > 1$ we cannot define anymore a measurements

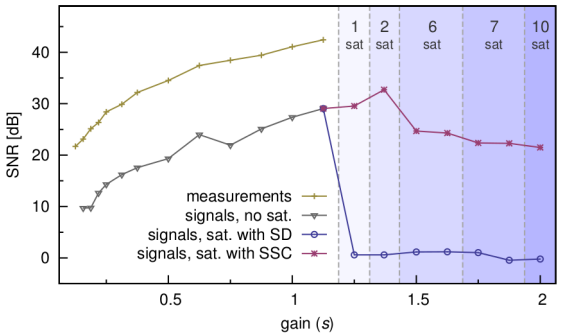


Fig. 14. Performance of the Fourier basis example at different signal gain s. The plot include both measurements SNR and reconstruction SNR when adopting the proposed smart saturation check (SSC) and when saturated measurements are simply dropped (SD). The number of saturated measurements per time window is also indicated.

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SNR, and we need to use the instants of saturation events to recover the input signal as in Sec. III-B. Intriguingly, when smart saturation checking is employed (see plot SSC in Fig. 14) performance is still increasing with s when only a limited number of saturation events are detected. This can be intuitively explained as due to two effects. First, here only a few of the 16 RMPI channels saturates, and most probably all the saturation events are observed at the end of the integration windows. The quantity of information recovered from saturation instants almost matches that of the V_{y_j}. Second, the values of non-saturated measurements is increasing, and so their conversions accuracy.

However, when both s and the number of saturated measurements further increase, we expect that many saturation events will be located far from the end of the integration window, so that the quantity of available information decreases, and the reconstruction performance with it. Yet, we are still able to reconstruct the input signal with an acceptable SNR. Note that for $s = 2$ we still have approximately $22\,\mathrm{dB}$ of reconstruction SNR when most of the measurements (i.e., 10 out of 16) reach saturation.

To fully understand the advantages of the saturation checking approach, we can compare results achieved when reconstruction is performed only with "good measurements", i.e., when measurements are dropped anytime a saturation event is detected as suggested in [36] (see plot SD in Fig. 5). Since M is taken as its minimum value according to (3), dropping saturated measurements reduces the data available to the CS decoder to an insufficient level, and, as expected, one is not able anymore to correctly reconstruct the input signal. As we can see in the figure, the reconstruction SNR has, in fact, an abrupt fall at $s \approx 1$, an event which does not occur in the SSC plot.

In conclusion, when using the saturation checking approach, optimal performance is achieved when the amplitude of the input signal is such that only a few measurements saturate. More importantly, performance gradually decreases when the input signal amplitude is either increased or decreased, but without any abrupt change. This is potentially very useful for biomedical signals, where amplitude may suddenly change or contact impedance can substantially vary. Conversely, this issue is critical in classical approaches, since input signal amplitude has always to be kept within a "safe range" in order to avoid saturation and an abrupt decrease in performance in case the input signal has an unexpected high peak value.

D. Test with real biomedical signals

To complete the testing of the prototype, we consider in this section real biomedical signals. More precisely, we take into account ECG and EEG signals (including regular, irregular and pathological ones) recorded from undisclosed healthy/unhealthy patients and made publicly available by the PhysioNet project [41]. In both cases, the rakeness approach has been exploited[4]. Only two rakeness-based sensing matrices (one for the ECG, one for the EEG) have been used in all the following examples. The correlation profile C^x, required to solve (4) has been estimated over a training set composed by a large amount of instances. Conversely, the presented examples refer to a different data set. This ensures the maximum fairness, since the C^x are not biased on any particular considered signal.

In the first example we consider an ECG signal with an heart-beat of approximately $1\,\mathrm{Hz}$ from a healthy patient. The signal is sampled at $f_s = 256\,\mathrm{Hz}$ and we use a time windows of length $NT = 0.5\,\mathrm{s}$, so $N = 128$. The number of

[4]The code used to generate the antipodal rakeness-based sensing matrices is available online at http://cs.signalprocessing.it.

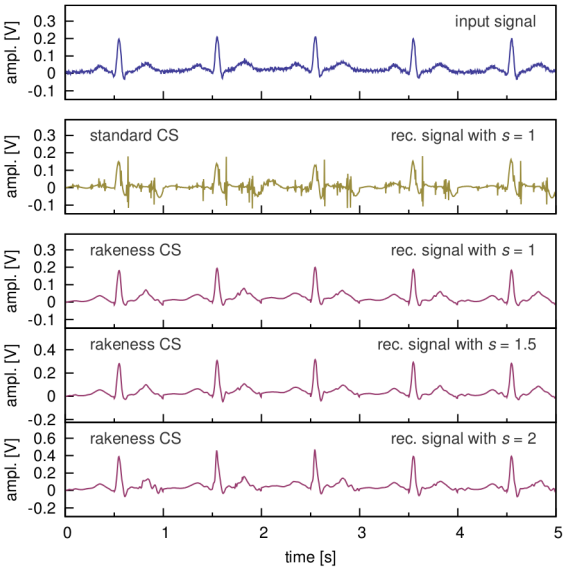


Fig. 15. Example of a real ECG signal with $f_s = 256\,\mathrm{Hz}$, $N = 128$, $M = 16$ (10 consecutive time windows are plotted). From top to bottom: input signal, reconstructed signal with the standard CS approach, i.e., by using independent $\phi_{j,i}$ symbols (no rakeness), and signal reconstructed using the rakeness CS with the three scale factor $s = 1$, $s = 1.5$ and $s = 2$.

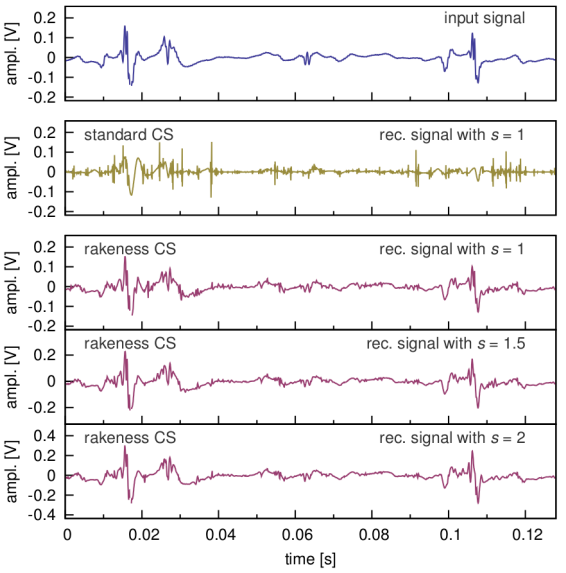
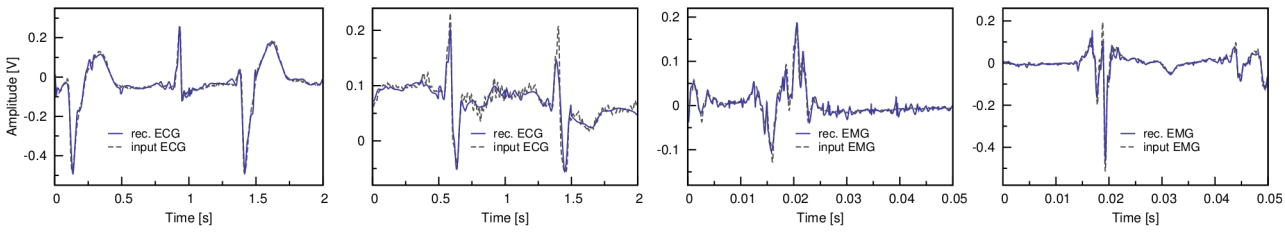


Fig. 16. Example of a real EMG signal with $f_s = 20\,\mathrm{kHz}$, $N = 256$, $M = 24$ (10 consecutive time windows are plotted). From top to bottom: input signal, reconstructed signal with the standard CS approach, i.e., by using independent $\phi_{j,i}$ symbols (no rakeness), and signal reconstructed using the rakeness CS with the three scale factor $s = 1$, $s = 1.5$ and $s = 2$.

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(a) Arrhythmia (b) Motion artifact (c) Myopathy (d) Neuropathy

Fig. 17. Short chunks of real pathological/irregular ECGs and EMGs (4 consecutive time windows are shown for each signal) compared with with the corresponding signals reconstructed by our AIC adopting the settings used in previous examples: (a) ECG signal track from a patient with arrhythmia (2.5 saturation events per time windows on average); (b) ECG signal corrupted by motion artifacts (1.75 saturation events per time windows); (c) EMG signal from a patient with myopathy (1.5 saturation events occur per time windows); (d) EMG signal from a patient with chronic low back pain and neuropathy (2 saturation events per time window).

measurement for each time windows is $M = 16$. The sparsity basis used for signal reconstruction is the Symmlet-6 family of the orthogonal Wavelet functions [43]. Results are shown in Fig. 15 using both the standard CS approach (i.e., the ϕ_j are i.i.d. binaries antipodal random vectors) and the rakeness approach, in the latter case, also for different input signal scale factors $s = \{1, 1.5, 2\}$. First, we can see that using a standard CS approach signal reconstruction is very poor, while exploiting the rakeness approach the performances are visibly much superior. Furthermore, we can see that the system is capable to tolerate a limited amount of saturation events. To show this, we have considered the input signal with three different scale factors, i.e., $s = 1$ where no saturation events are observed, $s = 1.5$ with an average number of 0.4 saturation events per time window, and $s = 2$, when 1.5 saturation events are detected per time windows. In all three cases the signal has been reconstructed without any noticeable performance loss. For all cases, the obtained compression factor is equal to $N/M = 8$.

In the second example we consider an EMG signal of an healthy patient. The EMG signal is usually sampled at a higher frequency with respect to the ECG [14], [37]. In this setting we consider $f_s = 20\,\mathrm{kHz}$, $N = 256$, with $NT = 12.8\,\mathrm{ms}$. The considered sparsity basis is, as in the previous example, the Symmlet-6 Wavelet function family, but, due to the high value of N, we have to set $M = 24$, which requires two IC prototypes to be simultaneously used. Results are shown in Fig. 16 for the standard and the rakeness approach, and for three different scale factors s. Again, we can see a clear failure in the reconstruction effort in the standard CS approach, while in the rakeness approach reconstruct of the input signal is successfully achieved for $s = 1$ (no saturation events detected), for $s = 1.5$ (an average of 1.2 saturation events per time window is present), and also for $s = 2$ (corresponding to 2.5 saturation events per time windows). The compression factor in this example is equal to $N/M \approx 10$.

Finally, we present a few tests on both irregular and pathological bio-signals. Fig. 17 shows small chunks of these uncommon signal instances taken from the Physionet database superimposed with the corresponding reconstructed signals. The system setting is the same as in the healthy cases considered above (i.e., $M = 16$ for ECG signals, and $M = 24$ for EEG signals). The input signal is always correctly reconstructed, even if a few saturation events are registered in all cases.

V. Conclusion

In this paper we have presented the hardware-algorithms co-design of a prototype of a CS-based AIC for biomedical signal acquisition implemented in Texas Instruments $180\,\mathrm{nm}$ CMOS technology. A rakeness based design of the CS acquisition sequences is exploited to increase the compression factor, thus reducing the amount of data necessary to represent the signal information content. Furthermore, the prototype includes a smart and innovative signal saturation checking mechanism, that allows to reconstruct the input signal even in presence of saturation with negligible costs in terms of hardware requirements. Measurements on real biomedical signals confirm the capability of the prototype to successfully acquire a signals with compression factor up to 8–10.

References

[1] M. A. Hanson, H. C. Powell, A. T. Barth, K. Ringgenberg, B. H. Calhoun, J. H. Aylor, J. Lach, "Body Area Sensor Networks: Challenges and Opportunities", *Computer*, vol.42, no.1, pp. 58–65, Jan. 2009.

[2] M. Khayatzadeh, X. Zhang, J. Tan, W. Liew, Y. Lian, "A 0.7-V 17.4-μW 3-Lead Wireless ECG SoC", *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 5, pp. 583–592, Oct. 2013.

[3] Y. Li, D. Zhao, W. A. Serdijn, "A Sub-Microwatt Asynchronous Level-Crossing ADC for Biomedical Applications", *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 2, pp. 149–157, April 2013.

[4] A. Rodriguez-Perez, M. Delgado-Restituto, F. Medeiro, A, "515 nW, 0-18 dB Programmable Gain Analog-to-Digital Converter for In-Channel Neural Recording Interfaces", *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 3, pp. 358–370, June 2014.

[5] D. L. Donoho, "Compressed Sensing," *IEEE Transactions on Information Theory*, vol. 52, no. 4, pp. 1289–1306, Apr. 2006.

[6] E. J. Candes, J. K. Romberg, K. Justin, and T. Tao, "Stable signal recovery from incomplete and inaccurate measurements," *Communications on Pure and Applied Mathematics*, vol. 59, no. 8, pp. 1207–1223, Aug. 2006.

[7] E. J. Candes and M. B. Wakin, "An Introduction to Compressive Sampling," *IEEE Signal Processing Magazine*, vol. 25, no. 2, pp. 21–30, Mar. 2008.

[8] J. Haboba, M. Mangia, F. Pareschi, R. Rovatti, and G. Setti, "A pragmatic look at some compressive sensing architectures with saturation and quantization," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 3, pp. 443–459, Sep. 2012.

[9] A.M.R. Dixon, E.G. Allstot, D. Gangopadhyay, D.J. Allstot, "Compressed Sensing System Considerations for ECG and EMG Wireless Biosensors", *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, no. 2, pp. 156–166, April 2012.

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[10] C. E. Shannon, "A Mathematical Theory of Communication," *The Bell System Technical Journal*, vol. 27, no. 3, pp. 379–423, Jul. 1948.

[11] U. Anliker *et al.*, "AMON: a wearable multiparameter medical monitoring and alert system," *IEEE Transactions on Information Technology in Biomedicine*, vol. 8, no. 4, pp. 415–427, Dec. 2004.

[12] E. Jovanov, A. Milenkovic, C. Otto, and P. de Groen, "A wireless body area network of intelligent motion sensors for computer assisted physical rehabilitation," *Journal of NeuroEngineering and Rehabilitation*, vol. 2, pp. 1–10, Mar. 2005.

[13] M. Lustig, D. Donoho, J. Santos, and J. Pauly, "Compressed Sensing MRI," *IEEE Signal Processing Magazine*, vol. 25, no. 2, pp. 72–82, Mar. 2008.

[14] F. Chen, A. Chandrakasan, and V. Stojanovic, "A signal-agnostic compressed sensing acquisition system for wireless and implantable sensors," in *Procceedings of 2010 IEEE Custom Integrated Circuits Conference*, Sep. 2010, pp. 1–4.

[15] H. Mamaghanian, N. Khaled, D. Atienza, and P. Vandergheynst, "Compressed Sensing for Real-Time Energy-Efficient ECG Compression on Wireless Body Sensor Nodes," *IEEE Transactions on Biomedical Engineering*, vol. 58, no. 9, pp. 2456–2466, Sept 2011.

[16] L. Bai and S. Roy, "Compressive Spectrum Sensing Using a Bandpass Sampling Architecture," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on*, vol. 2, no. 3, pp. 433–442, Sep. 2012.

[17] J. Zhang, Y. Suo, S. Mitra, S. Chin, S. Hsiao, R. F. Yazicioglu, T. D. Tran, and R. Etienne-Cummings, "An Efficient and Compact Compressed Sensing Microsystem for Implantable Neural Recordings," *IEEE Trans. Biomedical Circ. and Systems*, vol. 8, no. 4, pp. 485–496, Aug. 2014.

[18] X. Chen, E. Sobhy, Z. Yu, S. Hoyos, J. Silva-Martinez, S. Palermo, and B. Sadler, "A Sub-Nyquist Rate Compressive Sensing Data Acquisition Front-End," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on*, vol. 2, no. 3, pp. 542–551, Sep. 2012.

[19] J. Yoo, S. Becker, M. Loh, M. Monge, E. Candes, and A. Emami-Neyestanak, "A 100MHz-2GHz 12.5x sub-Nyquist Rate Receiver in 90nm CMOS," *2012 IEEE Radio Frequency Integrated Circ. Symp.*, pp . 31–34, 2012.

[20] M. Shoaran, M. H. Kamal, C. Pollo, P. Vandergheynst, and A. Schmid, "Compact Low-Power Cortical Recording Architecture for Compressive Multichannel Data Acquisition," *IEEE Trans. Biomedical Circuits and Systems*, vol. 8, no. 6, pp. 857–870, Dec. 2014.

[21] D. Gangopadhyay, E. Allstot, A. Dixon, K. Natarajan, S. Gupta, and D. Allstot, "Compressed Sensing Analog Front-End for Bio-Sensor Applications," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 426–438, Feb. 2014.

[22] M. Mangia, R. Rovatti, and G. Setti, "Rakeness in the Design of Analog-to-Information Conversion of Sparse and Localized Signals," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 5, pp. 1001–1014, May 2012.

[23] M. Mangia, F. Pareschi, R. Rovatti, G. Setti, and G. Frattini, "Coping with saturating projection stages in RMPI-based Compressive Sensing," in *Proceedings of 2012 IEEE International Symposium on Circuits and Systems*, May 2012, pp. 2805–2808.

[24] J. N. Laska, S. Kirolos, M. F. Duarte, T. S. Ragheb, R. G. Baraniuk, and Y. Massoud, "Theory and Implementation of an Analog-to-Information Converter using Random Demodulation," in *Proceedings of 2007 IEEE International Symposium on Circuits and Systems*, May 2007, pp. 1959–1962.

[25] E. Candes, "The restricted isometry property and its implications for compressed sensing," *Comptes Rendus Mathematique*, vol. 346, no. 9-10, pp. 589–592, May 2008.

[26] E. van den Berg and M. P. Friedlander, "Sparse optimization with least-squares constraints," *SIAM Journal on Optimization*, vol. 21, no. 4, pp. 1201–1229, 2011.

[27] M. Elad, " Optimized projections for compressed sensing", *Signal Processing IEEE Transactions on*, pp. 5695–5702, Dec. 2007.

[28] J. M. Duarte-Carvajalino and G. Sapiro, "Learning to sense sparse signals: Simultaneous sensing matrix and sparsifying dictionary optimization", *Image Processing, IEEE Transactions on*, pp. 1395-1408, July 2009.

[29] J. Xu, Y. Pi, Z. Cao, "Optimized projection matrix for compressive sensing," *EURASIP J. Adv. SignalProcess*, 2010.

[30] V. Cambareri, M. Mangia, F. Pareschi, R. Rovatti, and G. Setti, "A rakeness-based design flow for Analog-to-Information conversion by Compressive Sensing," in *Proceedings of the 2013 IEEE International Symposium on Circuits and Systems*, May 2013, pp. 1360–1363.

[31] R. Rovatti, G. Mazzini, G. Setti, S. Vitali, "Linear probability feedback processes," IEEE International Symposium on Circuits and Systems 2008, pp 548-55.

[32] R. Rovatti, G. Mazzini, G. Setti, "Memory-m Antipodal Processes: Spectral Analysis and Synthesis," IEEE Transactions on Circuits and Systems - I, vol. 56, n. 1, pp. 156-167, 2009.

[33] A. Caprara, F. Furini, A. Lodi, M. Mangia, R. Rovatti, G. Setti, "Generation of Antipodal Random Vectors With Prescribed Non-Stationary 2-nd Order Statistics," IEEE Transactions on Signal Processing, vol. 62, n. 6, pp 1603-1612, 2014.

[34] G. Jacovitti, A. Neri, G. Scarano, "Texture synthesis-by-analysis with hard-limited Gaussian processes," IEEE Transactions on Image Processing, vol.7, n.11, pp.1615–1621, Nov 1998.

[35] J.H. Van Vleck, D. Middleton, "The Spectrum of Clipped Noise," IEEE Proceedings, vol.54, n.1, pp. 2-19, 1966.

[36] J. N. Laska, P. T. Boufounos, M. A. Davenport, and R. G. Baraniuk, "Democracy in Action: Quantization, Saturation, and Compressive Sensing," *Applied and Computational Harmonic Analysis*, vol. 31, pp. 429–443, Nov. 2011.

[37] F. Chen, A. Chandrakasan, and V. Stojanovic, "Design and analysis of a hardware-efficient compressed sensing architecture for data compression in wireless sensors," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 3, pp. 744–756, Mar. 2012.

[38] M. Mangia, F. Pareschi, R. Rovatti, and G. Setti, "Leakage Compensation in Analog Random Modulation Pre-Integration Architectures for Biosignal Acquisition", *2014 IEEE Biomedical Circuits and System Conference*, pp. 432–435.

[39] B. Razavi, *Principles of Data Conversion System Design*. IEEE Press, 1995.

[40] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "An ultra-low power successive approximation A/D converter with time-domain comparator," *Analog Integr Circ Sig Process*, vol. 64, no. 2, pp. 183–190, Aug. 2010.

[41] A. L. Goldberger *et al.*, "PhysioBank, PhysioToolkit, and PhysioNet: Components of a new research resource for complex physiologic signals," *Circulation*, vol. 101, no. 23, pp. e215–e220, Jun. 2000.

[42] B. Murmann, "A/D converter trends: Power dissipation, scaling and digitally assisted architectures," *Custom Integrated Circuits Conference, 2008 (CICC2008)* pp 105-112, Sept. 2008.

[43] S. Mallat, *A Wavelet Tour of Signal Processing, Third Edition: The Sparse Way*, 3rd ed. Academic Press, 2008.



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