Time Stamp – A Novel Time-to-Digital Demodulation Method for Bioimpedance Implant Applications

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***Abstract*—Bioimpedance analysis is a non-invasive and inexpensive technology to investigate the electrical properties of biological tissues. The analysis requires demodulation to extract the real and imaginary parts of the impedance. Conventional systems use complex architectures such as I-Q demodulation. In this paper, a very simple alternative time-to-digital demodulation method or 'time stamp' is proposed. It employs only three comparators to identify or stamp in the time domain, the crossing points of the excitation signal and the measured signal. In a CMOS proof of concept design, the accuracy of impedance magnitude and phase is 97.06% and 98.81% respectively over a bandwidth of 10 kHz to 500 kHz. The effect of fractional-N synthesis is analysed for the counter-based zero crossing phase detector obtaining a finer phase resolution (0.51° at 500 kHz) using a counter clock frequency (f_{clk} = 12.5 MHz). Because of its circuit simplicity and ease of transmitting the time stamps, the method is very suited to implantable devices requiring low area and power consumption.**

***Index terms*—Bioimpedance, comparator, impedance demodulation, implantable devices, time-to-digital conversion.**

I. Introduction

BIOIMPEDANCE analysis is an inexpensive technology used to investigate the electrical properties of biological tissues [1]. It has a wide range of applications that can help in clinical status monitoring and diagnosis of diseases [2]. Example applications include human-machine interfaces [3], lung function monitoring [4], drug-screening [5], biosensing [6], and cancer detection [7].

Bioimpedance analysis is performed by injecting a known alternating current at different frequencies into the tissue and then recording a voltage response developed at the desired site on the tissue. The value of the real and imaginary parts of the measured impedance is derived from the magnitude and phase of the voltage response with respect to the excitation current. Such derivation, or demodulation, is the core of any bioimpedance measurement system, and its implementation often dictates the topology of other circuit blocks [8].

In-phase and quadrature (I-Q) demodulation is one of the most common methods used in bioimpedance analysis systems in both published papers [9]–[12], and commercial devices [13], [14]. The measured signal is multiplied by the I and Q signals at the same frequency as the current excitation. This demodulates the readout signal to dc with other frequency components modulated to higher frequencies that are rejected by low-pass filtering. This method requires the generation of the corresponding quadrature-phase signal, multipliers and low-pass filtering to obtain the I-Q components. In a digital approach, the measured signal is immediately digitized by an analog-to-digital converter (ADC) and multiplication and filtering are carried out in the digital domain. This contrasts with the analog approach, where these signals are generated, multiplied and filtered using analog circuits resulting in only two dc outputs to be digitized for further processing. It is reported in [15] that to achieve good signal-to-noise-ratio (SNR) and processing time, conventional approaches require complex circuits such as high order analog filters and high speed ADC which can be power demanding. Several methods have been used to reduce power consumption and design complexity, including square wave and pseudo-sine signals [11]. However, such techniques can suffer from significant errors due to the harmonics in the square waves. Elimination of these harmonic errors is a major concern [16], [17].

An alternative I-Q demodulation is the magnitude/phase detection method which employs peak and zero-crossing detection circuits [18]. The phase can be extracted with a simple counter, but the magnitude detection eventually results in a dc value that requires some form of digitization [19].

In recent research, bioimpedance analysis has been used to monitor the impedance changes which occur in neurons due to their activity [20], [21]. It may help to improve the localization of seizure foci in treatment-resistant epilepsy to aid surgical resection of the epileptogenic tissue [22]. For such small implantable devices including, for example, implantable impedimetric biosensors for monitoring blood biomarkers, an optimal design for demodulation will require minimal power consumption and an output signal that can be easily transmitted by a simple inductive link, for example, using impedance modulation. Several time-to-digital demodulation methods have been proposed but have limitations such as a narrow

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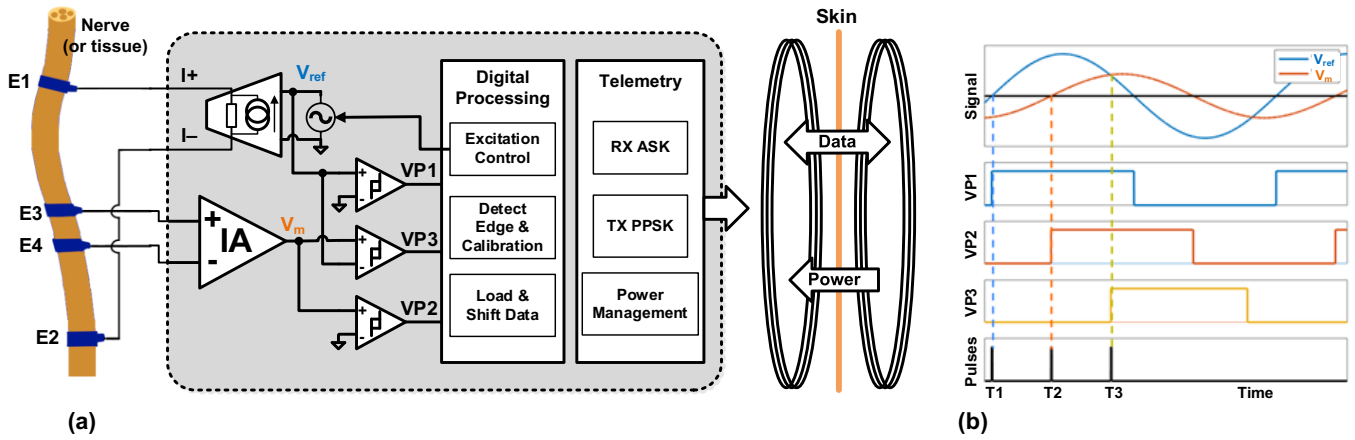

Fig. 1. Time stamp implant concept. (a) System block diagram. (b) Waveform and pulses in the time domain. The time stamp demodulation method uses three comparators to determine the zero crossing point of voltages V_{ref} and V_m ($T1$ and $T2$) and their crossing point ($T3$). The time delay $T1 - T2$ yields the phase of the bioimpedance and the time delays $T3 - T1$ and $T3 - T2$ its magnitude. V_{ref}: excitation signal generator; V_m: measured signal; $VP1, VP2, VP3$: comparator outputs.

bandwidth [23] or rather complex circuitry [24], [25].

In this paper, a novel *time stamp* magnitude and phase demodulation method which has minimal complexity and power consumption is proposed. The method only uses three comparators to check the crossing points between the excitation signals and the measured signals. Each crossing point is 'stamped' in the time domain and these time stamps can easily be transmitted for bioimpedance analysis.

The rest of the paper is organized as follows. Section II describes the concept of the proposed bioimpedance time stamp method and examines the effect of system non-idealities on its accuracy. Section III describes the design and implementation of a proof of concept developed based on the time stamp method. Section IV reports measured results using the system, and Section V compares the performance with other published work. Conclusions are drawn in Section VI.

II. System Architecture

A. Concept

Fig. 1(a) shows a conceptual diagram of an implant system using the proposed time stamp method. The implant interface comprises an excitation signal generator (V_{ref}) provided by, for example, a direct digital synthesizer or an oscillator, a differential current driver ($I+$, $I–$) for excitation and a differential instrumentation amplifier (IA) for signal acquisition. A digital processing module controls the signal generator and the loading and shifting of the acquired pulses from the three comparators. An inductive telemetry [26] provides the required system power and a means of communication with the implant for further processing.

In a tetrapolar (four-electrode) bioimpedance measurement configuration as shown in Fig. 1(a); the differential excitation currents are applied to a pair of electrodes (E1, E2) and the resulting potential V_m is measured from the other pair of electrodes (E3, E4). The proposed demodulation method reads the magnitude and phase of V_m at the output of the IA by employing only three comparators. Two comparators identify the timing of the zero crossing points of V_{ref} ($T1$) and V_m ($T2$) shown in Fig. 1(b). Time stamps $T1$ and $T2$ can be used to determine the phase difference between the original V_{ref} signal and the measured V_m signal from (1).

$$\theta = 2\pi \cdot \frac{T1-T2}{(1/f)} \tag{1}$$

where f is the excitation signal frequency and θ is the calculated phase delay between V_{ref} and V_m.

For the magnitude extraction, a third comparator is used to generate a pulse $VP3$ when V_{ref} (of known amplitude) and V_m (of unknown amplitude) signals cross at time $T3$. V_{ref} is directly related to the excitation current. Note that a second acquisition channel implemented in [18], [24] measuring a dummy resistor to obtain a reference can be avoided.

With all three time stamp values, the magnitude of V_m can be calculated. The voltage level at $T3$ is first calculated using (2), where A_{Vref} is the known amplitude of V_{ref}.

$$V_{T3} = A_{Vref} \cdot \sin[2\pi \cdot f \cdot (T3 - T1)]. \tag{2}$$

The unknown amplitude A_{Vm} of the measured signal V_m can be derived from (3).

$$A_{Vm} = \frac{V_{T3}}{\sin[2\pi \cdot f \cdot (T3-T2)]}. \tag{3}$$

This method is designed for the measurement of resistive and capacitive loads (i.e. negative V_m phase with respect to the current generated from V_{ref}) as expected of tissue impedance [22].

In a very low power implant system, data and power can be simultaneously transmitted over a single inductive link using, for example, passive phase-shift keying modulation (PPSK) [27]. The pulses $T1$, $T2$ and $T3$ in the simple time stamp system, which can be obtained by edge detectors from $VP1$, $VP2$ and $VP3$ can be transmitted directly at a reasonable rate to an external device featuring digital processing capability (e.g. FPGA), which then calculates the impedance values based on

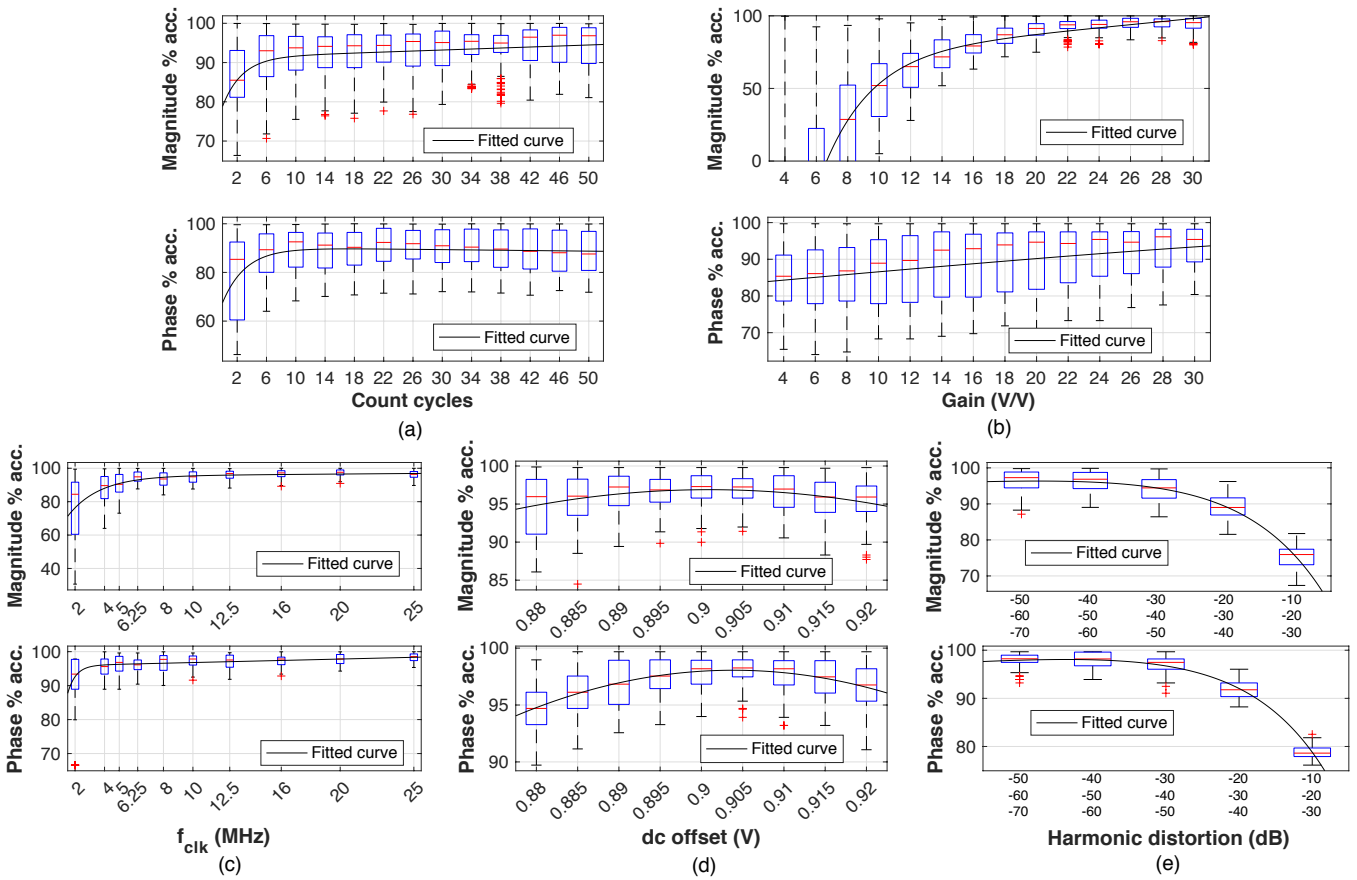

Fig. 2. Simulated performance with parameter sweep of (a) count cycles, (b) IA gain, (c) time stamp frequency, (d) dc offset, and (e) total harmonic distortion versus accuracy for both magnitude and phase at 200 kHz. All figures use boxplots with 100 iteration runs; the black curves show the average values. dc offset uses 'poly2' fit and the others use 'exp2' fit function in Matlab.

$T1$, $T2$ and $T3$ as described above.

B. Model and Simulation

The accuracy of the time stamp method can be influenced by several non-ideal factors in the signals such as the presence of harmonic distortion and circuit dc-offsets from the acquisition circuits and the noise present in the signals. A simulated model was, therefore, developed in Matlab to gain an insight into the effects of such non-idealities on the system performance by comparing the calculated and measured magnitude and phase. The model comprised a 200 kHz sinusoidal signal of 1 V_{p-p} for excitation, providing an output current of 4 mA_{p-p}, applied to a parallel RC load of 50 Ω and 100 nF. The resulting voltage developed across the load was recorded and processed with the excitation signal using the time stamp method. The default settings (when not swept) of the simulation used a front-end gain of 20 V/V, and both V_m and V_{ref} signals had a second, third and fourth harmonic distortion of -40 dB, -50 dB and -60 dB respectively, with white Gaussian noise added to all the signals with a SNR of 50 dB. To record the time lapses, 12.5 MHz was used for the time stamp counter frequency (f_{clk}) and 10 signal cycles were used for average accuracy results.

Random phase deviations were applied to the excitation signal by calculating the maximum phase delays that can occur for the selected f_{clk} in each iteration. This ensured asynchrony between the excitation signal frequency and the counter frequency f_{clk} used to obtain the time stamps. By sweeping selected parameters over 100 iteration runs, the simulation was used to observe the effects of the design parameters and specification variations on the system performance for phase and magnitude calculations.

1) Gain and Signal Cycles:

Fig. 2(a) and Fig. 2(b) show the plot of the accuracy of impedance magnitude and phase versus the number of signal cycles over which measurements were averaged and the front-end gain applied to the measured signal. Both parameters can be used to mitigate noise. In these sweeps, the SNR was reduced to 40 dB for analysis. In Fig. 2(a), the graphs show fairly consistent average accuracies of magnitude ranging up to 95% after a minimum of 10 signal cycles; while very fewer runs lead to low accuracies of around 75%. A similar pattern is also shown for the phase accuracy.

In the graphs in Fig. 2(b), optimum performance is observed at high values of IA gain, reaching up to 98% in magnitude and 94% in phase for a front-end gain of 30 V/V. The accuracies exhibit a greater variation with gain as it drops to near unity, falling exponentially on the magnitude graph and with a more linear relationship on the phase graph.

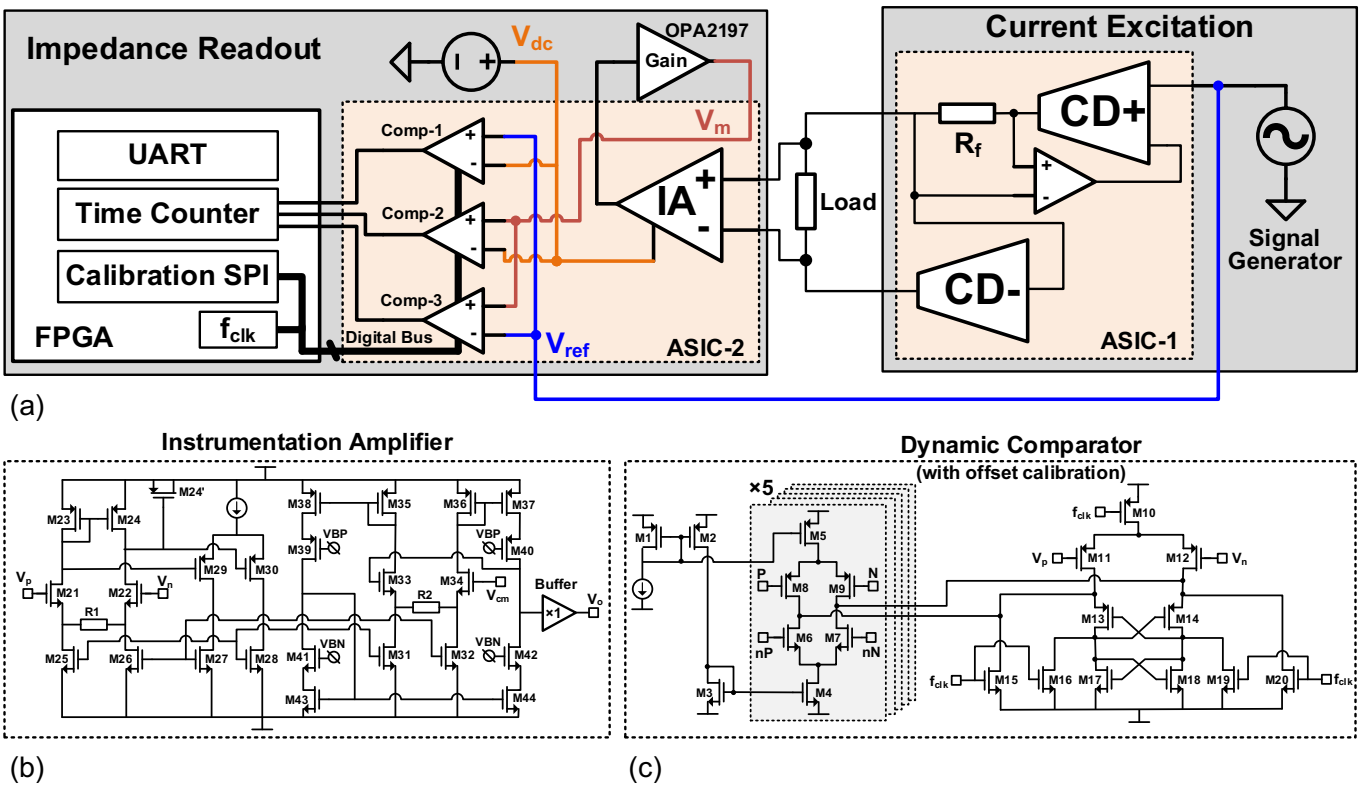

Fig. 3. (a) System diagram with current excitation and impedance readout. (b) Instrumentation amplifier based on current feedback. (c) Dynamic comparator with offset calibration. V_p and V_n: inputs of each circuit block; V_{cm} and V_{dc}: set the output common mode level; VPB and VPN: biasing voltages; DAC digital controls: P, nP, N, nN; f_{clk}: the clock signal for counter and dynamic comparators.

2) Time Stamp Counter Frequency:

A higher sampling rate to determine the time stamp values results in greater precision of measurements, which in turn provides more accurate calculations. Fig. 2(c) shows a rising trend in the accuracies of impedance magnitude and phase with a rising f_{clk}, reaching peak values of 97.3% on the magnitude plot and 98.9% on the phase plot. It is apparent that very low time stamp frequencies such as 2 MHz, which only samples a 200 kHz excitation signal ten times per cycle, results in average accuracies as low as 82%.

3) dc Offset Variation:

Electrode induced dc-offsets are usually removed by a high-pass filter during the first-stage of amplification [28], [29]. The remaining dc-offsets are due to circuit offsets such as comparator input offset. The accuracy of the calculated magnitude and phase with respect to a varying circuit dc offset of between ±20 mV (on the measured signal) from the reference point of 0.9 V can be characterized by a bell-shaped graph, as shown in Fig. 2(d). The average accuracies are better than 84% on both the magnitude and phase plots.

4) Total Harmonic Distortion (THD):

The added amplitudes of second, third and fourth harmonic distortions were swept in the measured signal. A gradual increase in all values showed falling accuracies of the calculated impedance magnitude and phase values, as illustrated in Fig. 2(e). This plot shows the consistent and acceptable performance of the system for THD with second, third and fourth harmonic components of -30 dB, -40 dB and -50 dB respectively. It shows that the exponential falls at extreme THD values which is expected considering the fundamental principle of the time stamp method.

III. System Implementation

A system was developed to evaluate the time stamp demodulation method. It has two main building blocks: the current excitation and impedance readout circuits as shown in Fig. 3(a). The current driver is an application specific integrated circuit (ASIC-1) based on [3]. It comprises a master current source (CD+) using an excitation voltage V_{ref} as input, and a slave current sink (CD–) providing the current return path. The constant current is controlled by feeding back the voltage across resistor R_f to the input of CD+. The transconductance is $G_m = 1/R_f \approx 4\,\text{mA/V}$. The CD– accomplishes the fully differential drive by inverting the potential measured at the output of CD+ and applying this inverted ac potential to the sink side of the load. This suppresses any common-mode voltage appearing at the IA input.

For the impedance readout block, ASIC-2 comprises an IA as shown in Fig. 3(b). It is based on current feedback topology with a high input impedance [30], transferring the differential input voltage to a current through resistor R_1, and copying the same current to resistor R_2; the transfer function of the IA is $V_o/(V_p - V_n) = R_2/R_1$. V_{cm} sets the desired output common-mode voltage level. This topology offers a high common-mode reject ratio and wide bandwidth suitable for bioimpedance

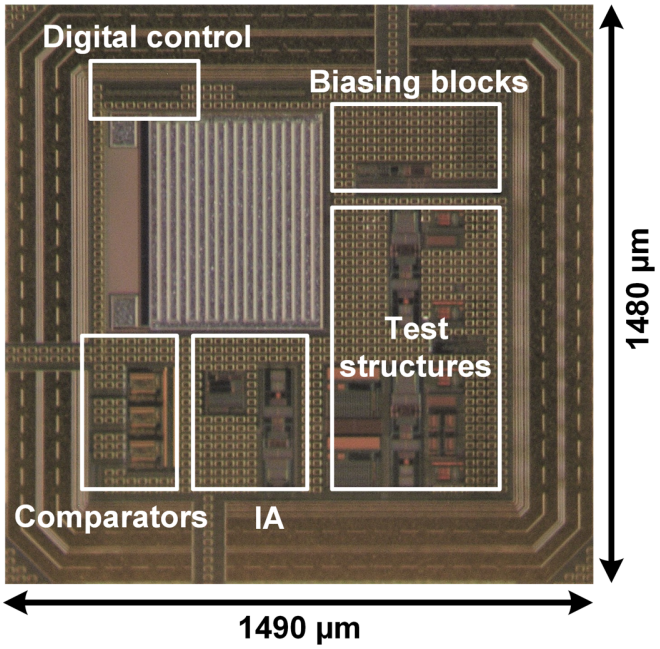

Fig. 4. Chip micrograph of ASIC-2 with the various circuits highlighted.

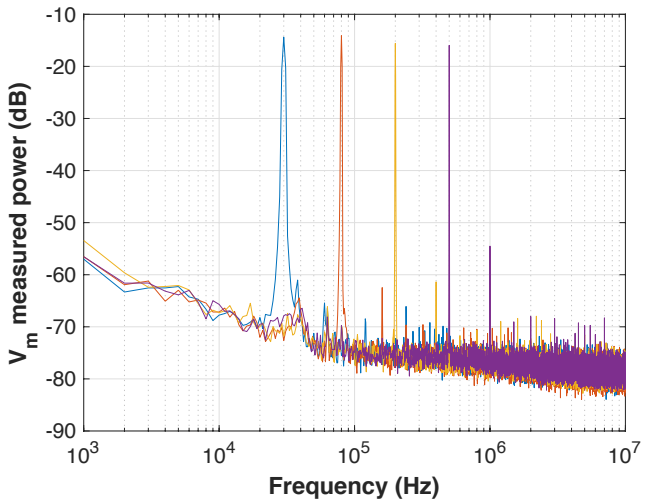

Fig. 5. Measured output spectrum of voltage V_m at 30 kHz, 80 kHz, 200 kHz and 500 kHz with output current of 200 μA_{p-p}, 400 μA_{p-p}, 800 μA_{p-p} and 2 mA_{p-p}, respectively.

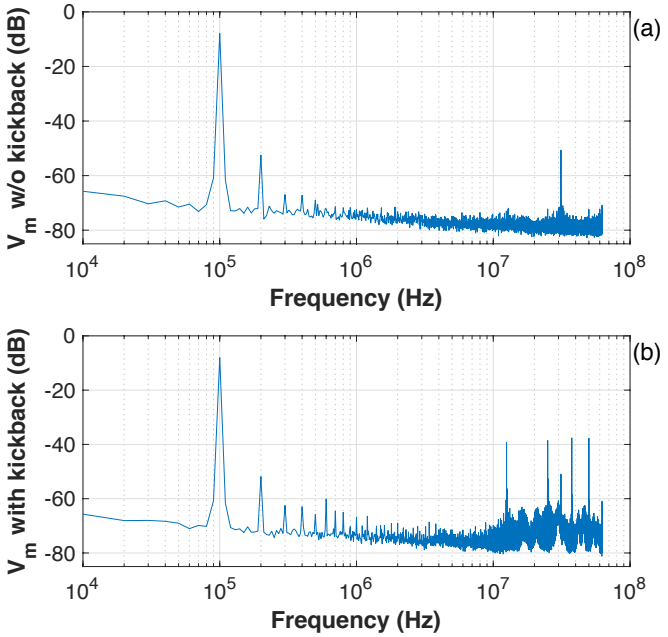

Fig. 6. Measured output spectrum of voltage V_m at 100 kHz; (a) without, (b) with kickback noise. Kickback noise always presents once the comparators are in operation.

applications [31]. The IA was designed to have a gain of 10 V/V, and with a separate non-inverting amplifier (using OPA2197) to provide additional amplification.

The core of the proposed demodulation method are the three comparators. In general, there are two types of comparator; the continuous-time comparator and the latched comparator. To achieve low-propagation delays, the former requires multiple gain-stages, and the high speed is at the expense of increased power consumption [18]. The latched comparator is often used in ADC designs, taking advantage of positive feedback, and operates at high speed without excessive static power. The dynamic comparator implemented is shown in Fig. 3(c). The counter clock f_{clk} is also used to operate the comparator. From simulation, it is observed that the accuracy is affected by any dc voltage offset and a method of calibration is needed to eliminate these. A 6-bit calibration digital-to-analog converter (DAC) was used as shown in Fig. 3(c). The DAC either sources or sinks currents into the discharging node of the comparator when in the regeneration phase, to re-balance any offset due to circuit mismatches or voltage offset at its inputs. The most-significant-bit controls the balancing source or sink to the comparator node, and the other 5 bits control the calibration current with a least-significant-bit current of 120 nA.

The readout logic was implemented on a Xilinx Artix-7 FPGA XC7A100T. The logic comprises a clock generator, a comparator calibration module, a UART communication module and two time-counters (*Phase* counter and *Cross* counter) interacting with the outputs from the comparators. The clock generator provides sampling clocks f_{clk} for both the comparators and the two 16-bit time-counters. Referring to Fig. 1(b) and Fig. 3(a), the *Phase* counter is enabled at the rising edge of Comp-1 output ($T1$ in Fig. 1) and stops at the rising edge of Comp-2 output ($T2$ in Fig. 1), hence logs the phase difference between V_{ref} and V_m. The *Cross* counter also starts at the rising edge of Comp-1, but stops at the rising edge of Comp-3 ($T3$ in Fig. 1). After the counters stop, their values are saved in an internal memory to be sent out via UART. To avoid false triggering of the counters by glitches, the outputs from the comparators are first sampled into three shift registers. A rising edge is only deemed true if all the bits in the shift register become '1'. The length of the shift registers is 2-bits. The dc offset of the comparators is also calibrated via UART, where a 6-bit code for each comparator is sent by the FPGA through SPI.

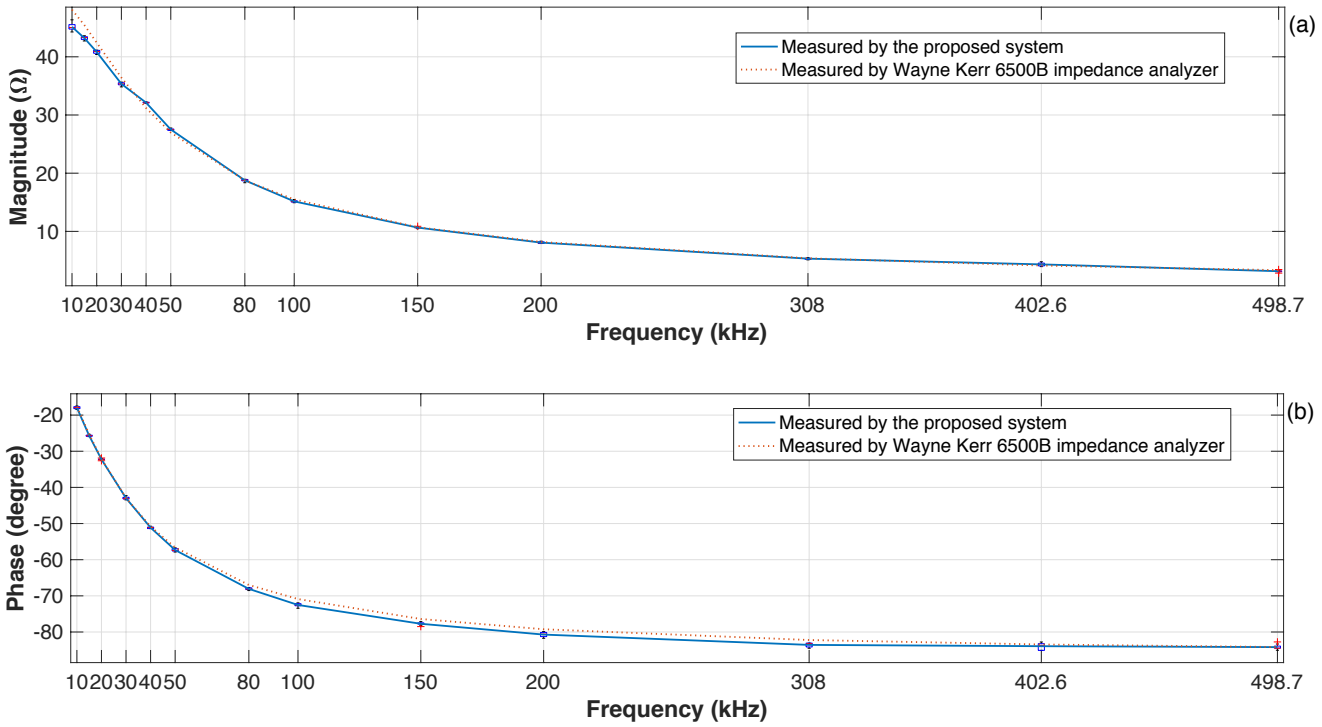

Fig. 7. Measured magnitude and phase of the RC load by the proposed time stamp system and the impedance analyzer.

IV. Measured Results

Both ASICs were designed using a CMOS 0.18-µm technology, and operate from ±1.65 V power supplies. In this work the active area of ASIC-2 for the time stamp circuits is about 0.65 mm^2 and its micrograph is shown in Fig. 4.

A. System Performance Evaluation

The system was set-up as shown in Fig. 3(a). A TTi TGA12104 signal generator was used to generate the excitation voltage. The system performance was evaluated by measuring a parallel RC load (50 Ω ||100 nF) from 10 kHz to 500 kHz. The RC load value was measured by a Wayne Kerr 6500B impedance analyser for reference to calculate the system magnitude and phase measurement accuracy. The overall gain of the voltage acquisition channel was boosted by OPA2197 to 70 V/V. To quantify the effects of limited bandwidth the system was calibrated from 10 kHz to 500 kHz to identify the gain and phase delays introduced by the analog front-end, excitation and recording circuits. A 20 Ω dummy resistor and an excitation current of 1 mA_{p-p} were used.

At fixed recording gain, depending on the impedance value of the test RC load (which varies with respect to frequency), the amplitude of the excitation current was adjusted with respect to frequency, with four settings; 200 μA_{p-p}, 400 μA_{p-p}, 800 μA_{p-p}, and 2 mA_{p-p}, for frequencies ≤ 30 kHz, ≤ 100 kHz, ≤ 200 kHz, and ≤ 500 kHz, respectively.

Fig. 5 shows the measured power spectrum of voltage V_m (the signal at the input to the comparators) with different current excitation amplitudes across the frequency span. For better SNR, and simplicity, the second channel of the signal generator was synchronized to the excitation voltage of the current driver (V_{exc}), but with an output amplitude of 1 V_{p-p} as the V_{ref} signal.

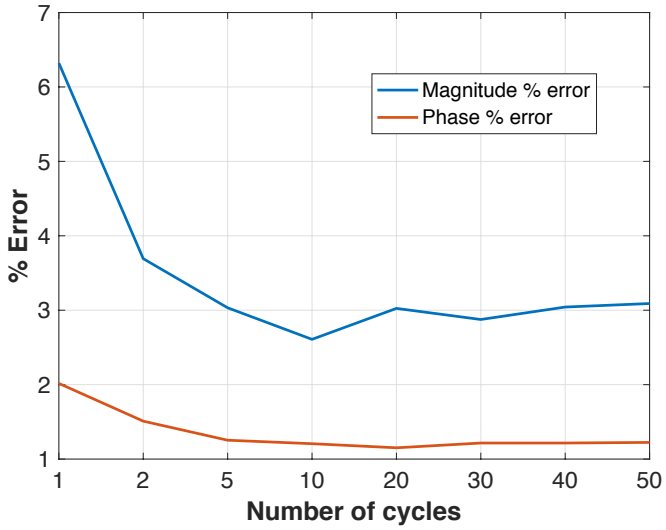

Fig. 8. Measured system accuracy with the RC load and different numbers of cycles applied.

For the counter and the clock of the dynamic comparator, f_{clk} was set to 12.5 MHz as a compromise point as shown in Fig. 2(c). The comparators were calibrated once for input-offset and the calibration DAC code was used throughout the testing. After connecting V_m and V_{ref} to the comparators, kickback noise was present. Fig. 6 shows the spectrum of the measured voltage V_m at 100 kHz with and without the kickback noise (when the comparator was off).

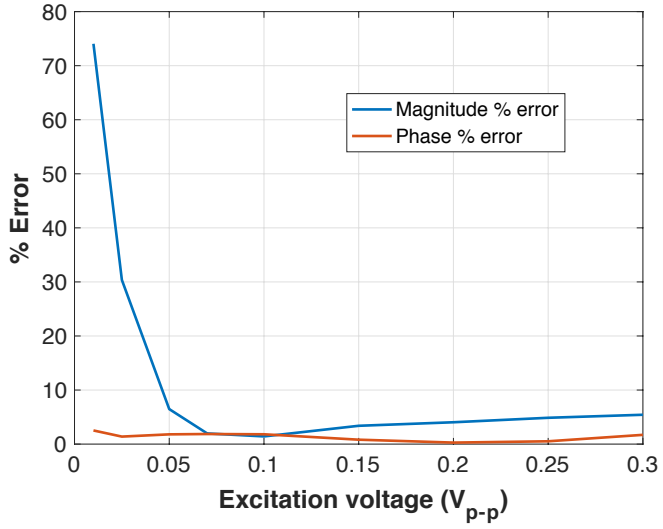

Fig. 9. Measured system error with the RC load and different excitation voltages applied from 10 mV_{p-p} to 300 mV_{p-p} at 50 kHz.

The measured RC load magnitude and phase are plotted in Fig. 7 together with the reference values measured by the impedance analyser. The number of cycles used is 25, and the boxplot is plotted with 10 iterations. The error is 2.94% for the magnitude and 1.19% for the phase over the frequency range measured. The effects of using different numbers of cycles were evaluated from 1 to 50 cycles with 10 iterations and the error for both amplitude and phase is plotted in Fig. 8. It shows that the error reaches saturation at around 3% for the magnitude and around 1.25% for the phase over the frequency bandwidth.

The effect of applying different excitation voltages (applying different excitation currents) while using the second synchronized channel output of 1 V_{p-p} as V_{ref} is shown in Fig. 9. A 50 kHz excitation voltage was swept from 10 mV_{p-p} to 300 mV_{p-p} with the RC load, resulting in different crossing points for $T3$ [see Fig. 10(e)]. This also gives an indication of the effect of different applied recording gains. The results show that the error is consistently small (less than 1.87%) for the phase measurement. This is expected as the variation applied does not alter the crossing points for phase measurement. The magnitude errors are significant at excitation voltages below 50 mV_{p-p}. The errors are below 5% for voltage excitation up to 250 mV_{p-p} and 5.4% at 300 mV_{p-p}.

Further details are shown in Fig. 10. From Fig. 10(e), the phase crossing is consistent for all the four plotted signals reflecting small phase measurement error. For small excitations, the large error in magnitude measurement is due to the small V_m (measured at the input of the comparator) which makes the system susceptible to noise such as kickback. As the magnitude of V_m increases, the crossing point of V_m and V_{ref} that leads to $T3$ [see Fig. 1(b)] moves forward. In terms of accuracy, the error is not significantly influenced with regard to the crossing point which indicates that above an appropriate threshold level, the proposed method is robust.

However, a small trend of error increase is observed. This could be due to two factors. As the excitation current (or recording gain) increases, the SNR increases but the timing reduces (similar to a decrease in the dynamic range). The

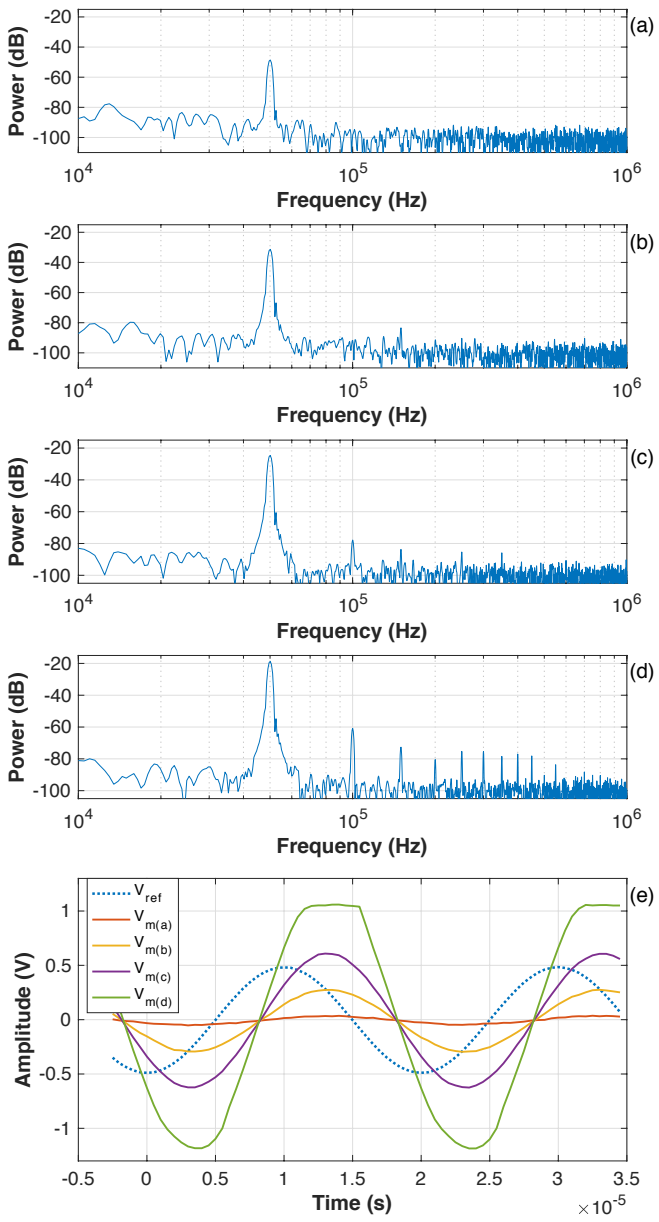

Fig. 10. System measurement with the RC load and different excitation voltages applied from 10 mV_{p-p} to 300 mV_{p-p} at 50 kHz. Measured output spectrum of recorded voltage after the IA at (a) 10 mV_{p-p}, (b) 70 mV_{p-p}, (c) 150 mV_{p-p}, (d) 300 mV_{p-p} of voltage excitation. Plot (e) includes different V_m signals (measured voltage before comparator) in the time domain using various excitations as shown from (a) to (d), as well as the reference voltage V_{ref}.

second factor is the THD. From Fig. 10(a) to Fig. 10(d) it can be observed that as the excitation current increases, the voltage induced on the load approaches the input and output compliance limits of the IA (first stage amplifier) and results in a reduction of THD in the measured voltage at the IA output propagating to the V_m signal.

In Fig. 10(e) note that at 300 mV_{p-p} excitation, the output voltage V_m (output of second stage gain) is severely saturated. However, this does not reduce the measurement accuracy drastically because the crossing point is preserved, assuming there is no severe saturation in the first stage of amplification. This fact means that there may be less need for a programmable

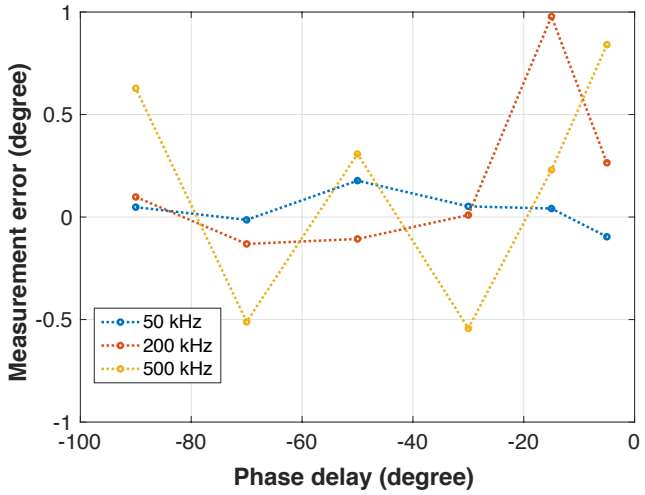

Fig. 11. Six different phase delays measured at 50 kHz, 200 kHz and 500 kHz plotted with an average of 250 cycles of readings.

gain amplifier. This would further reduce the design complexity and calibration procedure.

The power consumption of the IA is about 650 µW excluding the buffer and biasing. The power consumption of the comparators are 34.32 µW with f_{clk} set to 12.5 MHz.

B. Improved Accuracy with Fractional-N Synthesis

The principle of phase detection is a counter based 'zero-crossing check' which has been commonly used in magnitude/phase demodulation methods [19], [32], [33]. In such time-to-digital conversions, the clock frequency determines the resolution. Often to obtain higher resolution, especially at higher excitation frequencies (f_{ref}), a higher counter clock frequency is used (e.g. in [33] f_{clk} = 3.33 GHz), as the phase resolution is $360° \cdot (f_{ref}/f_{clk})$. In this paper, f_{clk} = 12.5 MHz, which is fed to both the dynamic comparators and the two counters. This clock corresponds to a time resolution of 80 ns that would provide one degree of resolution when f_{ref} = 34.7 kHz.

When f_{clk}/f_{ref} is not an integer, sampling both the reference voltage V_{ref} and measured voltage V_m at f_{clk} leads to a phase deviation in each signal cycle. This results in a fractional-*N* synthesis effect when taking the average readings from a number of signal cycles, thereby providing a finer resolution. When f_{clk}/f_{ref} is not an exact integer it can be rewritten as $f_{clk}/f_{ref} = Z + R$, where Z is an integer, and R is the fractional part of the division. Similar to fractional-*N* frequency synthesis [34], over *N* number of signal cycles, where *N* is the denominator of the lowest form of *R*, the counter registers *M* cycles of $k+1$ counts and $N-M$ cycles of k counts; the average counter value is then $k + (M/N)$ and the phase resolution becomes $360° \cdot (f_{ref}/f_{clk}) \cdot (1/N)$. The fractional-*N* effect indicates that fine phase resolution can be achieved by choosing specific frequency points that give large values of *N* but $Z + R$ remains close to the desired ratio. For example, for f_{clk} =12.5 MHz, and f_{ref} = 300 kHz, $f_{clk}/f_{ref} = 41 + 2/3$, hence $N = 3$ and the phase resolution is 2.88°, but at 301 kHz, $f_{clk}/f_{ref} = 41 + 159/301$, so $N = 301$, and the phase resolution is 0.0288°.

A special case is when f_{clk}/f_{ref} is an integer, where the phase resolution is fixed at $360° \cdot (f_{ref}/f_{clk})$ in the ideal case. But the presence of any noise varies the zero-crossing points, and results in small and varying phase deviations between V_{clk} and V_{ref}. In practice, therefore, f_{clk}/f_{ref} can never be an integer, and the fractional-*N* effect can still apply.

This effect may have been overlooked in previous designs. Given the slow changes of physiological response, e.g. neural signals (<1-2 kHz), this effect could be used to offer high accuracy with lower on-chip power consumption.

The phase detector accuracy was evaluated further in relation to the fractional-*N* synthesis effect. The system measured a resistor load (i.e. zero phase). The signal generator was used to accurately output six different phase delays δ_{set}. δ_{set} was set to give a phase delay on V_{ref} with respect to V_{exc}. [Note: as in the

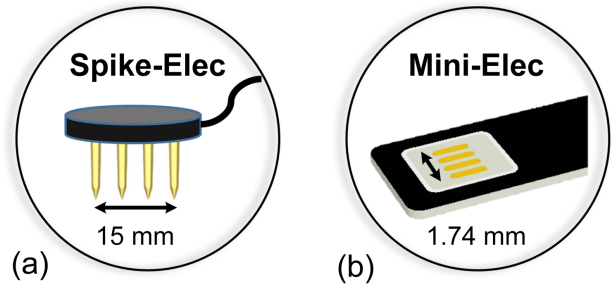

Fig. 12. The tetrapolar electrodes used for the in-vitro experiment. (a) Spike-pin electrodes. (b) Min-pad electrodes. Tested with 0.9% and 3% saline solutions.

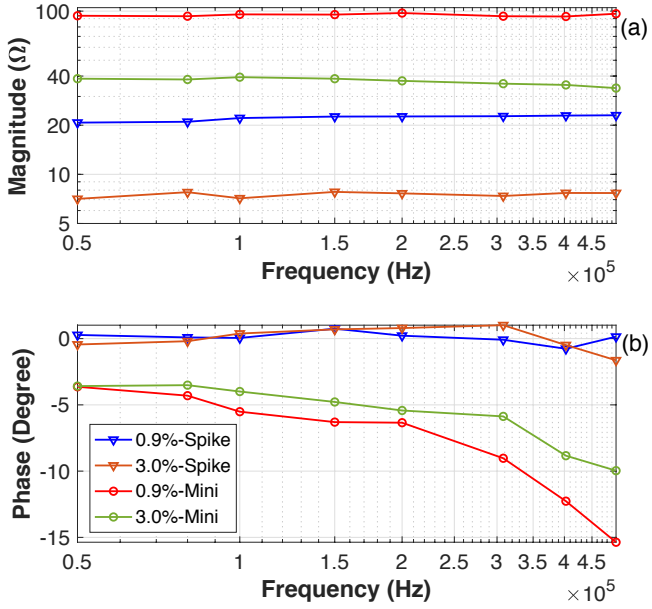

Fig. 13. Measured impedance magnitude (a) and phase (b) with the Spike-electrodes and Mini-electrodes. Tested with 0.9% and 3% saline solutions from 50 kHz to 500 kHz, plotted with 250 average data points. The impedance magnitude is plotted in log scale for better clarity.

TABLE I
COMPARISON WITH OTHER WORK

Parameter	[11]	[12]	[18]	[19]	[23]	**This work**
Technology	0.18 µm CMOS	0.13 µm CMOS	0.35 µm CMOS	0.35 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Magnitude Error	3% @ dc	8.4% @ 10 kHz	3.5% @ 100 kHz	0.28% @ 10 kHz	<3.12% @ 2kHz	2.94% over the bandwidth
Phase Error	-	7.5% @ 10 kHz	3.6˚ @ 100 kHz	0.12% @ 10 Hz	-	1.19% over the bandwidth 0.51˚ @ 500 kHz
Bandwidth	2 kHz / 20 kHz	10 kHz	100 Hz – 100 kHz	0.1 mHz – 100 kHz	2 kHz	**10 kHz – 500 kHz**
Demodulation method	I-Q pseudo-sine / square	I-Q sine	MP-D[1]	MP-D	T-D[2] semi ramp	T-D time stamp
Output format	10-bit digital output	8-bit digital output	Analog dc level	10-bit digital output	2 PWM[3] signals @ 2 kHz	**3 digital pulses**
Supply voltage	1.8 V	1.2 V	±2.5 V	3.3 V	1 V	±1.65 V
Power consumption	50.16 µW	42 µW	21 mW	320 µW	1.55 µW	684 µW[4]

[1] Magnitude and phase detection.
[2] Time to digital demodulation.
[3] Pulse width modulation.
[4] Accounting for the IA and comparators only.

previous measurements, V_{ref} was generated using the second channel of the signal generator and was synchronized ($f_{exc} = f_{ref}$ and $\delta_{set} = 0°$) to V_{exc} (for current excitation) as described earlier]. δ_{set} was set to $-5°$, $-15°$, $-30°$, $-50°$, $-70°$ and $-90°$ at 50 kHz, 200 kHz and 500 kHz. Since the load was resistive, the system measured the phase delays set by the signal generator. The results of phase measurement error are shown in Fig. 11. They are plotted using an average of $N = 250$ cycles of readings, and the system has a phase measurement accuracy of 0.07°, 0.26°, and 0.51°at 50 kHz, 200 kHz and 500 kHz respectively.

Note that the method has difficulties in measuring small absolute phase delays depending on excitation frequency. However, the system can be set to measure relative phase delays by adding a known constant phase. This phase can naturally come from the analog front-end or by setting a δ_{set} between V_{exc} and V_{ref} to increase the absolute phase between the measured V_m and V_{ref}. The actual phase delays due to the impedance load can then be extrapolated. The same idea is used in phase calibration of the analog front-end. This allows phase measurement from 0° to 90° (the bioimpedance phase range [35]).

C. In-Vitro Experiment

Two different tetrapolar gold-plated electrodes shown in Fig. 12 were evaluated using the system. The characteristics of the electrodes were evaluated by measuring the impedance of saline solutions with different concentrations (0.9% and 3%). The Spike-pin had a diameter of 1 mm with a pitch of 5 mm. The Mini-pad was 0.3 mm × 1.46 mm with a pitch of 0.58 mm. The outer electrodes were used for current excitation and the inner pair for voltage recording. Due to the electrode-induced dc-offset a high-pass filter was required for the proposed new method to function properly. A simple RC high-pass filter was inserted between the IA and OPA2197 with $f_{cut-off} = 838$ Hz. δ_{set} was set to $-30°$ in this experiment.

The experimental results are shown in Fig. 13. The Spike-electrodes measurement results show that the impedance of the saline solution is constant with zero phase across the frequency spectrum as expected. The impedance of 0.9% saline was ~22 Ω whereas the impedance of the 3% solution was ~7.5 Ω correctly reflecting the concentration levels of the test solutions. The same impedance ratio was also demonstrated by the Mini-electrodes, that is ~38 Ω and ~95 Ω respectively. The different design and size of the electrodes is reflected in the different impedance values. However, for the Mini-electrodes, a non-zero phase delay increasing with frequency was evident. This could be due to the small spacing between the measurement electrode pads. This leads to a parasitic and fringe-effect capacitor [36] which was not apparent in the Spike-electrodes where the electrodes are far part. In this in-vitro experiment, the system successfully measured the impedance of the test solutions and identified the characteristics of two very different types of electrode. This can aid design choices for different bioimpedance related applications.

V. COMPARISON AND DISCUSSION

Table I provides a comparison with other published work. The time stamp method and implementation reported here aims for proof of concept and provides good accuracy over a wide bandwidth from 10 kHz to 500 kHz. The highlight of the proposed method is its simplicity, particularly in terms of its output format. Only three pulses are required to demodulate the bioimpedance in comparison to the use of conventional 8- to 10-bit analog-to-digital conversion. With the information recorded in the time domain, the time stamp method can physically divide its 'analog-to-digital conversion' into two separate blocks; the simple on-site comparators, and the back-end off-site processing, which has great advantages in low power implantable designs.

In comparison to the other time-to-digital demodulation methods reported, while the phase detection process is similar, the difference is in the magnitude detection. In [23] the system uses a semi ramp signal, with DAC generated reference for comparison, achieving very low power consumption. However, the method might have limitations if the load changes its semi ramp shape, and this limits the bandwidth and capacitance range over which it can operate. In [24], the method locates the

$0.5T$ and $0.75T$ of the signal (where T is the signal period) using different capacitor discharge rates posing challenges due to possible process mismatches. The time window selected is narrow which leads to a complex circuit implementation [25]. Both [24] and [25] are simulation results and excluded from Table I. Lastly, the time stamp method is able to demodulate with less demands on the second-stage gain amplifier, which often requires additional calibration to accommodate different gains/phase delays at different frequencies. The benefit of fractional-N synthesis is also investigated allowing high accuracy with a relative low frequency clock for the counter.

As the current system is at the proof of concept stage, its power consumption has yet to be optimized. Further improvement towards the implant viability is anticipated, particularly on the current excitation block which requires THD better than 40 dB where other reported methods can be implemented with pseudo-sine or square waves.

VI. Conclusion

This paper has presented a novel time-to-digital demodulation method for bioimpedance analysis. Compared to the conventional methods, the time stamp method uses only three comparators to send three digital pulses needed for demodulation. A model has been built using Matlab to analyse the effect of a number of design variables on the accuracy of the method including gain, the number of cycles, counter frequency, dc offset and THD. A proof of concept system with ASICs has been developed, which can measure impedance with a magnitude measurement error of 2.94%, and a phase measurement error of 1.19% over a bandwidth of 10 kHz to 500 kHz. The effect of the number of cycles, recording signal magnitude and THD has been analysed to demonstrate its effect on the measurement accuracy. In addition, the effect of fractional-N synthesis has been analysed for the counter-based zero crossing phase detector obtaining a finer phase resolution (0.51° at 500 kHz) using a moderate counter clock frequency (f_{clk} = 12.5 MHz). An in-vitro experiment identified the characteristics of two very different types of electrode. The time stamp system shows great potential for low power bioimpedance applications.

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