An Integrated Microheater Array With Closed-Loop Temperature Regulation Based on Ferromagnetic Resonance of Magnetic Nanoparticles

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***Abstract*—Magnetic nanoparticles (MNP) can generate localized heat in response to an external alternating magnetic field, a unique capability that has enabled a wide range of biomedical applications. Compared with other heating mechanisms such as dielectric heating and ohmic heating, MNP-based magnetic heating offers superior material specificity and minimal damage to the surrounding environment since most biological systems are non-magnetic. This paper presents a first-of-its-kind fully integrated magnetic microheater array based on the ferromagnetic resonance of MNP at Gigahertz (GHz) microwave frequencies. Each microheater pixel consists of a stacked oscillator to actuate MNP with a high magnetic field intensity and an electro-thermal feedback loop for precise temperature regulation. The four-stacked/five-stacked oscillator achieves >19.5/26.5 V_{pp} measured RF output swing from 1.18 to 2.62 GHz while only occupying a single inductor footprint, which eliminates the need for additional RF power amplifiers for compact pixel size (0.6 mm × 0.7 mm) and high dc-to-RF energy efficiency (45%). The electro-thermal feedback loop senses the local temperature and enables closed-loop temperature regulation by controlling the biasing voltage of the stacked oscillator, achieving a measured maximum/RMS temperature error of 0.53/0.29 °C. In the localized heating demonstration, two PDMS membranes mixed with and without MNP are attached to the microheater array chip, respectively, and their surface temperatures are monitored by an infrared (IR) camera. Only the area above the inductor (∼0.03 mm^2) is efficiently heated up to 43 °C for the MNP-PDMS membrane, while the baseline temperature stays <37.8 °C for the PDMS membrane without MNP.**

***Index Terms*—Biosensor, CMOS SOI, electro-thermal feedback, integrated circuits, magnetic nanoparticle, microheater, multiphysics modeling, permeability, stacked oscillator, temperature regulation.**

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I. Introduction

TEMPERATURE plays an important role in determining the physiological behavior of biological systems, and therefore, enabling localized yet accurate temperature manipulation in cells and tissues finds a wide range of biomedical applications. For example, in neuroscience research, localized heating can activate thermal-sensitive ion channels [1]–[3], which has been explored to introduce ion flux and, in turn, stimulate action potentials of nearby neurons. Another application example is the hyperthermia treatment of cancer [4]–[7], which raises the local temperature of a tumor to 43–45 °C to disrupt cancer cells' ability to repair DNA damage. To avoid overheating and permanent heat damage to adjacent healthy tissues, it is critical to monitor the local temperature rise while ensuring the heat only occurs in the tumor. Additionally, controlled localized heating has been applied in expedited wound healing [8]–[10], temperature-controlled drug release [11]–[14], and bioanalytical techniques such as polymerase chain reaction (PCR) and temperature gradient focusing (TGF).

There are three mechanisms that can generate heat loss electrically, namely ohmic loss, dielectric loss, and magnetic loss, based on Joule's law as shown in (1),

$$P_{\text{loss}} = \tfrac{1}{2}\sigma|\mathrm{E}|^2 + \tfrac{1}{2}\omega\varepsilon''|\mathrm{E}|^2 + \tfrac{1}{2}\omega\mu''|\mathrm{H}|^2 \tag{1}$$

where ω is the angular frequency [rad/s], σ is the material conductivity [S], ε'' is the imaginary part of the permittivity [F/m], μ'' is the imaginary part of the permeability [H/m], $|\mathrm{E}|$ is the magnitude of the electrical field [V/m], and $|\mathrm{H}|$ is the magnitude of the magnetic field [A/m]. Although ohmic heating is the most prevalent technological choice for microheater designs, one major disadvantage is that it requires direct contact between heating elements (i.e., resistors) and targeted bio-samples. For dielectric heating, it is suitable for samples with drastically different dielectric properties from the surrounding environment [15]. However, in most biomedical applications, the permittivity difference between targeted cells/tissues and the surrounding environment is insignificant due to the high water content, resulting in poor specificity [16]. For magnetic heating, it is usually accomplished by incorporating magnetic materials such as magnetic nanoparticles (MNP). Since most bio-samples are non-magnetic, magnetic heating can support superior specificity than other modalities.

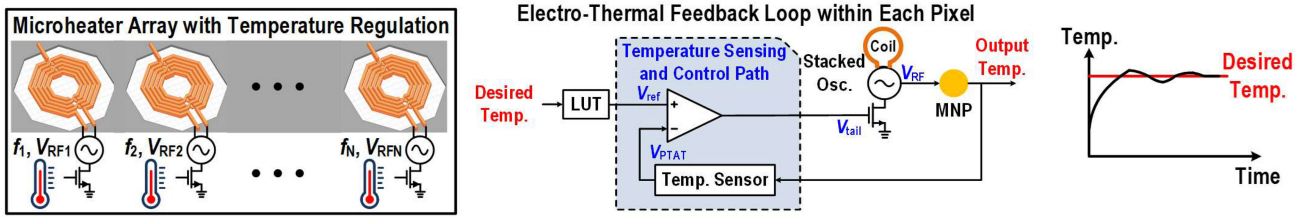

Fig. 1. The proposed microheater array with closed-loop temperature regulation. Each pixel consists of a stacked oscillator and an electro-thermal feedback loop.

However, for applications that require highly localized heating at the cellular level such as magnetogenetics [1] and cancer hyperthermia treatment [7], existing MNP-based thermal applicators, which mainly utilize kHz-MHz magnetic fields, face two challenges – low heating efficiency and limited spatial resolution. On the one hand, heating efficiency is low because the magnetic loss is proportional to the frequency, as shown in (1). Existing kHz-MHz magnetic heaters require high magnetic field intensity to realize sufficient heat, which can only be generated using bulky benchtop instruments with power consumption on the order of kW [17]. Power-consuming water-cooling systems are also needed to dissipate the ohmic loss generated by the magnetic coils [18], introducing additional power and size overhead. On the other hand, the heating spatial resolution is limited because it is challenging to fine control the local magnetic field distribution at kHz-MHz using bulky coils (e.g., 40-130 mm in diameter [17]) and to accurately deliver MNP to the targeted region. Note that MNP are usually injected into the bloodstream for *in vivo* applications; although they tend to accumulate in the target due to the enhanced permeability and retention (EPR) effect [19], they can still travel into surrounding tissues through blood vessels during circulation [20].

To address these challenges, we present a fully integrated magnetic microheater array with closed-loop temperature regulation in this paper, which is an extension of [21]. Its heating principle is based on the ferromagnetic resonance of MNP at GHz microwave frequencies, bringing two unique advantages. First, the required magnetic field strength is significantly reduced at GHz, leading to a fully integrated solution as opposed to conventional bulky benchtop magnetic field generators. Second, we can now manipulate the local magnetic field and heating profiles using on-chip inductors due to the high operating frequency, resulting in substantially improved spatial resolution at the sub-millimeter scale. The high spatial resolution also releases the burden of precise delivery of MNP to the target.

Fig. 1 illustrates the concept of the proposed microheater array. The array is 2-D scalable with each pixel consisting of a stacked oscillator and an electro-thermal feedback loop. The stacked oscillator is proposed here to enable significantly higher magnetic field strength over a conventional cross-coupled oscillator while occupying a single inductor footprint. This unique property eliminates the need for additional RF amplifiers, resulting in reduced pixel area and dc power consumption. In addition, the biasing voltage of the tail transistor $V_{\rm tail}$ is controlled by an electro-thermal feedback loop to enable precise temperature regulation. The efficacy and robustness of the proposed stacked oscillator and the electro-thermal feedback are verified by continuous six-day monitoring of the oscillator voltage swing and a closed-loop temperature regulation experiment, respectively, whose details are presented in Section IV. Finally, we perform a localized heating demonstration by attaching two PDMS membranes mixed with and without MNP to the microheater array chip and monitoring their surface temperatures. Only the area above the inductor ($\sim$0.03 mm^2) is efficiently heated up to 43 °C for the MNP-PDMS membrane, while the baseline temperature stays $<$37.8 °C for the PDMS membrane without MNP. To the best of our knowledge, this is the first fully integrated magnetic microheater array that achieves closed-loop temperature regulation and sub-millimeter spatial resolution.

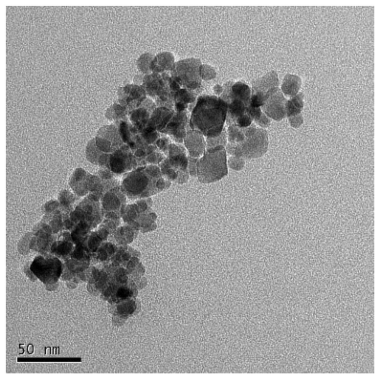

Fig. 2. Transmission electron microscopy (TEM) image of the MNP used in this work [24].

The rest of the paper is organized as follows. Section II presents the multiphysics modeling of the MNP-based heat generation at GHz. Section III presents the architecture of the microheater array chip and design details of the stacked oscillator and electro-thermal feedback loop. Section IV presents the measurement results and the localized heating demonstration. Section V concludes this paper.

II. Multiphysics Modeling

A. MNP Heating Mechanisms

MNP are a class of microscopic magnetic nanomaterial with a diameter of $<$100 nm [14], [22], whose magnetic properties are quite distinct from those of bulk magnetic materials. They can disperse in biological fluids and can be coated with various biologically functional compounds, enabling diverse biomedical applications. In this work, we use fatty-acid-coated 30-nm magnetite iron oxide nanoparticles (Fig. 2) due to their biocompatibility [23] and commercial availability [24].

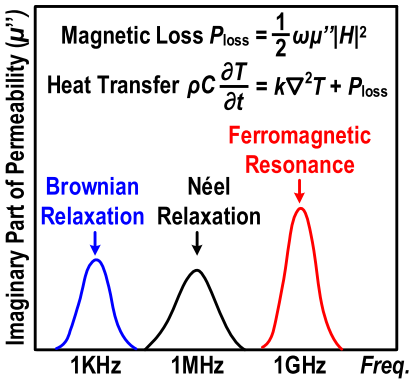

Fig. 3. An illustration of the imaginary part of the permeability of MNP over frequency.

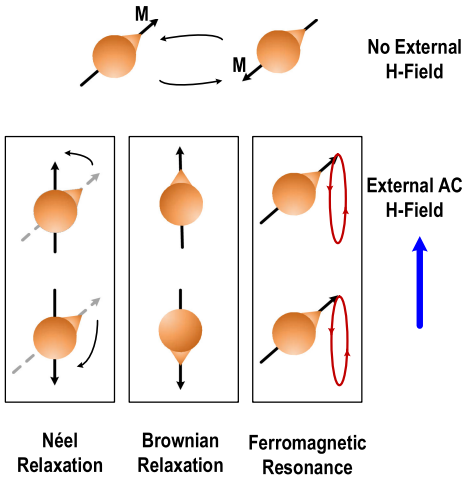

Fig. 4. MNP heating mechanisms: Néel relaxation, Brownian relaxation, and ferromagnetic resonance.

In general, there are three frequency-dependent heating mechanisms for MNP [25], namely Néel relaxation, Brownian relaxation, and ferromagnetic resonance (Fig. 3). At the length scale below a critical point, MNP can support only a single magnetic domain, behaving as a macro magnetic moment [14], [26]. This transition occurs at about 80 nm in diameter for MNP made of magnetite (Fe_3O_4) [14]. Due to the magnetic anisotropy, there exist two energetically favorable directions for the magnetic moment, which are antiparallel to each other and separated by an energy barrier (Fig. 4). When an external magnetic field is applied, heat can be generated by rotating the magnetic moment against the energy barrier (Fig. 4) [27]. If the magnetic moment rotates while the particle itself remains fixed, then the particle has undergone Néel relaxation, and thermal energy is dissipated by the rearrangement of atomic dipole moments within the crystal. If the nanoparticle itself performs mechanical rotation, then the particle has undergone Brownian relaxation, and the heat is generated through shear stress in the surrounding fluid. On the other hand, ferromagnetic resonance happens when the frequency of the external magnetic field is equal to the precession frequency of the magnetic moment (Larmor frequency) [28]. The power of the external magnetic field is then absorbed by

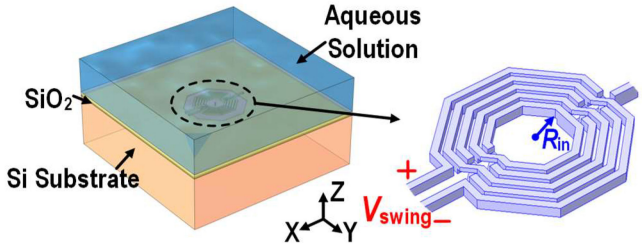

Fig. 5. COMSOL simulation setup.

MNP to sustain the precession and dissipated as heat. The heat loss of all three mechanisms can be modeled using the imaginary part of the permeability μ'' (or the imaginary part of the susceptibility χ''). An illustration of different heating mechanisms over frequency is schematically drawn in Fig. 3. The low-frequency (kHz-MHz) peaks are attributed to Néel and Brownian relaxations, whereas the ferromagnetic resonance usually happens at ∼GHz microwave frequencies.

B. Electro-Thermal Multiphysics Modeling

The two governing equations for MNP-based localized heating are the magnetic loss equation and the heat transfer equation, as

$$P_{\text{loss}} = \frac{1}{2}\omega\mu''|\text{H}|^2$$
$$\rho C\frac{\partial T}{\partial t} = k\nabla^2 T + P_{\text{loss}} \tag{2}$$

where T is the temperature [K], ρ is the density [kg/m^3], C is the specific heat capacity [J/(kg · K)], and k is the thermal conductivity [W/(m · K)]. The two equations are coupled by the power loss term P_{loss}, which serves as the volumetric heat source. $\rho C\frac{\partial T}{\partial t}$ on the left-hand side denotes the transient change of the heat energy, and $k\nabla^2 T$ on the right-hand side models the flow of the heat due to thermal conduction [29]. At the steady-state when $\rho C\frac{\partial T}{\partial t} = 0, k\nabla^2 T = -P_{\text{loss}}$, suggesting that under the same initial temperature and boundary condition, larger P_{loss}, which is proportional to the operating frequency and square of the magnetic field intensity, can lead to a higher temperature rise at the steady-state. For complex geometries such as on-chip inductors, the closed-form solutions, i.e., the local magnetic field distribution and temperature distribution, are difficult to derive. Hence, numerical solutions are found by dividing the region of interest into smaller discrete voxels, assigning the corresponding material properties (μ, ε, σ, ρ, C, and k) to each voxel, and then solving in a finite-element-modeling (FEM) simulator. We use COMSOL Multiphysics for simulations in this work and couple the electromagnetics module and the heat transfer module to evaluate the localized heating process.

A 3-D model is built in COMSOL, as shown in Fig. 5. The model includes the silicon substrate, the SiO_2 dielectric layer, an on-chip inductor, and a box of aqueous MNP solution directly in touch with the top surface of the chip. The on-chip inductor is designed using the top two metal layers (a 4-μm aluminum layer and a 3-μm copper layer) following the stack-up

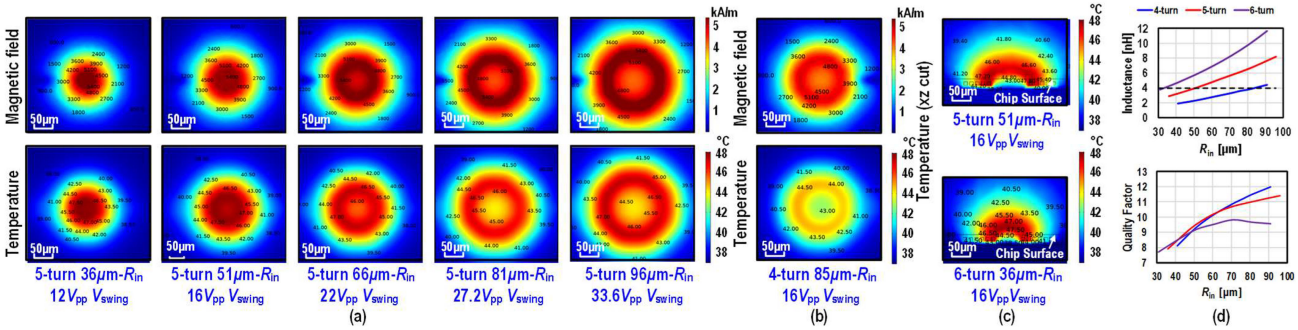

Fig. 6. Simulated magnetic field distributions and temperature distributions at 30 μm above the chip surface of (a) 5-turn inductors with different $R_{\rm in}$ and (b) a 4-turn inductor with 85 μm $R_{\rm in}$. (c) Simulated temperature distributions at the xz cut of a 5-turn inductor with 51 μm $R_{\rm in}$ and a 6-turn inductor with 36 μm $R_{\rm in}$. (d) Simulated inductances and quality factors of different inductor geometries at 1.5 GHz.

of the GlobalFoundries 45-nm CMOS SOI process. We set the imaginary part of the relative permeability of the MNP solution (1.4%wt) to be 0.03 at 1.5 GHz, which is estimated based on our preliminary material characterization.

The design of the on-chip inductor plays a dominant role in determining the local magnetic field and temperature distributions. Hence, inductors with different inner radii ($R_{\rm in}$) and number of turns are simulated using the setup in Fig. 5. The optimal inductor geometry is determined based on the trade-off between the simulated temperature/magnetic field distribution, the inductance, and the quality factor – our goal is to realize a relatively uniform temperature distribution on top of the coil while sustaining the oscillation at 1-2 GHz without excessive dc power.

In the simulations, we assume that the RF excitation current generated by the active oscillator core remains constant and thus, for different coil geometries, we scale $V_{\rm swing}$ proportional to their inductances. From Fig. 6(a), which is simulated at 30 μm above the chip surface, we notice that the local magnetic field intensity and temperature reach their peaks on top of the innermost turn of the inductor. In addition, a local temperature minimum in the middle starts to appear for 5-turn inductors when $R_{\rm in}$ is larger than 51 μm, suggesting that smaller $R_{\rm in}$ achieves better uniformity of temperature and magnetic field distributions. However, smaller $R_{\rm in}$ leads to smaller inductance [Fig. 6(d)], which may compromise the oscillator loop gain and startup condition. Therefore, we choose $R_{\rm in} = 51$ μm as the optimal radius for 5-turn inductors.

Next, we compare the simulation results with different numbers of turns. To realize the same inductance as a 5-turn 51-μm-$R_{\rm in}$ inductor, the required $R_{\rm in}$ increases to 85 μm for a 4-turn inductor [Fig. 6(d)], which results in not only a local minimum of the temperature in the middle of the coil but also a lower temperature rise [Fig. 6(b)]. On the other hand, although a 6-turn 36-μm-$R_{\rm in}$ inductor achieves similar size, distribution uniformity, and temperature rise as those of a 5-turn 51-μm-$R_{\rm in}$ inductor, its quality factor is 1.6× lower [Fig. 6(d)], and its outermost turn contributes little to the effective heating area [Fig. 6(c)]. Based on the trade-off discussed above, we select 5 turns with 51 μm $R_{\rm in}$ as the optimal inductor geometry, resulting in 4.0 nH inductance and 9.5 quality factor at 1.5 GHz.

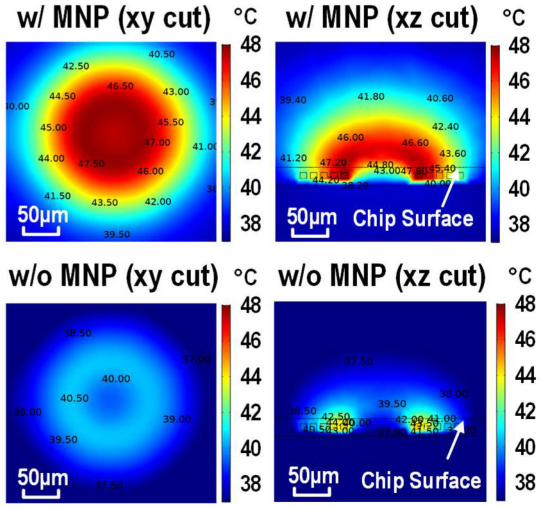

Fig. 7. Simulated temperature distribution with and without MNP. The xy cut is simulated at 30 μm above the chip surface.

Our targeted local thermal stress is up to 43 °C in this work, which is the threshold temperature for cancer hyperthermia and magnetogenetics applications. As the magnetic loss is proportional to the square of the magnetic field intensity, a large RF swing is the key to boost the local temperature rise. As shown in Fig. 7, using the selected 5-turn 51-μm-$R_{\rm in}$ inductor, a 16 $V_{\rm pp}$ RF swing at 1.5 GHz can realize >43 °C up to 80 μm above the inductor surface in the MNP solution. Note that generating such a high voltage swing at ∼GHz presents a significant challenge for the circuit design, which is the motivation of our proposed stacked oscillator (details presented in Section III). On the other hand, the temperature stays <40 °C for the solution without MNP, which typically does not affect the viability of cells and tissues if the duration of the thermal stress is short. The transient temperature rises with and without MNP at 30 μm above the center of the inductor are also shown in Fig. 8.

III. Integrated Microheater Array With Closed-Loop Temperature Regulation

The proof-of-concept microheater array chip has 12 pixels with a pixel size of 0.6 × 0.7 mm^2, as shown in Fig. 9.

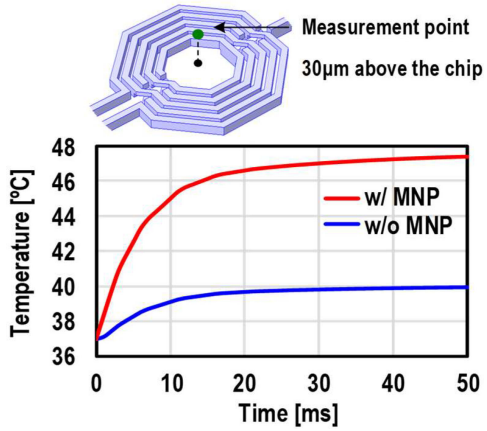

Fig. 8. Simulated transient temperature rises with and without MNP at 30 μm above the center of the inductor.

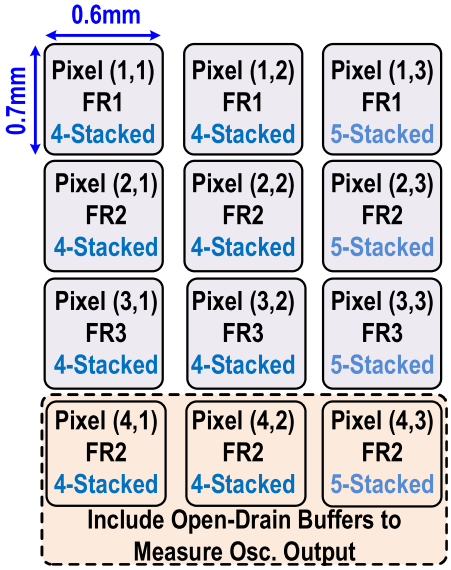

Fig. 9. Floorplan of the integrated microheater array.

The stacked oscillators in the first three rows of the array are designed with three different frequency tuning ranges (1.2–1.6 GHz, 1.5–2.1 GHz, and 2.0–2.6 GHz, respectively), allowing for efficient heating of a wide range of MNP with different ferromagnetic resonant frequencies due to their diverse sizes, material compositions, and nanostructures. The stacked oscillators in the last row are the same as those in the second row, except their outputs are capacitively coupled to open-drain buffers for testing purposes. The oscillators in the first and second columns are four-stacked, while those in the third column are five-stacked. A higher RF output swing can be generated with a larger number of stacked transistors, resulting in stronger localized magnetic field and thermal stress. This section presents the design details of the stacked oscillator and the electro-thermal feedback loop.

A. Stacked Oscillator

As the magnetic loss is proportional to the square of the magnetic field strength, a large RF swing is the key to increase the local temperature rise. Based on the multiphysics simulations presented in Section II, $>16\ V_{pp}$ RF swing is required at 1.5 GHz to realize >43 °C local temperature. Unfortunately, the maximum achievable output swing of conventional cross-coupled LC oscillators is twice the supply voltage, which is usually $<5\ V_{pp}$ for RF CMOS technologies, insufficient to generate the required magnetic field. One possible solution to boost the RF swing is to amplify the oscillator output using RF amplifiers [30]. However, additional inductors are needed in the design of RF amplifiers to serve as the resonating tank or the impedance matching network, which sacrifices the spatial resolution of the microheater array since the pixel size is dominated by the inductor footprint at GHz. Besides, RF amplifiers are power hungry at GHz, introducing significant dc power overhead.

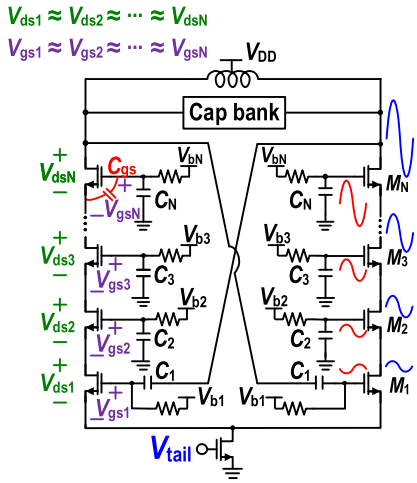

Fig. 10. Schematic of the stacked oscillator.

Inspired by the stacked PA design [31], we propose a stacked oscillator topology (Fig. 10), in which multiple transistors are connected in series ($M_1 - M_N$) to distribute the voltage stress and, in turn, to achieve a large RF output swing using a single inductor footprint. Unlike the cascode topology where the gates of the upper common-gate transistors are ac grounded, additional gate capacitors (C_2–C_N) are introduced to form a capacitive divider with the gate-to-source parasitic capacitance C_{gs} and allow for a voltage swing at the gate. The design goal is to gradually build up the voltage swing at the drain terminals from M_1 to M_N and to ensure the V_{DS} of each transistor is close to one another and smaller than the device breakdown limit. Different from stacked PA, the stacked oscillator requires a positive feedback loop to sustain oscillation. This is accomplished by connecting the oscillator output to the gate of M_1 after voltage attenuation by the capacitor C_1 to keep the V_{GS} of M_1 in the safe operating region. A tail transistor is used to adjust the oscillation amplitude, and its biasing voltage is controlled by the electro-thermal feedback.

SOI processes are particularly attractive for the stacked topology compared to bulk CMOS processes, due to the lack of body effect and relatively small parasitic junction capacitance. For SOI processes, the number of transistors that can be stacked is limited by the buried oxide (BOX) breakdown instead of

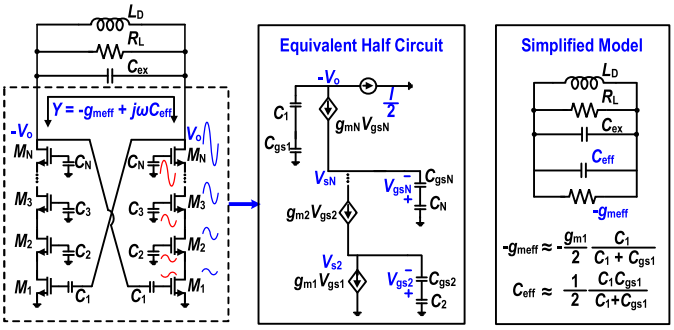

Fig. 11. Derivation of the small-signal equivalent circuit model of the cross-coupled stacked-transistor pair.

the drain-bulk stress. The BOX breakdown is >10V for the GlobalFoundries 45-nm CMOS SOI process used in this work. To leave some margin for safety, we implement four-stacked oscillators with a 6 V supply and five-stacked oscillators with a 7.5 V supply using 1.5 V thick-gate-oxide transistors.

The first design consideration is to ensure a robust oscillation startup condition. Therefore, we derive the small-signal equivalent circuit model of the cross-coupled stacked-transistor pair (Fig. 11) and analyze the loop gain. To simplify the derivation and establish an intuitive understanding of the circuit without compromising the accuracy, we include $C_{\rm gs}$ but ignore the gate-to-drain parasitic capacitance $C_{\rm gd}$ and the output resistance of the transistor $r_{\rm o}$. According to the equivalent half circuit model, we have

$$g_{\rm mN-1}V_{\rm gsN-1} = g_{\rm mN}V_{\rm gsN} + j\omega C_{\rm gsN}V_{\rm gsN} \tag{3}$$

where

$$V_{\rm gsN} = \frac{-C_{\rm N}}{C_{\rm N}+C_{\rm gsN}}V_{\rm sN} \tag{4}$$

The differential output admittance of the cross-coupled stacked-transistor pair can then be derived as

$$Y = \frac{I}{2V_{\rm o}} = \frac{-g_{\rm m1}g_{\rm m2}\cdots g_{\rm mN}}{2\,(g_{\rm m2}+sC_{\rm gs2})\cdots(g_{\rm mN}+sC_{\rm gsN})}\frac{C_1}{C_1+C_{\rm gs1}} + j\omega\frac{C_1C_{\rm gs1}}{2\,(C_1+C_{\rm gs1})} \tag{5}$$

Assuming transistor $g_{\rm m}$ is much larger than $j\omega C_{\rm gs}$, which is true for GHz oscillator designs where the oscillation frequency is much lower than the cutoff frequency of the transistor ($f_{\rm T}$), the amount of RF current flowing into the gate capacitors can be ignored, and (4) can be simplified as

$$Y \approx -\frac{g_{\rm m1}}{2}\frac{C_1}{C_1+C_{\rm gs1}} + j\omega\frac{C_1C_{\rm gs1}}{2\,(C_1+C_{\rm gs1})} = -g_{\rm m,eff} + j\omega C_{\rm eff} \tag{6}$$

The small-signal loop gain $A_{\rm v}$ can be calculated as

$$A_v = g_{\rm m1}\frac{C_1}{C_1+C_{\rm gs1}}R_{\rm L} \tag{7}$$

Here, $R_{\rm L}$ is the effective parallel resistance of output the LC tank, as

$$R_{\rm L} = Q_{\rm L}\omega_{\rm osc}L_{\rm D} \tag{8}$$

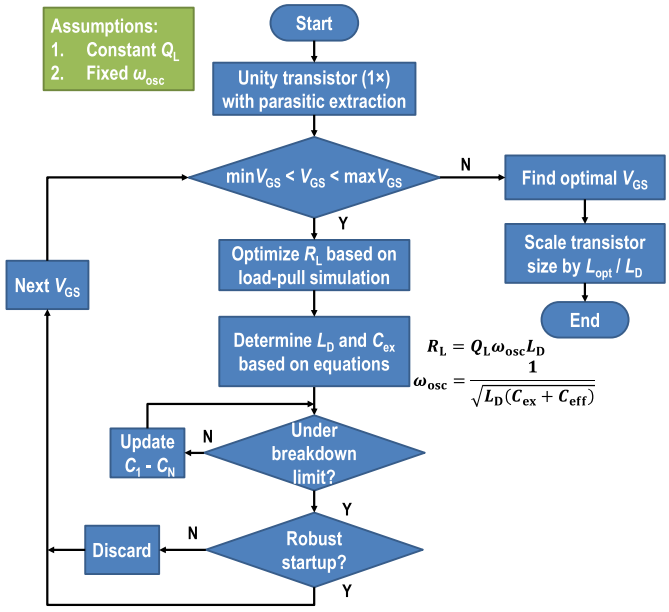

Fig. 12. Flowchart to optimize the dc-to-RF efficiency of the stacked oscillator.

$$\omega_{\rm osc} = \frac{1}{\sqrt{L_{\rm D}(C_{\rm ex}+C_{\rm eff})}} \tag{9}$$

where $L_{\rm D}$ is the output inductance, $Q_{\rm L}$ is the quality factor of the inductor, $\omega_{\rm osc}$ is the oscillation frequency, and $C_{\rm ex}$ is the additional capacitance in parallel with the output inductor. Although oscillators can start to oscillate as long as the loop gain is larger than 1, we use small-signal loop gain to be >2 as the criteria for a robust startup condition in the design.

The dc-to-RF efficiency of the oscillator is another critical design specification to minimize the dc power consumption and the undesired ohmic loss from transistors. Since an oscillator is inherently a large-signal circuit, here we borrow the PA load-pull optimization methodology [32] to find the optimal design parameters, including the transistor size, the biasing voltage for stacked transistors $V_{\rm GS}$, the additional parallel capacitance $C_{\rm ex}$, and the gate capacitances C_1-$C_{\rm N}$. The proposed optimization flow is summarized in Fig. 12, which not only optimizes the dc-to-RF efficiency but also considers the breakdown limit of stacked transistors and the oscillation startup condition. It is under the assumption that the quality factor of the inductor $Q_{\rm L}$ (∼9.5 from 3-D EM simulations) remains constant for different inductances, and the oscillation frequency is fixed.

The optimization starts with picking up an arbitrarily sized transistor, which we refer to as the unity transistor (1×), and extracting its layout parasitics to ensure accurate device modeling at GHz. Theoretically, the peak dc-to-RF efficiency is achieved when the load impedance is chosen in the way that the output voltage swing and the device current swing are simultaneously maximized [33]–[37]. Since the optimal load impedance is biasing dependent, we determine the optimal $R_{\rm L}$ for different $V_{\rm GS}$ based on large-signal load-pull simulations. Unlike the PA design that utilizes an impedance transformation network to realize the desired $R_{\rm L}$, here, $R_{\rm L}$ is the effective parallel resistance of the inductor. Therefore, once $R_{\rm L}$ is determined, the optimal

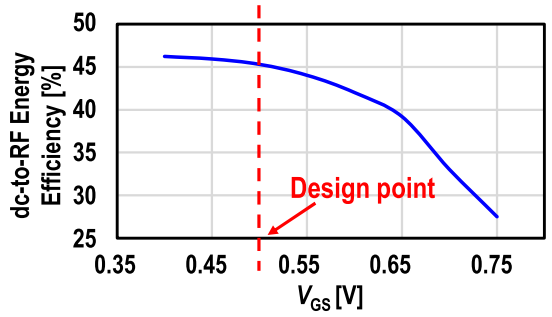

Fig. 13. Simulated dc-to-RF energy efficiency against the biasing voltage of the stacked transistors $V_{\rm GS}$.

$L_{\rm D}$ can be calculated based on (8), and the required $C_{\rm ex}$ to sustain the oscillation at the desired frequency can be calculated based on (9). Next, gate capacitances C_1-$C_{\rm N}$ are chosen to make sure all transistors are within the breakdown limit. Meanwhile, we also check the small-signal loop gain to ensure that a robust startup condition can be realized. This process is repeated by sweeping $V_{\rm GS}$. Once the optimal $V_{\rm GS}$ is determined, the last step is to scale the transistor size by a factor of $L_{\rm opt}/L_{\rm D}$, as the optimal inductor geometry and its corresponding inductance $L_{\rm opt}$ have been decided based on the multiphysics simulations in Section II.

According to the proposed optimization flow, the simulated dc-to-RF efficiency against the biasing voltage of stacked transistors $V_{\rm GS}$ is shown in Fig. 13. Intuitively, a smaller $V_{\rm GS}$ reduces the conduction angle in the large-signal operation, leading to a better energy efficiency. However, further decreasing $V_{\rm GS}$ will compromise the loop gain. Since <0.4 V $V_{\rm GS}$ can no longer guarantee robust oscillation startup across process and temperature variations and the efficiency remains similar for $V_{\rm GS}$ <0.5 V, we choose 0.5 V as our design point (Fig. 13). The proposed optimization methodology yields a final implementation of a four-stacked oscillator with 200 μm/112 nm transistor size and a five-stacked oscillator with 248 μm/112 nm transistor size, resulting in 45% simulated dc-to-RF efficiency.

The simulated drain, gate, drain-to-source, and drain-to-gate transient waveforms of each stacked transistor are shown in Fig. 14. The simulations include the layout parasitics and the EM-simulated output inductor. The gate and drain voltage swings gradually build up from the bottom transistor to the top, and only $V_{\rm g1}$ is out of phase due to the positive feedback. The simulation results also verify that $V_{\rm ds}$ and $V_{\rm dg}$ for different transistors are close to one another and within the breakdown limit of 3 V.

The frequency tuning of the stacked oscillator is enabled by a 4-bit binary-weighted capacitor bank, as shown in Fig. 15. There exists a trade-off between the frequency tuning range and the quality factor of the capacitor bank [38]. A larger transistor size for switches reduces the on resistance, which increases the quality factor; however, a larger transistor size results in a larger off capacitance, which compromises the tuning range. To alleviate this trade-off, the overall frequency tuning range is divided into three sub-ranges (1.2–1.6 GHz, 1.5–2.1 GHz, and 2.0–2.62 GHz), and the stacked oscillators in different rows of the array

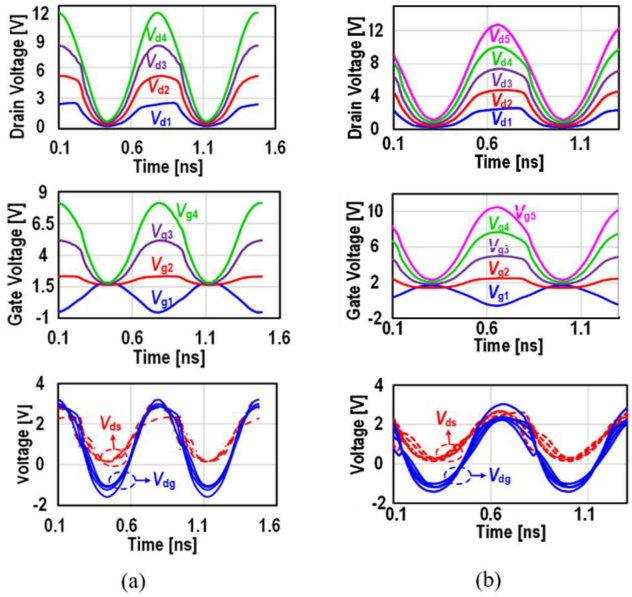

Fig. 14. Post-layout simulated drain, gate, drain-to-source, and drain-to-gate transient waveforms of each stacked transistor in (a) the four-stacked oscillator and (b) the five-stacked oscillator.

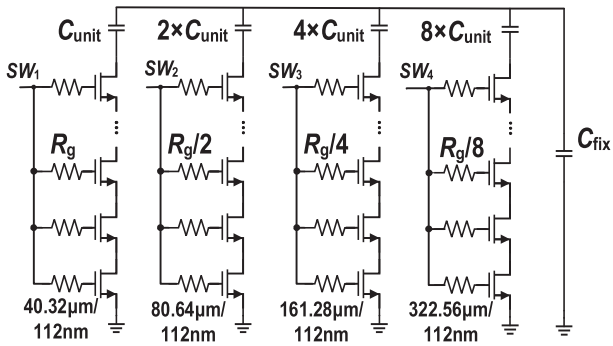

Fig. 15. Schematic of the 4-bit stacked capacitor bank.

are assigned with different sub-ranges. In addition, we optimize the capacitances of $C_{\rm unit}$ and $C_{\rm fix}$ and the size of the switches so that the output RF swing remains almost constant over the entire frequency range. The post-layout simulated frequency tuning range and the output RF swing of the stacked oscillators in the second frequency range are shown in Fig. 16. To ensure reliable operation of the switches, especially when they experience large RF swing in the off state, we implement a four-stacked switch with a large resistor $R_{\rm g}$ added to the gate. $R_{\rm g}$ introduces a voltage swing by forming a capacitive divider between $C_{\rm gs}$ and $C_{\rm gd}$, which prevents unwanted turning on and the breakdown of the switches [39]. The post-layout simulated transient waveforms for the stacked switches in the off state and the on state are shown in Fig. 17. The two sets of simulations verify that stacked switches always work in the safe operating region.

B. Temperature Sensing and Control Path

The temperature sensing and control path in each pixel senses the local temperature and generates the biasing voltage for the

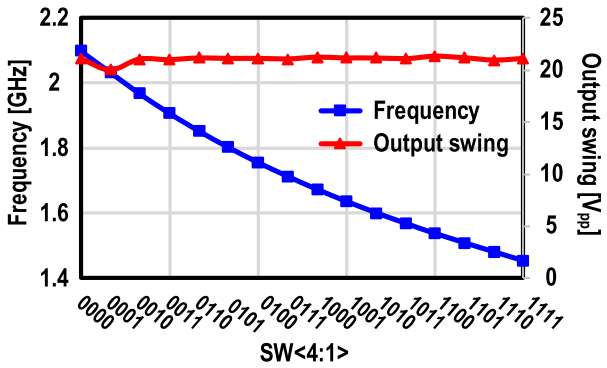

Fig. 16. Post-layout simulated frequency tuning range and output RF swing of the stacked oscillators in the second row of the microheater array.

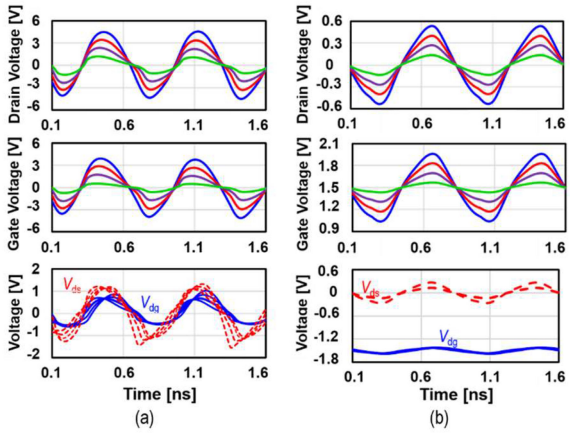

Fig. 17. Post-layout simulated transient waveforms for the stacked switches in (a) the off state and (b) the on state.

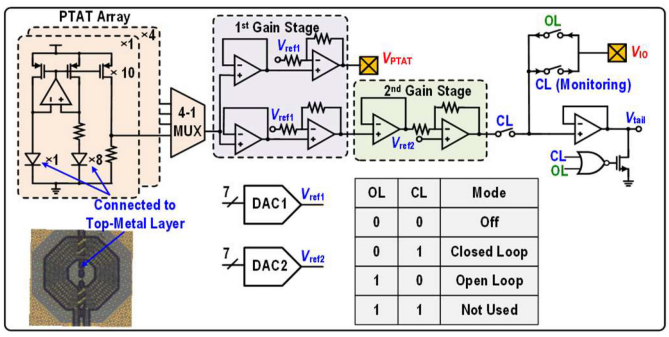

Fig. 18. The schematic of the temperature sensing and control path.

tail transistor of the stacked oscillator for closed-loop temperature control. Its circuit schematic is shown in Fig. 18. The first stage is a Proportional-To-Absolute-Temperature (PTAT) temperature sensor array [40]–[43]. Four diode pairs are placed at the four corners of the oscillator inductor and below the ground plane, which are relatively away from the active core of the stacked oscillator to avoid sensing the ohmic loss generated by the transistors. The diode pairs are routed to small top-layer floating metals in the middle of the inductor to sense the surface temperature. To minimize the coupling from the large oscillator RF swing, the floating metal pairs are placed in the symmetry plane, which is the virtual ground for the differential inductor.

Followed by a 4:1 MUX, the PTAT output is further amplified and buffered to regulate the biasing voltage $V_{\rm tail}$ of the tail transistor of the stacked oscillator. Two amplifier stages are used to ensure a large loop gain and their reference voltages are generated by two separate 7-bit coarse-fine resistor-string DACs [44]. $V_{\rm ref1}$ is set to guarantee the PTAT output is linearly amplified, and $V_{\rm ref2}$ is determined by the targeted temperature through a lookup table. A low impedance at $V_{\rm tail}$ is highly desired, especially outside the bandwidth of the unity-gain buffer, to filter out the coupling from the strong oscillation swing. Therefore, a 1 pF capacitator is added to $V_{\rm tail}$, which also introduces a pole to the temperature sensing and control path. Note that the dominant pole in the electro-thermal feedback loop is the thermal pole, which is usually below kHz [45]. All the electrical poles are designed and verified to be higher than 100 kHz. Thus, the electro-thermal feedback loop behaves as a first-order system without stability concerns.

The temperature sensing and control path can be configured into three modes using switches OL and CL [46]–[48]. First, in the closed-loop mode, the PTAT and gain stages are enabled to regulate $V_{\rm tail}$. The output voltages of the first and second gain stages are monitored by two separate I/O pads for the testing purpose. Second, in the open-loop mode, the stacked oscillator is controlled by an external biasing through $V_{\rm IO}$. The PTAT and two gain stages are turned off to save power. Third, in the off mode, the stacked oscillator is turned off by the pull-down transistor, and the entire temperature sensing and control path is also turned off.

To verify the thermal regulation behavior, we perform a transient closed-loop electro-thermal simulation using Cadence Virtuoso and COMSOL, with the flowchart shown in Fig. 19 [49]. At each discrete time instant $t_{\rm i}$ (every 1 ms in our simulations), an electrical simulation is performed at the local temperature $T(t_{\rm i})$, from which $V_{\rm tail}$ and the RF swing of the stacked oscillator $V_{\rm swing}(t_{\rm i})$ are recorded. Then $V_{\rm swing}(t_{\rm i})$ is applied to the differential inductor for transient thermal analysis in COMSOL using the setup in Fig. 5, resulting in an updated local temperature $T(t_{\rm i+1})$. This process is repeated until thermal equilibrium is observed. An example following this simulation flow is shown in Fig. 20. The electro-thermal feedback loop is enabled at $t = 45$ ms, and the temperature is eventually settled at 45 °C. The overall loop gain including the T-to-$V_{\rm swing}$ conversion and the $V_{\rm swing}$-to-T conversion is calculated as approximately 27 dB from Cadence Virtuoso and COMSOL simulations.

IV. Measurement Results

The integrated microheater array chip is fabricated in the GlobalFoundries 45-nm CMOS SOI technology. The chip microphotograph is shown in Fig. 21 with a zoom-in view of the microheater pixel (0.7 mm × 0.6 mm). An on-chip Serial-to-Parallel-Interface (SPI) is implemented for digital programming. The clock, data, and latch signals of the SPI interface are generated by a data acquisition (DAQ) module (Measurement Computing USB 1608G). The biasing voltages of the stacked

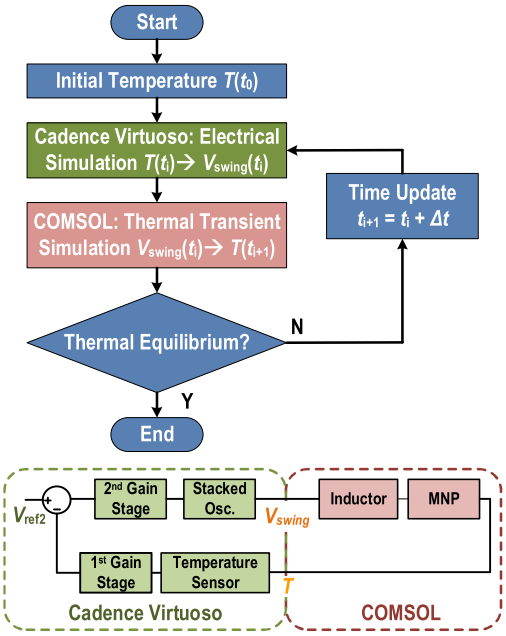

Fig. 19. Electro-thermal simulation flowchart to simulate the closed-loop temperature regulation behavior.

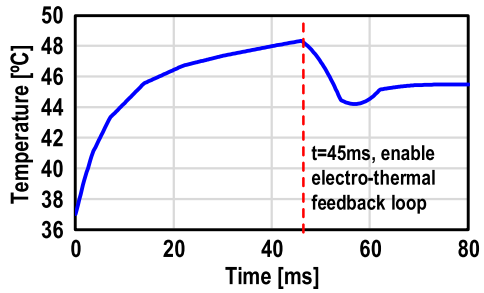

Fig. 20. Transient temperature response following the electro-thermal simulation in Fig. 19.

transistors are generated using resistive dividers between the supply voltage of the oscillators and the ground on the printed circuit board (PCB), which can be readily implemented on-chip. The biasing voltages are 0.7V, 2V, 3.5V, and 5V for four-stacked oscillators and 0.65V, 2V, 3.5V, 5V, and 6.5V for five-stacked oscillators. The supply voltages are 6V and 7.5V for four-stacked oscillators and five-stacked oscillators, respectively. This section presents the measurement results of the stacked oscillator, the temperature sensing and control circuit, and a localized heating demo.

A. Electrical Characterization of the Stacked Oscillator

To monitor the output swing of the stacked oscillator, an open-drain buffer is added to the fourth row of the array and capacitively coupled to the oscillator output, as shown in Fig. 22. A dummy buffer is added to the other side to maintain differential symmetry. The drain terminal of the open-drain buffer is wire bonded to the PCB and routed to an SMA connector via a 50 Ω transmission line. An off-chip bias tee is connected between the SMA connector and the spectrum analyzer.

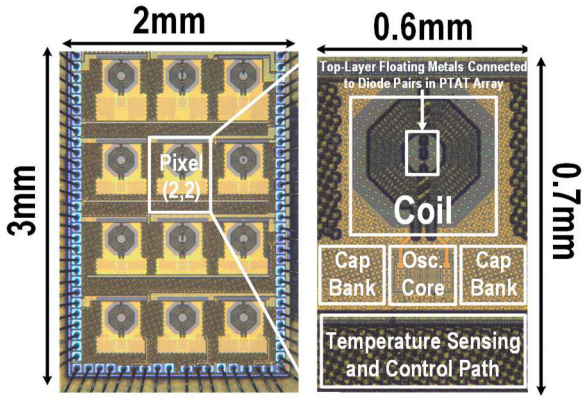

Fig. 21. Microphotograph of the integrated microheater array chip.

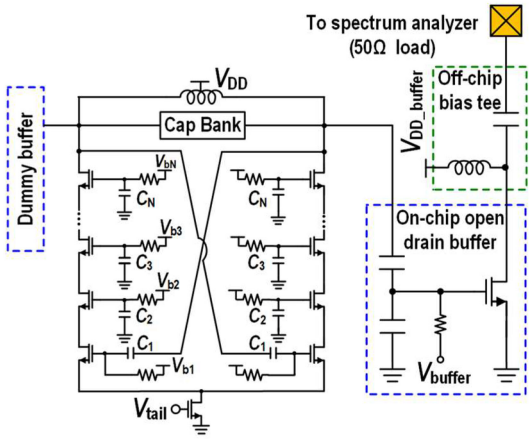

Fig. 22. An open-drain buffer is capacitively coupled to the oscillator output to measure the oscillator output swing.

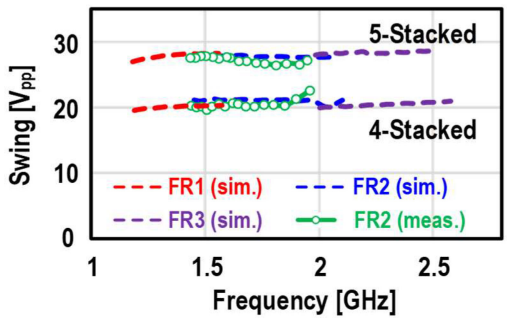

Fig. 23. Measured and simulated RF swing of the stacked oscillators.

The measured and simulated RF swings of the four-stacked and five-stacked oscillators are shown in Fig. 23. The measured RF swing is $>19.5\ V_{pp}$ for the four-stacked oscillator and $>26.5\ V_{pp}$ for the five-stacked oscillator from 1.44 to 1.95 GHz, which is very close to our simulation except for a slight frequency down-shift. By reducing the biasing voltage of the tail transistor V_{tail}, the oscillation amplitude can be backed-off (Fig. 24). This property is used in the electro-thermal feedback to lower the output RF swing and the dc power if a lower temperature is desired. In addition, during a continuous six-day monitoring

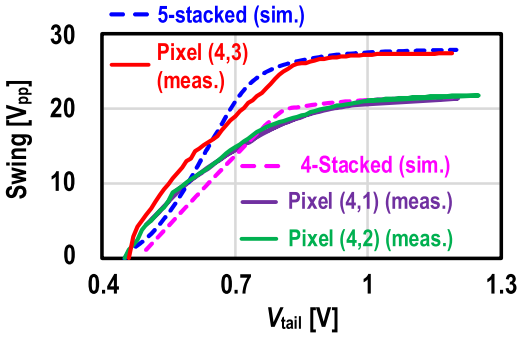

Fig. 24. Measured and simulated RF swing against the biasing voltage of the tail transistor $V_{\rm tail}$ at 1.45 GHz.

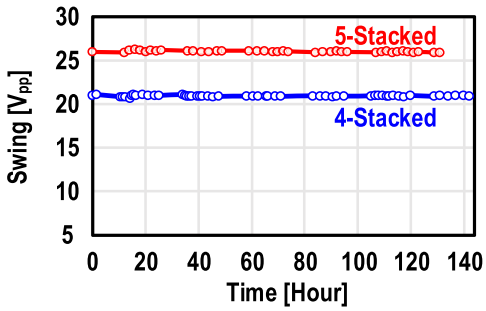

Fig. 25. Continuous six-day measurement of the stacked oscillator output.

Fig. 26. The temperature sensing and control path is measured in a temperature chamber.

(Fig. 25), the oscillation swings remain constant for both four-stacked and five-stacked oscillators, verifying the safe and robust operation of the stacked transistors.

B. Electrical Characterization of the Temperature Sensing and Control Path

The temperature sensing and control path is characterized in a temperature chamber (Fig. 26). The measured $V_{\rm PTAT}$, which is the temperature sensor output amplified by the first gain stage (highlighted in Fig. 18), against the ambient temperature is shown in Fig. 27. The response slope is 27 mV/°C from 24 to 48 °C, presenting good linearity and aligning with our simulation. The measured $V_{\rm IO}$, which is the output of the second gain stage (highlighted in Fig. 18), against the ambient temperature is shown in Fig. 28. The measured temperature-to-$V_{\rm tail}$ conversion gain is −220 mV/°C. The operating temperature range of the

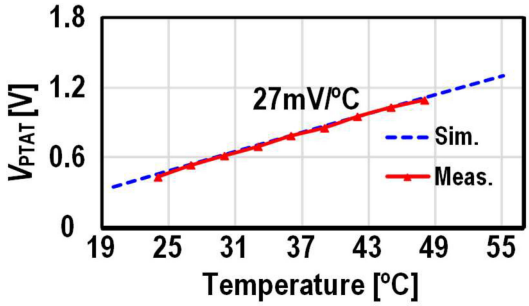

Fig. 27. Measured $V_{\rm PTAT}$ versus temperature.

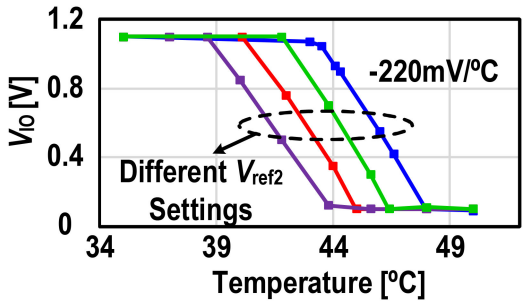

Fig. 28. Measured VIO versus temperature.

electro-thermal feedback loop can be fine-tuned by adjusting the DAC setting of $V_{\rm ref2}$.

C. Localized Heating Demo Using PDMS Membranes

Two PDMS membranes mixed with and without MNPs are used to validate the localized heating performance of the magnetic microheater array. The reason we choose to work with PDMS membranes instead of MNP fluid is to simplify the packaging and avoid shorting bonding wires in the fluid. The PDMS membranes are fabricated following the protocol in [50], and the process is summarized in Fig. 29. We first prepare a sacrificial layer using a photoresist (AZ5209) after the substrate pre-treatment. Next, we mix the PDMS (Sylgard 184 Silicone Elastomer, Dow Corning Corporation) with MNP with a concentration of 3.25%wt. The MNP-PDMS mixture is thoroughly stirred for 20 minutes followed by sonication in a sonic bath at 35 °C for an hour. Then the MNP-PDMS mixture is spin-coated on the sacrificial layer [50] and cured at 125 °C for 20 minutes. Afterward, the wafer is soaked in an acetone solution for 2 minutes, and the MNP-PDMS membrane floats on the solution surface after the sacrificial layer is dissolved. The thickness of the membrane is estimated to be 36 μm based on the speed and duration parameters used in the spin coating [51]. Finally, the membrane is cut into small pieces and attached to the chip surface.

The measurement setup of the PDMS-membrane-based localized heating demonstration is shown in Fig. 30. The temperature distribution on the membrane surface is monitored using an IR camera (Infratec VarioCAM HD 900) and real-time displayed on the computer.

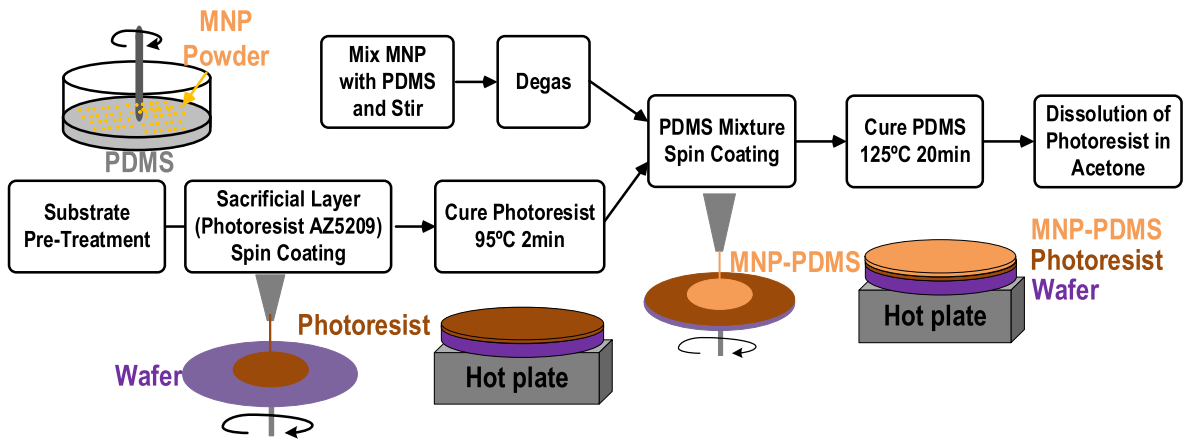

Fig. 29. Fabrication protocol of the PDMS membrane mixed with MNP.

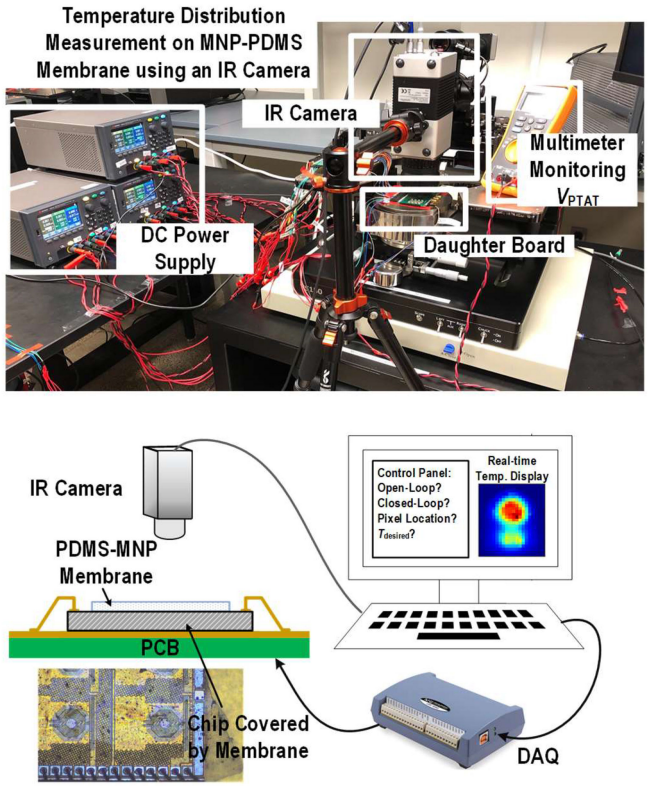

Fig. 30. Measurement setup of the localized heating demonstration using PDMS membranes with and without MNP.

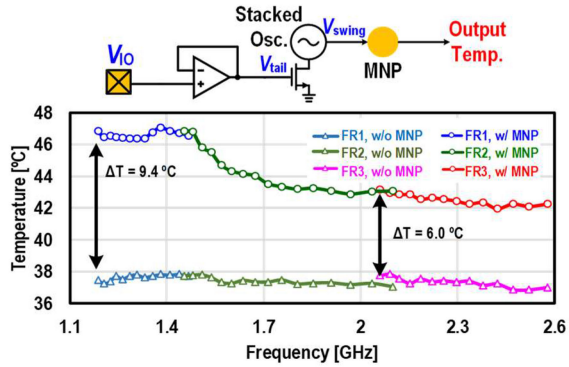

Fig. 31. Open-loop demonstration: measured surface temperatures of PDMS membranes with and without MNP against oscillation frequency.

In the open-loop demonstration (Fig. 31), $V_{\rm tail}$ is biased off-chip through $V_{\rm IO}$. We use the three stacked oscillators in the second column to measure the local temperature rise in the three different frequency ranges. For the PDMS membrane mixed with MNP, the local temperature is between 41.93 and 47.05 °C. On the other hand, for the PDMS membrane without MNP, the local temperature stays below 37.8 °C under the same biasing condition. The measured temperature distributions at 1.45 GHz on the PDMS membrane surfaces with and without MNP are shown in Fig. 32. Only the area above the inductors (∼0.03 mm^2) is efficiently heated up.

In the closed-loop demonstration, we first program the DAC setting of $V_{\rm ref2}$ based on the targeted temperature. $V_{\rm tail}$ is then automatically generated through the electro-thermal feedback loop. Fig. 33 summarizes the settled temperature $T_{\rm settled}$ against the desired temperature $T_{\rm desired}$. $T_{\rm settled}$ is the average IR camera reading over 5 minutes at 1 frame/s frame rate. Extra calibration steps, e.g., correlating the camera reading with on-chip PTAT voltage and comparing the camera reading of the PCB with the known ambient temperature, were performed to guarantee the accuracy of the temperature measurement. The maximum/RMS temperature error is 0.53/0.29 °C from 37 to 49 °C. A smaller temperature error can be potentially achieved by increasing the number of bits of the DAC.

Finally, two adjacent pixels in a row or in a column are enabled simultaneously, verifying the sub-millimeter spatial resolution of the local temperature profile, as shown in Fig. 34. Again, only the area above the inductors (∼0.03 mm^2) within each pixel is efficiently heated up. Good magnetic isolation is the key to minimize the mutual coupling between adjacent pixels, which is achieved by employing an on-chip ground plane between inductors.

Note that there exists a tradeoff between the penetration depth, spatial resolution, and heating efficiency. Compared to magnetic heaters at KHz-MHz based on Néel or Brownian

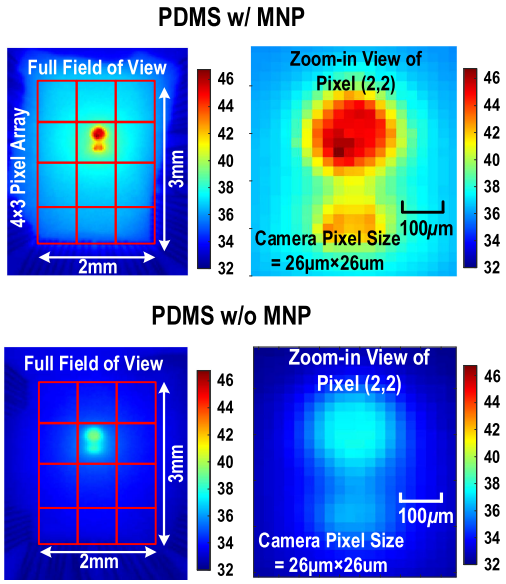

Fig. 32. Open-loop demonstration: surface temperature distribution with and without MNP when pixel (2, 2) is enabled.

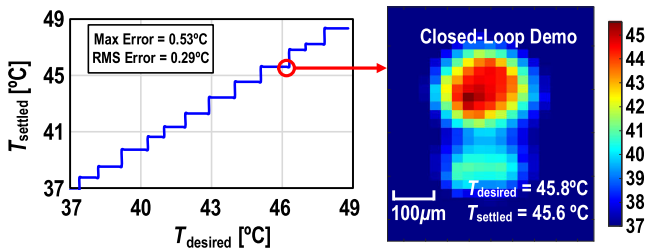

Fig. 33. Closed-loop demonstration: settled temperature versus the desired temperature and a zoom-in view of the surface temperature distribution.

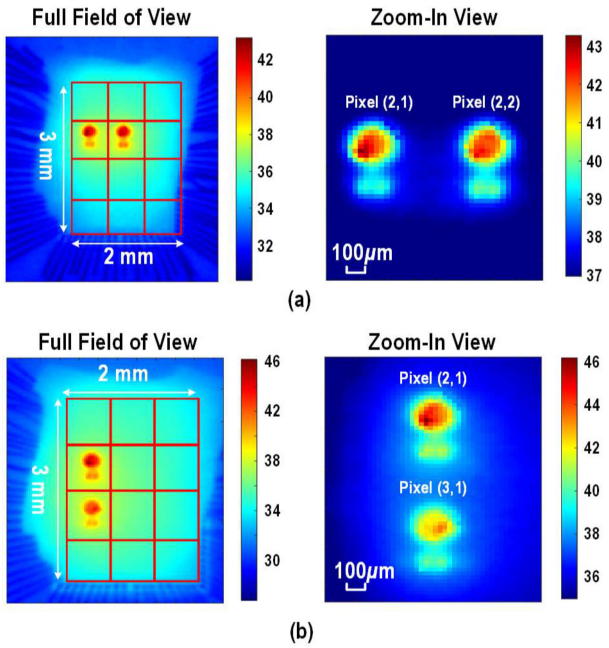

Fig. 34. Surface temperature distribution when two adjacent pixels (a) in a row or (b) in a column are enabled simultaneously.

TABLE I
PERFORMANCE COMPARISON TABLE WITH EXISTING MNP-BASED THERMAL APPLICATORS

	This Work	[30]	[17]
Heating Mechanism	**Ferromagnetic Resonance**	Ferromagnetic Resonance	Brownian, Néel Relaxation
Frequency Range	**1.18GHz – 2.62GHz**	1.8GHz – 2.4GHz	100KHz – 500KHz
Size of Coil	**5-Turn On-Chip Coil, 220μm/51μm Outer/Inner Diameter**	1.5-Turn On-Board Coil, 1.9mm × 1.9mm Internal Area	3D Round Coil, 40-130mm Diameter
Spatial Resolution	**0.6mm × 0.7mm**	65.8mm × 4mm	>40mm × 40mm
Number of Pixels	**12**	1	1
Max. RF Swing or Heating Power	**>19.5V_{pp} for 4-Stacked >26.5V_{pp} for 5-Stacked**	24.6V_{pp}	5KW – 12KW
Max. Magnetic Field	**9.1kA/m**	N/A	110.4kA/m
dc Power	**<0.36W per Pixel†**	>4.56W (PA power only)	3.3KW – 6.6KW
dc-to-RF Efficiency	**>45% (sim.)**	33% for PA + Isolator	N/A
Thermal Regulation	**Yes**	No	No
Technology	**45nm CMOS SOI**	PCB including custom PA chip (0.32μm SOI), VCO chip (0.13μm CMOS), etc.	Benchtop
Size	**6mm²**	421mm²	60cm × 35cm × 50cm

†dc power can be backed off at smaller RF swing.

relaxation, the spatial resolution and heating efficiency get better as the frequency increases to GHz, but at the cost of reduced penetration depth. The ∼100 μm penetration depth achieved in this proof-of-concept platform is targeted for *in-vitro* and microfluidics heating experiments, which is less of a concern since the diameter of a cell typically ranges between 10 and 100 μm. For *in-vivo* applications that require larger penetration depth at millimeter to centimeter scale, one promising solution is to decrease the operating frequency to hundreds of MHz, where the reduced ferromagnetic resonant frequency has been demonstrated by material engineering of MNP [52], and the proposed microheater core, i.e., the stacked oscillator, can be readily implemented. Alternatively, one can increase the dimension of the inductor at the expense of reduced spatial resolution, e.g., an on-board inductor with an internal area of 1.9 mm × 1.9 mm is implemented in [30], achieving >3.5 mm penetration depth at 2 GHz.

V. CONCLUSION

This paper presents a first-of-its-kind fully integrated magnetic microheater array based on the ferromagnetic resonance of MNP at GHz microwave frequencies. Table I summarizes the key specifications of the design and compares them with state-of-the-art MNP-based thermal applicators. Powered by the proposed stacked oscillator, this work offers the highest spatial resolution, the lowest dc power consumption, and the best dc-to-RF energy efficiency. In addition, precise closed-loop temperature regulation is achieved by the proposed electro-thermal feedback loop. With these features, the presented high-resolution magnetic microheater array would be applicable in a wide range of biomedical applications requiring localized heating.

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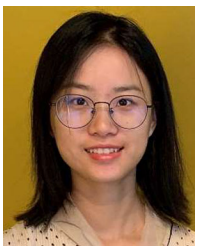

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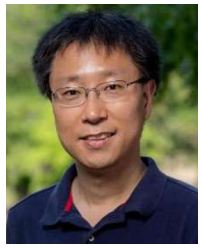

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