

Guest Editorial

Special Issue on Selected Papers From ISCAS 2021

THIS Special Issue of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS highlights a selection of biomedical research papers from the 2021 IEEE International Symposium on Circuits and Systems (ISCAS 2021) in Daegu, Korea. Due to COVID-19, ISCAS 2021 was organized as a hybrid conference from May 22 to 28, 2021. As the flagship international conference of IEEE Circuits and Systems Society, ISCAS 2021 was driven by the theme “Smart Technology for an Intelligent Society” aiming to emphasize the potential of the CAS Society to find multidisciplinary solutions for the societal and engineering challenges of our times. The papers in this special issue were selected out from a comprehensive list of papers those presented in the sessions of ISCAS 2021 with strong focus on biomedical applications.

Based on technical review scores from independent experts worldwide, 30 highly ranked papers which covered circuits and systems for biomedical applications in ISCAS 2021 were invited to submit their extended versions for consideration in the Special Issue. This Special Issue received 23 contributions and after a thorough peer review process with iteration of manuscript revisions, a final set of 8 papers was accepted to form this Special Issue.

A brief description of these papers, which are listed in the order that they appear in the special section, is provided below.

The paper titled “Sub-100 μ W Multispectral Riemannian Classification for EEG-based Brain–Machine Interfaces” reports an energy-efficient classifier for brain–machine interfaces that enable the users to control machines by merely thinking of performing a motor action. The classifier achieves 75.1% accuracy on a 4-class motor imagery classification task. The technique was optimized using mixed-precision quantization for achieving an ideal accuracy-cost trade-off for wearable applications. The classifier was implemented and tested on a low power micro-controller.

The paper titled “Q-PPG: Energy-Efficient PPG-based Heart Rate Monitoring on Wearable Devices” presents an energy-efficient heart rate monitor for wearable devices. To tackle motion artifacts caused by movements of the subject’s arm, this work proposes a design space exploration methodology to generate a rich family of deep temporal convolutional networks for heart rate monitoring. The proposed accurate quantized network achieves 4.41 beats per minute of mean absolute error with an energy consumption of 47.65 mJ and a memory footprint of 412 kB.

The paper titled “Multimodal Multiresolution Data Fusion Using Convolutional Neural Networks for Wearable Sensing” reports a novel convolutional neural network model for the fusion of multimodal and multiresolution 1-dimensional signals from different sensors. A fusion model with electrocardiogram, peripheral oxygen saturation signal, and abdominal movement signal demonstrated an accuracy of 99.72% and a sensitivity of 98.98%. The proposed fusion model is also estimated to consume 5.61 μ J per classification.

The paper titled “A Multi-Channel Stimulator With High-Resolution Time-to-Current Conversion for Vagal-Cardiac Neuromodulation” presents an integrated stimulator for a cardiac neuroprosthesis to restore the parasympathetic control after heart transplantation. The proposed stimulator proposes a novel capacitor time-based digital-to-analog conversion using only 250 nA as a bias current. The stimulator consists of 16 independent channels and each channel can deliver 550 μ A under a 30 V output stage.

The paper titled “Evaluation of Level-Crossing ADCs for Event-Driven ECG Classification” introduces a novel methodology for optimizing design parameters of level-crossing analog-to-digital converters (LC-ADCs). The authors proposed using a one-dimensional convolutional neural network based classifier to evaluate the event-driven data from various LC-ADC models. With classification performance comparable to a Nyquist sampled ADC, the proposed ADC model offers 3x data compression while maintaining the signal-to-distortion ratio of more than 21 dB. Furthermore, this model requires only 49% FLOPS for classification in comparison with a uniformly sampled model.

The paper titled “A 4.49 nW/Pixel Light-to-Stimulus Duration Converter-Based Retinal Prosthesis Chip” presents a photodetector and simulator array architecture intended for retinal prostheses. Compared to prior approaches that convert light to stimulus amplitude or to fixed-amplitude pulse rate, this approach converts detected light level into a stimulus duration. Photodetectors and electrodes are overlaid to increase density. A 288-pixel prototype IC was fabricated in 0.18 μ m CMOS. The implemented chip provides 25.5 dB stimulation dynamic range with a power consumption of 4.49 nW/pixel, and experimental results using mouse retinal ganglion cells demonstrate the effectiveness of the approach for modulating spiking response as a function of light intensity.

The paper titled “A Polar-demodulation-based Impedance-measurement IC Using Frequency-shift Technique with Low Power Consumption and Wide Frequency Range” presents an IC architecture for impedance measurement, intended for applications in biosensing and electrochemical impedance spectroscopy.

(EIS). The architecture uses a frequency-shift technique to extend the impedance sensing operation up to 10 MHz, and polar demodulation using a current sensing reference resistor is employed. Measured results from a $0.18\text{ }\mu\text{m}$ CMOS prototype IC demonstrate $756\text{ }\mu\text{W}$ while supporting a measurement frequency range from 100 Hz to 10 MHz with maximum magnitude and phase errors of 1.1% and 1.9° , respectively.

The paper titled “Ultra-Thin Chips with ISFET Array for Continuous Monitoring of Body Fluids pH” presents an pH sensor system-on-ultra-thin-chip (SoUTC) architecture designed and fabricated using a $30\text{ }\mu\text{m}$ thick CMOS substrate. The thin substrate enables a deformable IC for integration into wearable pH sensing platforms. The core of the SoUTC is an 8×8 array of integrated ISFET sensors with in-pixel current-mode readout. The paper includes both multiphysics modeling of the ISFET electrode-electrolyte interface, as well as experimental characterization of a prototype IC fabricated in a $0.35\text{ }\mu\text{m}$ process and thinned to form the UTC. Each ISFET pixel provides $576\text{ }\mu\text{m}^2$ ion sensing area and consumes $6.28\text{ }\mu\text{W}$. Experimental measurement of pH in culture media, as well as presented packaging approaches for the SoUTC, demonstrate the potential for use of the approach continuous monitoring of pH in sweat and other biofluids.

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Prof. Kea-Tiong (Samuel) Tang (Incoming Editor-in-Chief), Prof. Timothy Constandinou (Deputy Editor-in-Chief), and the Technical Committee (TC) of Biomedical and Life Science Circuits and Systems, for giving us the opportunity to organize this Special Issue. We also wish to thank the ISCAS 2021 Organising Committee and Technical Program Committee members. We are grateful to IEEE Publishing Operations personnel for their great efforts and patience in finalizing this special issue. We sincerely hope that you enjoy the papers in this special issue and find its contents informative and useful.

DEEPU JOHN, *Guest Editor*
School of Electrical
and Electronics Engineering
University College Dublin
D04V1W8 Dublin, Ireland
deepu.john@ucd.ie

TONY TAE-HYOUNG KIM, *Guest Editor*
School of Electrical
and Electronic Engineering
Nanyang Technological University
50 Nanyang Avenue, Singapore 639798
thkim@ntu.edu.sg

MATTHEW L. JOHNSTON, *Guest Editor*
School of Electrical Engineering
and Computer Science
Oregon State University
Corvallis, OR 97331 USA
matthew.johnston@oregonstate.edu



Deepu John (Senior Member, IEEE) received the B.Tech. degree in electronics and communication engineering from the University of Kerala, Thiruvananthapuram, India, in 2002, and the M.Sc. and Ph.D. degrees in electrical engineering from National University Singapore, Singapore, in 2008 and 2014, respectively. He is currently an Assistant Professor with the School of Electrical and Electronics Engineering, University College Dublin, Dublin, Ireland.

From 2014 to 2017, he was a Postdoctoral Researcher with Bio-Electronics Lab, National University Singapore. Previously, he was a Senior Engineer with Sanyo Semiconductors, Japan. His research interests include low-power biomedical circuit design, energy-efficient signal processing, and edge computing. He was the recipient of the Institution of Engineers Singapore Prestigious Engineering Achievement Award in 2011, Best Design Award at the Asian Solid-State Circuit Conference in 2013, and IEEE Young Professionals, Region 10 Individual Award in 2013. He was a Member of the organizing committee/technical program committee for several IEEE conferences, including TENCON, ASICON, ISCAS, BioCAS, and ICTA. He was the Guest Editor of IEEE

TRANSACTIONS ON CIRCUITS & SYSTEMS-I and IEEE OPEN JOURNAL OF CIRCUITS & SYSTEMS. He is currently an Associate Editor for IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS & SYSTEMS, IEEE TRANSACTIONS ON CIRCUITS & SYSTEMS-II, and WILEY *International Journal of Circuit Theory & Applications*. He is also a Member of BioCAS Technical Committee in the IEEE CAS Society.



Tony Tae-Hyoung Kim (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Korea University, Seoul, South Korea, in 1999 and 2001, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Minnesota, Minneapolis, MN, USA, in 2009. From 2001 to 2005, he was with Samsung Electronics, Hwasung, South Korea, where he performed the research on the design of high speed SRAM memories, clock generators, and IO interface circuits. From 2007 to 2009, he was with IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, and Broadcom Corporation, Edina, MN, USA, where he performed the research on circuit reliability, low-power SRAM, and battery-backed memory design. In 2009, he joined Nanyang Technological University, Singapore, where he is currently an Associate Professor. He has authored or coauthored more than 190 journal articles and conference papers, and holds 17 U.S. and Korean patents registered. His current research interests include computing-in-memory for machine learning, ultra-low power circuits and systems for smart edge computing, low-power and high-performance digital, mixed-mode, and memory circuit design,

variation-tolerant circuits and systems, and emerging memory circuits for neural networks.

Dr. Kim was the recipient of the IEEE ISSCC2019 Student Travel Grant Award, Best Demo Award at APCCAS2016, Low Power Design Contest Award at ISLPED2016, best paper awards at 2014 and 2011 ISOC, AMD/CICC Student Scholarship Award at IEEE CICC2008, Departmental Research Fellowship from the University of Minnesota in 2008, DAC/ISSCC Student Design Contest Award in 2008, Samsung Humantech Thesis Award in 2008, 2001, and 1999, and ETRI Journal Paper of the Year Award in 2005. He was the Chair of the IEEE Solid-State Circuits Society Singapore Chapter in 2015–2016 and is Chair-Elect/Secretary of the IEEE Circuits and Systems Society VSATC. He was on numerous conferences as a Committee Member. He is the Corresponding Guest Editor of IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS), an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE ACCESS, and *IEIE Journal of Semiconductor Technology and Science*.



Matthew L. Johnston (Senior Member, IEEE) received the B.S. degree in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Columbia University, New York, NY, USA, in 2006 and 2012. He was a Co-Founder and the Manager of Research with Helixis, Carlsbad, CA, USA, a Caltechbased spinout developing instrumentation for realtime DNA amplification, from 2007 to its acquisition by Illumina, San Diego, CA, USA, in 2010. From 2012 to 2013, he was a Postdoctoral Scholar with Bioelectronic Systems Lab, Columbia University. In 2014, he joined Oregon State University, Corvallis, OR, USA, where he is currently an Associate Professor with the School of Electrical Engineering and Computer Science. His current research interests include the integration of sensors and transducers with silicon integrated circuits, stretchable circuits and sensor systems, lab-onCMOS platforms, bio-energy harvesting, and low-power distributed sensing.

Dr. Johnston was the recipient of the 2020 Semiconductor Research Corporation (SRC) Young Faculty Award. He is currently an Associate Editor for IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS. He is also on the Biomedical and Life Science Circuits and Systems Technical Committee and Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society.