An 8-Channel Ambulatory EEG Recording IC with In-Channel Fully-Analog Real-Time Motion Artifact Extraction and Removal

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Following an experimental study on electrode-skin interface electrical characteristics for dry electrodes in the absence and presence of motions, the paper presents the channel architecture, its detailed signal transfer function analysis, circuitlevel implementation, and experimental characterization results. Our measurement results show an amplification voltage gain of 48.3dB, a bandwidth of 300Hz, rail-to-rail input DC offset tolerance, and 41.5dB artifact suppression, while consuming 55µW per channel. The system's efficacy in EEG motion artifact suppression is validated experimentally, and system-and circuitlevel features and performance metrics of the presented design are compared with the state of the art.

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Keywords: Electroencephalography (EEG), motion artifact detection, motion artifact removal, electrode-skin interface, mixed-signal architecture, neural recording, wearable EEG, brain-computer interface.

I. Introduction

Thanks to enabling non-invasive accessible means for monitoring brain's neuronal activities at a relatively-high temporal resolution, wearable and flexible ambulatory Electroencephalography (EEG) headsets have gained significant popularity over the past few years [1]–[4]. These devices aim to provide a fast, low-cost, and medically-relevant alternative to the existing clinical setups [5], [6], thus, facilitating long-term outpatient EEG monitoring. To enable quick setup time and comfortable use, rigid/flexible dry (i.e., gel-free) contact or non-contact electrodes are utilized in these devices, which comes at the cost of having a significantly higher and more variable interface impedance due to the less-stable electrode-skin connection. The impedance variations result in fairly-large fluctuations in the signal's magnitude and DC level, commonly known as *motion artifacts* [7], [8]. Since any physical activity of the patient (e.g., talking, chewing, etc.) could cause electrode movements, hence impedance variation, motion artifacts are considered random in nature both in terms of occurrence rate and severity.

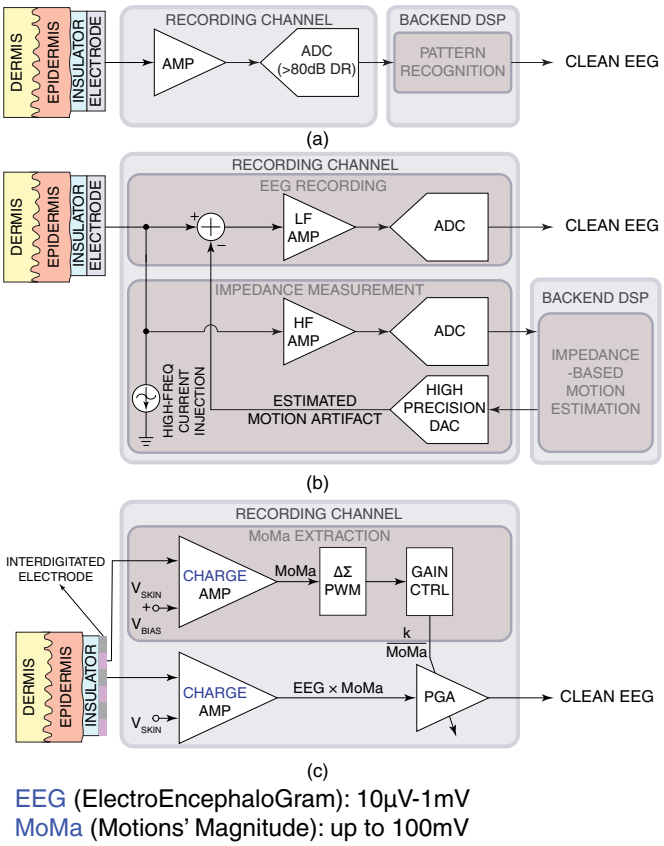

Fig. 1. Simplified block diagram of conventional methods used for motion artifact removal using (a) pattern recognition and (b) impedance-based artifact estimation. (c) Top-level block diagram of the proposed in-channel analog method for motion artifact extraction and removal.

As shown in Fig. 1(a), conventionally, various digital signal processing (DSP) pattern recognition algorithms have been used to extract motion artifacts in recorded bio-signal (e.g., electrocardiography (ECG)) recordings [9]–[11]. However, this approach is not suitable for artifact removal from EEG signals as (a) unlike ECG, EEG signals do not have a specific repetitive pattern, and (b) artifacts ($\sim$100mV) are typically orders of magnitude larger than EEG signals ($\sim$10-100μV), requiring power-hungry high-dynamic-range (i.e., >80dB) recording

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circuits to amplify and quantize the signals without being saturated by the artifacts [12], [13].

Fig. 1(b) shows a popular alternative approach, in which high-frequency (out of EEG band) current pulses are injected to the skin and the resulted voltage is recorded through a parallel path to measure the interface impedance, which is used to estimate the real-time magnitude of motion artifacts. The estimated artifact is then subtracted from the amplifier's input to significantly reduce its dynamic range. To prevent any risk of instability and signal distortion, the overall latency of the feedback loop has to be made strictly small, which comes at the cost of limiting the estimator's complexity, hence its accuracy [5]. Poor artifact estimation leads to subtraction residues that are larger than the actual EEG signal (i.e., signal drown in noise). Therefore, while the amplifier saturation is avoided, the EEG activity is lost. The estimation accuracy also depends on the resolution and speed of the digital-to-analog converter (DAC) that converts the estimated artifact back to the analog domain to be subtracted from the input signal. Typically, power constraints prevent from employing a high-resolution high-speed DAC (e.g., digital signal processing and 12-bits DACs require 54μW for 3-channel ECG recording [5]).

In this work, we first study the electrode-skin interface electrical characteristics for dry non-contact electrodes in the absence and presence of motions through various experimental measurements. Based on the results of this study, we then present a new recording front-end architecture, (Fig. 1(c)) with a dual signal path: an upper path uniquely designed to generate an output voltage that is proportional to the real-time motions' magnitude (MoMa), and a lower path that is a signal amplifier with a gain that is proportional to MoMa. As shown in Fig. 1(c), the proposed architecture also has a second amplification stage with a gain that is set by the upper path's output to be inversely proportional to motions' magnitude (i.e., k/MoMa). The two cascaded amplifiers yield an overall constant gain that is independent of motions magnitude.

The most important advantages of the presented idea are:

1) It is implemented *in-channel*, which is particularly beneficial for EEG recording, where the electrodes are physically distant from each other (compared to intra-cranial EEG (iEEG)) and are typically connected to a central processing unit through long wires. As such, it is preferred to quantize the recorded EEG signals at the electrode site before sending them to the central unit to prevent signal-to-noise ratio (SNR) degradation due to noise/interference. By conducting artifact detection and removal in-channel, the required input dynamic range (DR) for the analog-to-digital converter (ADC) reduces from 80-90dB (i.e., EEG + artifact) to 50-60dB (i.e., cleaned EEG), which significantly reduces power consumption. Additionally, it makes each recording channel a stand-alone unit and needless of a backend processing unit for its operation, hence improves channel count *scalability* and reduces the number of interconnecting wires.

2) The motion artifact extraction and removal are both done in the analog domain, making the proposed method's efficacy independent of the accuracy of ADCs and DACs used for digitizing the interface impedance and converting artifact estimation back into the analog domain, respectively (e.g., as in method shown in Fig. 1(b)).

3) The proposed channel architecture translates artifacts into gain modulations and then removes them by applying the exact inverse gain. This makes the method's efficacy independent of the artifact pattern or severity, unlike the DSP-based methods that use pattern recognition algorithms to detect and remove artifacts.

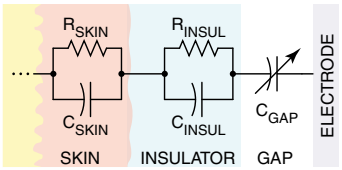

Fig. 2. Electrical model of electrode-skin interface impedance for dry non-contact electrodes.

This paper extends on an earlier report of the principle and demonstration in [15], and offers (a) theoretical and experimental characterizing of the electrode-skin interface, (b) a more detailed analysis of the proposed architecture and its circuit-level implementation, and (c) additional system- and circuit-level experimental measurement results.

The rest of the paper is organized as follows. In Section II, using an experimental statistical approach, we will investigate the effect of various electrode movements on the electrode-skin interface impedance. Section III defines signal-correlated and -uncorrelated artifacts and analytically describes how they appear at the output of charge and voltage amplifiers, which will be the basis of artifact extraction by the proposed recording front-end architecture presented in Section IV. Section V discusses the circuit-level implementation of the full recording channel, which includes circuits for motions extraction and removal, as well as band-pass filtering stages. Section VI presents the electrical and experimental measurement results and compares this work with the state of the art. Section VII concludes the paper.

II. Interface Impedance Characterization

Fig. 2 shows a commonly-used electrical circuit model of the electrode-skin interface (ESI) impedance for dry non-contact electrodes [16]. As shown, the gap between the electrode and the skin is modeled by a capacitance, typically in the range of 1pF-1nF. The values of electrical elements in the ESI model depend on the insulating layer properties, the electrode physical dimensions and material, as well as the amount of pressure applied to the electrode.

We implemented a custom-designed flat dry electrode (circular, diameter: 17mm, insulation thickness: 0.9 mil) to study the effect of various motions on the ESI impedance. Fig. 3(a) shows how well the experimental measurement results for the custom-made electrode's ESI admittance matches the model prediction when R_{SKIN}=1MΩ, C_{SKIN}=10nF, R_{INSL}=1GΩ, C_{INSL}=50pF, and C_{Gap}=1nF. This experiment is conducted while no relative motion is present between the electrode and the skin. Occurrence of motions typically change the values of R_{INSL}, C_{INSL} and C_{Gap}. Considering the magnitude of each element in the model, the overall ESI admittance at the frequency band of interest is dominated by C_{INSL} and C_{Gap} and can be reasonably approximated by a capacitor.

Fig. 3(b) shows how the measured interface capacitance varies in the presence of different random motions. The data is collected by placing the electrode on the skin and measuring interface admittance under various facial gestures that could

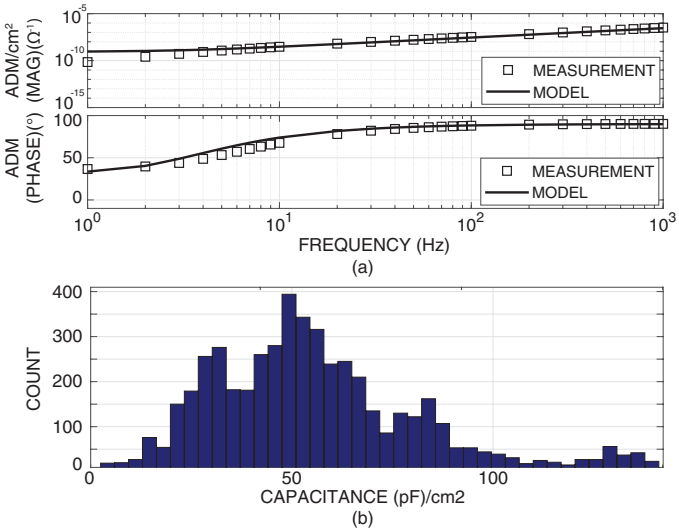

Fig. 3. (a) Experimentally measured admittance/cm^2 magnitude and phase of the electrode-tissue interface for a custom-designed dry non-contact electrode. (b) Experimental results of 10,000 interface capacitance/cm^2 measurements of the non-contact electrode in the presence of various types of motions.

result in motion artifacts. Over the course of the experiment, 10,000 admittance measurements were conducted at 100Hz and the results show an average of 59pF and a standard deviation of 25.4pF for the electrode-skin interface capacitance/cm^2. Based on this experiment, and as expected, increasing the pressure applied to the electrode towards the skin result in increasing the C_{INSL} as well as the total capacitance, and decreasing the pressure results in total capacitance reduction.

III. Uncorrelated and Correlated Motion Artifacts in Voltage and Charge Amplifiers

Considering the capacitive electrode-skin interface described in the previous section, any electrode motion could vary the interface capacitance (C_{ESI}), hence, change the current flowing through it. Compared to a fixed capacitor, the current of a varying capacitor has an extra term (i.e., $V_C\frac{dC}{dt}$) that is proportional to the voltage across the capacitor and the rate of capacitance variation,

$$i_C = C\frac{dV_C}{dt} + V_C\frac{dC}{dt}. \tag{1}$$

To investigate how this would affect the recorded signal, we devised a test setup with two electrodes, in which a sine wave is applied to one of the electrodes that is attached to the skin, and the second electrode is placed at a reasonable distance from the first electrode and is connected to the recording circuit. The second (i.e., recording) electrode is a dry non-contact one and various motions are applied to it during the experiment. The recording was conducted once using a conventional capacitive-feedback voltage amplifier (Fig. 4(a)), and then a charge amplifier (Fig. 4(b)). Fig. 4(c) shows how C_{ESI} variations affect the measured output of the voltage amplifier. The voltage across C_{ESI} is

$$V_{C_{ESI}} = v_{EEG} + V_{skin} - V_{elec}, \tag{2}$$

where v_{EEG} is the EEG signal, V_{elec} is the recording electrode's DC potential, and V_{skin} is the skin's DC potential. This results in the input current to be

$$\begin{aligned} i_{C_{ESI}} &= C_{ESI}\frac{dv_{EEG}}{dt} + C_{ESI}\frac{d(V_{skin}-V_{elec})}{dt} \\ &+ v_{EEG}\frac{dC_{ESI}}{dt} + (V_{skin}-V_{elec})\frac{dC_{ESI}}{dt} = \\ &C_{ESI}\frac{dv_{EEG}}{dt} + v_{EEG}\frac{dC_{ESI}}{dt} + (V_{skin}-V_{elec})\frac{dC_{ESI}}{dt} \end{aligned} \tag{3}$$

Since the amplifier's input is AC coupled, there is no DC path to control V_{elec}. Therefore, its difference with V_{skin} (i.e., $V_{elec}-V_{skin}$) could take a wide range of values (i.e., a few mV to >100mV). As a result, $(V_{elec}-V_{skin})\frac{dC_{ESI}}{dt}$ typically ends up being much larger than $v_{EEG}\frac{dC_{ESI}}{dt}$ and $C_{ESI}\frac{dv_{EEG}}{dt}$. When this large current is integrated on the feedback capacitor C_F, it results in a sizable artifact at the output of the amplifier, as shown in Fig. 4(c). It should be noted that this artifact is of random nature due to the unpredictability of the interface capacitance variations and lack of control on the electrode potential (V_{elec}). Recording μV-level EEG signals in the presence of such large artifacts requires boosting the input DR from 10μV-1mV range to 10μV-200mV (i.e., an increase of ~46dB), which translates into a proportional increase in power consumption. Additionally, even if the high DR is somehow achieved, the unpredictability of the artifacts makes it a highly challenging signal processing task to separate them from the EEG signals. Considering that the interface capacitance variations (i.e., $\frac{dC_{ESI}}{dt}$) are unavoidable in wearable devices, the only alternative for removing these artifacts is to take control of the DC voltage across C_{ESI} (i.e., $V_{C_{ESI}-DC} = V_{skin} - V_{elec}$), and ideally set it to zero.

Fig. 4(b) shows how the voltage amplifier of Fig. 4(a) is turned into a charge amplifier by removing C_{IN} and directly connecting the electrode to the inverting terminal of the OTA, which allows for direct control of V_{elec}. Using this control, $V_{C_{ESI}-DC}$ could be minimized by setting $V_{elec} = V_{skin}$. Even if they are not perfectly equal down to the μV level, the difference could be made small enough to reduce the signal's dynamic range by orders of magnitude and completely remove the above-mentioned risk of amplifier saturation during motion artifacts. Fig. 4(d) shows the measurement results confirming that when the $V_{C_{ESI}-DC}$ is set to zero, the $V\frac{dC}{dt}$ term reduces to $v_{EEG}\times\frac{dC_{ESI}}{dt}$, hence the input current will be $v_{EEG}\times\frac{dC_{ESI}}{dt} + C_{ESI}\times\frac{dv_{EEG}}{dt}$, which gets integrated on the feedback capacitor and generates a $v_{out} = \frac{C_{ESI}}{C_F}\times v_{EEG}$. This results in a voltage gain (C_{ESI}/C_F) that is linearly proportional to the value of the varying C_{ESI}. Therefore, C_{ESI} variations caused by random motions translate into linear modulation of the output signal's amplitude, which we call motion-modulated EEG (MM-EEG). This is a great improvement compared to the previous situation (Fig. 4(c)), in which motions resulted in large random-shaped artifacts on the output signal.

The above discussion suggests that if we have knowledge of the real-time value of motions magnitude (MoMa), we could use that to demodulate the MM-EEG and achieve clean EEG signals at the output. The theoretical analysis and circuit implementation of this idea, which is the core of our proposed architecture, are presented in the next sections.

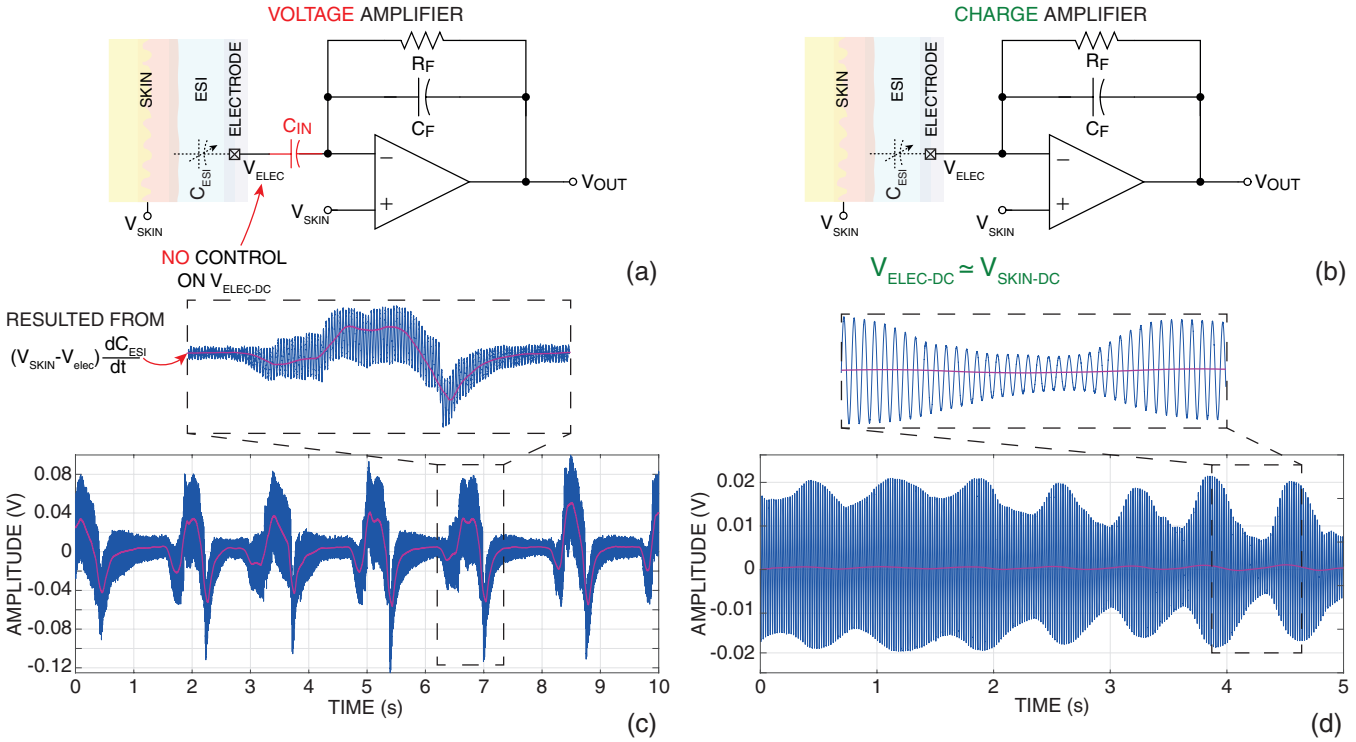

Fig. 4. Simplified schematics of (a) an AC-coupled capacitive-feedback voltage amplifier, and (b) a charge amplifier. The impact of electrode movements on their output signal shown in (c) and (d), respectively.

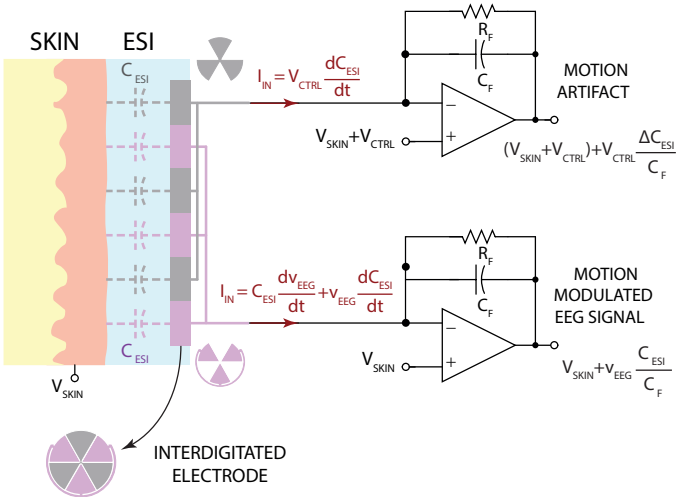

Fig. 5. Dual-path parallel recording architecture with two outputs: motion-modulated EEG signal (lower path), and interface capacitance variations (upper path).

IV. Dual-Path Analog Front-End for Motion Artifact Extraction

As discussed in Section I, the proposed recording front-end architecture has two parallel paths. As such, a custom-designed interdigitated electrode (similar to what we have previously reported in [4]) is employed. The symmetry and inter-digitation of this particular electrode design ensures perfect matching of the electrode-skin interface (e.g., C_{ESI}) characteristics for the two paths. We will show experimental results proving this matching later in this paper. As shown in Fig. 5, the two sections of the electrode are connected to two identical charge amplifiers, each similar to the circuit discussed in Fig. 4(b). The only difference between the two paths is that the voltage at the OTA's non-inverting input is set to V_{SKIN} for the lower path (LP), and $V_{SKIN} + V_{CTRL}$ for the upper path (UP). This results in $V_{C_{ESI}-DC} = 0$ for the lower path, and $V_{C_{ESI}-DC} = V_{CTRL}$ for the upper path. Considering that the ac part of the $V_{C_{ESI}}$ for both paths is the EEG signal (v_{EEG}), using (1), the input current through the C_{ESI} can be written as

$$I_{IN} = \begin{cases} C_{ESI}\frac{dv_{EEG}}{dt} + v_{EEG}\frac{dC_{ESI}}{dt} + V_{CTRL}\frac{dC_{ESI}}{dt} & \text{(UP)}, \\ C_{ESI}\frac{dv_{EEG}}{dt} + v_{EEG}\frac{dC_{ESI}}{dt} & \text{(LP)}. \end{cases} \quad (4)$$

The integration of I_{IN} on the feedback capacitance defines the output voltage of the two paths. Given that the amplitude of the EEG signal is lower than 1mV, by setting the V_{CTRL} to be much larger than the maximum magnitude of the v_{EEG} (e.g., >50mV), the integration of the first and the second terms of the UP's I_{IN} (i.e., $\int C_{ESI}\frac{dv_{EEG}}{dt} + v_{EEG}\frac{dC_{ESI}}{dt} = v_{EEG} \times C_{ESI}$) will be negligible compared to the integration of the third term (i.e., $\int V_{CTRL}\frac{dC_{ESI}}{dt} = V_{CTRL} \times C_{ESI}$). Therefore, the output voltages of the two paths can be written as,

$$V_{OUT} \approx \begin{cases} (V_{SKIN} + V_{CTRL}) + V_{CTRL}\frac{\Delta C_{ESI}}{C_F} & \text{(UP)} \\ V_{SKIN} + v_{EEG}\frac{C_{ESI}}{C_F} & \text{(LP)} \end{cases} \quad (5)$$

Ignoring V_{SKIN} (a DC term that will be removed in the a subsequent amplification), LP's output is the MM-EEG

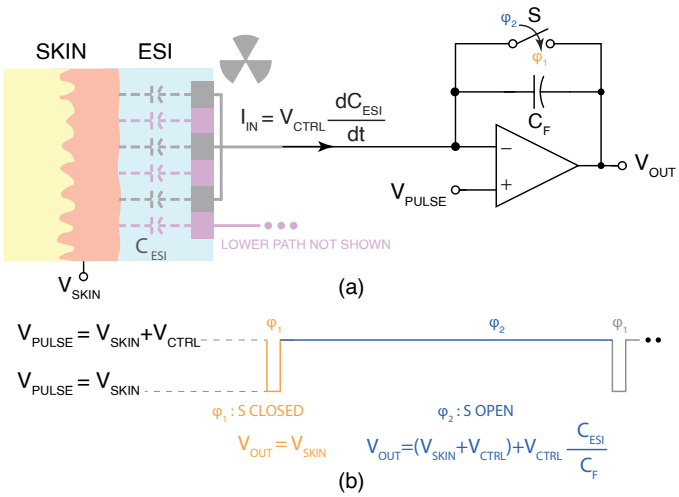

Fig. 6. (a) Modified upper path's charge amplifier to generate C_{ESI} instead of ΔC_{ESI} at the output, and (b) its timing and output signal during the two operating phases.

described in the previous section, in which the v_{EEG} is amplified by a factor of $1/C_F$ and modulated by the variable C_{ESI}. Ideally, if we can extract the real-time value of C_{ESI} from the UP's output, then the LP's output could be multiplied by k/C_{ESI} to achieve a clean EEG (k being a constant). However, the UP's output has ΔC_{ESI} term instead of C_{ESI}.

Fig. 6(a) shows a modified version of UP circuit, in which the feedback resistor is replaced with a switch, which results in C_{ESI} (instead of ΔC_{ESI}) to appear at the UP's output. As shown in Fig. 6(b), during ϕ_1, the non-inverting input of the OTA is set to V_{SKIN} and the switch S_1 is closed to make the inverting input also equal to V_{SKIN}. During ϕ_2, S_1 is opened, and the non-inverting input terminal is raised to $V_{CTRL} + V_{SKIN}$. Therefore, a charge of $V_{CTRL}\frac{C_{ESI}}{C_F}$ is transferred to the feedback capacitor, resulting in

$$V_{OUT} = V_{CTRL} + V_{SKIN} + V_{CTRL}\frac{C_{ESI}}{C_F}, \tag{6}$$

where V_{CTRL} and V_{SKIN} are known DC voltages (hence, can be removed in a subsequent stage, as described in the next section) and the third term is proportional to the absolute value of C_{ESI}. Having C_{ESI} extracted, we can now compensate for the motion artifacts in real time by cascading a 2^{nd}-stage amplifier to the first stage's LP, and setting its gain proportional to $1/C_{ESI}$ to render a C_{ESI}-independent overall gain.

V. In-Channel Motion Artifact Removal

Fig. 7(a) shows the top-level block diagram of the proposed front-end architecture and how the outputs of the first stage's two paths (LP and UP) are connected to the second stage of amplification. As shown, the LP's output (i.e., the MM-EEG = EEG×MoMa) is fed to a programmable gain amplifier (PGA) whose gain is controlled by the UP's output through a ΔΣ-PWM block.

Fig. 7(b) shows the detailed implementation of the ΔΣ-PWM block. It generates pulses with a duty cycle proportional to the amplitude of the first stage's UP output. As shown, the sum of the input current I_{R1} and the feedback current I_{R2} is integrated on the feedback capacitor. The polarity of the resulting voltage decides the output of the comparator in the next clock cycle. I_{R2} itself is set based on the comparator's decision on the previous input sample (i.e., $\frac{V_{P1}-V_{set}}{R_2}$ for D=1 and $\frac{V_{P2}-V_{set}}{R_2}$ for D=0). As the comparator output is reset in each clock period, a D-type flip flop (DFF) is used after the comparator to prevent the propagation of this reset event to the next stage. The DFF clock is delayed by 100ns with respect to the comparator clock (10% of the clock cycle), which allows enough time for the comparator to make a decision.

The ΔΣ structure and the OTA feedback force the inverting input terminal and the output voltages of the OTA to be held at V_{set}. The 1-bit DAC is implemented with an NMOS ($\frac{20\times250n}{250n}$) and a PMOS ($\frac{30\times250n}{250n}$) that are connected to V_{P1} and V_{P2}, respectively. V_{P1} and V_{P2} are set to the minimum and maximum voltages of the first stage's UP output. Therefore, when PWM output (D) is zero, the DAC's output is V_{P2} and when PWM output is VDD, the DAC's output is V_{P1}. Nodal analysis at the inverting input of the OTA where $R_1 = R_2$, results in (7) that shows the relationship between the duty cycle of PWM output (D) and its input voltage.

$$\begin{aligned} DV_{P1} + (1-D)V_{P2} + MoMa &= 2V_{set} \\ D &= \frac{MoMa + V_{P2} - 2V_{set}}{V_{P2} - V_{P1}} \end{aligned} \tag{7}$$

As it was shown in the previous section, the first stage's UP output has a term that is proportional to C_{ESI} (i.e., $V_{CTRL}\frac{C_{ESI}}{C_F}$), as well as unwanted DC terms (i.e., $V_{CTRL} + V_{SKIN}$). To remove the DC terms, V_{set} is chosen in a way that $2V_{set} - V_{P2}$ is equal to $V_{CTRL} + V_{SKIN}$. Replacing these two terms in (7), the duty cycle will be

$$D = \frac{V_{CTRL}}{V_{P2} - V_{P1}} \times \frac{C_{ESI}}{C_F} = \alpha \times \frac{C_{ESI}}{C_F}. \tag{8}$$

where α is constant, thus D is linearly proportional to C_{ESI}. We used this PWM signal to set the gain of the PGA proportional to $1/C_{ESI}$, thus removing C_{ESI} from the overall gain.

As shown in Fig. 7(c), the PGA's feedback path is formed by a resistor in series with a switch S_2. The two form a cycled resistor with an equivalent resistance of R/D, where D is the duty cycle of the control pulse of the switch [17]. Therefore, by using the PWM signal to control the cycled resistor's switch, the PGA's gain will be

$$Gain_{PGA} = \frac{R_{F_{PGA}}}{D \times R_{in}} = \frac{R_{F_{PGA}}.C_F}{\alpha.R_{in}.C_{ESI}}. \tag{9}$$

Multiplying this by the first stage's LP gain (as they are cascaded) results in an overall channel gain that is independent of C_{ESI}, hence, remains constant during motions,

$$Gain_{overall} = \frac{R_{F_{PGA}}.C_F}{\alpha.R_{in}.C_{ESI}} \times \frac{C_{ESI}}{C_F} = \frac{R_{F_{PGA}}}{\alpha.R_{in}}. \tag{10}$$

To filter the high-frequency switching noise of the cycled-resistor, a feedback capacitor ($C_{F_{PGA}}$) is placed in parallel with the switched resistor. The upper cut-off frequency of this structure is equal to $\frac{D}{2\pi R_{F_{PGA}} C_{F_{PGA}}}$. Accordingly, the $C_{F_{PGA}}$ is chosen in a way that for any reasonable D (i.e., $D > 0.01$), the cut-off frequency of the PGA is greater than the EEG bandwidth in order to prevent any unintended attenuation of the EEG signal. Fig. 7(d) shows the circuit schematic of the employed wide-swing folded cascode OpAmp in the PGA

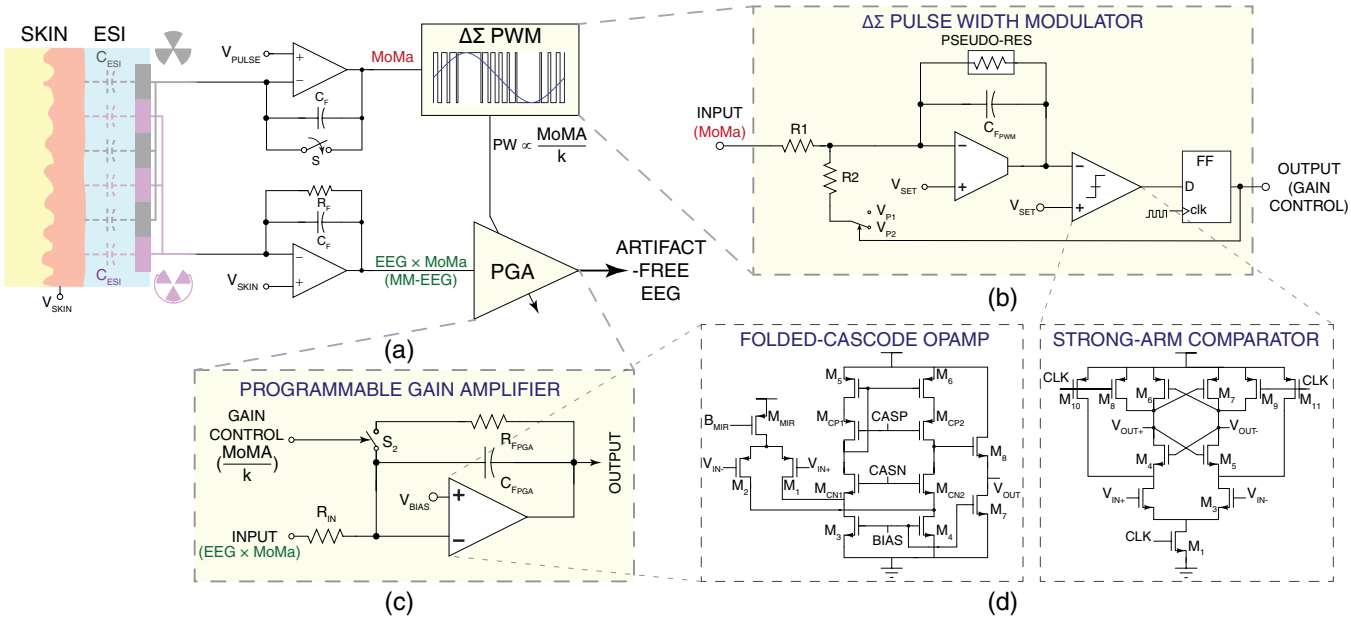

Fig. 7. (a) Top-level block diagram of the proposed recording front-end. Circuit schematic of the (b) ΔΣ-PWM, (c) the PGA, and (d) the opamp and comparator blocks used in the proposed design.

block and the strong-arm comparator used in the PWM block.

Fig. 8(a) shows the top-level block diagram of the presented IC, which includes 8 EEG-recording and one reference channels. As shown, the two-stage front-end circuit described in previous sections is followed by a fully-differential two-stage bandpass filter that is employed in each channel to further suppress the high-frequency switching noise generated by the PGA's feedback path. The output of the PGA from the reference channel is fed to this filter in each recording channel. Fig. 8(b) shows the detailed schematic of the two-stage filter. The figure also depicts the circuit schematic of the employed differential folded cascode OTA and its common-mode feedback (CMFB) circuit, both used in the bandpass filter.

VI. Experimental Measurement Result

The described 8-channel EEG recording IC was designed and fabricated in a 130nm standard CMOS technology. The micrograph of the $3\times4\text{mm}^2$ integrated circuit is shown in Fig. 9. Each recording channel is highlighted and the channel dimensions are annotated.

The presented channel's experimental measurement results show a gain of 48.3dB (3dB bandwidth:300Hz) and input-referred noise power spectral density of $187\text{nV}/\sqrt{Hz}$ (measured at 100Hz), which is in the same order as the noise generated by the non-contact electrode-tissue interface [16]. Fig. 10 shows the measured capacitance from the motion artifact extraction path (i.e., first stage's UP) plotted versus the capacitance calculated based on the gain variations in the EEG recording path (i.e., first stage's LP). The high correlation between the interface capacitances measured at the output of the two paths attest to the expected matching between them due to the symmetry of the custom-designed inter-digitated electrode.

Fig. 11 shows the experimental measurement results validating the efficacy of the PWM and PGA blocks in conducting artifact removal. For this test, a motion-affected signal (a 300Hz sine wave modulated with a 20Hz signal) is fed to the PGA, and its gain is controlled by the output of the ΔΣ-PWM block. By demodulating the input signal, the PGA extracts the clean sinusoidal signal from the mix. The linearity of the PWM block (i.e., the ratio of the pulse width to the input voltage) is of crucial importance in ensuring the efficacy of the motion artifact removal. Indeed, achieving excellent linearity is the main reason that a ΔΣ-based structure was employed for the PWM instead of the more conventional varactor-based designs.

Fig. 12 shows the experimentally measured power spectral density of motion-contaminated and cleaned signals, confirming the efficacy of the PWM-controlled PGA in removing the extra tones due to motion artifacts without causing almost any spectral leakage or spurs, confirming the excellent linearity. The FFT plot of the motion-affected signal has a tone at 300 Hz, which represents the signal of interest, and two extra tones at 280 Hz and 320 Hz, which are $f_{Input} \pm f_{Motion}$. The output FFT illustrates that the two extra tones are attenuated by >41.5dB, effectively eliminating the motion artifacts.

To further test the performance of the ΔΣ-PWM experimentally, it was fed with an arbitrary input voltage with a range of ±50mV (i.e., the full scale range of MoMa (UP's output)) and its output was used to control the PGA's gain. As presented in Fig. 13, our measurement results show that through controlling the PGA's gain, the ΔΣ-PWM block can remove an arbitrary motion signal added to the input EEG with less than 1% error.

One of the known drawbacks of using dry electrodes with large ESI impedance is the common-mode rejection ratio (CMRR) degradation due to the considerable mismatch between the input capacitances of different channels. As shown in Fig. 14, in order to improve the CMRR, a feedback loop, similar to the driven right leg (DRL) loop used in ECG recording, is employed. In this circuit, output voltages of all channels are averaged using a passive structure, and the average is amplified and fed back to the body through an additional electrode. As illustrated in Fig. 15, our measurement results show that

TABLE I. Comparison to the state of the art

	[18]	[5]	[19]	[20]	[21]	This work
Technology	N/R	0.18μm	0.18μm	0.18μm	40nm	0.13μm
Application	EEG/ECG	ECG	ExG	ECG	ECG	EEG
Supply (V)	3.3	1.8	1.8	5	1.2	1.2
Power/Ch (W)	600μ	80μ	105μ	155μ	7.3μ	55μ
Voltage Gain	1000	75-300	140,700,1200	1,2.8,4.5,10	7.7	260
Programmable	No	Yes	Yes	Yes	No	Yes
Z_{IN} (Ω) @50Hz	N/R	1G	100M	5G	1G	Charge Amp
Bandwidth (Hz)	<100	<200	<300	<100	<200	<300
Offset Tolerance (mV)	R-to-R	R-to-R	$\pm$350	R-to-R	R-to-R	R-to-R
Motion Artifact Detection	No N/A	Yes Current injection	Yes Current injection	No -	No -	Yes Parallel recording
Motion Artifact Removal	No -	Yes Off-Chip	No -	No -	No -	Yes On-Chip
Impedance Measurement Frequency	N/A	1KHz	1KHz	N/A	N/A	Same as EEG signals

N/R: Not reported, N/A: Not Applicable

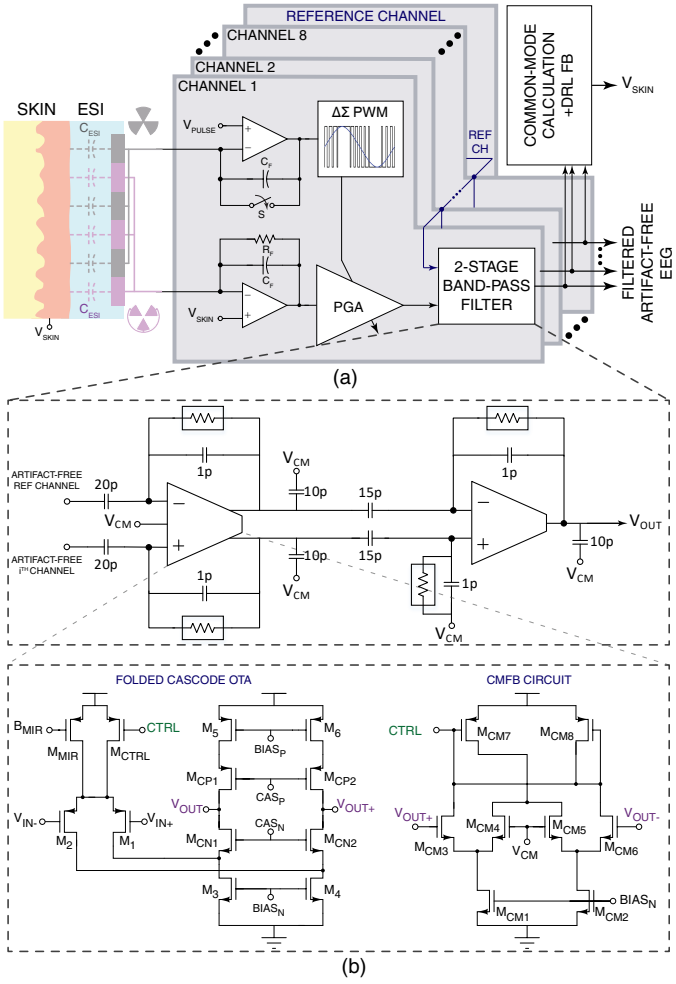

Fig. 8. (a) Top-level block diagram of the presented 8-channel EEG recording IC, showing the full circuit schematic of the proposed channel architecture and its connection to the reference channel. (b) Circuit schematic of the employed two-stage bandpass filter and the input-stage OTA used in its implementation.

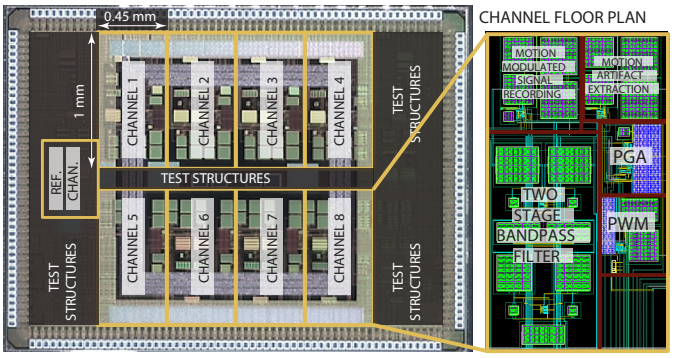

Fig. 9. The chip micro-graph and the layout floorplan of one of the recording channels.

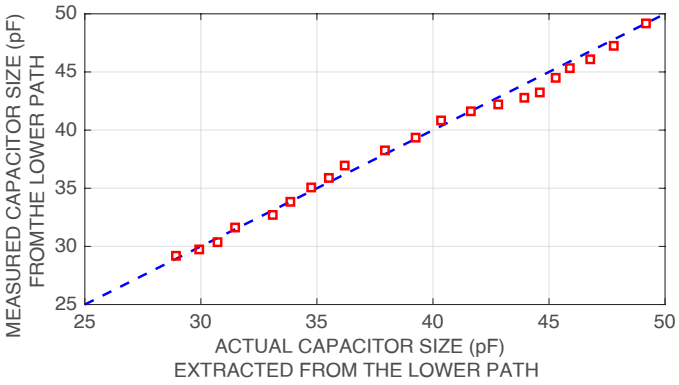

Fig. 10. Measurement result validating excellent matching between the extracted C_{ESI} from the front-end's UP and the actual capacitance measured from the front-end's LP. The results confirm the efficacy of the proposed circuit in precise extraction of C_{ESI} as well as the almost perfect matching of the two sections of the custom-designed inter-digitated electrode.

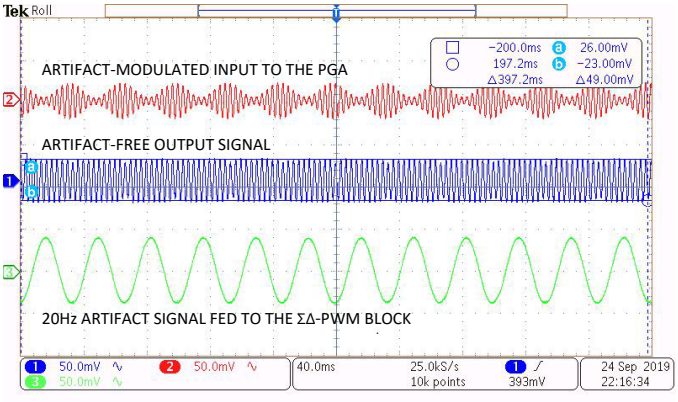

Fig. 11. Measurement results showing the efficacy of the presented ΔΣ-PWM and the PGA blocks in separating the signals and artifacts at arbitrary frequencies through automatic gain control.

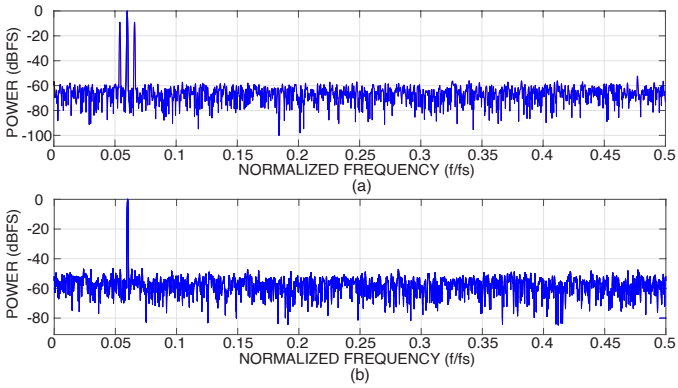

Fig. 12. Measured power spectral density of (a) the motion-modulated EEG and (b) the cleaned EEG, confirming the linearity and efficacy of the PWM+PGA in artifact removal.

activating the DRL loop attenuates the powerline noise by >36dB.

Additionally, the described adaptive PWM-based gain control, which was primarily designed to remove motion artifacts, is leveraged to further enhance the CMRR. Fig. 16 shows the measured CMRR of two channels with and without dynamic gain control. In this experiment, the input capacitance of the two paths of the recording front-end (UP and LP) are set to 10pF for channel1 and 11pF for channel2 (i.e., an intentional 10% mismatch). An 11.33dB (at 60Hz) CMRR improvement is measured when the PWM-based dynamic gain control in the artifact removal block is utilized to improve common-mode rejection.

The effect of DC offset between the ideal value set by the DRL loop and the actual skin potential (i.e., $V_{elec} - V_{skin}$) is evaluated by monitoring the magnitude of motion artifacts on the recorded signal when there is a 100mV, 10mV, 1mV or zero DC voltage difference across the electrode-tissue interface capacitance (C_{ESI}). We conducted surface EEG recording experiments under various electrode motions when different values for $V_{elec}-V_{skin}$ were applied. We expected the recorded signals to contain three components: (i) pure EEG signals, (ii)

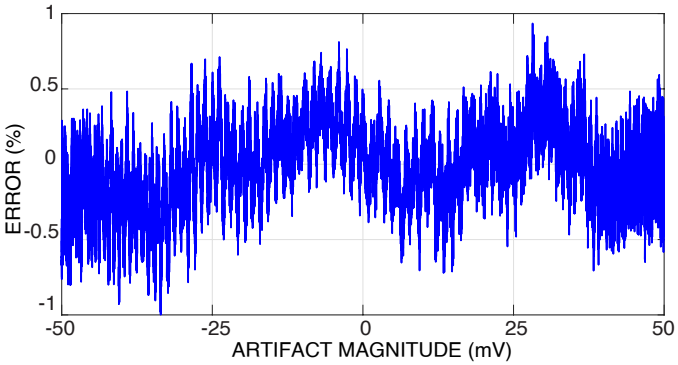

Fig. 13. Measured error in removing artifacts with varying arbitrary magnitude (full-scale range) using the combination of the ΔΣ PWM and PGA.

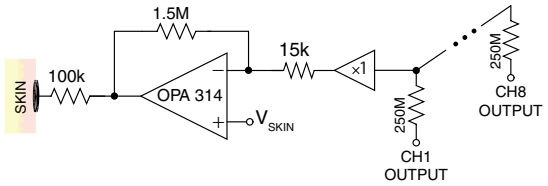

Fig. 14. Schematic of the circuit used for DRL loop to the body for CMRR enhancement.

EEG-correlated artifacts in the form of linear gain modulations (similar to artifacts shown in Fig. 4(d)) and (iii) EEG-uncorrelated artifacts due to the intentional DC bias difference between the electrode and the skin (similar to artifacts shown in Fig. 4(c)). Next, the effect of the EEG-correlated artifacts were removed using the strategy presented in Section V. As a result, the remaining artifacts on the signal are of the EEG-uncorrelated type, which are associated with the magnitude of $V_{elec} - V_{skin}$, as was discussed in Section III. The resulted signal is plotted in Fig. 17, illustrating the impact of different DC offset magnitudes on the quality of EEG recording. As shown in this Figure, for large DC voltage differences, the C_{ESI} variations cause large EEG-uncorrelated artifacts on the recorded signal, which makes EEG signal recovery practically impossible. However, with the proper skin biasing through the DRL loop, this DC difference is made sufficiently small (i.e., <1mV), resulting in *uncorrelated* artifacts that are small enough not to affect the efficacy of the presented architecture for *correlated* motion artifact removal, or the required DR for the recording circuit.

We also used pre-recorded EEG signals (CHB MIT Scalp EEG Database [22]) and randomly contaminated them with motion artifacts extracted from our experimental measurements before feeding them to the presented circuit. Comparing the recorded signals without (Fig. 18(a)) and with (Fig. 18(b)) the motion artifact removal activated, it is evident that the artifacts are suppressed significantly using the presented architecture. It should be noted that since the recording is performed with the presented architecture and with V_{skin} set exactly equal to V_{elec}, all EEG-uncorrelated artifacts are blocked by the front-end and the artifacts appearing in Fig. 18(a) are in the form of gain modulation, which are detected and removed by the circuit, once the artifact removal is activated as shown in Fig. 18(b).

Table I compares this work with the state of the art wearable

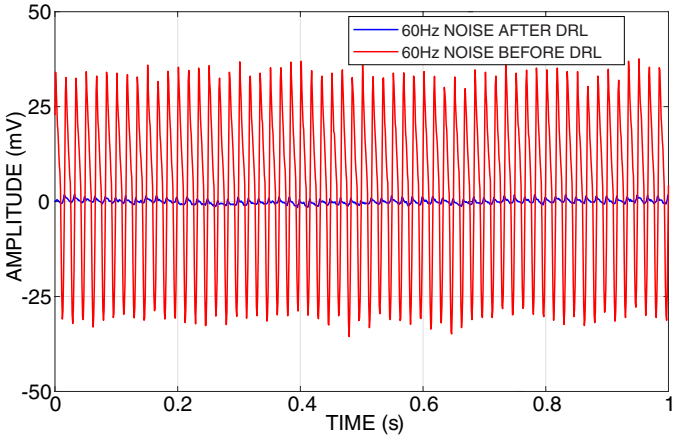

Fig. 15. Measurement result showing the 60Hz noise attenuation before and after using the presented CMRR enhancement loop.

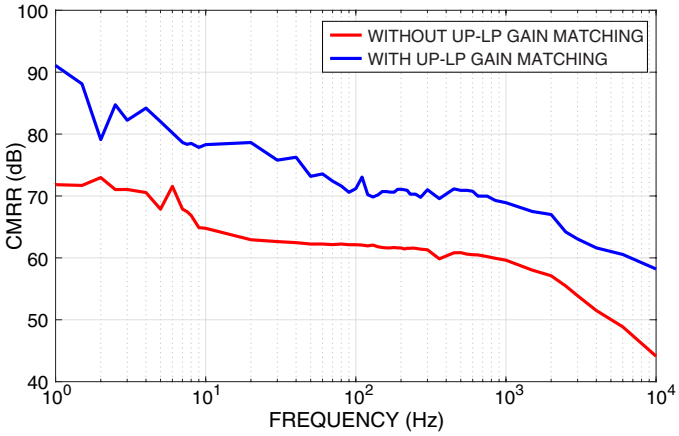

Fig. 16. Measurement results showing CMRR enhancement achieved by the presented dynamic gain control.
Note: Neither of the two curves represent the nominal CMRR of the presented design because an intentional 10% mismatch between the capacitances of the interdigitated electrode is applied for this experiment.

bio-signal recording microsystems in terms of system-level and circuit-level performance and features. The presented work is the only design that offers both detection and removal of motion artifacts *in-channel* and *on-chip*. In addition, the in-channel ADC-free implementation makes the design needless of a central backend signal processing unit, hence further relaxes the overall system complexity and improves its channel-count scalability. Moreover, since the proposed method for artifact detection is needless of a current injection at an out-of-band frequency (typically, 1kHz [5], [8]), it yields a higher accuracy in extracting the real-time interface impedance, and consumes the lowest power per channel among works that feature artifact extraction.

VII. Conclusion

In this paper, we first experimentally characterized the electrode-tissue interface impedance variations of dry EEG electrodes in the presence of random physical movements.

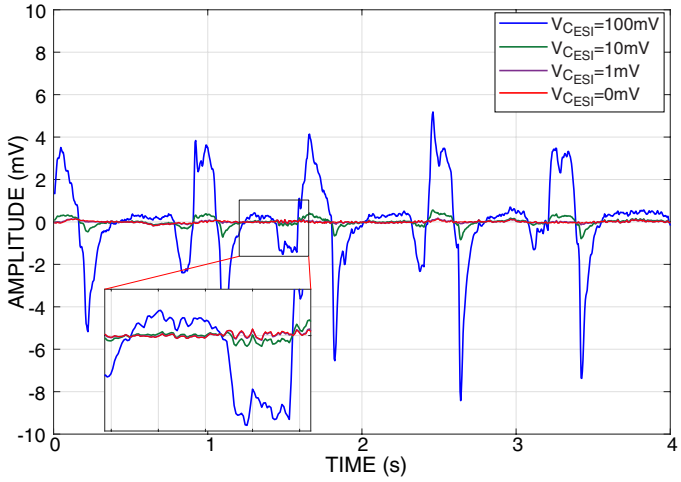

Fig. 17. Measurement results showing the impact of the magnitude of the DC voltage across C_{ESI} on the severity of uncorrelated artifacts that appear on the recorded EEG.

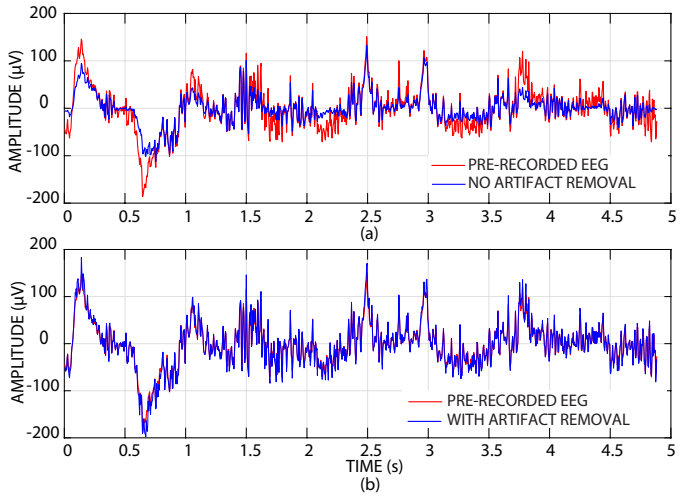

Fig. 18. Experimental evaluation of the presented architecture's efficacy in motion artifact removal using motion-contaminated pre-recorded EEG signals: (a) The artifact removal is off: motion artifacts appear frequently and cause large nonlinear time-varying changes in the recording voltage gain. (b) The artifact removal is on: gain variations are almost completely compensated by the proposed circuit and no significant distortion is observed.

The characterization results were used to explain how motion artifacts are manifested in the EEG recording when conventional analog front-end architectures are used. Based on the acquired knowledge, we proposed, analyzed, developed, and experimentally tested an analog dual-path feed-forward architecture for EEG recording and simultaneous in-channel motion artifact extraction and removal. Compared to the state-of-the-art, the proposed front-end is needless of any digital signal processing and any tissue current injection for interface impedance estimation. This has resulted in improving energy efficiency, size, and complexity of the solution by avoiding power hungry high-DR data converters and auxiliary current stimulators, as well as minimizing the number of connections between electrodes and central processing unit. A 12mm^2

IC was fabricated in a 130nm CMOS technology, integrating 8 channels of the presented architecture for EEG recording. The design analysis and the VLSI circuit implementation are described in details and system- and circuit-level experimental characterization results are reported. The presented measurement results confirm a voltage gain of 48.3dB, a bandwidth of up to 300Hz, rail-to-rail input DC offset tolerance, and 41.5dB artifact suppression while consuming 55μW per channel.

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