A Highly Integrated Lab-on-a-CMOS Platform for Real-Time Monitoring of E. Coli Growth Kinetics

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Abstract—Existing miniaturized and cost-effective solutions for bacterial growth monitoring usually require offline incubators with constant temperature to culture the bio-samples prior to measurement. Such a separated sample preparation and detection scheme requires extensive human intervention, risks contamination, and suffers from poor temporal resolution. To achieve integrated sample preparation and real-time bacterial growth monitoring, this paper presents a lab-on-a-CMOS plat-form incorporates an optical sensor array, temperature sensor array, micro-heaters, and readout circuits. Escherichia coli's (E. coli) optimum growth temperature of 37 °C is achieved through a heat regulation system consisting of two micro-heaters and an on-chip temperature sensor array. A photodiode array with an in-pixel capacitive trans-impedance amplifier to reduce inter-pixel cross-coupling is designed to extract the optical information during bacterial growth. To balance the footprint, power consumption, and quantization speed, a 10bit column successive-approximation register (SAR)/single-slope (SS) dual-mode analog-to-digital converter (ADC) is designed to digitize the temperature and optical signals. Fabricated in a standard 0.18 um CMOS process, the proposed platform can regulate the sample temperature to 37 +/- 0.2/0.3 °C within 32 mins. Enabled by an on-chip heat regulation system and photodetectors, the prototype demonstrates a real-time monitoring of bacterial growth kinetics and antibiotic responses. Minute-level temporal resolution is achieved as this proposed platform is free of extensive and time-consuming human intervention. The proposed platform can be viably used in contamination sensitive applications such as antibiotic tests, stem cell cultures, and organ-on-chips.

Index Terms—ADC, CMOS sensor array, E. coli, heating regulation, lab-on-a-CMOS, micro-heater, optical sensing.

I. INTRODUCTION

Bacterial is one of the first life forms to appear on earth and is ubiquitous in daily life. Although most bacteria in the human body and around the human living environment are harmless, several species of bacteria are pathogenic. They lead to infectious diseases, some of which are fatal. The emergence of bacterial infection and increased incidence of antimicrobial resistance due to the widespread use of antibiotics in medicine, intensive animal industry, etc. [1], [2], pose severe public health threats worldwide. One of the common diseases caused by bacterial, viral, and parasitic organisms is diarrhea. It has been identified by the World Health Organization (WHO)

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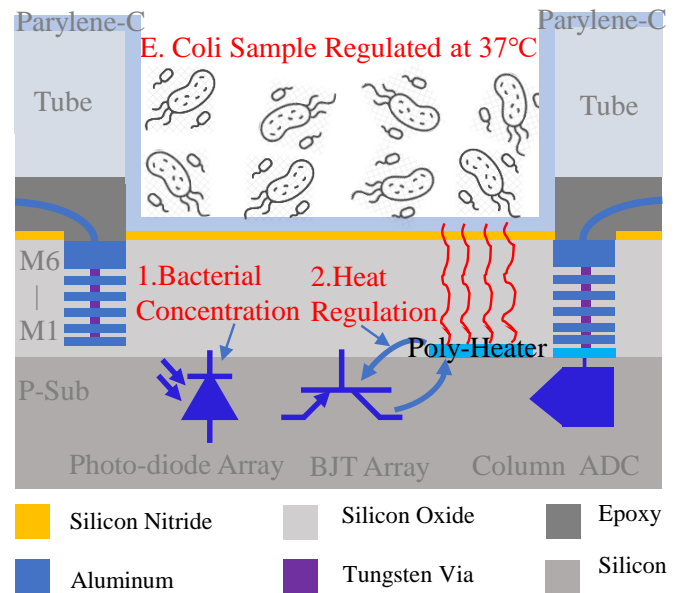

Fig. 1: A lab-on-a-CMOS platform for real-time monitoring of bacterial growth.

as the second leading cause of death in children under five years old, and there are nearly 1.7 billion cases of childhood diarrhoeal disease yearly [3]. To improve human's life quality, various solutions were employed to counter the challenges caused by harmful bacteria, including medicine, healthcare, antibiotic susceptibility tests (ASTs), environmental monitor-ing, food screening, etc [4]–[8]. Most of the studies and applications related to microbes need to explore their growth characteristics, including their nutritional and energetic physi-ology, survival, and proliferation under different conditions. Therefore, probing the growth process of microbes is an essential step and of great significance [9]. For example, in medicine and pharmaceuticals, monitoring microbe growth is crucial for researching and developing of antibiotics, antivirals, and vaccines. Understanding microbial growth patterns helps in determining the appropriate treatment strategies. While in the food industry, monitoring microbial growth is critical to ensure food products are safe for consumption. Contamination by harmful bacteria, such as Salmonella or E. coli, can cause foodborne illnesses.

To date, various methods have been proposed to assess the cell growth characteristics. These methods can be categorized into offline and online, with a noticeable trend shifting from

offline to online approaches. One of the reasons is offline methods require extensive manual intervention, stimulating the occurrences and rapid developments of various online techniques to observe the characteristics of microbial growth [10]. Among them, CMOS-based techniques have drawn significant attention due to their compatibility with the advanced semiconductor industry. This feature allows for miniaturization, reducing reagent and sample volume and enabling mass manufacturing at low cost. Particularly, CMOS-based techniques have been pursued as they could be integrated with other sensors, actuators, and on-chip electronics, providing comprehensive sensing and actuating capabilities for bio-applications that increasingly demand integrated analysis.

Nowadays, CMOS ion-sensitive-field-effect-transistor (IS-FET) [11]–[15], capacitive and impedance sensors [16]–[18] have been widely used in various bio-sensing applications, including the monitoring of bacterial kinetics. Recently, optical-based methods, specifically characterizing the amount of scattered or absorbed light by bacteria and correlating directly with bacterial population sizes, also show a great potential to advance the other online and automated methods for microbial growth monitoring [15], [19]–[21].

Nonetheless, existing works mainly focus either on detection while paying less attention to the preparation of testing samples or solely on cell incubation. Separated sample preparation and detection cause several challenges for accurate cell monitoring. First, it is prone to contamination and also suffers from limited temporal resolution due to constant manual operation. Moreover, constant perturbation of incubation environments and growth could lead to inaccurate results, especially for monitoring anaerobic microbes. One challenge to achieving an online and integrated cell analysis platform is the integration of cell detection and culturing. Temperature is one of the most stressful factors that demands careful attention and maintenance. By providing the optimum temperature, bacterial growth can be promoted, enabling faster reproduction and larger populations [22]. Meanwhile, a stable temperature environment minimizes temperature dependence of bacteria growth as well as on-chip instrumentation. However, this temperature requirement by sensing target is overlooked by most existing works that perform the experiment without temperature regulation [17], [20]. Some methods involve culturing the sample in an incubation chamber to handle the temperature impact. Nevertheless, these systems require manual pipetting of the sample periodically for subsequent cell testing [13]–[15]. Simply placing the whole testing setup in the temperature chamber avoids these potential negative impacts but results in a limited application scenario due to the requirement of a bulky temperature chamber [21]. To decrease the temperature impact, reduce the manual intervention to a minimum, achieve higher temporal sensing resolution, and lower the contamination risk, it is essential to design an integrated cell incubation and detection platform with well-regulated temperature (e. g., 37 °C for Escherichia coli (E. coli)) for bacteria growth. Moreover, on-chip readout electronics is also very necessary to be integrated to reduce the cost, power consumption, size, etc., towards portable bio-sensing systems [23].

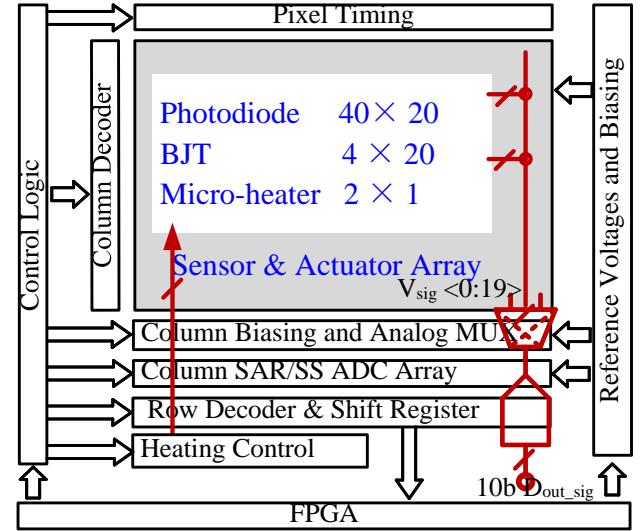The major contribution made by this work to push the

Fig. 2: Block diagram of the proposed LoC platform.

research boundaries of the present cell monitoring is proposing a highly integrated Lab-on-a-CMOS (LoC) platform to probe the feasibility of integrated sample preparation and real-time bacterial monitoring under the required temperature environment. Although there have been reported thermal regulation systems for various applications, such as DNA polymer chain reaction (PCR) and cell culturing [24]–[27], to the best of our knowledge, this is the first attempt to combine optical sensor, temperature regulation, and on-chip readout electronics, providing an integrated analysis on a highly integrated CMOS chip for real-time bacterial growth monitoring and its response to antibiotics. The proposed LoC, an extension of [28], as shown in Fig.1, uses CMOS photodiodes to detect optical signal correlating with bacterial concentration. The LoC also integrates micro-heaters, temperature sensors, and additional electronics to regulate the on-chip sensing targets to the desired temperature. A tube coated with parylene-c is mounted and glued above the packaged chip for sample culturing. Following brief introduction and simulation results of this work in the conference paper [28], this paper presents detailed circuit implementation, characterization results of individual sensor nodes, analog-to-digital converter (ADC), temperature regulation, and on-chip biologic test, as well as discussions of the proposed LoC platform.

The remainder of this paper is organized as follows. Section II introduces the system architecture of the proposed LoC platform, circuit implementation, and system operation. The characterization results of the fabricated CMOS chip and discussions are illustrated in Section III. Section IV presents on-chip bacterial culturing and detection to demonstrate the proposed functionalities, followed by conclusions of this work in Section V.
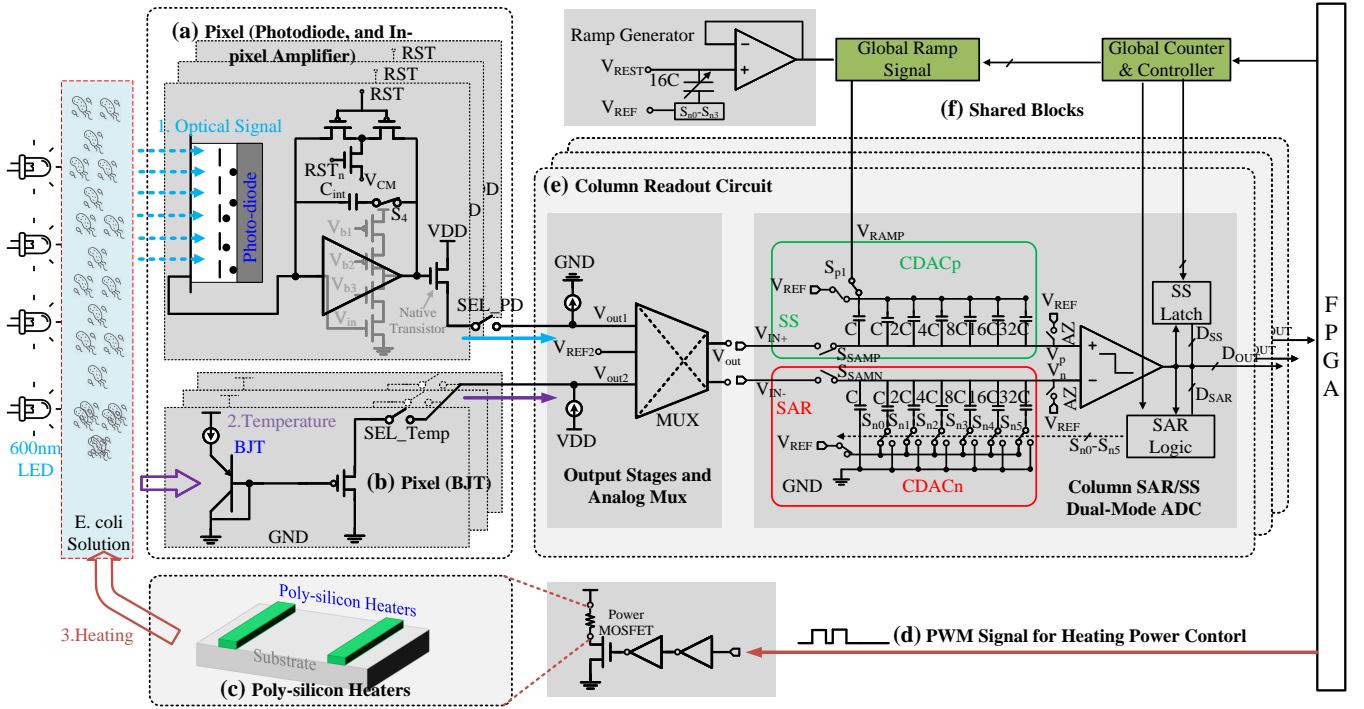
Fig. 3: Circuit implementation of proposed lab-on-a-CMOS platform. (a) photodiode and in-pixel CTIA readout circuit; (b)(c) BJT and thermal actuators for temperature regulation; (d) off-chip electronics for on-chip heating power control; (e) analog multiplexer and column dual-mode SAR/SS ADC shared by optical and temperature signal paths; (f) global ramp signal generator, counter and controller shared by column readout circuit; ISFET sensor is also integrated with photodiode within the same pixel [28] but it's not used in the chip testing and experiment.

II. DESIGN OF THE LAB-ON-A-CMOS PLATFORM

A. Chip Architecture

The proposed LoC platform employs a column-parallel architecture, as illustrated in Fig. 2. It consists of a photodiode array, temperature sensor array, micro-heaters, column ADC, biasing circuit, row decoders, and input/output channels (I/O). Since the bacteria are present in suspension format in the Luria Broth (LB) medium, the bacterial density is not uniform across the whole tube. To accurately measure the bacterial concentration, two approaches can be considered. The first is to implement a single photodiode with a sufficient sensing area capable of accommodating all the bio-samples above the CMOS chip. Alternatively, a photodiode array can be designed, distributing sensor nodes across the CMOS chip. In this case, an averaged measurement of the sensor array is utilized to indicate the concentration of the bio-sample. Due to the limitation of stacking optical, temperature sensors, and heaters on the same substrate in the standard CMOS process, the optical sensor is implemented as an array. This approach allows for adequate space allocation to accommodate the heaters and temperature sensors, enabling sensor fusion achieve integrated analysis for bio-samples. The implemented optical sensor array consists of 40×20 photodiodes. The current generated by the photodiode is converted to a voltage by a capacitive transimpedance amplifier (CTIA) within the pixel instead of a column amplifier to reduce the interference in the column. Similarly, the temperature sensor is also designed as an array to detect the averaged temperature of the solution. In the column, photocurrent and temperature signals are multiplexed to share a column analog-to-digital converter (ADC) with an adjustable reference voltage. The 20 ADC outputs are multiplexed to 5 I/O channels, severing for digitized results output.

The heating power provided by the on-chip micro-heaters are controlled by an off-chip pulse-width modulation (PWM) signal. The temperature sensor array and micro-heaters consist of a feedback system that regulates the on-chip samples to a specific temperature. An FPGA provides the chip control signals and receives the data back for subsequent processing.

B. Optical Sensing

As shown in Fig. 3. Once the light source is on, light emission will travel through the on-chip bacteria and reach the photodiode underneath. An in-pixel CTIA [29] is employed to convert the photocurrent to voltage instead of using 3T APS to pursue a higher sensitivity [30]. The resulting output voltage of the CTIA can be described as:

$$V_{out} = \frac{I_{pd} \times t}{C_{int}} \qquad (1)$$

where I_{pd} is the photocurrent decided by the input light strength and bacterial concentration, t is the integration time, and C_{int} is the feedback capacitor. With a fixed input light intensity and integration time t, I_{pd} and thus V_{out} solely
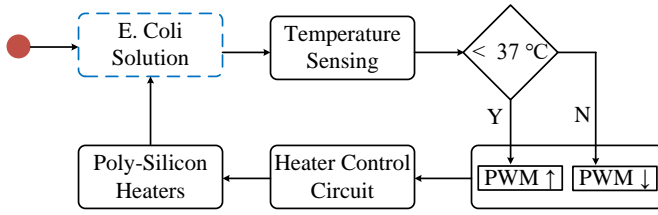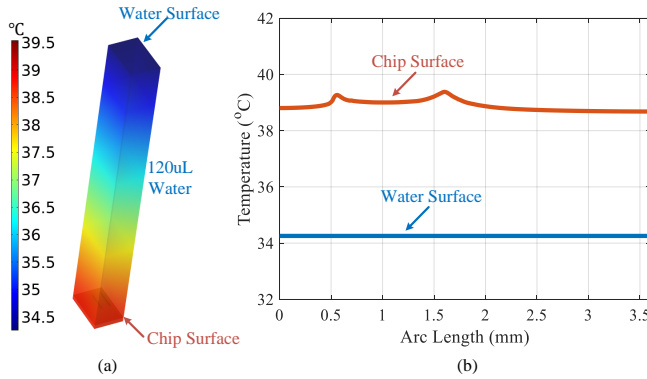
Fig. 4: Flow chart for heating regulation.

Fig. 5: FEM simulation for chip heating regulation. (a) temperature profile of thermal system using poly-silicon heaters for 120uL water; (b) diagonal temperature profile of chip and water surfaces.

dependents on bacterial concentrations. Assuming the CTIA has an ideal operational transconductance amplifier (OTA), the photodiode is held at a constant voltage. Therefore, any photocurrent I_{pd} generated will be integrated on C_{int}. By designing a small C_{int}, the pixel output V_{out} can be highly sensitive to I_{pd}, as described by Eq. 1. Instead of choosing a Metal-Insulator-Metal (MIM) capacitor, which has a much larger minimum capacitance, the C_{int} is implemented using a Metal-oxide-Metal (MoM) Capacitor with a capacitance of 7.5 fF to boost the optical sensitivity. For a larger signal range, 3.3 V devices are used. A native transistor is employed in the pixel's driving stage to provide a larger voltage swing due to its lower threshold voltage. The photodiode employs an N-well/p-sub structure with a size of 8.5 um × 8 um. The operational transimpedance amplifier is a single-ended cascode common-source amplifier with an open-loop gain of 65 dB. A 3T low leakage reset switch is used to reduce its leakage current injected into the integration node of the CTIA [31].

C. Heating Regulation

The temperature regulation is realized through a temperature sensor array, two poly-silicon heaters, FPGA, and a heater control circuit, as shown in Fig. 3b to Fig. 3d. The temperature sensing front-end is implemented with a diode-connected bipolar junction transistors (BJT) instead of a MOS-FET counterpart, considering to have better accuracy after one-point calibration [32]. The temperature signal is buffered before digitization by a p-channel source follower to maintain

its linearity. The temperature signal is simulated to have a sensitivity of 2 mV/°C and excellent linearity (R^2=1) within a sensing range of 20 °C to 60 °C [28].

The flow chart for heating regulation is shown in Fig. 4. Starting from sensing the temperature of the on-chip E. coli solution, the FPGA will compare the sensed temperature with predefined value, which is 37 °C in this application. Depends on the temperature comparison result, FPGA will change the PWM signal accordingly. Through the heater control circuit and poly-silicon heaters, the PWM signal from the FPGA is transformed into heating power for the E. coli solution. The micro-heaters are connected with an off-chip power MOSFET switch. The control signal is buffered by two inverters to control the power MOSFET so as to reduce the signal delay. Using this thermal closed-loop feedback, the temperature of the E. coli solution, therefore can be regulated to a predefined value of 37 °C. It should be noted that the heat generated by the chip itself, although negligible compared to heaters, is also sensed by temperature sensors and, therefore, regulated by the thermal feedback loop.

Poly-silicon heater, commonly used as a thermal actuator for a variety of physical sensors [33]–[36], is employed as a heating source and implemented on the CMOS chip. The width of each heater is designed to be 10 um, and the total length is 3900 um to enclose the sensor array. Serpentine routing is used to break the long line into a parallel format to be easily integrated with other blocks. The heating power provided by a single heater is designed to be 270 mW. The FEM simulation for chip heating regulation is illustrated in Fig. 5a, while the diagonal temperature profiles of chip and water solution surfaces are provided in Fig. 5b. Using 40% of the total power consumption to heat 120 uL water, the designed heating regulation system can reach an averaged temperature crossing 34.3 °C to 39 °C, which corresponds to a desired temperature of 37 °C +/- 2/2.7 °C for the whole on-chip liquid. The maximum standard deviation of temperature distribution at xy planes occurs at the bottom plane of the sample solution, which is 0.21 °C. At the middle plane of the sample solution, the standard deviation of temperature distribution drops to 2.7 ×10^{-6} °C. The temperature distribution is more uniform at the solution top which shows a standard deviation of merely 3.8 ×10^{-8} °C as revealed by the FEM simulation. The temperature of the sample solution decreases linearly along the z-axis. The center temperature of the z-axis 36.6 °C. equals the average temperature along the z-axis. This equivalence indicates the center temperature could be used to represent the average temperature of the sample solution.

D. Column SAR/SS Dual-Mode ADC

The temperature signal and optical signal share a 10b column ADC through an analog multiplexer, as shown in Fig. 3e, for signal digitization. The column ADC is implemented as a successive approximation-register (SAR) and single-slop (SS) dual-mode to balance the chip area, power, and quantization speed [37]. A similar ADC structure is also shared by another design [38], and the major difference lies in achieving different sampling rates. The input analog signal

(a) 6b SAR Mode   **(b) 4b SS Mode**
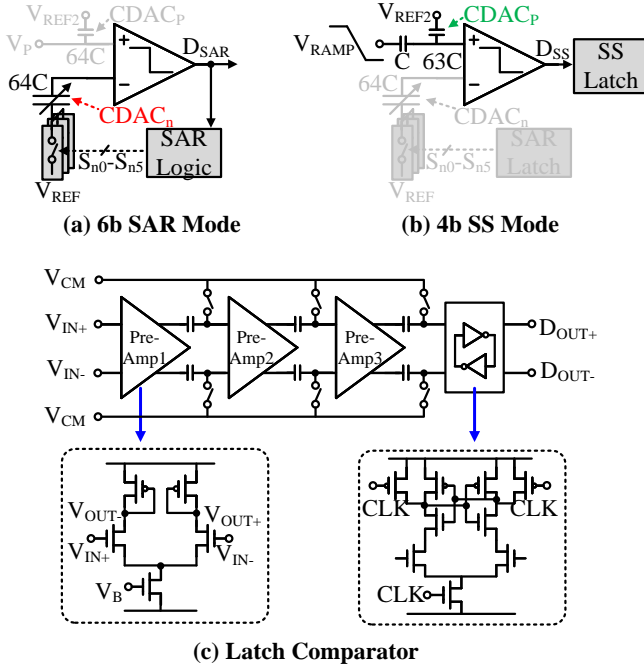
(c) Latch Comparator

Fig. 6: Column SAR/SS dual-mode ADC. (a) 6b SAR mode; (b) 4b SS mode; (c) continuous 3-stage latch comparator

is sequentially converted into upper 6b and lower 4b using SAR ADC and SS ADC, respectively. As shown in Fig. 3f, V_{RAMP} for SS ADC is generated by a global capacitive digital-to-voltage converter (DAC), which has higher accuracy than the current source type and consumes less power than resistive ladder DAC. All the column SS ADCs share a global counter to further reduce the chip area.

The operation of this hybrid ADC is shown in Fig. 6a and Fig. 6b. After the analog signals pixel output DC voltage and signal, respectively, are sampled, $CDAC_n$ capacitor array controlled by SAR logic is employed for the $6b_{MSB}$ quantization. During the SAR ADC operation, $CDAC_p$, is held at V_{VREF2} after sampling. For the subsequent 4b SS quantization, the least capacitor 1C of $CDAC_p$ is used to couple the ramping voltage, V_{RAMP}, to trigger the SS latch. During the SS operation, the other capacitors of $CDAC_p$ remain connected to V_{REF2} while the $CDAC_n$ remains controlled by SAR latch. External ramping voltage can also be applied to the SS ADC for error correction to improve the integral non-linearity (INL) and differential non-linearity (DNL). As shown in Fig. 6c, the latched comparator is designed with a 3-stage pre-amplifier to suppress the latch noise [39]. Each pre-amplifier has an open-loop gain of 4. SAR and SS ADC share the latched comparator to reduce the column area. Auto-zeroing is first initialized for every quantization loop to remove the pre-amplifier's offset.

E. System Operation

The operation flow for the proposed LoC is illustrated in Fig. 7a. The LoC platform starts with heating regulation. It's completed through a thermal feedback control system consisting of temperature sensing and heating power control,
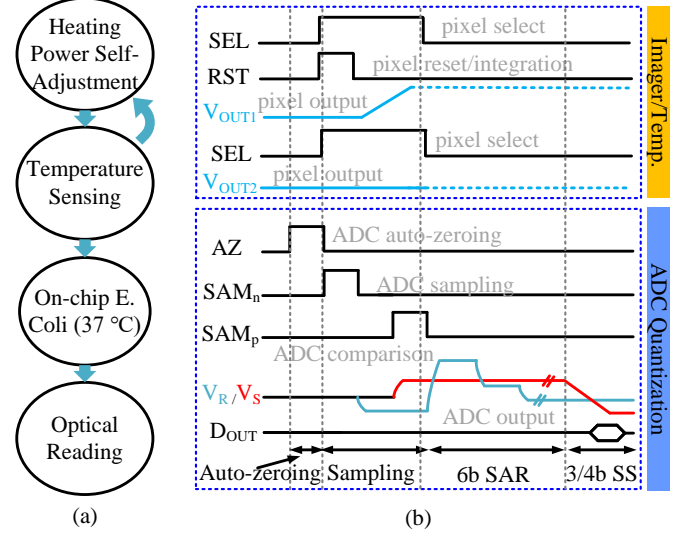

Fig. 7: (a) operation flow of the proposed system; (b) timing diagram.

following the flow chart illustrated in Fig. 4. After the on-chip sample is heated and stabilized at the targeted 37 °C, which is the optimum growth temperature of E. coli, optical sensing is performed to monitor the bacterial growth in real-time. For the temperature sensing and optical sensing process, the timing diagram is shown in Fig. 7b. For optical sensing, ADC first performs auto-zeroing and then samples the reset voltage and signal from the selected photodiode pixel for quantization. While for temperature sensing, ADC uses an off-chip temperature-independent reference voltage and quantizes the temperature signal from a selected BJT pixel. The rest of the operation sequentially follows the SAR and SS ADC logic, generating 10b digital code and is delivered to FPGA for subsequent processing. Since a large sampling capacitor is used and array averaging is performed in the signal readout, the limiting factors for system performance are linearity and quantization noise instead of random circuit noise.

III. EXPERIMENTAL RESULTS

A. Chip Fabrication and Testing Platform

A prototype LoC platform is fabricated using a standard 0.18 um 1P6M CMOS process. The chip micrograph with the main block highlighted is shown in Fig. 8a. The chip occupies a silicon area of 2 mm × 3 mm. 4 × 20 BJTs are designed, and one temperature pixel is inserted every 10 photodiodes. Two poly-silicon micro-heaters lie at the two sides of the sensor core. The sensing part occupies a chip area of 612 um × 1470 um. SAR/SS ADC successfully fits in the column pixel slice due to its hybrid topology.

The chip is wire-bonded on a customized printed circuit board (PCB) and glued with epoxy to prevent the bonding pads and bonding wires from electric shortage during wet testing, as depicted in Fig. 8b. An additional parylene-c layer is coated on the epoxy to prevent chemical contamination and facilitate chip cleaning. A reservoir is glued above the fabricated chip
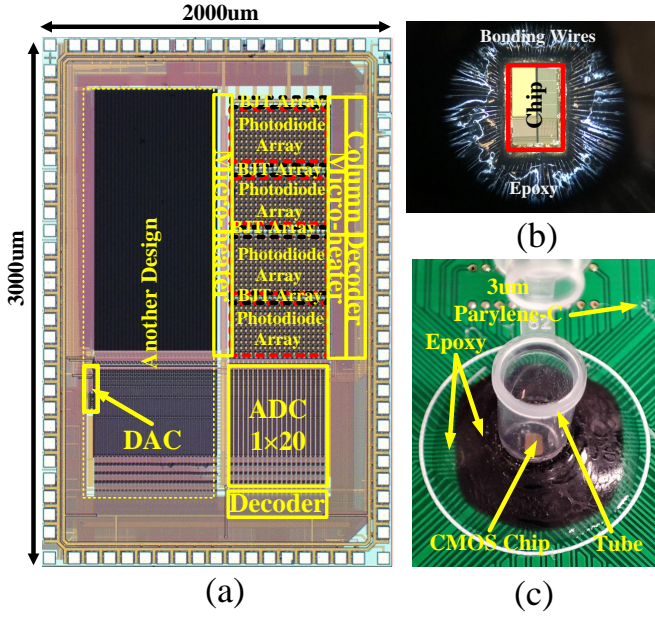
Fig. 8: (a) Chip micrograph with major blocks highlighted; (b) chip wire-bonded and packaged with epoxy for wet testing; (c) chip on PCB packaged with a tube for bacteria; this core board is coated with 3um thick parylene-c.
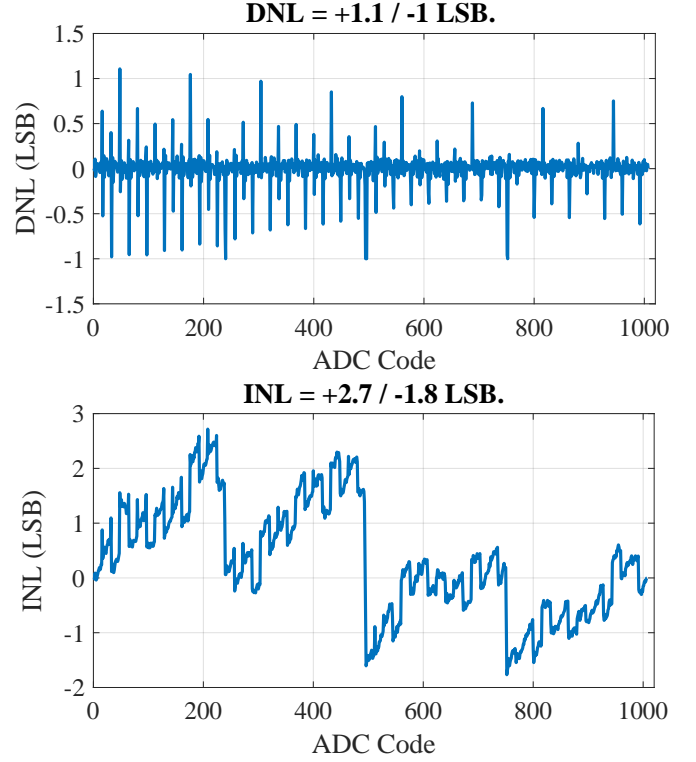

Fig. 9: ADC static performance

Fig. 10: Averaged ADC outputs of the temperature sensor array, its linear fit within the temperature range of interest and sensing accuracy. The temperature measurement errors are calculated using a two-point calibration method.

to accommodate the bacterial sample for real-time growth monitoring, as shown in Fig. 8c. A 3D printed chamber is mounted on the chip-bonded PCB, working as an LED light stand and reducing environmental light and temperature influence. The chip-bonded PCB is inserted into an FPGA and connected with an off-chip circuit for the LED light source and heating power control. The FPGA is connected to a PC through a USB connection to facilitate the configuration of the chip control program and data visualization. To better observe the growth kinetics of bacterial samples, The chip testing setup is placed on a shaker to reduce the sample sedimentation. The whole testing setup is placed in a dark chamber to eliminate the environmental light influence and further reduce the environmental temperature impact.

B. ADC Static Performance

ADC static performance, DNL, and INL, are characterized and shown in Fig. 9. Running at 100 kSPS, the SAR/SS ADC achieves a DNL of +1.1/-1 LSB and INL of +2.7/-1.8 LSB. There are 5 missing codes in total and capped in 1 LSB. Code length variation mainly occurs during the transition from SAR to SS mode. This nonlinearity is due to the parasitic layout mismatch and latch comparator noise. The static performance can be improved to +0.82/-0.9 LSB DNL and +2.2/-1.1 LSB INL using a redundant bit for error correction through external ramping voltage. However, the ADC resolution drops 1b accordingly. The achieved INL and DNL are sufficient for the acquisition of temperature and optical signals without calibration and error correction.

C. Temperature Calibration and Regulation

The accuracy of the BJT-based temperature sensor is first measured to verify its functionality and reliability to be employed in the heating regulation system. The averaged ADC outputs within the temperature range of interest are plotted in Fig. 10. Two-point calibration method, the first data point 23.6 °C and the last data point 51.7 °C, are used to calibrate the temperature and ADC outputs. The achieved sensing accuracy

Fig. 11: Temperature sensor array calibration using temperatures of on-chip sample measured by thermal couple.
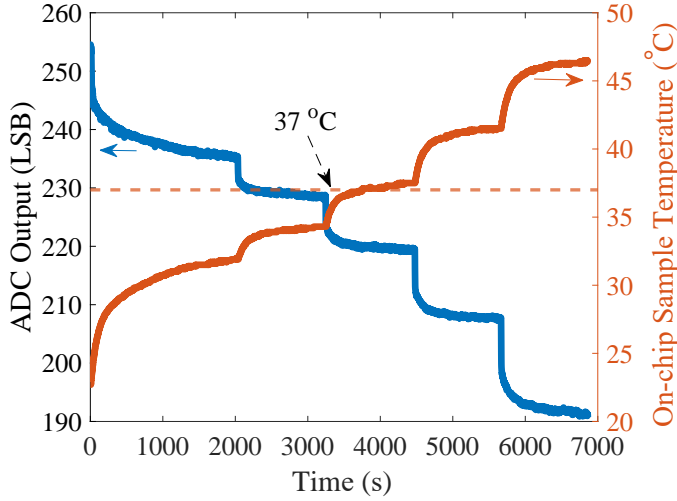

Fig. 13: Robustness testing for temperature regulation by manually changing the full heating power to simulate sharp environmental temperature variations; (a) temperature responses of on-chip sample solution; (b) variation of PWM heating power cycle controlled by the temperature feedback system.
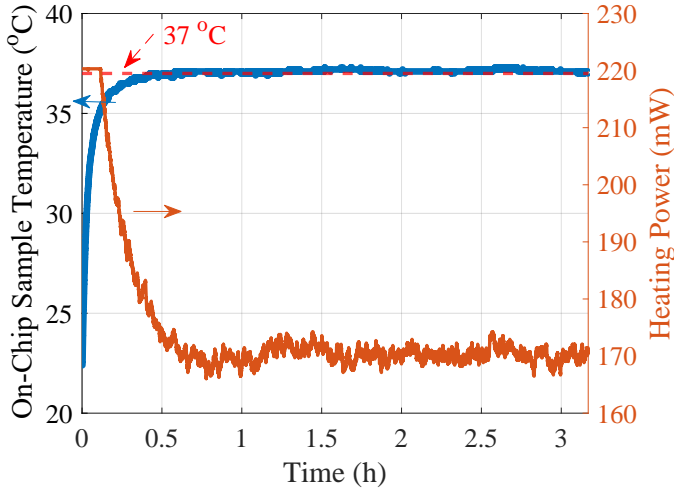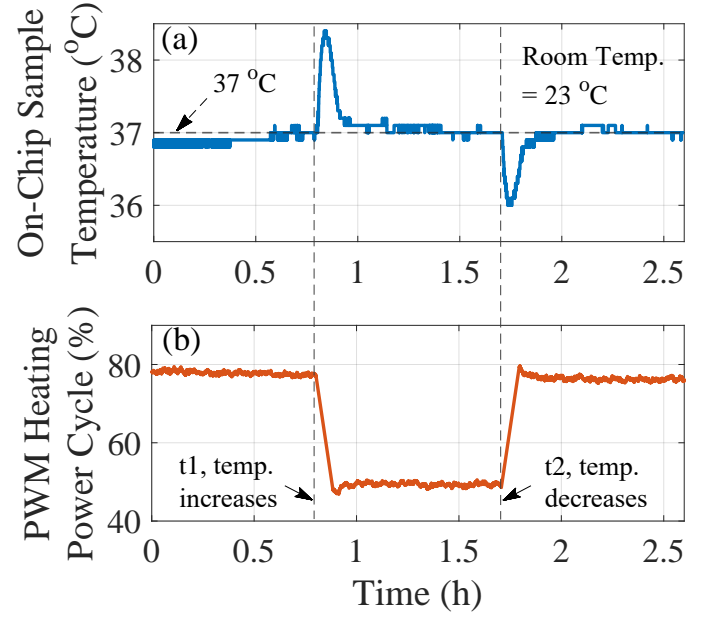

Fig. 12: Temperature response of on-chip sample solution during the temperature regulation from room temperature to 37 °C with correlated heating power.

is +0.15/-0.37 °C as shown in Fig. 10.

After verifying the temperature sensing performance, temperature calibration is performed to correlate the averaged temperature sensor array output to the temperature of the on-chip solution sample measured by a thermal couple. A 120 uL LB is filled in the plastic tube, and the thermal couple is inserted to measure the sample temperature. The heater control PWM is varied at a step of 12.5% modulation cycle to provide different heating power until the stabilized temperature surpasses the targeted 37 °C. Temperature sensor array output and thermal couple output are recorded, as shown in Fig. 11. After interpolation, the ADC output of the temperature sensors, which correlates to a specific on-chip sample's temperature, 37 °C in this case, is obtained.

After the temperature calibration, a temperature regulation

aiming at 37 °C is performed to heat up a 120 uL LB solution. Targeting the ADC value of the temperature sensor array obtained from the temperature calibration experiment, the PWM wave's width controlled by FPGA representing heating power, is delivered to the micro-heaters through a temperature feedback system. The temperature response of the on-chip sample solution measured by the thermal couple and the calculated real-time heating power in the time domain is illustrated in Fig. 12. The heating power starts at full heating capacity to heat the sample, leading to a quick temperature ramping, which is observed in the temperature response. The heating power gradually decreases when the sample temperature gradually reaches the targeted 37 °C. The heating power remains around 170 mW when the sample temperature stabilizes at 37 °C with a maximum temperature fluctuation of 0.3 °C, mainly due to temperature sensor inaccuracy and possible latency of the feedback system. The response time t63 (31.6 °C) and t90 (35.5 °C) are 147s and 502s, respectively. Without obvious overshoot, the temperature reaches 37 °C using 32 mins in total. To maintain a low voltage operation, the maximum applied heating power is only 40% of the designed full heating capacity, which indicates the response time can be significantly reduced by increasing the heating power.

To further verify the robustness of the proposed temperature regulation capability, the heating power is intentionally changed to simulate a sudden environmental temperature variation. As shown in Fig. 13, the on-chip sample temperature stabilizes at 37 +/- 0.1/0.2 °C with a PWM heating power cycle of around 78.0%. At time node t1, the voltage applied to the heaters is manually increased from 17.5 V to 21.5

V to simulate a sharp environmental temperature variation. Under the same heating power cycle, the instant on-chip heating power spike causes the average temperature of the chip surface to suddenly rise 4.4 °C as measured by the on-chip temperature sensor array. Since the on-chip temperature deviates from the preset value, the heating power cycle changes accordingly to regulate the on-chip temperature back to 37 °C through the temperature feedback control system, as illustrated in section II. As shown in Fig. 13b, the heating power cycle decreases after time node t1 and eventually stabilizes at around 49% with a measured average heating power of 168.2 mW. It should be noted that the heater resistance also changes when the applied voltage changes as well as during the heating regulation process. During the simulated increase in environmental temperature, the temperature of on-chip sample solution progressively rises and peaks at 38.4 °C, as shown in Fig. 13a, thereafter decreases and later remaining at 37 +/- 0.2/0.1 °C. After the on-chip sample temperature stabilizes at 37 °C, the voltage applied to heaters is reversed from 21.5 V to 17.5 V to observe the heating system's response to a simulated decrease in environmental temperature. Under the same heating power cycle, the on-chip heating power, therefore decreases 49.3 mW. This heating power dip leads to an average temperature of chip surface fall 2.9 °C. Since the on-chip temperature is lower than the preset value, the temperature feedback control system increases the heating power cycle to compensate for the heat loss. During the heating compensation process, the temperature of on-chip sample solution gradually decreases and reaches the minimum value of 36 °C, then increases to a stabilized value of 37 +/- 0.1 °C. During the simulated sharp variations of environmental temperature as large as 4.4 °C, the temperature feedback system successfully regulates the temperature of on-chip sample solution to 37 °C with a maximum error of 0.2 °C. The precisely regulated temperatures in response to sharp environmental temperature changes demonstrate the robustness of the proposed temperature control system.

D. Optical Sensor Array Calibration

To characterize the chip's optical response, E. coli samples with 600nm optical density (OD_{600nm}) measured by spectrophotometer, ranging from OD_{600nm}=0.203 to OD_{600nm}=1.160 are tested under the same 600nm light strength. LB (OD_{600nm}=0.046) could serve as the baseline for the other measurements. A precision current source is employed to control the light strength of 600 nm LED. The precision current source also ensures the input light reference remains unchanged during each test to reduce the experimental error.

Fig. 14a illustrates the averaged outputs of the photodiode array with array non-uniformity for different E. coli concentrations. For higher E. coli concentration, the input light is shielded more thus less light is seen by the photodiodes under the bacterial sample. As expected, the measured ADC output decreases with E. coli concentration increases and shows a high linear relation. The array non-uniformity refers to how closely the individual optical sensors perform in terms
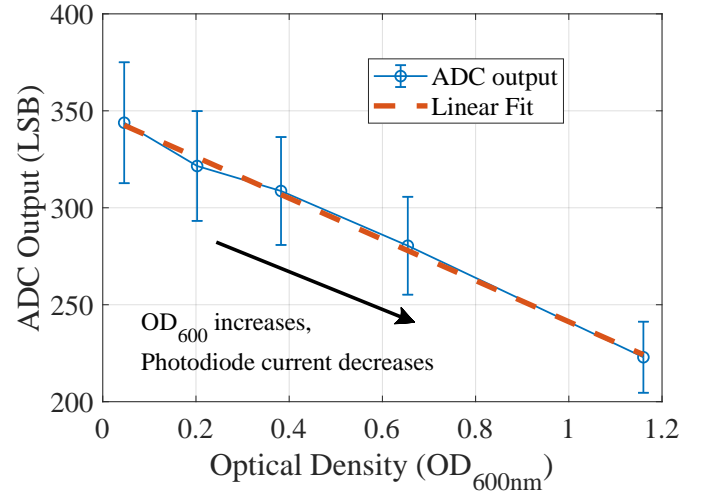
(a) Averaged ADC outputs of photodiode array under the testing of LB concentration OD_{600nm}=0.046 and E. coli concentration ranging from OD_{600nm}=0.203 to OD_{600nm}=1.160. The error bars represent the array non-uniformity of the whole photodiode array's output.
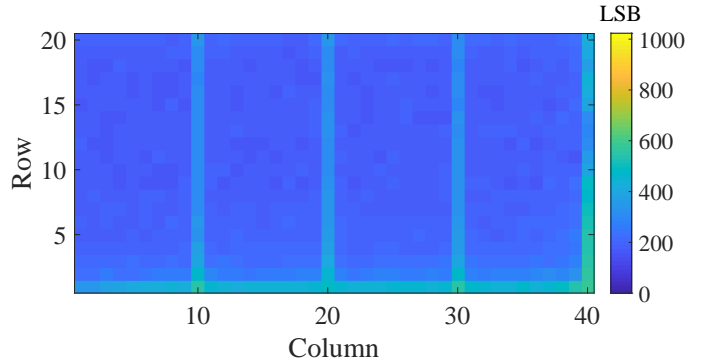
(b) Optical response of photodiode array to E. coli OD_{600nm}=1.160

Fig. 14: Optical responses to E. coli

of optical response. It directly shows the variance in the optical response across different photodiodes. The measured optical responses show a relatively high array non-uniformity which is as expected, as the sample under test is a bacterial suspension, therefore, E. coli is not evenly distributed over the photodiode array. The array non-uniformity also comes from the asymmetric layout of the photodiode array because of the integration of ISFET and temperature sensors. Fig. 14b shows the optical response of the photodiode array to E. coli at OD_{600nm}=1.160, in which the photodiode column next to the temperature sensor column shows a higher optical response than other photodiode columns. However, the exhibited array non-uniformity is not significant as it's the averaged optical outputs are recorded to monitor the concentration variation during E. coli's growth. Moreover, these photodiodes with the higher response could be used independently when E. coli concentration goes to extremely high that beyond the sensing range of normal photodiodes as implemented on this chip. Nonetheless, the designers may have to consider the array non-uniformity if a similar design intends to sense the localized imaging instead of averaged optical information as this work does.

TABLE I: LoC Specifications

Parameters	Specifications
Technology	0.18um 1P6M Standard CMOS
[1]Chip Area	2 mm × 3 mm
Power Supply	Analog: 3.3 V
	Digital: 3.3 V & 1.8 V
Photodiode Array	40 × 20
BJT Array	4 × 20
Micro-Heater Array	2 × 1
Pixel Size	[2]Dual-Mode: 26 um × 32um
	BJT: 26 um × 16 um
Temperature Variation	37 +/- 0.2/0.3 °C
Heating Response Time (T63 & T90)	147 s & 502 s
Power	Total: 211 mW
	[3] Heaters: 170 mW @ 17.5 V
	CMOS Chip: 41 mW
Optical Sensitivity	106 LSB/OD$_{600nm}$
[4]ADC Resolution	10b
Sample Volume	120 uL
Temporal Resolution	5 min
System Features	Temperature Regulation
	Optical Detection

Note: [1]The chip area is shared by the proposed LoC and another design; [2]photodiode and ISFET, pH mode sensor is not demonstrated;[3]when on-chip sample temperature reaches equilibrium at 37 °C; [4] simulation result.

IV. REAL-TIME GROWTH KINETIC MONITORING

In this section, real-time monitoring of E. coli kinetics with and without antibiotics is performed to demonstrate the functionality of the proposed LoC. The real-time monitoring of LB is first performed to test the reliability of the LoC, and the experimental result also could work as the baseline for the subsequent optical measurements. Fresh E. coli samples are cultured overnight in a 37 °C specialized incubator before being pipetted to be tested by the proposed LoC. The sample volume used for testing is 120 uL, and the same sample volume is used in temperature calibration for all the real-time monitoring experiments. To accurately reveal the optical information of E. coli samples during growth, the optical signal reading postpones until the on-chip temperature stabilizes at 37 °C so as to minimize the temperature influence on the photocurrent. Each real-time monitoring runs 11 hours in total with an optical signal sampling interval of 5 min. Considering LED light also generates heat when it is on, and the distance between the LED light and bacterial sample is a few centimeters, the LED light is only turned on during the optical signal readout phase to reduce its thermal disturbance on the E. coli sample. Since the testing setup is placed on an incubator shaker, 40 frames of the optical signal are averaged to improve accuracy and reduce shaking-induced disturbance.

The real-time monitoring of experimental results of LB, and E. coli samples with and without antibiotics are illustrated in Fig. 15. The LB sample is added with antibiotics as well to prevent bacterial contamination, which may vary the experi-

mental results. The minimum inhibitory concentration (MIC) of antibiotics used for E. coli is less than 10 ug/mL [42]. For demonstration purposes, the added antibiotics concentration is 100 ug/mL, which can efficiently suppress the bacterial metabolism for the entire monitoring time. As expected, the optical response of LB over 11 hours remains unchanged due to the lack of bacterial growth. Also, the optical response of E. coli with antibiotics added does not exhibit any changes over the entire monitoring period. Both the signals of LB and E. coli with antibiotics slightly drift around 2 LSB after 11 hours of continuous testing, possibly due to the LED light strength drifting. This slight signal drift does not affect the experiment results, and it can be removed using the optical response of LB as the signal baseline. In terms of experimental results of normal E. coli growth, three experiments are performed to verify the functionality of the proposed system. For all the three trials, the ADC outputs all show decreasing trends. Compared with experimental results of LB and E. coli with antibiotics, these decreasing trends of ADC outputs can be regarded as changes in bacterial concentration induced by growth. Therefore, the proposed functionality monitoring the bacterial growth kinetic is verified. As observed, no lag phases are shown in the optical-based growth curves due to their large initial optical densities. The signal changing rates at the initial stages show much larger slopes than those in the later stages during these entire monitoring processes, which match the typical growth curve of E. coli [43]. For all the trials over 11 hours of continuous monitoring, the equivalent optical densities of the total approximated optical responses are OD$_{600nm}$=0.208, OD$_{600nm}$=0.338, OD$_{600nm}$=0.166, respectively. The growth rates are smaller than a typical E. coli's, mainly due to the lack of oxygen in the culturing tube. Though a shaker is employed to prevent sedimentation and insufficient mixing of oxygen and LB, the surface tension of the culturing tube most likely still causes difficulty.

Table I summarize the key specification of the proposed LoC. Enabled by an on-chip temperature regulation system, the LoC maintains precise temperature control. A quick response time T63 of 147 s is achieved, only consuming 40% of the full heating capacity. The optical signal detected by the photodiode shows great linearity, which could facilitate signal calibration in field testing. With a better testing sample reservoir, the 120 uL bacterial sample volume and the heating response time can be further reduced. The heating power starts from 220 mW and decreases to 170 mW when the on-chip sample reaches the equilibrium at 37 °C. The on-chip electronics dissipate a total power of up to 41 mW.

The key performance comparison with other related works is summarized in Table II. The proposed LoC achieves real-time monitoring of E. coli growth and on-chip temperature regulation, thus, possessing the least human intervention and contamination risk. Considering a sensitivity of 106 LSB/OD$_{600nm}$, the experimental results of optical detection exhibits 2 LSB signal drift, proving it is a highly reliable detection method, specifically, compared with ISFET [14], [15]. Implemented in the standard CMOS process, our highly integrated LoC demonstrates its cost-effective and small form-factor prospects. Highly integrated CMOS system and small
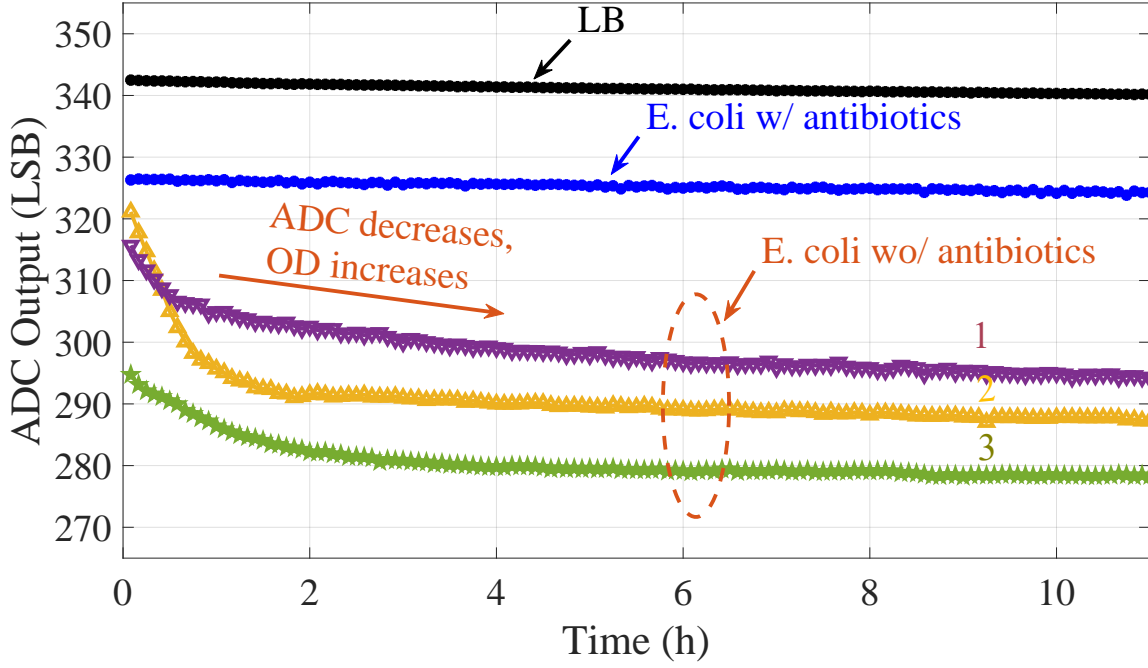
Fig. 15: Real-time optical signal of LB, E. coli with(w/) and without (w/o) antibiotics over 11 hours; antibiotic composition:10,000 unit/mL penicillin & 10 mg/mL streptomycin.

TABLE II: Key Performance Comparison

	This work	Lab-on-Chip	TBCAS	TBCAS	TBCAS	Sci. Rep.	Sens. Actuators. B
	2020	2017 [14]	2021 [15]	2010 [17]	2019 [40]	2021 [21]	2009 [41]
Technology	Standard 0.18um	In-house fabrication	Standard 0.18um	Standard 0.18um	In-house fabrication	Commercial Image Sensor	In-house fabrication
Chip Size [mm^2]	2 × 3	-	1.7 × 2	2	2820	5.7 × 4.3	7 × 15
Supply Voltage [V]	3.3 & 1.8	-	3.3 & 1.8	1.8	-	-	-
Sensing Target	E. coli	E. coli	E. coli	E. coli	E. coli	S. epidermidis	E. coli
Sample Volume	120uL	20uL	4mL	-	50uL	1-2uL	-
Method	Optical Photodiode	pH ISFET	pH CMOS ISFET	Capacitance Capacitive Sensor	Resonant Frequency Ring Resonator	Optical Photodiode	Impedance Impedimetric Sensor
Array Size	20 × 40	4 × 8	4 × 8	2 × 2	2 × 1	-	2 × 1
Sensitivity	106LSB/OD$_{600nm}$	32mV/pH	221mV/pH	255mV/fF	-	-	-
Temporal Resolution	5min	Offline Monitoring	Offline Monitoring	Offline Monitoring	2min	20min	60min
[1]ADC Resolution	10b	Off-chip Instrument	Analog	6b	Off-chip Instrument	-	Off-chip Instrument
Off-chip Instrument	Shaker	Incubator	Incubator	-	Incubator Microscope	Incubator, Fan Thermoelectric-Cooler	Fermentor
Off-chip Component	FPGA, LED CMOS Inverters	Source Meter Ag/AgCl	FPGA Ag/AgCl Light Source	FPGA 3-Axis Robot Dispensing System	Phase Network-Analyzer Temp. & RH	Camera Board LED	Impedance-Analyzer DAQ
Incubation Temperature	37°C	37°C	37°C	28°C	24°C	37°C	37°C
Temperature Regulation	On-chip BJTs Micro-Heaters	Offline Incubator	Offline Incubator	Offline Control	Offline Chamber	Offline Incubator	Offline Incubator

chip footprint could also potentially result in less power consumption due to the less usage of off-chip components and smaller heater loss. These demonstrated advantages make the proposed LoC stand out from the reported works that are fabricated in-house or need off-chip instrumentation [21], [40], [41].

As a continuation of this research, the development of an even miniaturized microchamber holds promise for reducing the volume of bio-samples, leading to enhanced vertical temperature uniformity and improved heat regulation response time. Specifically, for localized imaging sensing and high temperature-dependence applications, optimizing the system integration as well as the heater design could be pursued to achieve superior horizontal temperature uniformity. Furthermore, a monolithic integrated LoC platform could effectively decrease the reliance on off-chip components, necessitating the integration of an on-chip feedback control algorithm and the use of high-voltage processes to incorporate the heater driving circuit.

V. Conclusion

This paper presents a highly integrated lab-on-a-CMOS platform implemented in a standard 0.18 um CMOS process, featuring from-sample-to-answer for online monitoring of bacterial growth. Temperature sensor array and micro-heaters are designed to form a temperature feedback control system. This temperature control system successfully provides an optimum temperature of 37 °C for bacterial growth with demonstrated robustness. The optical sensing results reliably distinguish LB, E. coli with and without antibiotics added testing samples. The highly integrated yet miniaturized CMOS sensors and actuators platform promise to monitor the bacterial kinetics with minimum human intervention and reduced risk of contamination, thus taking one step further towards field testing.

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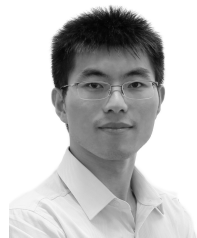
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