Mixed-Mode Simulation Approach to Characterize the Circuit Delay Sensitivity to Implant Dose Variations

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***Abstract*—Process, device, and mixed-mode (device/circuit) simulation-based approach is presented for 0.1-μm gate length CMOS technology optimization and sensitivity analysis. The disposable spacer-based 0.1-μm NMOS and PMOS transistors with excellent short channel characteristics are designed using process and device simulations. The implant-dose sensitivity of the device parameters around the nominal value are estimated. The halo implant and super steep retrograde channel implant dose fluctuations are found to have a profound effect on device characteristics. It is shown that the mixed-mode device/circuit simulation can be used as an excellent tool to connect the circuit delay sensitivity to underlying process parameters. The simulation results demonstrate that the relation between circuit and process parameters is highly nonlinear for the deep submicron technology.**

***Index Terms*—Circuit delay, CMOS technology, disposable spacer, mixed-mode simulation, sensitivity analysis.**

I. Introduction

THE TRANSISTOR mismatch due to random variations in process parameters has become one of the major issues in deep submicron (DSM) technology. The term transistor mismatch refers to the fact that supposedly identical transistors at the design phase come out as distinct devices after manufacturing [1] due to process variations. The process variations are due to extrinsic and intrinsic factors [2]–[4]. The extrinsic factors include variation in implantation dose and energy, oxidation, and annealing temperature, etc. On the other hand, the intrinsic factors include variations due to random fluctuation of channel dopant number, interface, and fixed oxide charge. Both the extrinsic and intrinsic factors influence the transistor output parameters which, in turn, have a significant impact on circuit performance and yield [5]. The transistor mismatch effect will become worse in the future due to demanding requirement on process tolerance. Hence, there is a dire need to develop a very good understanding on the impact of variation in a given unit process on resulting variation in a given circuit parameter. This will enable the process engineering and manufacturing team to define appropriate process monitor and control criterion for all the unit processes involved. This will also help during the technology development phase to select a particular process integration scheme that could minimize the mismatch among various available options.

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Several statistical approaches have been proposed to relate circuit parameters to SPICE parameters [6], [7] and device parameters to process parameters [8]. The conventional circuit sensitivity analysis evaluates the parameter variations at process voltage and temperature (PVT) corners through Monte Carlo analysis. This is of great value for yield and performance estimation of a given circuit design for a specific technology. The circuit delay fluctuation as a function of random variation in SPICE parameters can be obtained through this technique.

In this work, we propose to perform mixed-mode simulations, which bring the process-simulated devices directly into the netlist of a circuit wherein both circuit and device equations are solved simultaneously. This technique has the advantage of being accurate as it has been pointed out in [9] that SPICE parameters may not capture the device behavior very accurately in the DSM regime. Further, the circuit-delay variation can be related directly to process parameter. In this work, we have used the computer-aided design tools from Integrated System Engineering (ISE). We perform only the worst case analysis for each process parameter rather than rigorous Monte Carlo analysis for statistical distribution. Section II describes the design and optimization of 0.1-μm NMOS and PMOS devices using the disposable spacer technique. The nominal device is targeted to exceed the performance guidelines of the International Technology Roadmap for Semiconductors (ITRS) [10]. Section III gives the effect of the implant dose variation on the dc and ac performance of the transistor. Section IV illustrates the two–stage inverter circuit sensitivity on implant dose variation. It is shown that circuit-delay variation is nonlinear with respect to process variation. Also, the pocket halo implant and super steep retrograde channel implant (SSRC) implant are shown to have the maximum impact.

II. Transistor Design

In realizing 0.1-μm transistor, for an initial estimate of device topography and various doping profiles, a boundary and doping editor tool, MDRAW-ISE was used. The device structural parameters such as oxide thickness, junction depth, halo location etc. were optimized to get the best 0.1 μm device characteristics with a maximum off current of 1.0 nA/μm. DIOS-ISE was then used to realize the target device structure through process simulation. The starting wafer type was assumed to be p-epi on p^+ with epi concentration of $10^{16}/cm^3$. SSRC was defined using In and Sb implants for NMOS and PMOS transistors, respectively. Boron and phosphorous pocket halo implants at a 30° tilt were used to control the short channel effects [11], [12]. The

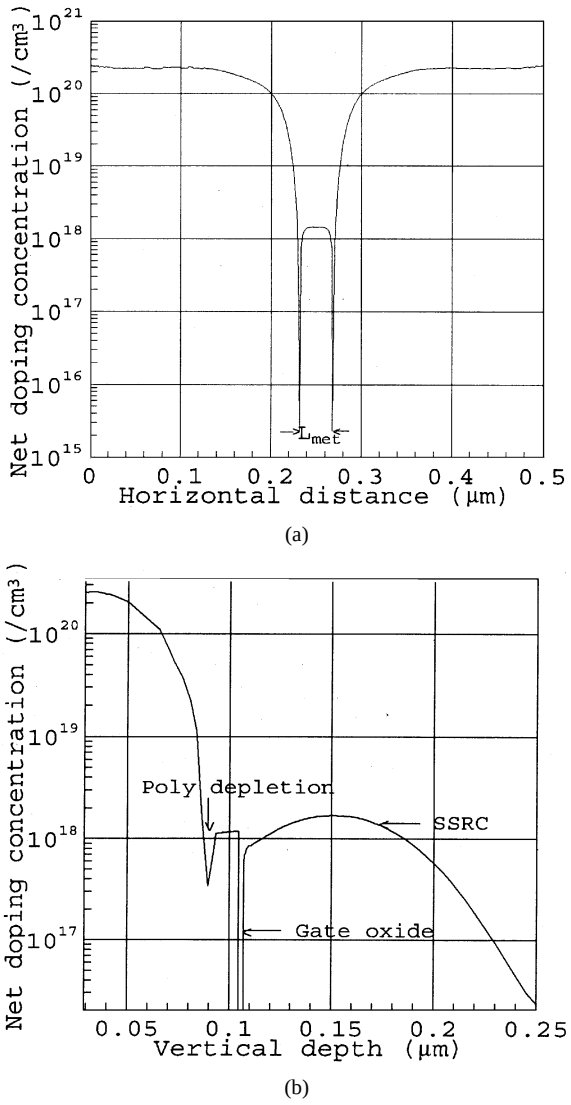


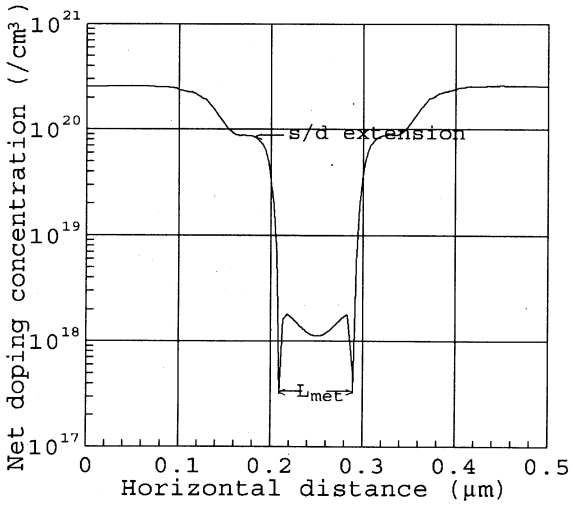
Fig. 1. Doping profiles of the device, simulated from the conventional single spacer technique. Cut lines are taken (a) horizontally, between source and drain, 200 Å below oxide/Si interface and (b) from the mid-top and vertically down in the poly-Si and crossing the gate oxide. Poly-depletion and In SSRC profiles can also be seen.

conventional single spacer technique resulted in an unoptimized NMOS transistor with the doping profiles as shown in Fig. 1. Fig. 1(a) is the doping profile with the cutline taken horizontally 200 Å below the oxide/Si interface. There is no distinct shallow extension. The metallurgical channel length $L_{\rm met}$ is less than 0.07 μm. The pocket halo is not perfectly defined. Fig. 1(b) shows the doping profile in the poly-Si where the cutline is taken from the mid-top of poly-Si vertically down beyond gate oxide. The dip in the doping concentration in poly-Si is indicative of significant poly depletion, and, in fact, n-p junction formation in poly-Si. We observed a tradeoff in terms of poly depletion versus source/drain (s/d) junction lateral diffusion and/or gate dopant penetration into the channel [13]. Increasing s/d energy decreased poly-Si depletion, but it also increased As penetration in the channel. Similarly, increasing post s/d implant rapid thermal annealing (RTA) temperature, decreased poly-Si depletion but also decreased effective channel length significantly due to the lateral diffusion.

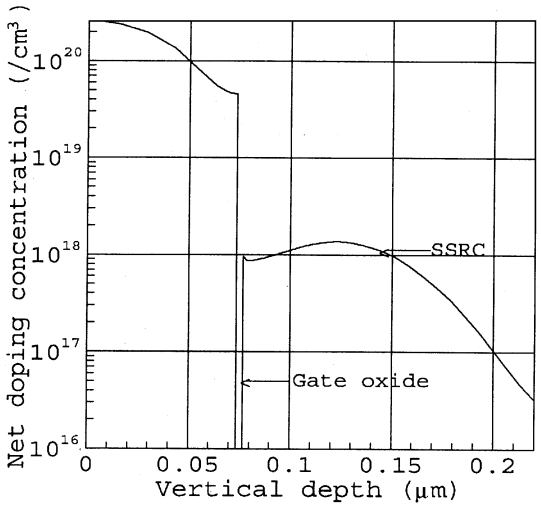
TABLE I
PROCESS SEQUENCE FOR THE DISPOSABLE SPACER TECHNIQUE FOR THE NOMINAL NMOS AND PMOS DEVICE (D0), WITH IMPORTANT PROCESS PARAMETER VALUES. QUANTITIES IN BRACKETS ARE FOR PMOS DEVICE. HIGHLIGHTED STEPS ARE THE IMPLANT PARAMETERS OF INTEREST TO STUDY THE PROCESS SENSITIVITY

	Process Steps and Parameter values
1.	**In(Sb) SSRC: $5.7\times10^{12}cm^{-2}$ /180 keV ($5.7\times10^{12}cm^{-2}$ /200 keV)**
2.	20Å gate oxide @ 800°C
3.	0.1μm gate poly thickness
4.	2 nm poly-reoxidation @ 800°C
5.	96 nm disposable nitride spacer
6.	**As(B) s/d: $6\times10^{15}cm^{-2}$/30 keV ($1\times10^{15}cm^{-2}$/5 keV)**
7.	RTA: 1050°C/20 s
8.	Etch the 96 nm disposable spacer
9.	**As (B) s/d extension:$1\times10^{15}cm^{-2}$/7 keV ($1\times10^{14}cm^{-2}$/1.0 keV)**
10.	**B(P) Halo:$30^o/6.65\times10^{12}$ cm^{-2}/10keV ($30^o/5.85\times10^{12}$ cm^{-2}/25 keV)**
11.	Final RTA: 1050°C/4 s
12.	Deposit 40 nm final spacer
13.	Cobalt silicidation and Al metallization

In order to overcome poly-Si depletion without compromising short channel behavior, the disposable spacer process is used [14]. The sequence of deep s/d and s/d extension implant is reversed by making use of disposable spacer. The main steps in the process sequence are listed in Table I for both NMOS and PMOS devices with important parameter values. The doping profiles for NMOS device using this technique are shown in Fig. 2. Cutlines are taken identical to that of Fig. 1. From Fig. 2(a), shallow s/d extensions are visible as the variation of the doping concentration and also metallurgical channel length $L_{\rm met}$ is comparatively larger than that of Fig. 1. Both shallow extension and $L_{\rm met}$, are very important in controlling the short channel effect. Further poly-Si depletion effect is completely absent as seen from Fig. 2(b). Fig. 3 shows the NMOS transistor structure obtained using disposable spacer technique. The device topography and various doping profiles are conformable with [10], [14], and [15]. The PMOS transistors have deeper junction than NMOS due to high diffusivity of Boron. The shallow extension/deep junction depth for NMOS and PMOS are approximately, 0.04 μm/0.1 μm and 0.05 μm/0.15 μm, respectively. The gate s/d overlap length is maintained at about 15 nm for the parasitic series resistance considerations. DESSIS-ISE has been used for device simulation with Hydrodynamic model [16]–[18] for velocity overshoot and VanDort's model for channel quantization [18], [19]. An interface trap density of $5\times10^{10}/\text{cm}^2$ is applied at the Si/Oxide boundary during the simulation. The disposable spacer device yields superior device characteristics with NMOS and PMOS on state



(a)



(b)

Fig. 2. Doping profiles of the device, simulated from the disposable spacer technique. Cut lines are taken (a) horizontally, between source and drain, 200 Å below oxide/Si interface and (b) from the mid-top and vertically down in the poly-Si and crossing the gate oxide. Compare the metallurgic channel length in (a) with that of Fig. 1(a); s/d extension and In SSRC profiles can also be seen.

currents of 0.954 mA/μm and 0.397 mA/μm, respectively, at a leakage current of 1.0 nA/μm.

III. Implant Dose Sensitivity of Device Characteristics

The four implantation steps highlighted in Table I define the device parameters. All these steps can potentially impact the dc and ac performance. Halo and SSRC implants control threshold voltage whereas s/d extension and deep s/d control parasitic resistance and short channel behavior thereby influencing the dc parameters. Similarly, all these implants can control poly-depletion and junction capacitance, thereby influencing the total capacitance. However it would be very enlightening for process control to know the relative importance of these implants. As an example, we have studied the implant dose variation. To study the implant dose sensitivity, the four highlighted parameters in the Table I are varied $\pm$10% from that of NMOS and PMOS nominal devices (D0). This results in a total of eight devices (D1-D8). Further, we have included two more devices (D9 and D10) in both NMOS and PMOS, for the worst case current fluctuations corresponding to simultaneous variations in all the implant steps, and these devices were called as the process corner devices or the worst case devices [20]. The device label definitions are given in Table II. Devices D1-D10 are process simulated for both NMOS and PMOS devices by DIOS-ISE. For all these devices, dc and ac characteristics are extracted by DESSIS-ISE. The relative deviation of any parameter x, about its nominal value $x_{\rm nom}$ is calculated as $\Delta x = (x - x_{\rm nom})/x_{\rm nom}$.

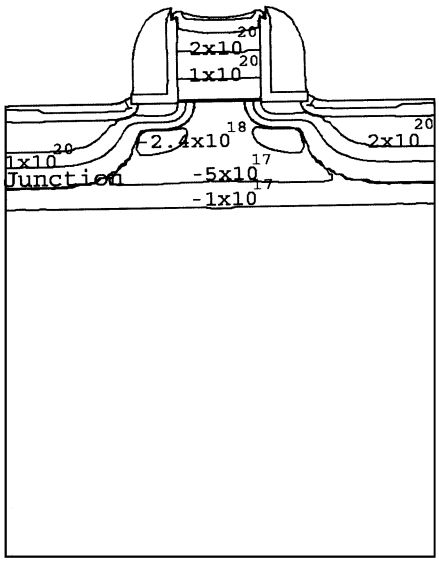


Fig. 3. Process simulated nominal NMOS device. Doping contours with labeled values are indicated. The spacer and silicided regions are also visible.

TABLE II
Device Label Definitions ($-$ and $+$ Signs Correspond to Decrease and Increase in Dose, Respectively). D0 Is the Nominal Device With all Nominal Doses

Devices	% deviation in dose			
	halo	SSRC	deep s/d	s/d extension
D1	-10	0	0	0
D2	+10	0	0	0
D3	0	-10	0	0
D4	0	+10	0	0
D5	0	0	-10	0
D6	0	0	+10	0
D7	0	0	0	-10
D8	0	0	0	+10
D9	+10	+10	-10	-10
D10	-10	-10	+10	+10

Fig. 4 shows the $I_{\rm ds} - V_{\rm gs}$ characteristics for the nominal device (D0) and the worst and best case corner devices (D9 and D10) for both NMOS and PMOS devices. Fig. 5 shows the $C_{\rm gg} - V_{\rm gs}$ characteristics for D0, D9, and D10 for both NMOS and PMOS devices in the saturation region. The ac extractions are performed at 100 kHz over the full range of gate voltage, i.e., $|V_{\rm gs}| = 0 - 1.5$ V. Corresponding to a 10% variation in implant dose, percentage deviations in dc parameters ($I_{\rm off}$, $I_{\rm on}$, and V_t in

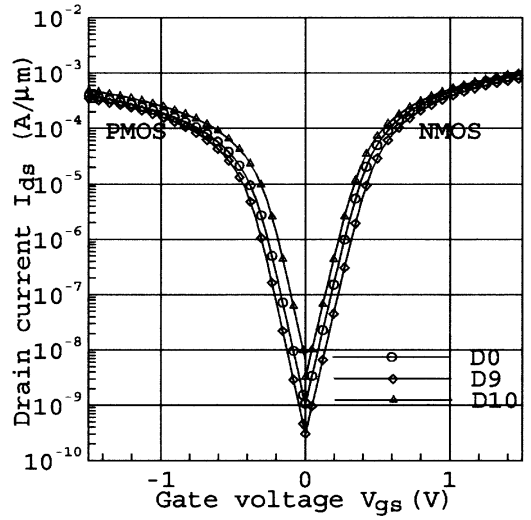


Fig. 4. $I_{\rm ds} - V_{\rm gs}$ characteristics for D0, D9, and D10 for both NMOS and PMOS devices with $|V_{\rm ds}| = 1.5$ V and width, $\rm W = 1\,\mu m$.

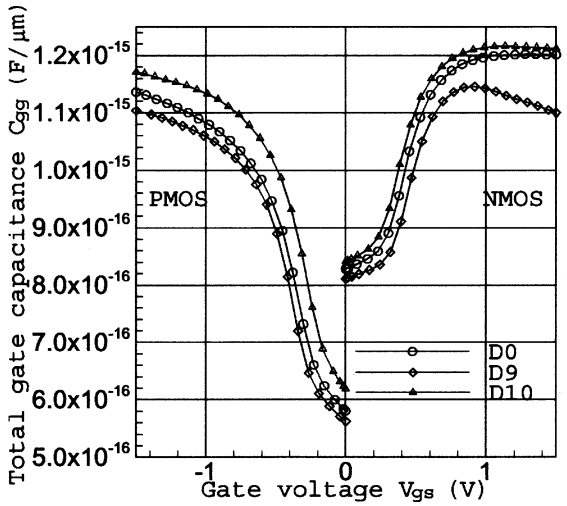


Fig. 5. $C_{\rm gg} - V_{\rm gs}$ characteristics for D0, D9, and D10 for both NMOS and PMOS devices with $|V_{\rm ds}| = 1.5$ V and f $= 100$ KHz.

the saturation region) are tabulated in Table III for both NMOS and PMOS devices. The V_t is extracted using the constant current technique at a current value of $40\ nA \times (W/L_g)$, with $\rm W = 1\,\mu m$ and $L_g = 0.1\,\mu$m. The nominal NMOS/PMOS have a saturation V_ts($@|V_{\rm ds}| = 1.5$ V) of 0.23/0.22 V. It can be seen that the halo implant and SSRC implant steps have the biggest impact on the variations, suggesting that these steps have to be very tightly controlled in manufacturing. The percentage deviation in $C_{\rm gg}$ is tabulated in Table IV for both NMOS and PMOS devices. SSRC, s/d extension, and deep s/d implants are important in controlling the capacitance value. However, the variation in the gate capacitance $C_{\rm gg}$ is typically lower compared to the variation in DC parameters, since the gate capacitance is mainly dominated by the oxide thickness. However, for the accurate prediction of CMOS circuit delay, the CV/I metric is affected by the capacitance variations as well. Some poly-Si depletion effect is evident from the $C_{\rm gg} - V_{\rm gs}$ characteristics.

TABLE III
PERCENTAGE DEVIATION ($\%\Delta$) IN DC PARAMETERS IN THE SATURATION REGION FOR BOTH THE NMOS AND PMOS DEVICES

Devices	@$\mid V_{ds} \mid$=1.5V					
	NMOS %Δ			PMOS %Δ		
	I_{off}	I_{on}	V_t	I_{off}	I_{on}	V_t
D1	122.0	4.8	-13.6	97.5	5.3	-10.3
D2	-52.7	-5.7	11.6	-47.2	-4.5	10.7
D3	33.3	-2.4	-5.2	74.8	11.1	-9.8
D4	-16.9	-5.0	2.6	30.5	7.0	-5.7
D5	-7.0	-1.4	1.3	-23.0	-3.0	6.1
D6	7.9	1.3	-1.9	33.7	3.0	-5.2
D7	-23.2	-2.0	2.6	-26.9	-4.0	6.2
D8	28.7	2.0	-4.5	35.8	3.8	-5.1
D9	-71.3	-13.1	19.4	-69.9	-11.6	20.7
D10	203.5	8.0	-18.7	540.8	24.2	-31.2

TABLE IV
PERCENTAGE DEVIATION IN TOTAL GATE CAPACITANCE $C_{\rm gg}$ IN SATURATION REGION FOR NMOS AND PMOS DEVICES

Devices	%ΔC_{gg} @$\mid V_{ds} \mid$=1.5V for			
	NMOS @V_{gs}		PMOS @V_{gs}	
	0.0V	1.5V	0.0V	-1.5V
D1	0	0	0	0
D2	0	0	0	0
D3	1	-5	2	0
D4	-1	-6	1	-1
D5	0	-1	-1	-2
D6	0	1	1	1
D7	-1	-1	-2	-1
D8	1	0	2	1
D9	-2	-8	-3	-3
D10	1	1	6	3

IV. IMPLANT DOSE SENSITIVITY OF CIRCUIT DELAY

A two-stage inverter circuit as shown in Fig. 6 is simulated at $V_{\rm dd} = 1.5$ V. Eleven, two-stage inverter circuits C0-C10 (using D0-D10, respectively, of Table II, for both NMOS and PMOS devices) were configured by generating SPICE-netlist and mixed mode simulated for an input pulse of 150-ps width and 5-ps rise and fall time. The output waveforms for the three circuits, nominal (C0), worst (C9), and best (C10) are superimposed at the rising and falling edges of the input pulse as shown in Fig. 7(a) and (b), respectively. Various terminal voltages as defined in Fig. 6, along with the circuit label, give the identification of the corresponding curve. Table V consolidates, for the first stage of the inverter circuits C1-C10, the percentage deviation in delay (τ), relative to the nominal circuit C0, and the average percentage delay, loaded with an identical second stage inverter. Significant deviation in the circuit delay is evi-

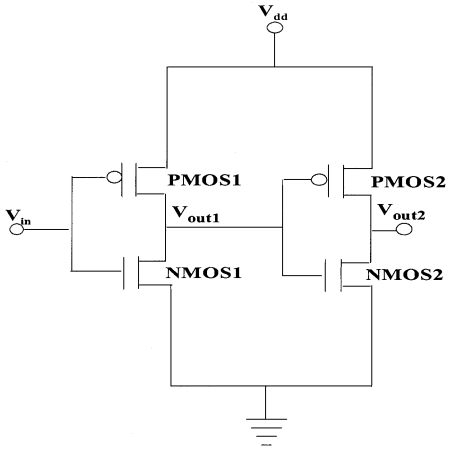


Fig. 6. Two-stage CMOS inverter circuit used in simulation. The NMOS/PMOS transistors have $W = 1\ \mu m/2\ \mu m$.

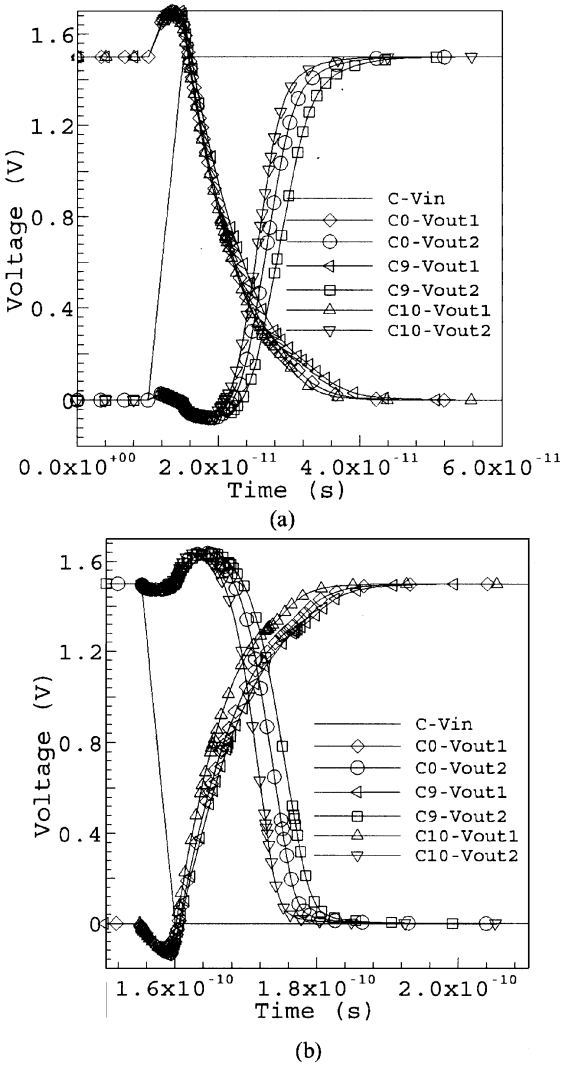


Fig. 7. Transient waveforms of the two-stage inverter circuits C0, C9, and C10 (a) at the rising edge and (b) at the falling edge of the input pulse.

dent from these results. Also, the variations will get amplified with the complexity of the circuit as is evident from the difference in the first and second stage output of the inverter chain.

TABLE V
PERCENTAGE DEVIATION IN CIRCUIT DELAY (τ) PARAMETERS. THE REFERENCE IS THE RISING OR FALLING EDGE OF THE INPUT PULSE. THE NOMINAL CIRCUIT C0 HAS A 8.0-ps RISING DELAY AND A 8.4-ps FALLING DELAY. THE LAST COLUMN IS THE AVERAGE OF THE PERCENTAGE DEVIATION IN RISING AND FALLING DELAYS

Circuits	$\%\Delta\tau_{out1}$ @ the V_{in}		Mean $\%\Delta\tau_{out1}$
	rising edge	falling edge	
C1	-4.5	-3.7	-4.1
C2	3.8	3.7	3.7
C3	-6.3	7.0	0.4
C4	-9.1	8.0	-0.6
C5	2.3	1.0	1.6
C6	-2.3	-1.0	-1.7
C7	2.3	0.2	1.2
C8	-2.3	-0.2	-1.2
C9	9.1	11.7	10.4
C10	-15.9	-2.7	-9.3

The area factor for PMOS is taken twice that of the NMOS in the mixed-mode simulation to account for the carrier mobility difference. Further, the two process corners corresponding to C9 and C10 result in different amount of delay variation, namely, 11.7% and 15.9%, indicating the nonlinearity between the circuit and process parameters. The halo implant and SSRC implant steps have dominant effect on circuit delay.

V. CONCLUSION

Excellent device characteristics have been realized for a 0.1-μm gate length NMOS and PMOS transistor using the disposable spacer technique. The decoupling of the poly-Si gate activation process and the shallow extension formation process is responsible for this performance enhancement. Among the four implant parameters, the pocket halo and SSRC implants have the significant effect on the transistor leakage and saturation currents, which finally impact the circuit delays. These process steps have to be tightly controlled in manufacturing to decrease mismatch effect. The device mismatch, in turn, results in circuit delay variation which has implications on the yield of the circuit. A proper physical model is necessary to correlate the circuit performance to underlying processes for the DSM technology. This would facilitate guidelines for process engineering to improve the manufacturing yield. The asymmetry in percentage deviation in delay, between the circuit C9 and C10 at the rising and the falling edges, implies a nonlinearity between process and device/circuit parameters.

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REFERENCES

[1] H. P. Tuinhout, A. H. Montree, J. Schmitz, and P. A. Stolk, "Effects of gate depletion and boron penetration on matching of deep submicron transistors," in *Proc. Int. Electron Devices Meeting Tech. Dig.*, 1997, pp. 631–634.

[2] K. A. Bowman, X. Tang, J. C. Eble, and J. D. Meindl, "Impact of extrinsic and intrinsic parameter fluctuations on CMOS circuit performance," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1186–1193, Aug. 2000.

[3] T. Mizuno, J.-I. Okamura, and A. Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFETs," *IEEE Trans. Electron Devices*, vol. 41, pp. 2216–2221, Nov. 1994.

[4] P. A. Stolk and D. B. M. Klaassen, "The effect of statistical dopant fluctuations on MOS device performance," in *Proc. IEDM Tech. Dig.*, 1996, pp. 627–630.

[5] A. J. Bhavnagarwala, X. Tang, and J. D. Meindl, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE J. Solid-State Circuits*, vol. 36, pp. 658–665, Apr. 2001.

[6] C. Michael and M. Ismail, "Statistical modeling of device mismatch for analog MOS integrated circuits," *IEEE J. Solid-State Circuits*, vol. 27, pp. 154–166, Feb. 1992.

[7] N. Herr and J. J. Barnes, "Statistical circuit simulation modeling of CMOS VLSI," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 15–22, Jan. 1986.

[8] P. M. Zeitzoff, A. F. Tasch, W. E. Moore, S. A. Khan, and D. Angelo, "Modeling of manufacturing sensitivity and of statistically based process control requirements for a 0.18 μm NMOS device," in *Proc. Int. Conf. Characterization Metrol. ULSI Technol., Amer. Inst. of Phys., CP449*, 1998, pp. 73–81.

[9] V. Palankovski, N. Belova, T. Grasser, H. Puchner, S. Aronowitz, and S. Selberherr, "A methodology for deep sub-0.25 μm CMOS technology prediction," *IEEE Trans. Electron Devices*, vol. 48, pp. 2331–2336, Oct. 2001.

[10] SIA, international technology road map for semiconductors, Process, integration, devices and structures (PIDS), pp. 8–33, 2001.

[11] Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S.-H. Lo, G. A. Sai-Halasz, R. G. Vishwanathan, H.-J. C. Wann, S. J. Wind, and H.-S. Wong, "CMOS scaling into nanometer regime," *Proc. IEEE*, vol. 85, pp. 486–504, Apr. 1997.

[12] Q. Xu, H. Qian, H. Yin, L. Jia, H. Ji, B. Chen, Y. Zhu, M. Liu, Z. Han, H. Hu, Y. Qiu, and D. Wu, "The investigation of key technologies for sub-0.1 μm CMOS device fabrication," *IEEE Trans. Electron Devices*, vol. 48, pp. 1412–1420, July 2001.

[13] H. C. Srinivasaiah and N. Bhat, "Optimization of 0.1 μm NMOS transistor using disposable spacer technique," in *Proc. VLSI Design Test Workshops*, Bangalore, India, Aug. 2001, pp. 298–303.

[14] J. Schmitz, M. Van Gestel, P. A. Stolk, Y. V. Ponomarev, F. Roozeboom, J. G. M. Van Berkum, P. C. Zalm, and P. H. Woerlee, "Ultra shallow junction formation by outdiffusion from implanted oxide," in *Proc. IEDM Tech. Dig.*, 1998, pp. 1009–1012.

[15] S. B. Herner, H. J. Gossmann, R. T. Tung, and B. P. Gila, "Ultrashallow junction in silicon using single-crystal $CoSi_2$ as a dopant source," *Electrochem. Solid-State Lett.*, vol. 1, no. 3, pp. 150–152, 1998.

[16] Y. Apanovich, E. Lyumkis, B. Polsky, A. Shur, and P. Blakey, "Steady-state and transient analysis of submicron devices using energy balance and simplified hydrodynamic models," *IEEE Trans. Computer-Aided Design*, vol. 13, pp. 702–711, June 1994.

[17] P. Lugli, "The Monte Carlo method for semiconductor device and process modeling," *IEEE Trans. Computer-Aided Design*, vol. 9, no. 11, pp. 1164–1176, Nov. 1990.

[18] *ISE TCAD Release 6.1 Manual*, Zurich, Switzerland, 1999.

[19] M. J. Van Dort, P. H. Woerlee, and A. J. Walker, "A simple model for quantization effects in heavily-doped silicon MOSFET's at inversion conditions," *Solid-State Electron.*, vol. 37, no. 3, pp. 411–414, 1994.

[20] S. R. Nassif, A. J. Strojwas, and S. W. Director, "A methodology for worst-case analysis of integrated circuits," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 104–113, Jan. 1986.

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