Guest Editorial Special Section on Contemporary and Emerging Issues in Physical Design

Physical design (PD) has always occupied a key position in the design flow because: 1) it defines the physical locations of transistors and interconnect wires; 2) it supports and handles different VLSI technologies for lithography and fabrication; and perhaps the most important; and 3) the scope of PD can span from early interactions with system planning, high-level synthesis, and logic synthesis, to back-end performance optimization, and design for manufacturing.

Owing to its special position in the flow from RTL to layout, PD is considered to have high leverage in the optimization of chip area, power, thermal, and timing QoR, as well as the design turn-around time. In order to close the performance, power, and productivity gaps between microprocessors and ASICs, researchers have been focusing on different techniques to automate PD methods usually found in high-performance custom designs. Datapath synthesis, multibit flip-flop, nontree clock structures, and full-custom-quality clock buffer synthesis are examples of such efforts. Research efforts in automating those custom-designed PD methods may also help in the convergence of various design methodologies because designers tend to adopt distinct back-end flows for different design targets. In other words, the same PD flow can then be used for both high-performance microprocessors and low-power ASICs.

Scaling has also become more and more difficult because of such different walls as thermal, power, ILP, memory, frequency, and lithography limits. Future design technologies and new manufacturing processes have recently been proposed, which is another major reason why newer PD topics involving, for instance, FinFETs, multiple patterning lithography process, electron-beam, 3-D designs, OPC/CMP co-optimization have been attracting more and more attention. As PD sits in between early planning, logic synthesis, and manufacturing process in the design flow, new PD algorithms are needed whenever next-generation technologies are introduced.

In view of these trends, the papers in this Special Section highlight several studies on contemporary and emerging issues in physical design. The first paper demonstrates that today's CMOS-oriented EDA tools can be repurposed for the design of ASICs using the emerging vertical slit field effect transistors (VeSFETs). It shows that the VeSFET-based designs could have a power advantage over CMOS-based designs at the same performance. For the second paper, instead of replacing all registers with single-bit retention registers such that data can be retained during sleep mode, it replaces only selected registers with multibit retention registers to reduce the negative impacts on the area and leakage power that such retention registers can have in power-gated designs. The third paper deals with the placement of noise sensors for runtime noise management so that power integrity can be guaranteed. The proposed solutions attempt to maximize the noise sensing quality and could significantly reduce the miss rate of voltage emergency detections. The fourth paper searches for the better geometric programming models to solve conflicting power and skew objectives for the contemporary clock network buffer sizing problem. In the fifth paper, the winning team of the 2013 International Symposium on Physical Design Discrete Gate Sizing Contest explains in detail how they achieved top-notch results to the simultaneous gate sizing and Vt assignment problem. The sixth paper focuses on the target clock period selection and severe short path padding problem to better utilize the timing error detection and correction mechanism of resilient circuits. The seventh paper solves the problem of escape routing for mixed-pattern signals, which include both differential pairs and single signals. Finally, the last paper presents an analog verification scheme for SRAM dynamic stability under threshold-voltage variations.

We hope this special section will stimulate more research on contemporary and emerging issues in physical design, and the readers will enjoy the selected manuscripts. We would like to thank all the authors and reviewers for their tremendous efforts in making this special section the best possible.

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Dr. Sze was invited to serve in the academic/research community, for example, as the Technical Program Chair for the International Symposium on Physical Design (ISPD) 2013, as the Silicon-Design/Back-End Track Chair of the 2013 and 2014 Design Automation Conference designer-track sessions, as the Contest Chair of the global routing and clock network synthesis contests in ISPD 2008, 2009, and 2010, and as the Computer-Aided Network Design Track Chair for International Symposium on Circuits and Systems 2011 and 2012. He was a recipient of the ACM Special Interest Group on Design Automation Technical Leadership Award, and has received several IBM Technical/Invention Awards.