A g_m/I_D Methodology Based Data-Driven Search Algorithm For the Design of Multi-Stage Multi-Path Feed-Forward-Compensated Amplifiers Targeting High Speed Continuous-Time ΣΔ-Modulators

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***Abstract*—This work presents a methodology for sizing transistors of a multi-stage, multi-path capacitor-less feed-forward compensated operational amplifiers employed in advanced CMOS process implementation of continuous-time bandpass ΣΔ-modulators. The paper describes the methodology: on system level, dealing with the placement of poles and zeros; and on circuit level, discussing issues related to biasing, frequency response and other important performance metrics of the basic diff-pair. Algorithms are provided to simplify mathematical aspects of the work. The validity and the limitations of the proposed methodology are further discussed from the single-pole system used to model the individual amplification stages of the multi-stage amplifier. The worthiness of the proposed methodology in sizing the transistors of complex amplifier structures such as the capacitor-less multi-stage, multi-path feed-forward-compensated amplifiers is demonstrated using two design examples. A 3rd-order amplifier with a DC gain of 52.6 dB and that reaches a unity-gain frequency of above 14 GHz while consuming only 5.6 mA from a 1 V supply; and a 4th-order amplifier with DC gain of 73.5 dB that achieves a 25.7 dB gain at 1 GHz while consuming 4.8 mW are designed in 28nm CMOS FDSOI.**

***Index Terms*—search algorithm, Matlab script, multi-stage, multi-path, feed-forward compensation, operational amplifier, g_m/i_D methodology, sigma delta modulator, continuous time**

I. Introduction

HIGH-speed bandpass ΣΔ modulators are employed in receiver front-ends for direct conversion of RF signals to digital. Feedback-form high-order ΣΔ modulator are favored as their signal transfer function (STF) can be designed to maximize rejection of out-of-band signals [1]. In a continuous-time (CT) implementation of the feedback type delta-sigma modulators, the requirements are stringent on the amplifiers compared to feed-forward topologies. In reference [1], a DC gain of at least 40 dB at the center frequency of the modulator was targeted for a -80 dBc distortion and 1% coefficient variation. Similarly, reference [2] demonstrates that for a single-amplifier resonator targeting operation at a sampling frequency of 2 GHz, DC gain should be at least 31 dB at 0.5 GHz. In the latter case, the chosen DC gain ensures that the resonance frequency error is within 15%—a value comparable to resistor and capacitor variations in CMOS implementation due to process corners.

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In advanced CMOS nodes where the supply voltage is usually not more than 1 V, gain boosting techniques which rely on transistor stacking are not useful. For this reason, amplifiers each with moderate DC gains are cascaded to reach the required gain [3]–[8]. Depending on the requirements, different methods can be adopted to compensate these multi-stage amplifiers. For example, Miller-type capacitor compensations are good candidates to reach high unity-gain-frequency, f_u, as they push non-dominant poles far away from f_u. The resulting response looks like that of a single-pole system with a -20dB/dec roll-off up to f_u [9]. The price of using the capacitor-based compensation is, then, the gain magnitude at frequencies within an order of f_u is relatively low. For this reason, capacitor-based miller-compensated amplifiers are more suited to reach the desired gain levels at frequencies at least two orders below f_u.

Capacitor-less feed-forward compensation methods have become the topology of choice for amplifiers in applications that require high gain at high frequency [3], [10], [11]. According to the DC gain and bandwidth requirements of the applications they target, amplifiers of different orders have been used. For instance:

- a seventh-order of more than 45 dB DC gain and a f_u of 15 GHz in 65 nm CMOS [1],
- a fifth-order of approximately 49 dB DC gain and a f_u of 6.7 GHz in 28nm CMOS [12],
- a fourth-order with DC gain of 84.3 dB and a f_u of 1.19 GHz in 40 nm CMOS [6],
- a third-order of 30 dB DC gain and a f_u of 8.6 GHz in 28nm CMOS [13], or
- a second-order of 46 dB DC gain and a f_u of 7.8 GHz in 40 nm CMOS [14].

While the design of each of the stages is straight-forward as they are often simple differential pairs, the placement of the poles of each stages is less explored. For a 2nd-order, a detailed mathematical relationship between the poles and the zeros created by the feed-forward path based on a single-pole amplifier model is developed in [3]. For higher orders, equations can be developed, as in [15], that are not rigorous but that can help narrow the design space. With the intuition developed with those equations, the amplification stages can be sized so as the resulting pole and zero

$$A_{mi}(s) = \frac{A_{omi}}{1 + \frac{s}{P_i}}, \quad i = 1, 2, \ldots, n \tag{1}$$

where A_{mi} and A_{omi} are the TF and DC gain of the i^{th}-stage main path amplifier, respectively.

$$A_{fi}(s) = \frac{A_{ofi}}{1 + \frac{s}{P_i}}, \quad i = 2, 3, \ldots, n \tag{2}$$

where A_{fi} and A_{ofi} are the TF and DC gain of the i^{th}-stage feed-forward path amplifier. A_{of1} is equal to zero.

$$TF_{S_n}(s) = \prod_{i=1}^{n} A_{mi}(s) + A_{f2}(s) \prod_{i=3}^{n} A_{mi}(s) + A_{f3}(s) \prod_{i=4}^{n} A_{mi}(s) + \ldots + A_{fn}(s) \tag{3}$$

where S_n is a 3-by-n array containing $\left\{[A_{om1}, \ldots, A_{omn}]; [0, A_{of2}, \ldots, A_{ofn}]; [P_1, \ldots, P_n]\right\}$

locations render a stable multi-stage amplifier. The use of geometric programming to reach optimal designs has also been demonstrated for two-stage miller amplifier [16]. Other works have also employed optimization methods on simpler amplifier circuits [17]. However, the literature is scarce when it comes to sizing of transistors of multi-stage amplifiers targeting high speed ΣΔ-modulators. In this paper, we present a g_m/I_D methodology based data-driven search algorithm for sizing of transistors of a capacitor-less, multi-stage, multi-path feed-forward compensated operational amplifiers. Section II starts with a brief system-level description of a feed-forward-compensated amplifier. This is followed with an overview of the design methodology and a detailed discussion of the main blocks that are part of the search algorithm. The validity of the proposed methodology is further explored by taking an example. Section III presents design examples. A high DC gain fourth-order amplifier targeting a bandpass ΣΔ-modulator with a center frequency of up to 1 GHz is designed in 28nm CMOS FDSOI. This design example is used to compare the response of the sized amplifier with desired transfer function. An additional example, a high unity-gain frequency 3$^{\text{rd}}$-order amplifier, is discussed in section III. The designed examples are compared to similar amplifiers in published works in section IV. The paper is concluded in section V.

II. Description of the Methodology

A FF-compensated amplifier realization in which the amplification stages are arranged in a transversal filter inspired structure can be found in [11]. On the contrary, a realization which enables better sharing of unit amplifiers and which possesses less ambiguity with respect to relative phases of the input and output signals can be found in [3]. A simplified system-level diagram of an n$^{\text{th}}$-order FF-compensated op-amp based on the latter is shown in Figure 1. The main path consists of a cascade of n amplification stages with gain A_{mi} ($i \in 1, 2, 3, \ldots, n$). The feed-forward amplification stages with gain A_{fi} ($i \in 2, 3, \ldots, n$) share an output pole P_i ($i \in 1, 2, 3, \ldots, n$) with corresponding amplification stages of the main path from the second stage. Each pole is defined by the total resistance (R_i) and total capacitance (C_i) at the output of each stage. Assuming the amplifiers at each stage are represented by a single-pole transfer functions as in (1) and (2), the transfer function of the whole amplifier can be formulated as in (3). An n^{th}-order feed-forward compensated amplifier has n poles and $n-1$ zeros. The magnitudes of the zeros are set by the relative weights of the feed-forward and main path amplification stages [3], [15]. It is clear that as the number of stages increases, stabilizing the amplifier through intuitive choice of relative strengths of the amplification stages becomes a tedious work. This is exacerbated by the fact that the equations that define a pole or a feed-forward zero of a multi-stage amplifier contain many variables and are long expressions. For low-pass ΣΔ-modulator applications, the required poles are lower in frequency and can be defined by inserting a large capacitor at the output of each stage [6], [18]. However, for a bandpass modulator, the poles should not be reduced in value by introducing external capacitors as the response is required to reach multi-GHz frequencies. Thus, the poles are likely to be defined by parasitic components at the interface of two amplification stages. Hence, any method of stabilizing the transfer function should take the parasitics of the circuit into consideration.

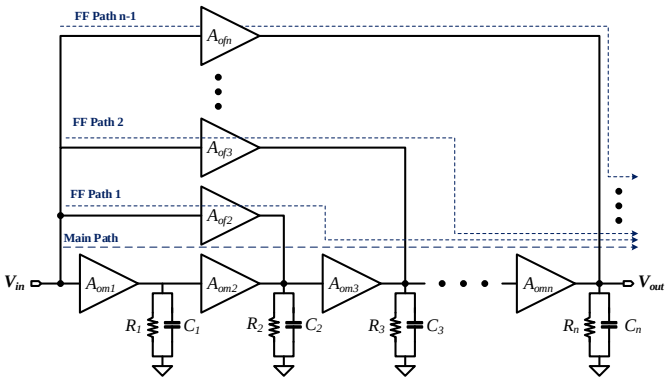


Figure 1: System-level diagram of an n$^{\text{th}}$-order FF-compensated op-amp

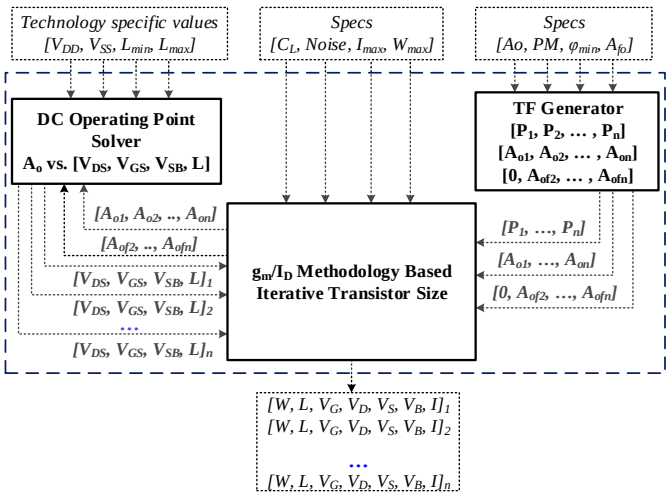


Figure 2: Block diagram of the proposed sizing methodology

A block-diagram of the proposed g_m/i_D-methodology based data-driven search algorithm is shown in Figure 2. It takes as input the specification of the feed-forward amplifier. Depending on the technology selected and the limits put by it, it generates the sizes of the transistors, the current consumption per stage and the body biasing voltages required for each of the transistors. It has three main blocks. In the following sub-section, a description of these blocks is presented without delving into circuit-specific choices.

A. Components of the Proposed Design Methodology

The three main blocks of the system in Figure 2 are the transfer function (TF) data generator, the DC operating point solver and the main part which is the iterative transistor sizing block.

The TF data generator takes as inputs four parameters of the amplifier specification. These are: total desired DC gain (A_o), phase margin (PM), minimum phase (φ_{min}) for frequencies below f_u, and gain at the center frequency of the bandpass ΣΔ-modulator (A_{f_o}). The reason φ_{min} is included, in addition to the PM value, is to guarantee unconditional stability as there are cases where phase responses cross the 180° line and rebound to above 180° at the unity-gain frequency [1]. The fourth input value is required because the selected transfer function should have high gain up to, or even beyond, f_o as is expected from amplifier in a bandpass ΣΔ-modulator [2]. The purpose of this block is, then, to generate a set of transfer functions that meet the afore-mentioned requirements. The generation of the transfer functions is entirely dependent on the input values i.e. no circuit-level information is added to select the transfer functions. It is based on the general transfer function in equation (3). However, once the transfer functions that fulfill the requirements are stored, poles and DC gains for each of the amplifier stages of the n^{th}-order feed-forward compensated amplifier shown in Figure 1 are generated based on a single-pole amplifier model. These pole and DC gain values are eventually passed to the size generator. Circuit information is taken into consideration at this stage. As can be seen in the implementation of this block in algorithm 1, the poles are generated from a limited range of values. The maximum pole value is set by the maximum f_u per stage, which itself is derived from a maximum current consumption per stage, and the capacitive load to be driven by the amplifier. The minimum pole value sets the maximum frequency beyond which the gain of the multi-stage amplifier starts to decrease. Since stable multi-stage amplifiers usually have a steep roll-off factor, depending on the number of stages and the required DC gain, the minimum pole value is set carefully. Unless the desired gain at f_o is equal to the amplifier DC gain, in which case a first-order amplifier could suffice, the minimum pole value is set at a fractional value of the f_o. To increase the number of TF solutions which the algorithm generates, the minimum pole frequency could safely be placed decades smaller than f_o. The downside of such a choice is that large computational time is required before an efficiently sized amplifier is obtained. As the minimum pole value approaches f_o, the target gain at f_o would approach the 3-dB value or the choices would be limited and the algorithm would take longer to arrive at a solution. Taking a 4$^{\text{th}}$-order amplifier with a DC gain of 60 dB as an example, if the desired gain at f_o is 20 dB, the minimum pole should not be higher than $f_o/10$ as the amplifier's gain response is less likely to fall more than -40 dB/dec. The other concern in setting the minimum pole value is the computation time required to generate the transfer functions. It can be defined in conjunction with the maximum DC gain for an operation in a constant unity-gain frequency i.e. if f_u of each stage is fixed, then the minimum pole value is f_u divided by the maximum DC gain. For the DC gains, the maximum value is set as a function of many variables: area, maximum current and linearity among others. The first term in equation (3) makes the biggest part of the DC gain. Hence, a typical value of DC gain for each stage can be obtained by dividing the total desired DC gain by the number of stage of the amplifier.

Algorithm 1 TF generation for n-stage amplifier

Input values: $A_{o_min}, PM, \varphi_{min}, A_{f_o}$
Output values: A_{om}, A_{of}, P_1
A_{om_vec}: a set of possible main-path DC gains
A_{of_vec}: a set of possible feed-forward DC gains
P_{1_vec}: a set of poles for each stage
DEFINE $NumSim = ({}^{A_{om_vec}}P_n)({}^{A_{of_vec}}P_n)({}^{P_{1_vec}}P_n)$
function TransferFunction($A_{om_vec}, A_{of_vec}, P_{1_vec}$)
    S_3 = GenerateTuples($A_{om_vec}, A_{of_vec}, P_{1_vec}$)
    while i ≤ $NumSim$ **do**
        Build $TF_{S_{3_i}}$ for $S_3(i)$ using (3)
        Calculate PM_i, φ_{min_i}, A_{o_i}, $A_{f_o_i}$ of $TF_{S_{3_i}}$
        if $A_{o_i} \geq A_{o_min} \wedge PM_i \geq PM \wedge$
            $\varphi_{min_i} \geq \varphi_{min} \quad \wedge A_{f_o_i} \geq A_{f_o}$ **then**
            save $TF_{S_{3_i}}$ as TF_{soln}
        end if
        increment i
    end while
    return A_{om_soln}, A_{of_soln}, and P_{1_soln}
end function
function GenerateTuples($A_{om_vec}, A_{of_vec}, P_{1_vec}$)
    S_{n_Aom} is a set of all n-permutations of A_{om_vec}
    S_{n_Aof} is a set of all n-permutations of A_{of_vec}
    S_{n_P} is a set of all n-permutations of P_{1_vec}
    S is the structure containing all groups of: $\{S_{n_Aom}, S_{n_Aof}, S_{n_P}\}$
    $S_3(i)$ is the i^{th}-member of 3-permutations of S
    return S_3
end function

As its name suggests, the main objective of the DC solver block is to find a DC operating point of the transistors of each of the amplification stages in the multi-stage amplifier such that a desired DC gain can be realized. Each transistor in any of the amplification circuits is biased in a DC operating region which is defined in terms of $V_{GS}, V_{DS}, V_{SB}, and\ L$ values. This is based on the fact that the DC gain of a single amplification stage (either A_{mi} or A_{fi}) can be expressed as a ratio of $(g_m/I_d)_{mi/fi}$ and $(g_{ds}/I_d)_{mi} + (g_{ds}/I_d)_{fi}$. These ratios can in turn be extracted from a pre-computed lookup table containing the

above-mentioned four DC values [2], [19], [21]. As long as these DC values are the equal, the DC gain value for the new transistor is guaranteed to be equal to that of the reference transistor regardless of the relative difference between the drain-to-source current (or the width) of new transistor and the reference transistor. While computing the gain in such a simplified expression may not always be accurate for all types of amplifier topologies, it holds in this case as the circuits that are used to realize the amplification stages are simple structures composed of basic differential amplifiers [22]. Owing to this practical assumption, a brute-force search on the four DC points of each transistor can give a list of all possible DC gain values, but it would generally render the method inefficient and would be at the detriment of resources as it needs long simulation time especially when the design space is wide. To speed up the DC solver, the search algorithm for each transistor and for the whole circuit is constrained. With respect to the multi-stage amplifier, each amplification stage is constrained using:

- technology-dependent values e.g. $VDD, VSS, L_{min}, L_{max}$ and values of $V_{GS/GD/GB/SD/SB/BD}$ according to the safe operating area
- system-level circuit constraints e.g. input and output common-mode voltages.

Moreover, the DC operating point solver part of the algorithm is constrained for each transistor within a narrow area of operating points defined by:

- overdrive voltage (VOV) = gate-to-source voltage (V_{GS}) - threshold voltage (V_T)
- saturation margin (V_{DSmarg}) = drain-to-source voltage (V_{DS}) - saturation voltage (V_{DSAT})
- input peak-to-peak voltage and
- output voltage swing.

The VOV and V_{DSmarg} are selected to ensure that the transistors are in active region while the input peak-to-peak voltage helps control the input-referred noise-limited signal-to-noise ratio (SNR) of the amplifier.

The third and main block is the iterative transistor size generator. A simplified structure of the block is shown in Algorithm 2. It takes the gain-bandwidth product values of each amplification stage, as defined by the pole and DC gain of the stages, from the TF data generator and uses it to size the g_m values of the transistors of each amplification stage at the operating point corresponding to the DC gain as defined by the DC data generator corresponding to the DC gain values. Since the amplification stages are modeled with a single-pole transfer function, their gain-bandwidth product is also their unity-gain frequency. The sizing is started from the last stage as the output load is known. Self-loading are taken into consideration using iterative method as illustrated in [2], [21]. The total capacitive load at the output of each amplification stage is defined by the self-loading capacitors plus the input load, mainly C_{gg}, of the subsequent stage. Initially the self-loading capacitors are assumed zero. Using the estimated g_m and the g_m/I_d values, which is derived from the DC operating point, the drain current is calculated. Afterwards, the width is estimated for a current density value defined by the DC operating point of each transistor [2]. The self-loading capacitors are updated with the new width value. Then the width is iteratively approximated to a final value after having calculated new values of self-loading capacitors with the the previous width value. The final sizes are returned based on additional requirements such as maximum width value, maximum current and noise.

The iterative transistor size generator has the least impact on the speed of the methodology. As long as pole and gain values of each stage are generated by the TF generator and their corresponding DC parameters are obtained from the DC solver, the speed of this last block depends only on the maximum width, maximum current and noise values set at the end of the algorithm. The compromise in this last block of the methodology is whether the designer accepts the maximum width in the generated solution or launches another run in search of new smaller width value.

Important to the DC and size generators is the data from which the transistor operating point parameters are extracted. These DC data are the basis for the g_m/I_D-methodology utilized in this paper. Briefly, a transistor operating point information (such as: drain current, intrinsic capacitors, drain-source conductance, thermal and flicker noise) are tabulated in a four dimensional array by simulating the transistor for a range of V_{GS}, V_{DS}, V_{SB}, and L values and at a specific width. Based on these information, different set of ratios e.g. g_m/I_d, current density (j_n or j_p) or g_{ds}/I_d are extracted or the operating information are extrapolated at a new combination of V_{GS}, V_{DS}, V_{SB}, and L values [21]. The results presented in this paper are based on simulation data of a 10 μm width 28nm CMOS FDSOI regular threshold voltage (RVT) and low threshold voltage (LVT) transistors at different process and temperature corners. Normally, sizing is carried out at a single corner. To reduce effects of process variation on the designed circuit, two methods could be followed. The first one is to design the circuit for the worst process corner. The problem with this approach is that it tends to give the most pessimistic estimation. The more realistic approach is–the second approach–to design a circuit in a typical process corner but with some tolerance on key parameters. The second approach is also in line with the nature of the proposed methodology as the algorithm tends to generate multiple solutions.

Even though the presented methodology can be improved to take into account layout dependent interconnect parasitic capacitances, for reasons mentioned hereafter they are not included in the algorithms. As is known, the size and number of interconnect parasitic capacitances are dependent on the design rule book of a specific foundry and the technology it provides. They are also highly dependent on the skill and experience of the designer who does the layout. Given these facts, it is more objective to present the methodology for the design of a circuit with only model generated parasitic capacitance take into account and, perhaps, a representation of a few interconnect parasitic capacitances at critical nodes. For these reasons, the presented algorithms take into account only parasitic capacitances predicted by the CEA-Leti UTSOI2.1 transistor model [23], [24].

Regardless of the afore-mentioned reasons, there is a possi-

Algorithm 2 Iterative multi-stage amplifier sizing

1: Input values: C_L, $Noise_{max}$, I_{max}, W_{max}
2: Output values: $[W, L, V_{GS}, V_{DS}, V_{SB}, I]$
3: S_{DC_soln}: a set parameters passed from the DC solver $\left\{V_{GS_soln}, V_{DS_soln}, V_{SB_soln}, L_{soln}\right\}$
4: S_{TF_soln}: a set parameters passed from the transfer function generation block $\left\{[A_{om1_soln}, \ldots, A_{omn_soln}];\ [0, A_{of2_soln}, \ldots, A_{ofn_soln}];\ [P_{11_soln}, \ldots, P_{1n_soln}]\right\}$
5: S_{fu_soln}: f_u of each amplification stage $\left\{2\pi A_{om1_soln} P_{11_soln}, \ldots, 2\pi A_{omn_soln} P_{1n_soln}\right\}$
6: **function** IterativeSizing(S_{TF_soln}, S_{DC_soln})
7: **for** each passed TF **do**
8: $[W_n, L_n, V_{GS_n}, V_{DS_n}, V_{SB_n}, I_n, C_{in_n}]$=
9: SizeStage(S_{TF_soln}, S_{DC_soln}, C_L)
10: $C_{L_stage} = C_{in}$
11: $[W_{n-1}, L_{n-1}, V_{GS_n-1}, V_{DS_n-1}, V_{SB_n-1}, I_{n-1}, C_{in_n-1}]$=
12: SizeStage($S_{TF_soln}, S_{DC_soln}, C_{L_stage}$)
13: Call SizeStage for stages: $n-2, \ldots, 1$
14: S_W is a set of widths: $\{W_n, \ldots, W_1\}$
15: S_I is a set of currents: $\{I_n, \ldots, I_1\}$
16: Estimate input-referred thermal noise
17: **if** $\max(S_W) \leq W_{max} \wedge \max(S_I) \leq I_{max}$
18: $\wedge$ input noise $\leq Noise_{max}$ **then**
19: Save sizes, current, bias voltages
20: **end if**
21: **end for**
22: **return** $[W, L, V_{GS}, V_{DS}, V_{SB}, I]_{saved}$
23: **end function**
24: **procedure** SizeStage(S_{TF_soln}, S_{DC_soln}, C_{L_stage})
25: **while** q $\leq$ *NumLoop* **do**
26: **if** q ≥ 2 **then**
27: Update C_{L_stage} with non-zero value of C_{dd}
28: **end if**
29: calculate j_n, j_p and g_m/I_d
30: estimate g_m using f_u and C_{L_stage}
31: find current using g_m and g_m/I_d
32: size transistors widths using j_n, j_p and current
33: estimate C_{gg} and C_{dd} using lookup table and W
34: increment q
35: **end while**
36: **return** $[W, L, V_{GS}, V_{DS}, V_{SB}, I, C_{gg}]$
37: **end procedure**

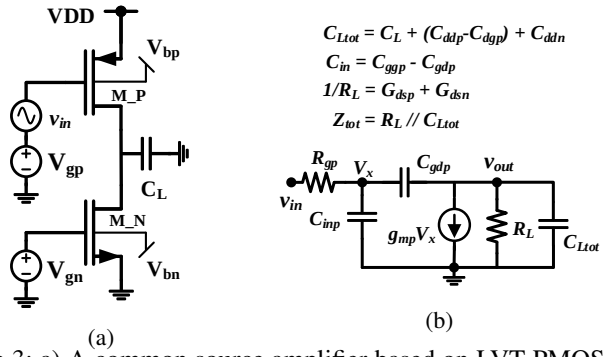
bility to improve the algorithms so that interconnect parasitic capacitances would be considered. The metal wires used to route the input and output signals of the amplifiers run along the dimensions of the transistors. If the transistors are divided into multiple fingers, the length of the wires would directly be affected by the length of the transistor and the number of fingers. A metal-to-substrate capacitance estimation, based on a specific metal interconnect of a given technology and dependent on the dimensions of the transistor, can be carried out and added to the total capacitive load of an amplification stage. This can be accomplished, for instance, in line 33 of Algorithm 2. Since such an estimated value is expected to be much smaller than the other parasitic values, its effect on the convergence of the procedure at the end of Algorithm 2 is negligible. However, it also does not mean that once the transistors are sized in this manner, the parasitic capacitance would be the same as predicted by the algorithm for reasons mentioned in the above paragraph.

B. Validity of the proposed methodology

The strength of the g_m/I_d methodology is that it takes into account short-channel effects. Since the transistors are sized based on values extracted from current advanced transistor models, these effects are inherently taken care of. For example, in a simplified transistor model, the current is assumed to be constant in saturation region even as the drain voltage increases beyond the V_{DSAT} value. This assumption fails to work in short-channel devices as the amount of drain-to-source current varies with the value of the drain voltage due to an effect termed as drain-induced barrier lowering (DIBL). To make the proposed methodology relevant for short-channel devices,the drain voltage needs to be considered. One of the strengths of the afore-mentioned g_m/I_d methodology is, then, that the sizing of the transistors is dependent on all terminal voltages, which includes V_{DS}, of the transistors and its length [21]. Other effects such as gate-induced drain leakage (GIDL) are more interesting in sub-threshold operation of the transistor or in applications where the value of the leakage current is a key metric.

One of the drawbacks of the proposed sizing methodology is that it relies on a single-pole approximation of the frequency response of the amplifiers. Whereas such a model can adequately approximate amplifiers at sub-GHz unity-gain frequencies for the reason that the gain of an amplification block in feed-forward-compensated amplifier is so small that f_u is nearly a decade away from the dominant pole. As f_u increases, however, even amplifiers with simple topologies deviate from the model due to the effects of non-dominant poles and zeros. Owing to this limitation, some adjustments are made to increase the effectiveness of this methodology. To explain these corrective measures, an example is taken. The circuit in Figure 3a depicts a single-stage common-source (CS) amplifier with a PMOS LVT input transistor and an NMOS RVT active load transistor and Figure 3b is its small-signal equivalent (SSE) circuit based on a general high frequency transistor model [25]. It should be noted that the following discussion on the frequency response of the single-ended CS amplifier can be safely adopted to explain similar issues in the differential amplifier since a half-circuit equivalent of a typical diff-pair is identical to the SSE circuit in Figure 3b.

The SSE model does not include the source and drain parasitic access resistances because their effect at the frequency of interest can be minimized using layout methods and they are not taken into account. Since the body of *M_P* is at the same AC-potential as its source, the intrinsic gate-to-source (C_{gs}) and gate-to-body (C_{gb}) capacitances are summed into the input capacitance. Having combined the drain-to-source conductances of the PMOS and NMOS transistors (g_{dsp} and g_{dsn}) into R_L, the two poles and a right-hand-side (RHS) zero



(a) (b)

Figure 3: a) A common source amplifier based on LVT PMOS and RVT NMOS, and b) its small-signal equivalent circuit

$$P_1 \approx \begin{cases} \dfrac{-1}{R_{gp}}\left[C_{inp} + C_{gdp}\left(1 + Z_{tot}\left(g_{mp} + \dfrac{1}{R_{gp}}\right)\right)\right], & \text{if } R_{gp} > 0 \\ -\dfrac{1}{R_L(C_{Ltot} + C_{dgp})}, & \text{if } R_{gp} \approx 0 \end{cases} \tag{4}$$

$$P_2 \approx \begin{cases} -\left[\dfrac{1}{Z_{tot}}\left(\dfrac{1}{C_{inp}} + \dfrac{1}{C_{gdp}}\right) + \dfrac{1}{R_{gp}C_{inp}} + \dfrac{g_{mp}}{C_{inp}}\right], & \text{if } R_{gp} > 0 \\ 0, & \text{if } R_{gp} \approx 0 \end{cases} \tag{5}$$

$$Z_{RHS} = \frac{g_{mp}}{C_{gdp}} \tag{6}$$

of this circuit can be derived to be as equations (4), (5) and (6), respectively [26].

1) Effect of Non-dominant Pole: The second pole appears because of the parasitic access resistance of the gate. Normally, this resistance can be combined with the source resistance of the input voltage and be dealt with on a higher level. For example, if the amplifier is part of an integrator or a resonator, R_{gp} would be used to define the input referred noise or to calculate the corner/center frequency of the integrator or resonator (together with the feedback capacitance). In the designed multi-stage amplifiers (in section IV), its value is significant only at the input of the first amplification block. Furthermore, as can be deduced from equation (5), this pole lies beyond the transit frequency (f_T) of the transistor (simplified approximation locates it at ($g_{mp}/(2\pi C_{gg})$). If an amplifier's f_u is less than the transistor f_T, the influence of the non-dominant pole on the frequency response is minimal. Nevertheless, the possibility of both the non-dominant pole and the zero being located near each other beyond the f_T value is significant. The rule of thumb is to choose the phase margin of the multi-stage amplifier with a tolerance enough to accommodate the combined effect of the RHS zero and the second pole on frequencies beyond the unity-gain frequency. Consequently, transfer functions with a decreasing phase response near the unity-gain frequency of the multi-stage amplifier are more likely to drop their phase margin than those whose phase response curve rises or plateaued near f_u.

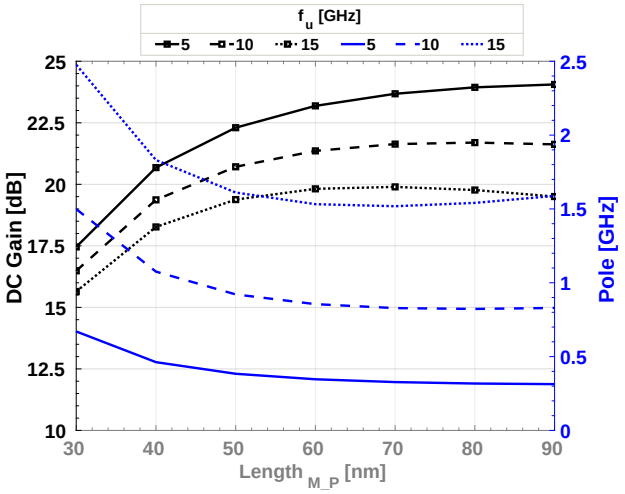


Figure 4: Gain and dominant pole of the CS amplifier as length of the input PMOS transistor changes while the ratio of RHS zero to f_u is held constant at 10. Square markers are for DC gain plots.

2) Effect of RHS Zero: The RHS zero does not depend on the value of the extrinsic gate, source, or drain access resistances. It is created by the gate-to-drain overlap capacitance. Its effect on the transfer function is detrimental as it raises the gain by 20 dB/dec starting at its frequency value while it adds -90° to the phase response starting at one-tenth of its value. To minimize its effect on the single-pole model of the amplifier, it is noted that the circuit should be designed so that the zero is located at ten times the unity-gain frequency of the amplifier.

To explore the possibility of placing the RHS zero at ten times f_u and the associated power consumption budget and the required transistor sizes, the CS amplifier is designed for a constant unity-gain frequency and a corresponding constant RHS zero value. Briefly, the setup can be described as follows: the load capacitance has a value equal to the load the multi-stage amplifier (in section IV) would drive i.e. 500 fF, V_{DS} is held at half of the VDD value and the length of the PMOS input is varied. The load transistor has a constant g_m/I_D value of ten. Lower values g_m/I_D deliver high speed operation in strong-inversion so long as the drain-to-source voltage is kept above the overdrive voltage. The reason a value of a ten is selected is that the high speed signal of the feed-forward path of the multi-stage amplifiers (in section IV) would be carried by the NMOS transistors and this value leaves enough room for the output voltage to drop while guaranteeing the transistor is in saturation. The result of the design for a minimum NMOS length and for three different f_u values is discussed in the following paragraph.

The gain and dominant pole values are plotted in Figure 4 for unity-gain frequencies of 5, 10 and 15 GHz. To minimize current consumption and corresponding transistor sizes, a minimum length is selected for the load transistor. It can be ascertained from the graph that the unity-gain-frequency stays constant for different lengths of the input PMOS transistor. The pole increases as f_u increases. As expected, the gain improves

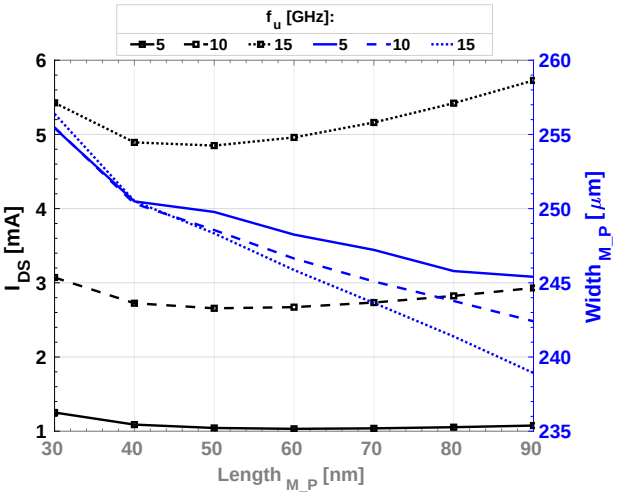


Figure 5: Current and width of the input PMOS transistor at constant RHS zero to f_u ratio of 10. Square markers are for I_{DS} plots.

by few dBs as the input transistor length is increased. The second plot in Figure 5 shows current consumption and width of the input transistor. To reach higher unity-gain frequencies without proportional increase in the gate-to-drain overlap capacitance, the current is increased using the overdrive voltage rather than the width of the transistor. That is the reason the width falls slightly as the length increases. The same behavior could be seen in Figure 4 with the slight bending of the gain.

For the proposed methodology to be effective, the unity-gain frequency of the multi-stage amplifier should not be more than the f_u values at which each amplification block is defined. The assumption is that if the influence of the unaccounted RHS zero and second pole is negligible at the f_u values of each amplification stage, their combined effect on the multi-stage feed-forward compensated amplifier should equally be small as long as the f_u is kept within range. The DC gain and pole values of Figure 4 are taken as limits in the TF generation block. The width and current values in Figure 5 also help to set the maximum dimension sizes at which a transfer function is accepted by the algorithm. The maximum DC gain limit could be increased by selecting a longer load transistor, but the maximum width limit would also have to be raised.

III. Design Examples

To validate the methodology, a 4th-order and a 3rd-order amplifiers are designed in 28nm CMOS FDSOI. Since the amplifiers are required to be unconditionally stable, higher orders were not chosen. The 4th-order is designed strictly using the methodology explained so far and the results that will be shown in the next subsection are based on Cadence Spectre simulation of the sizes generated by the algorithm without any significant tweaking. High DC gains value were the requirement for the 4th-order amplifier. The 3rd-order pushes the limits on the unity-gain-frequency discussed in the previous section. Hence, the sizes that are generated with the algorithm have been tweaked slightly to correct for discrepancies (discussed in this section). After tweaking, the number of fingers of the transistors and in some cases the size of the PMOS transistors are adjusted so that the current consumption and the DC voltages remain the same as those generated by the algorithm.

A. A 4th-Order Amplifier with A_o = 73.5 dB

The main AC and DC requirements for which the 4th-order amplifier is designed for are listed below:

- $A_o \geq$ 60 dB
- $\varphi_{min} \geq$ -160°
- $PM \geq$ 45°
- $A@1GHz \geq$ 30 dB
- $VOV \geq$ 70 mV
- $V_{DS\,marg} \geq$ 50 mV

The values for gain, phase and load capacitance were derived from the requirements of a flexible bandpass delta-sigma modulator which has a sampling frequency ranging from 1 GHz to 4 GHz. The DC parameters are chosen as they are practical minimum values that ensure the transistors' operation in saturation region.

Based on these requirements, transfer functions are generated. A small sample of the generated TFs is plotted in Figure 6. All of them fulfill the requirements, for instance, it can be observed that they intersect at the 1 GHz line to meet the 30 dB minimum value. The iterative sizing algorithm reads these TFs one by one and generates sizes until the limit on maximum width and noise are fulfilled.

To realize the design, the circuit in Figure 7 is chosen for its simplicity and modularity. The basic block in each stage of the circuit is a pseudo-differential current re-use amplifier [22]. The half-circuit small-signal equivalent of this basic amplifier block is similar to that of the CS amplifier in Figure 3. Unlike bulk CMOS technologies, the 28nm FDSOI can be biased with a wide range of voltages at its body. Thus, output common-mode variation can be detected using an amplifier or a passive network and the correction voltage can be fed back to the amplifier through the body terminal of the the NMOS tail transistor; and this is the reason no CMFB provisions are made in the AC-carrying parts of the diff-pair [27]. Each amplifier

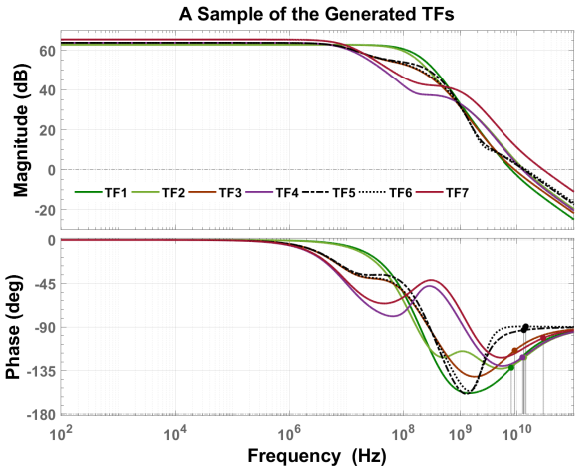


Figure 6: A sample of the generated TFs for the specification of the 4th-order amplifier. Depending on the range of gains and poles chosen, thousands of TFs could be generated.

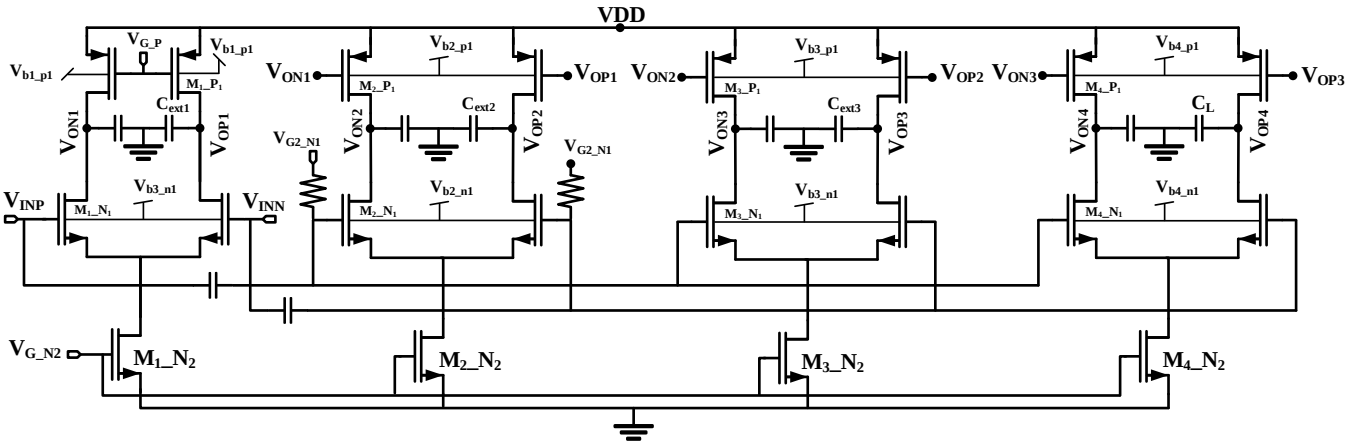


Figure 7: The 4th-order FF-compensated op-amp. External capacitors are added to account for interconnection parasitic capacitors

Table I: Sizing of the transistors of the 4th-order amplifier

	1st-stage	2nd-stage	3rd-stage	4th-stage
$W_{M_P_1}$ [μm]	1.68	86.51	445.47	302.01
L_{M_P1} [nm]	30	45		
$W_{M_N_1}$ [μm]	0.56	5.41	27.86	18.89
L_{M_N1} [nm]	30			
$W_{M_N_2}$ [μm]	1.73	23.23	119.63	81.10
L_{M_N2} [nm]	120			
I_d [mA]	0.04	0.51	2.52	1.72

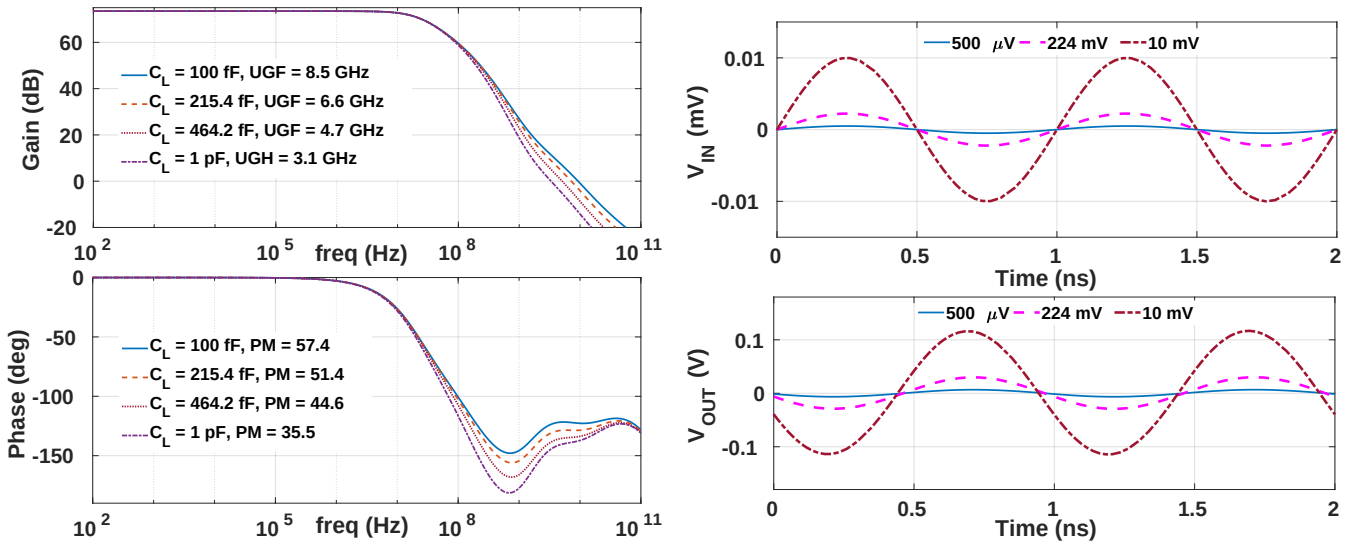
stage has an additional capacitive load to account for parasitics resulting from interconnects during layout.

The main path signals are carried by LVT PMOS transistors and the feed-forward signals pass through RVT NMOS transistors. These choices enable the output voltages of each stage to drive the next stage input transistor without the need for additional DC biasing circuit. Besides, the PMOS transistors are capable of amplifying the signals by the moderate gains expected at each stage whereas the NMOS transistors could achieve higher speeds in the feed-forward paths.

Both the LVT PMOS and RVT NMOS are created in a p-Well—albeit in different layout blocks owning to separation distance imposed by design rules. Naturally, their bodies are biased by the lowest voltage level in the circuit. In other words, the LVT PMOS and RVT NMOS are more likely to require the same body bias voltages than an RVT PMOS and an RVT NMOS. The additional benefit of the selected topology is then the required number of body bias voltages that has to be generated using a reference circuit could be minimized by fixing the bias voltages of the two transistors in advance to be the same. This advantage is less likely to materialize if the two transistors were of the same flavor.

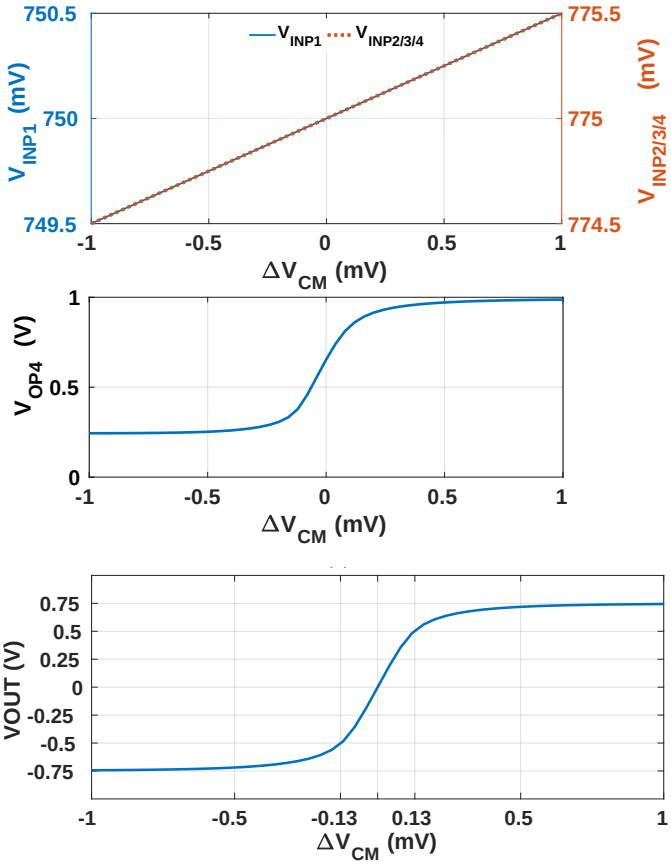
The algorithm prioritizes solutions which require minimum number of distinct body-bias voltages. In this design, all the body-bias voltages of the PMOS transistors are equal to zero likewise the bodies of the NMOS transistors are biased at zero volt. This result allows for a special advantage of creating both the NMOS and PMOS transistors in the same p-well block as illustrated in [28]. The feed-forward path NMOS transistors starting from the second stage requires an input bias voltage slightly higher than those of the first stage NMOS transistors. The detailed sizing and consumption of the amplifier is in Table I. The PMOS transistors sizes have the largest spread. The third stage consumes the highest current at 2.52 mA and has the transistor with the maximum width—at 445.47 μm. There is uniformity in the lengths generated as most similar types of transistor have equal lengths. The sized amplifier is simulated using latest version of the Cadence Spectre circuit simulator. Since the target application is a high speed bandpass modulator, the thermal noise generated by the transistors dominates the noise contribution of the amplifier. The input-referred thermal noise of the 4th-order amplifier is 13.5 $nV/sqrt(Hz)$. The sized amplifier consumes a total of 4.78 μA from a voltage supply of $1V$.

The small signal and large signal performances of the circuit are verified using DC, AC and transient simulations. The small-signal magnitude and phase responses for capacitive loads ranging from 100 fF to 1 pF are plotted in Figure 8a. The circuit achieves a DC gain of 73.5 dB and maintains a gain of at least 20 dB at 1 GHz. The UGF drops from 8.5 GHz to 3.1 GHz for an order of magnitude increases in the load. The stability of the circuit falls below the targeted phase margin value of 45° when the capacitive load is changed by twofold from its expected value. In Figure 9, the differential input DC is varied by up to ±1 mV around the common mode DC values of 750 mv for the first stage and 775 mV for the remaining stages. In Figure 9a, only the positive single-ended input and output signals are shown. The differential output swings from -750 mV to 750 mV. From Figure 9a, it can be observed that the positive output signal approaches the supply value of 1 V when increasing, but is limited to around 250 mV when decreasing due to the headroom required to bias the tail transistor. The circuit is linear for close to ±500 mV of the differential output swing. Since the DC gain is 73.5 dB, this linear operation is only achieved for a small range of only up to ±130 μV input magnitudes. Nevertheless, the input ranges increases as the frequency of operation changes. Since the targeted application for this type of circuit is in bandpass ΣΔ-modulators, it is also interesting to know how the circuit responds to large magnitude high frequency input signals. Figure 8b shows the output response as the differential



(a) (b)

Figure 8: a) Effect of load variation on the frequency response of the 4th-order amplifier, b) transient response of the 4th-order amplifier to a sinusoidal 1 GHz input signal



(b)

Figure 9: The 4th-order amplifier DC output swing: a) single-ended input and output, b) differential output signal

magnitude of a 1 GHz sinusoidal input is increased beyond μV ranges. Since the gain is expected to be smaller at higher frequency, it can be noticed that the circuit operates linearly even at an input signal of 10 mV. As predicted by the phase response of the circuit, the input and output signal experience a phase-shift of close to 180°.

B. Discrepancy Between Algorithm and Spice

The frequency response of the designed amplifier is compared to the TF generated by the algorithm. The plots are shown in Figure 10. The amplifier achieves a higher DC gain at 73.5 dB, but it falls below the gain of the transfer function from the generator as frequency increases. For example, the generated TF achieves a gain of 54 dB at 250 MHz whereas the simulated amplifier has a gain of 49 dB at the same frequency. The Spice simulated amplifier and the TF generated response achieve a phase margin of approximately 44° and 48°, respectively. Although the responses of the sized amplifier and the TF from the generator have similar curvatures, they differ in some important points.

There are discrepancies between the original transfer function and the response of the sized amplifier when targeting multi-GHz unity-gain frequencies. As the purpose of the methodology is to simplify design at high frequencies, it is important to discuss the causes of these differences so that a more accurate result could be obtained. The main causes of the discrepancies are presented as follows:

1) Small Width Errors: The g_m/I_D methodology calculates the size of a transistor based on DC-based current density factor and the drain-to-source current of the transistor which, in turn, is estimated based on the AC-defined transconductance value and DC-defined g_m/I_D. It takes the assumption that behavior of a transistor and parameters such as g_m/I_D, g_m/g_{ds}, g_m/C_{gg} could be predicted from a reference size transistor as long as both are placed in identical DC operating points. This assumption holds when the new transistor can be partitioned into many versions of the reference transistor i.e. when the new transistor is bigger in size. However, for a transistor whose width is smaller than that of the reference transistor, the predictability is limited as the errors between computed parameters is high [21]. Even though large transistor sizes are

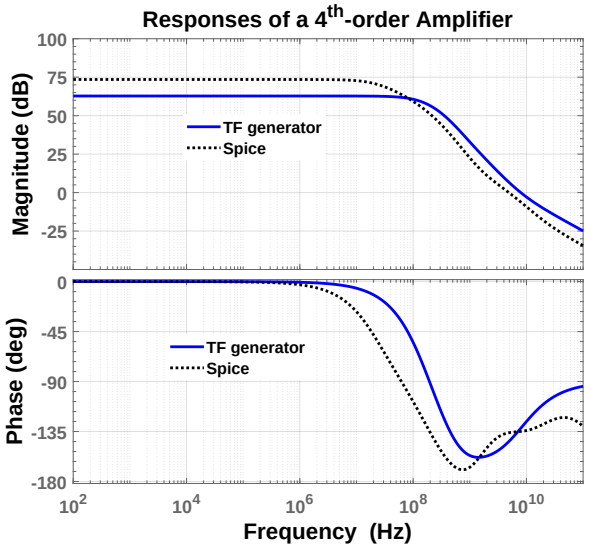


Figure 10: Gain and phase responses of the 4th-order amplifier. The solid blue lines are from by the TF generator part of the algorithm and the dotted black lines are the spice simulation results of the sized amplifier.

the norm in multi-stage amplifiers, there are cases where the algorithm has to rely on smaller feature sizes to achieve the requirements. Such scenario results in discrepancy between the simulated behavior of a sized amplifier and the original transfer function.

As a remedy to this problem, a minimum width limit could be introduced into the algorithm. The only drawback is that it would require longer simulation time to shuffle through the generated transfer functions and arrive at an acceptable solution. Nonetheless, it a compromise worth considering.

2) Fractional Width Ratios: One of the main drawbacks of the proposed methodology stems from the fact that the algorithm only generates widths whose ratio against the reference width is fractional. Besides, the finger length and multiplicity factor are assumed to be unity. As the transistor are large, they have to be divided for layout without changing the behavior of the circuit. That is why once the size of the transistor is estimated by the algorithm, it is divided into an approximate integer multiple of the reference finger width. Normally, the circuit changes slightly as the DC behavior does not always follow exactly that of the reference transistor.

To regain the desired DC operating point, parametric simulation based on the number of fingers and multiplicity of the transistor would be required. In the given example, the DC point is re-calibrated to that predicted by the algorithm using the predicted drain-to-source current as verification parameter. A constraint related to the above discussion, against which the 4th-order and 3rd-order amplifiers had to be designed, is that transistors in the 28nm CMOS FDSOI have a maximum finger width limit due to self-heating associated with the buried oxide. This limitation is taken as an upper bound on the finger width of the transistors.

3) Deviations near f_u: The effect of non-dominant pole and RHS zero is already discussed in section II and recommendations are suggested to mitigate the discrepancy caused by this. One solution that seems obvious looking at the sample transfer functions in Figure 6 and which readers may pose is: why TFs with a PM around 90° are not prioritized? The reason is that the algorithm does not always resolves these types of transfer functions within the acceptable range of current and width values. As indicated in section II, the best TF are the ones with rising phase responses.

4) Precision of DC Operating Point Solver: The DC operating point solver chooses DC bias points depending on the main path and feed-forward gains values of each of the stages. Unless a large DC database is used, the A_{om} and A_{of} values are usually approximated. The algorithm uses two parameter when comparing DC gains in the DC solver block. For instance, let A_{o_in} be DC gain which is input to the block and let A_{o_cal} be the DC gain which is taken from the database to be compared (or which can also be calculated in real time from the input DC voltages). A simple comparison would require A_{o_cal} to be rounded to a known decimal point, *dec_pt*, and be accepted to be equal to A_{o_in} with some tolerance of *gain_tol*. The value of the tolerance is usually dependent on the magnitude of the required input DC value. The same tolerance would not be used if an amplification stage is required to have a small gain, say 5 dB, and a large gain, say 25 dB. These two parameters (*dec_pt* and *gain_tol*) directly affect the speed of the simulation. For a more conservative estimate, the values of these two parameters are set tighter and the number of viable solutions that the algorithm ends up finding would be less. If they are set more liberally, there would be more solutions. The transfer function of the circuit whose transistors are sized from the solutions generated using the latter case would match less precisely to the intended transfer function. This causes discrepancies which can partly be reduced by tweaking the dimensions of the sized transistor using SPICE-like transistor-level simulators. Generally, the precision with which the gain values are defined has a direct impact on the simulation duration of the algorithm.

C. A 3rd-Order Amplifier with f_u = 14.7GHz

The transfer functions to which the 3rd-order amplifier is sized are generated for the same specifications as those of the 4th-order amplifier in the previous example. The exceptions are the DC gain, which is lowered to 50 dB, and the minimum phase, which is improved to -150°. The limits on the DC gain and pole frequency are taken from the results in section II. Naturally, many amplifiers with different sizes were generated

Table II: Sizing of the transistors of the 3rd-order amplifier

	1st-stage	2nd-stage	3rd-stage
$W_{M_P_1}$ [μm]	0.82	59.5	138
L_{M_P1} [nm]	30	40	30
$W_{M_N_1}$ [μm]	0.4	57.8	343.7
L_{M_N1} [nm]	30	50	
$W_{M_N_2}$ [μm]	0.9	38.5	228.9
L_{M_N2} [nm]	120		
I_{tot} [mA]	5.623		

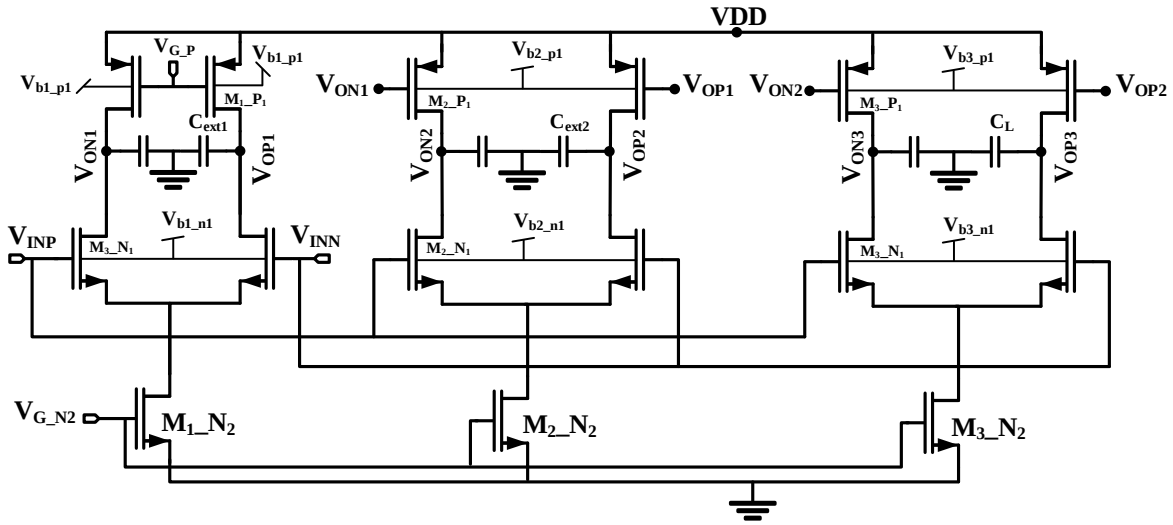
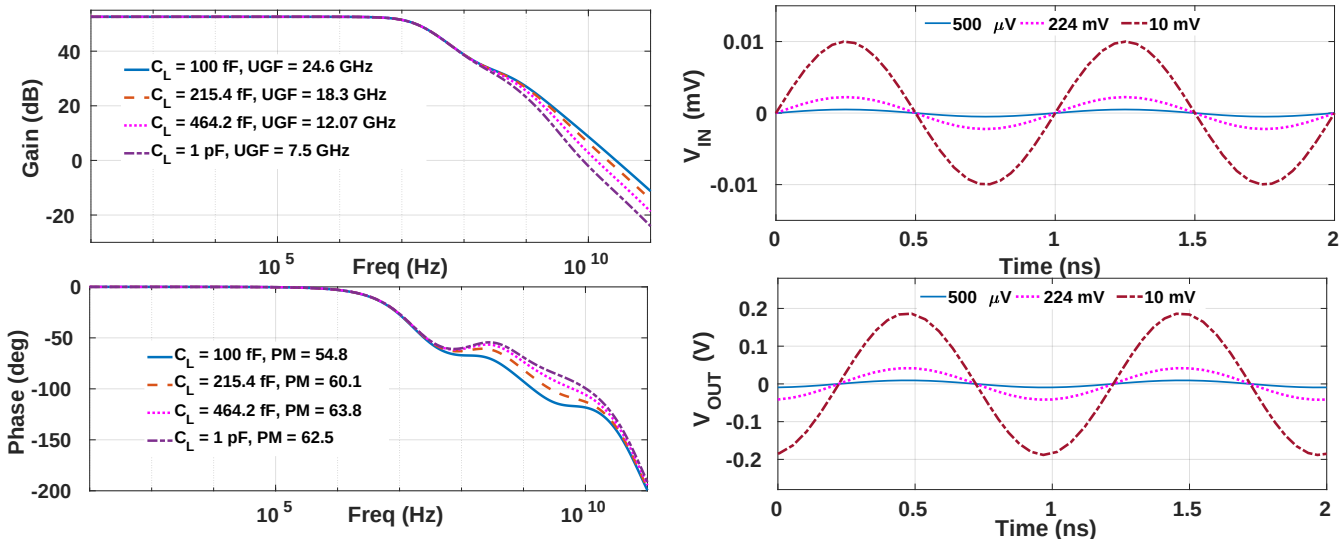
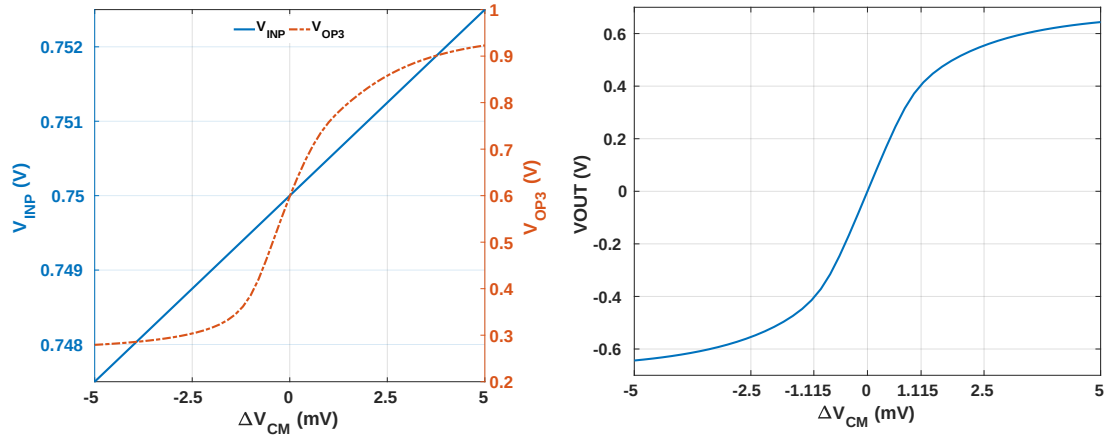


Figure 11: The 3rd-order FF-compensated op-amp. Additional external capacitors were considered in the algorithm to compensate for layout generated interconnect parasitic capacitors.



(a) (b)

Figure 12: a) Effect of load variation on the frequency response of the 3rd-order amplifier, b) transient response of the 3rd-order amplifier to a sinusoidal 1 GHz input signal



(a) (b)

Figure 13: The 3rd-order amplifier DC output swing: a) single-ended input and output, b) differential output signal

Table III: Comparison of the designed examples with multi-stage amplifiers featured in ΣΔ modulators. The tabulated values are obtained from the referenced papers.

REF.	Simulation Results	Order	Gain [dB]				f_u	Power Supply	Power	Process
			DC	250MHz	1GHz	2GHz	[GHz]	[V]	[mW]	[nm]
[1]	pre-layout	5th	70	60	19 ‡	8 ‡	6	1.0/±2.5	100	65
[7]	pre-layout	4th	73	27 ‡	15 ‡	6 ‡	3 ‡	1.25	2	65
[15]	pre-layout	4th	59.6	50	28	167	7	1.2	10	65
[6]	post-layout	4th	84.3	26 ‡	5 ‡	–	1.19	1.1	10.8	40
[2] §		**4th**	**52.4**	**54**	**35**	**23**	**11**	**1.2**	**23**	**65**
This	**pre-layout**	**4th**	**73.5**	**47.8**	**22.6**	**11**	**4.9**	**1.0**	**4.8**	**28**
work		**3rd**	**52.6**	**33.56**	**25.7**	**19.8**	**14.7**	**1.0**	**5.6**	**28**

‡ extracted from simulation plots § The same methodology in 65nm

by the algorithm for these specifications. The one which will be presented below is interesting in that it contrasts well with the results obtained for a 4th-order amplifier.

The circuit of the 3rd-order amplifier is shown in Figure 11. It is built from the same basic differential amplifier discussed before. The only difference is that the PMOS transistors require a body biasing voltage different from the common biasing of the feed-forward NMOS transistors. The sizes of the transistors are in Table II. There is less uniformity in length values than in the 4th-order amplifier. However, the maximum width is comparably smaller. The power consumption increases by close to 17% while the input-referred thermal noise is lowered to a value of 5.3 $nV/sqrt(Hz)$. DC, AC and Transient simulations are carried out to determine the response of the designed circuit to small and large input signals. The frequency response of the amplifier is plotted in Figure 12a for different capacitive loads. The circuit achieves a DC gain of 52.6 dB and a gain of 25.7 dB at 1 GHz driving a 400 fF load. The amplifier is unconditionally stable with a phase margin of 63.9°. In this amplifier, the effect of non-dominant poles and zeros is clearly visible. Due to the high unity-gain frequency that this amplifier achieves, the phase response near the f_u has a falling shape, due to unaccounted for non-dominant poles, than what normally should have been—rising above the defined φ_{min}. The circuit remains stable with a minimum phase margin of 54.8° as the load varies by an order of magnitude starting from 100 fF whilst its UGF changes from 24.6 GHz to 7.5 GHz. The circuit delivers an almost stable gain performance up to 1 GHz. The response of the designed circuit to large DC signals is depicted in Figure 13. The positive single-ended outputs are plotted in Figure 13a and the DC value around which the variation occurs can be clearly seen from this figure. In Figure 13, it can be observed that the differential DC output swings linearly for up to ±400 mV. This occurs while the differential DC input varies ±1.115 mV. For larger inputs, the amplifier output plateaus as the output transistors are not longer in saturation region and the circuit tends to deviate from the normal behavior. As the input frequency increases, the circuit operates linearly for larger input signals. The time domain response of the circuit for a 1 GHz sinusoidal signal is shown in Figure 12b. As the differential input is raised up to 10 mV, the circuit linearity is maintained and the output reaches a 200 mV peak voltage. As expected from the phase response of the circuit, the phase shift input and output signal is around 90°.

IV. Comparison of the Designed Amplifiers

The main purpose of the proposed methodology is to provide the designer with an ability to assess different performance corners and thereby save design time. However, it strengthens the argument for using this method if improvements in performance can be demonstrated by designing circuits following this methodology. In line with this, the afore-mentioned example circuits are compared to the state of the art. It is important to read the comparison table keeping in mind that some of the performances of the referenced works are post-layout simulation results of experimentally-measured modulators, but the examples are simulation results of the sizes generated by the proposed design methodology. Although consideration are given to layout effects, for instance, adding interstage interconnect capacitances, the proposed methodology is mainly important in shortening design time from system to transistor level design.

In Table III, the 4th-order and 3rd-order amplifiers that have been discussed in the previous section are compared to multi-stage amplifiers that are published as part of continuous-time bandpass ΣΔ-modulators. Reference [2] is a 4th-order operational amplifier in 65 nm CMOS technology that was designed following the proposed methodology; it is added to put the results into context. Before discussing results from other works, the three designed amplifiers are compared using the following commonly used figure-of-merit (FoM) [29]

$$FoM = \frac{f_u\, C_L}{Power} \tag{7}$$

Since the amplifiers are multi-stage, GBW is replaced by f_u and to account for different supply voltage, current consumption is replaced by power consumption. As the load capacitor used in the different works in Table III are not known, the comparison using this FoM is limited to the three works designed following the proposed methodology. Taking a unit of $^{MHz\,pF}/_{mW}$, an approximate value of 1050, 408 and 191.3 is obtained for the 3rd-order and 4th-order in 28 nm and the 4th-order in 65 nm, respectively. Although the 4th-order amplifier in 65 nm technology achieves highest gain at 1 GHz and 2 GHz frequencies, the designs in 28 nm FDSOI improve the general performance as compared by the FoM.

The amplifiers in [1], [7], and [15] were designed to work in bandpass ΣΔ modulators at f_s = 0.8 GHz, 0.8 GHz and 1 GHz, respectively. Reference [15] achieves a unity-gain-frequency of 7 GHz at a power consumption of 10 mW. In comparison, the 3rd-order in 28 nm reaches twice the unity-gain frequency while halving the required power consumption. Furthermore, the gain at 2 GHz is improved from 11 dB to 19.8 dB making the 3rd-order more fit for multi-GHz sampling modulators.

Reference [2] improves the gain at 2 GHz by 12 dB compared to [15] and by 17 dB with respect to that of [7]. Compared to [1], this work improves the gain performance at both 1 GHz and 2 GHz by 15 dB. It also consumes less than 25% while relying only on a 1.2 V supply.

Reference [1] has the highest low frequency gain, but that comes at huge power consumption. There are similar works in [30] and [31] which are designed to drive loads at more than four times of those of the design examples. Reference [6] targets low pass modulators. Its high frequency performance is compromised for increase in low-frequency gain.

V. Conclusion

This paper presents a sizing methodology for multi-stage, multi-path, feed-forward-compensated operational amplifiers. The method is explained in detail taking high speed continuous-time bandpass ΣΔ-modulators as target application. Search limits for different input parameters where the methodology is most reliable are proposed. Unlike conventional design methods, the proposed methodology is based on a database which would have to be generated for the desired technology. However, it saves valuable design once the initial set-up is complete. Three design examples in two advanced technology nodes are provided to demonstrate the effectiveness of the methodology. Compared to the state of the art, the examples improve performance metrics important in the targeted application by achieving the highest unity-gain-frequency and the highest gain beyond 1 GHz frequency.

VI. Acknowledgment

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References

[1] H. Shibata, R. Schreier, W. Yang, A. Shaikh, D. Paterson, T. C. Caldwell, D. Alldred, and P. W. Lai, "A DC-to-1 GHz Tunable RF Delta Sigma ADC Achieving DR = 74 dB and BW = 150 MHz at f0 = 450 MHz Using 550 mW," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2888–2897, Dec. 2012.

[2] F. T. Gebreyohannes, M.-M. Louërat, and H. Aboushady, "Design of a 4th-order feed-forward-compensated operational amplifier for Multi-GHz sampling frequency continuous-time bandpass sigma-delta modulators." in 2019 IEEE Int. Symp. on Circuits and Systems (ISCAS), May. 2019.

[3] B. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 237–243, Feb. 2003.

[4] R. Schreier, N. Abaskharoun, H. Shibata, D. Paterson, S. Rose, I. Mehr, and Q. Luu, "A 375-mW Quadrature Bandpass Delta-Sigma ADC With 8.5-MHz BW and 90-dB DR at 44 MHz," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2632–2640, Dec. 2006.

[5] C.-Y. Lu, J. F. Silva-Rivas, P. Kode, J. Silva-Martinez, and S. Hoyos, "A Sixth-Order 200 MHz IF Bandpass Sigma-Delta Modulator With Over 68 dB SNDR in 10 MHz Bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1122–1136, Jun. 2010.

[6] A. Edward, Q. Liu, C. Briseno-Vidrios, M. Kinyua, E. G. Soenen, A. I. Karsilayan, and J. Silva-Martinez, "A 43-mW MASH 2-2 CT SigmaDelta Modulator Attaining 74.4/75.8/76.8 dB of SNDR/SNR/DR and 50 MHz of BW in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 448–459, Feb. 2017.

[7] H. Chae, J. Jeong, G. Manganaro, and M. P. Flynn, "A 12 mW Low Power Continuous-Time Bandpass delta sigma Modulator With 58 dB SNDR and 24 MHz Bandwidth at 200 MHz IF," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 405–415, Feb. 2014.

[8] H. Chae and Flynn, Michael P., "A 69 dB SNDR, 25 MHz BW, 800 MS/s Continuous-Time Bandpass Modulator Using a Duty-Cycle-Controlled DAC for Low Power and Reconfigurability," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 649–659, Mar. 2016.

[9] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 9, pp. 1041–1056, Sep. 2001.

[10] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20mw 640mhz cmos continuous-time adc with 20mhz signal bandwidth, 80 db dynamic range and 12 bit enob," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2641 – 2649, Dec. 2006.

[11] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*, 2nd ed. Hoboken ; New Jersey: John Wiley & Sons Inc., 2017.

[12] Y. Dong, J. Zhao, W. W. Yang, T. Caldwell, H. Shibata, Z. Li, R. Schreier, Q. Meng, J. B. Silva, D. Paterson, and J. C. Gealow, "A 72 dB-DR 465 MHz-BW Continuous-Time 1-2 MASH ADC in 28 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2917–2927, Dec. 2016.

[13] Y. Dong, W. Yang, R. Schreier, A. Sheikholeslami, and S. Korrapati, "A Continuous-Time 0-3 MASH ADC Achieving 88 dB DR With 53 MHz BW in 28 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2868–2877, Dec. 2014.

[14] C. Briseno-Vidrios, A. Edward, A. Shafik, S. Palermo, and J. Silva-Martinez, "A 75-MHz Continuous-Time Sigma-Delta Modulator Employing a Broadband Low-Power Highly Efficient Common-Gate Summing Stage," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 657–668, Mar. 2017.

[15] X. Yang and H.-S. Lee, "Design of a 4th-order multi-stage feedforward operational amplifier for continuous-time bandpass delta sigma modulators." in 2016 IEEE Int. Symp. on Circuits and Systems (ISCAS), May. 2016, pp. 1058–1061.

[16] M. Hershenson, S. Boyd, and T. Lee, "Optimal design of a CMOS op-amp via geometric programming," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 1, pp. 1–21, Jan. 2001.

[17] B. De Smedt and G. Gielen, "Watson: design space boundary exploration and model generation for analog and RF IC design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 2, pp. 213–224, Feb. 2003.

[18] Q. Liu, A. Edward, D. Zhou, and J. Silva-Martinez, "A Continuous-Time MASH 1-1-1 Delta-Sigma Modulator With FIR DAC and Encoder-Embedded Loop-Unrolling Quantizer in 40-nm CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 4, pp. 756–767, Apr. 2018.

[19] F. Silveira, D. Flandre, and P. G. A. Jespers, "A g_m/I_D based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sep. 1996.

[20] J. Ou and P. M. Ferreira, "Implications of Small Geometry Effects on g_m/I_D Based Design Methodology for Analog Circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 1, pp. 81–85, Jan. 2019.

[21] P. G. Jespers and B. Murmann, *Systematic design of analog CMOS circuits using pre-computed lookup tables*. Cambridge ; New York: Cambridge University Press, 2017.

[22] J. S. Mincey, C. Briseno-Vidrios, J. Silva-Martinez, and C. T. Rodenbeck, "Low-Power G_m−C Filter Employing Current-Reuse Differential Difference Amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 6, pp. 635–639, Jun. 2017.

[23] T. Poiroux, O. Rozeau, P. Scheer, S. Martinie, M. Jaud, M. Minondo, A. Juge, J.-C. Barbe, and M. Vinet, "Leti-utsoi2.1: A compact model for utbb-fdsoi technologies–part i: Interface potentials analytical model,"

Electron Devices, IEEE Transactions on, vol. 62, pp. 2751–2759, 09 2015.

[24] T. Poiroux, O. Rozeau, P. Scheer, S. Martinie, M.-A. Jaud, M. Minondo, A. Juge, J.-C. Barbe, and M. Vinet, "Leti-utsoi2.1: A compact model for utbb-fdsoi technologies - part ii: Dc and ac model description," *Electron Devices, IEEE Transactions on*, vol. 62, pp. 2760–2768, 09 2015.

[25] V. Kilchytska, S. Makovejev, M. K. Md Arshad, J.-P. Raskin, and D. Flandre, "Perspectives of UTBB FD SOI MOSFETs for Analog and RF Applications," in *Functional Nanomaterials and Devices for Electronics, Sensors and Energy Harvesting*, A. Nazarov, F. Balestra, V. Kilchytska, and D. Flandre, Eds. Springer International Publishing, 2014, pp. 27–46.

[26] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Eds., *Analysis and design of analog integrated circuits*, 5th ed. New York: Wiley, 2009.

[27] Q. Wang, H. Shibata, A. Liscidini, and A. C. Carusone, "A Digital Filtering ADC With Programmable Blocker Cancellation for Wireless Receivers," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 681–691, Mar. 2018.

[28] R. Taco, I. Levi, M. Lanuzza, and A. Fish, "Low voltage logic circuits exploiting gate level dynamic body biasing in 28nm utbb fd-soi," *Solid-State Electronics*, vol. 117, pp. 185 – 192, Mar. 2016.

[29] X. Peng and W. Sansen, "Transconductance with capacitances feedback compensation for multistage amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 7, pp. 1514–1520, Jul. 2005.

[30] Y. Dong, J. Zhao, W. Yang, T. Caldwell, H. Shibata, R. Schreier, Q. Meng, J. Silva, D. Paterson, and J. Gealow, "A 930mw 69db-DR 465mhz-BW CT 1-2 MASH ADC in 28nm CMOS," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan. 2016, pp. 278–279.

[31] H. Shibata, V. Kozlov, Z. Ji, A. Ganesan, H. Zhu, D. Paterson, J. Zhao, S. Patil, and S. Pavan, "A 9-GS/s 1.125-GHz BW Oversampling Continuous-Time Pipeline ADC Achieving –164-dBFS/Hz NSD," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3219–3234, Dec. 2017.



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