Synthesis of mm-Wave Wideband Receivers in 28nm CMOS Technology for Automotive Radar Applications

Fábio Passos, Miguel Chanca, Elisenda Roca, Rafael Castro-López, *Member, IEEE,* and Francisco V. Fernández, *Member, IEEE*

***Abstract*—A new strategy for millimeter-wave circuit and system synthesis, where the accuracy of electromagnetic simulations can be achieved in optimization-based design methodologies without sacrificing efficiency, is presented and tested within a real industrial project. This is done by properly partitioning the system, generating libraries of passive devices which are electromagnetically simulated prior to any circuit optimization, generating performance trade-offs at different hierarchical levels with multi-objective optimization algorithms and hierarchically composing lower level sub-blocks. With this proposed solution, an entire millimeter-wave system, from the passive component level up to the system level, has been designed and compared with the results obtained from a conventional design approach, demonstrating the outstanding capabilities of the methodology.**

***Index Terms*— millimeter-wave circuits, ADAS, circuit synthesis, transformers.**

I. Introduction

ADVANCED driver assistance systems (ADAS) have nowadays been motivating many research efforts in order to improve the driver experience and safety. ADAS enable features such as collision warning, lane shift warning, adaptive cruise control, pedestrian crash avoidance, etc. ADAS is heavily dependent on automotive radar technology, which is required to cover the 76-81 GHz band for high range resolution [1]. Therefore, due to the high operation frequency, the design of millimeter-wave (mm-Wave) circuits and systems is of utmost importance for the deployment of ADAS technologies. Recent results proved the feasibility and suitability of monolithic microwave integrated circuit (MMIC) radars for operation in the 76-81 GHz band and opened the way towards automotive radars on a single chip. Such systems included the mm-Wave front-end receiver MMIC (Rx MMIC), transmitter (Tx MMIC), a channel and signal processing unit and a phase-lock loop (PLL) on a monolithic die [2],[3]. A simplified block diagram of a typical transceiver used in automotive radar applications is shown in Fig. 1.

In order to design such system, mm-Wave designers usually rely on traditional approaches, where different parts of the circuit are designed independently and iteratively (e.g., first design the actives then the passives). However, due to the immense design space and different performance trade-offs, it is a challenge to find optimal system designs by using such methodologies. Moreover, mm-Wave ICs are extremely dependent on passive devices (i.e., inductors and transformers), and current commercial process design kits do not provide accurate passive device models for the mm-Wave range (i.e., above 40 GHz). Analytical equivalent lumped-element models for integrated passive components have been developed but are not accurate enough in the mm-Wave range. As a result, designers need to rely on design experience and electromagnetic (EM) simulators to predict passive device performances. Such procedure may involve a large number of

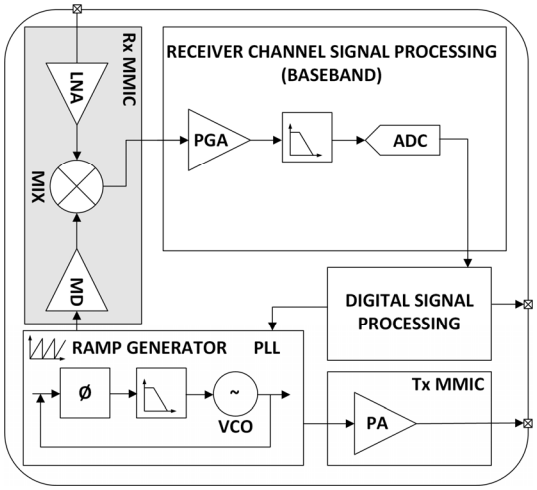

Fig. 1. Simplified block diagram of a typical transceiver used in automotive radar applications.

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iterations and is usually time consuming, even for experienced designers.

Synthesis methodologies that use optimization algorithms have been successfully applied in the last decade to the design of analog and radio-frequency (RF) circuits in most cases [4]-[7], RF systems in few cases [8], and, in scarce occasions, mm-Wave circuits [9],[10]. However, none has been applied and tested in an industrial environment.

These methodologies can automatically design circuits sidestepping the manual iterative processes and reaching optimal designs. Nevertheless, accurately designing passive components is still a drawback, especially when using optimization-based strategies. In the past, EM simulators have been integrated within synthesis methodologies to design RF circuits [5]. However, by incorporating an EM simulator within an optimization loop, the efficiency of the optimization suffers dramatically. Therefore, such approach will not yield the required quality of designs for the mm-Wave range under typically limited computational resources.

In order to improve such efficiency, some approaches removed the EM simulator from the optimization loop and employed surrogate-assisted methodologies. In [9],[10], a single-objective optimization algorithm is used to design a linear mm-Wave amplifier while optimizing just one transformer. The costly EM simulations of the transformer are replaced by a machine-learning approach that progressively increases the accuracy of a local surrogate model of the transformer by adding the EM simulation results of promising ones. However, the approach is only valid for one single passive device (transformer), which is clearly not the case for most mm-Wave circuits. Moreover, since the design space exploration is based on a coarse surrogate model that is progressively refined with additional samples, there is a risk that the optimization process will converge to a suboptimal region.

Therefore, it is possible to conclude that current solutions to automatically design mm-Wave circuits are not practical and do not ensure optimal results. But it is not only that: automated approaches for mm-Wave systems simply do not exist. Therefore, there is a need for an efficient and accurate methodology that is capable of providing optimal mm-Wave circuits and systems in practical times, while optimizing all passives and aiming at EM accuracy.

In order to solve these challenges, a solution is proposed here based on a proper system partitioning into hierarchical levels. At the lowest level, efficient sampling techniques are used to generate sets of passive structures, which are electromagnetically simulated and stored, building therefore a library for such structures. During the synthesis of any mm-Wave circuit, these libraries are explored and the optimization algorithm can select the structures needed to reach optimal designs, as explored in [11] at the circuit level. By applying such methodology, no EM simulation is performed during the optimization loop, but, even so, EM accuracy is guaranteed. Performance trade-offs at the circuit level are obtained with multi-objective optimization algorithms, and, by hierarchically composing lower level sub-blocks, system-level performance trade-offs can be obtained

The methodology proposed in this work was validated in an industrial environment, to replicate the design of a transceiver used in ADAS applications. This paper will show results obtained for the design of the Rx MMIC in Fig. 1 using the proposed methodology. The Rx MMIC is composed of a low-noise amplifier (LNA), a mixer driver (MD) and a mixer (MIX). It must be taken into account that the circuit/system topologies used in this work and their specifications are intended for an actual product and not an academic problem formulation. Therefore, the demands are much higher.

The rest of this paper is organized as follows. In Section II, the proposed methodology is explained in detail. Section III presents the design of an Rx MMIC as experimental results. Afterwards, in Section IV, conclusions are outlined.

II. MM-WAVE SYSTEM SYNTHESIS STRATEGY

A. Methodology Overview

The design of mm-Wave circuits is formulated as an optimization problem, where circuits are automatically designed while optimizing some design goals (optimization objectives) and meeting some specifications (optimization constraints). Most mm-Wave systems are defined by dozens or even hundreds of design variables. Hence, directly performing an optimization-based synthesis with such a search space is virtually impossible because the optimization process would hardly converge.

Therefore, to be able to design such complex systems, this work uses a design methodology based on divide-and-conquer strategies, where the system is hierarchically partitioned and bottom-up (BU) synthesis methodologies are applied. In BU synthesis, the desired system is first decomposed into several hierarchical levels. Then, the design process starts with the optimization at the lowest level. The results at each level are then used in the optimization at the upper level of the hierarchy, until the system level is reached. In this type of design methodologies, multi-objective optimization algorithms are commonly used so that the information passed to the upper level is not a single design solution but a Pareto-optimal front (POF), which represents the best trade-offs among performances available for a given circuit topology. Hence, it is in the composition of these POFs up the hierarchy where the power of BU synthesis lies [8].

In this work, the strategies to adopt this general design methodology in the design of the Rx MMIC shown in Fig. 1 (including the LNA, MD and MIX) will be described. The BU hierarchy used in this work is illustrated in Fig. 2. The lowest level (device level) is the passive component library, the second level (circuit level) is comprised by the LNA and the MD, and the MIX is designed during the system level optimization (the motivations to promote the MIX optimization to the system level will become clear in Sections II.D and III). With such methodology, it is possible to remove the EM simulations from the optimization loop itself, while being able to keep EM accuracy in optimization-based approaches.

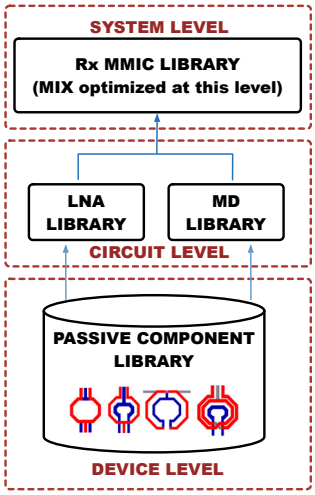


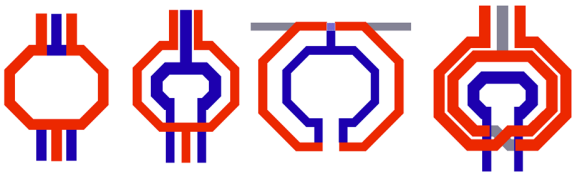
Fig. 2. Illustrating the BU methodology, from device- to system-level synthesis. The LNA and MD are generated during the circuit level, while the MIX is optimized during the system level optimization.

B. *Passive Component Library Creation*

To create the libraries, the designer must select the desired design space, which technique is going to be used to efficiently cover the design space, and which passive structures may be necessary for circuit synthesis. In this work, the considered structures for mm-Wave circuit design are shown in Fig. 3. Typical baluns and transformers are considered, as well as hybrid structures such as the 7-port structure in Fig. 3c). The purpose of using such 7-port structure formed by three inductors (two half-turn inductors and a symmetrical inductor with center tap) will be illustrated in Section III. The three inductors are electromagnetically simulated as one single structure so that the interactions between inductors are accounted for.

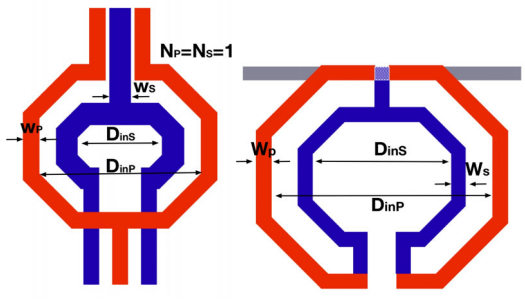
Fig. 4a) illustrates the top-view of a 6-port octagonal symmetrical transformer. The geometry of this transformer is usually defined by six geometric parameters: number of turns of primary coil (N_P) and secondary coil (N_S), inner diameter of the primary (D_{inP}) and secondary (D_{inS}) and turn width of the primary (w_P) and secondary (w_S). Fig. 4b) illustrates the geometrical parameters of the 7-port structure. For the sake of simplicity, such structure is defined by the same geometrical parameters as the transformer in Fig. 4a) (instead of describing the two half-turn inductors with separate geometry, they are considered as if they were a single coil).

Different techniques can be used to sample the design space,



(a) (b) (c) (d)

Fig. 3. Considered structures for library creation. a) 1:1 6-port balun (stacked transformer). b) 1:1 6-port transformer c) 7-port structure built with two half-turn inductors and a symmetrical inductor with a biasing transmission line and d) 2:1 6-port transformer.



(a) (b)

Fig. 4. Illustrating the location of each port and the geometrical parameters of the considered structures. a) 6-port octagonal symmetrical transformer. b) 7-port structure containing three inductors, defined by the same geometrical parameters as a transformer.

either by creating a geometrical parameter grid, or by using other sampling techniques such as Monte Carlo (MC), Quasi-Monte Carlo (QMC) or Latin Hypercube Sampling (LHS). Each device sample is electromagnetically simulated. The description in terms of S-parameters versus frequency of each passive structure is saved and can then be used during circuit simulation in order to accurately emulate the behavior of such structure. In this way, the proposed methodology enables a new mm-Wave circuit synthesis strategy that alleviates the computational limitations of EM simulations because the passive structure library creation is performed a priori and independently from the circuit under optimization. Therefore, the libraries must only be generated once for each technology and then they can be used in different circuit optimizations.

After the passive component libraries are created, the devices must be properly organized so that the optimizer can select them in a clever and efficient manner [7]. In this work an index mapping technique was used which takes into account the performances of the transformers and organizes them accordingly [8]. Alternatively, the passive device samples could also be used to generate surrogate models of transformers and baluns, in a similar manner to the surrogate models of inductors developed in [12].

C. *mm-Wave Hierarchical System Synthesis*

Following the BU design methodology in Fig. 2, at the circuit level, POFs for the LNA and the MD are generated by using a multi-objective optimization algorithm. In this work, the Non-dominated Sorting Genetic Algorithm (NSGA-II) is used [13]. NSGA-II is based on the evolution of a set of solutions (i.e., individuals) along a certain number of iterations (i.e., generations). As illustrated in Fig. 5, the design space is formed by the transistor sizes, bias sources and the passive component library described in Section II.B. Circuit performances are evaluated with an RF simulator. The output of the optimization algorithm is a Pareto-optimal front, consisting of a set of points exhibiting optimal trade-offs between the LNA or MD performances. After the optimization, the obtained POFs are organized and indexed by their performances and considered as an optimized library of the circuit/system under optimization.

Then, the Rx MMIC level optimization starts. At this level, illustrated in Fig. 5, the design space is formed by the points of

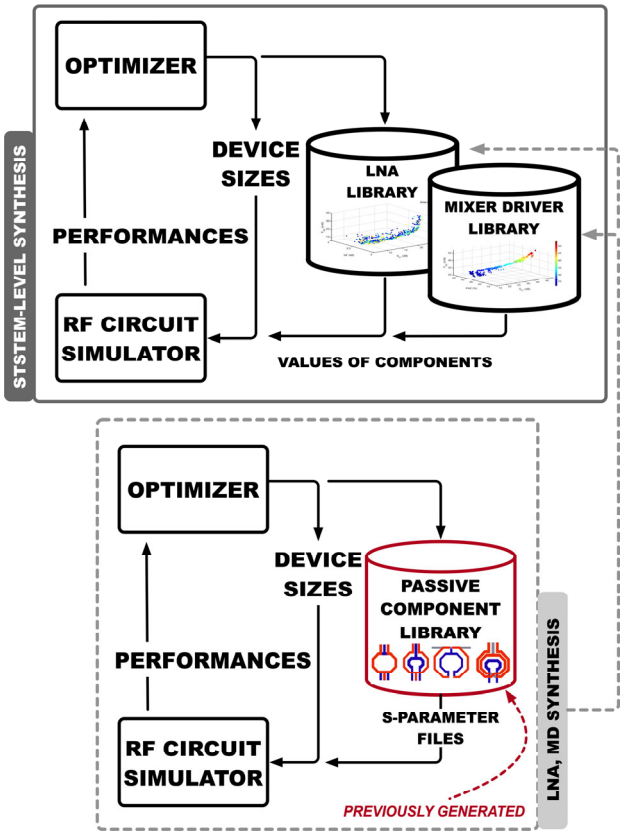


Fig. 5. Illustrating the circuit-level (LNA and MD) synthesis and the system level synthesis, where the LNA and MD libraries are used as search space for the system optimization.

the circuit level POFs and the design variables of all devices that have not been included in the circuit level blocks. If a multi-objective optimization algorithm is used here, POFs can also be generated at this level, enabling the selection of the desired system design a posteriori.

During the optimizations at both levels, each circuit/system achieved is completely feasible with all components fully designed and, therefore, no re-design iterations are required. To the best of the authors' knowledge, the work reported here is the first one where this type of BU methodology is applied to the entire system-circuit-device hierarchy for a mm-Wave system.

D. Partitioning Strategy

An important aspect to discuss is how should the system be hierarchically partitioned, i.e., how many hierarchical levels should be considered and which blocks at each level. To a large extent, the partitioning strategy imitates the designer, because the divide-and-conquer strategies applied by designers are usually the smartest way to proceed. This means that for the system at hand, partitioning of the Rx MMIC in LNA, MD and MIX is a good approach. Each block has a well-defined functionality and the performances of interest for them can be identified. Together with this, some other considerations related to the intrinsic properties of the POF composition in BU approaches should be taken into account:

1) POFs are the outcome of the minimization/maximization of conflicting objectives subject to some constraints. Therefore, it should be possible to find such formulation for all the performances of interest of each block. These performances should also be handled independently of other blocks.
2) POFs are generated using multi-objective optimization algorithms. Although many-objective optimization algorithms constitute a hot area of research [14], most algorithms find difficulties beyond four objectives. Therefore, the number of necessary objectives at each level should not go beyond those numbers. On the other hand, the BU composition is based on the idea that the density of points in lower level blocks is sufficiently high. If the number of objectives increases, the number of points required to keep an appropriate density increases exponentially, and so does the computational effort to generate the POF.
3) Partitioning in blocks should significantly decrease the size of the search space at higher levels.

The specific application of these considerations depends on the selected topologies and the system specifications, which are discussed in Section III.

III. Experimental Results

The synthesis methodology presented in Section II can be applied to any mm-Wave system, technology process and operating frequency. In this Section, experimental results are shown for the design of the Rx MMIC shown in Fig. 1 in a 28-nm CMOS technology. The system must operate properly for the entire 65-85 GHz band (20 GHz of bandwidth) and with a supply voltage V_{DD}=0.9V.

A. Passive Component Library

For most applications in the mm-Wave range, the design space of the transformers and baluns in Fig. 3 given by $D_{inP,S}\in$ [20, 100]µm and $w_{P,S}\in$[5, 10]µm is large enough to obtain a wide range of performances. In this paper, only transformers with one and two turns were considered. However a library can be created for any N_P:N_S transformer.

In this work, the QMC technique is used to generate the passive structure sampling. A total of 1,150 structures were generated, divided as follows: 150 6-port baluns (Fig. 3a), 500 6-port transformers (Fig. 3b), 250 7-port three-inductor structure (Fig. 3c) and 250 2:1 6-port transformers (Fig. 3d). EM simulations were performed with ADS Momentum. The time needed for the simulation of all 1,150 transformers was around 24 hours in a machine with a 6-core Intel® Xeon® E5-2630 v2 processor at 2.60 GHz.

B. Circuit-level Synthesis

In this sub-section, the optimization of both circuit blocks (LNA and MD) used in the Rx MMIC is illustrated. Regarding the LNA design, the circuit topology considered is the two-stage LNA shown in Fig. 6. This LNA uses three transformers, whose center taps are used for biasing the circuit. Fig. 7a) shows

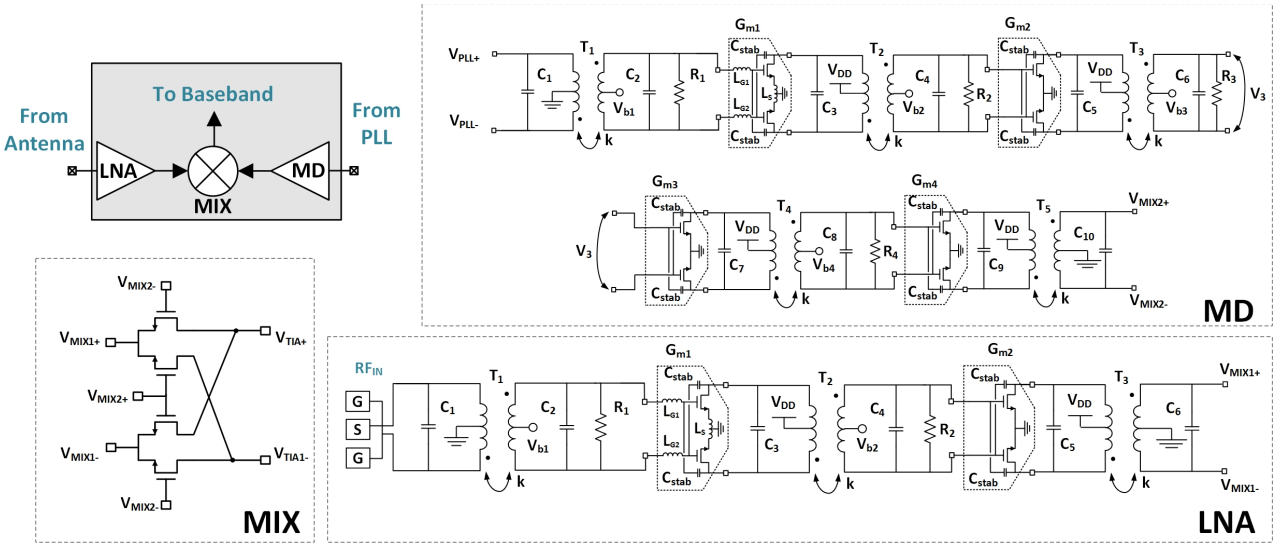


Fig. 6. Simplified schematics of the mm-Wave Rx MMIC blocks (LNA, MD and MIX).

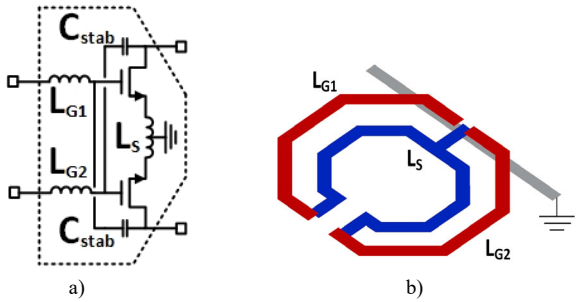


Fig. 7. First stage active block represented by G_{m1} in the LNA in Fig. 6. a) Schematic view showing its three inductors and b) passive structure used during optimization containing the three inductors to consider interactions.

the first stage of the LNA (G_{m1}), which is a common-source (CS) differential pair. The parasitic capacitance between the NMOS gate and drain (C_{GD}) is responsible for the degradation of the LNA stability and therefore such capacitance should be neutralized in order to improve stability [3]. This can be performed by adding a capacitance in parallel to C_{GD}. This parallel capacitance, known as stability capacitor (C_{stab}), is included in both NMOS transistors of the pair. Also, note in Fig. 7a) the three inductors that are used to provide a wideband input matching. Fig. 7b) shows this three-inductor structure, where each half-turn inductor (L_{G1} and L_{G2}) is connected to the gate of the NMOS and the symmetric center-tapped inductor is connected to both sources of the NMOS transistors. Although the source inductor degenerates the NMOS transistors, thus decreasing the gain of the LNA, it is, on the other hand, very useful to increase the circuit matching bandwidth, which was mandatory for the industrial application. The second stage of the LNA, as shown in Fig. 6, is a simple CS differential pair, also with the usage of C_{stab} to improve stability.

The LNA has several important performance parameters that need to be considered during the design process: noise figure NF, gain S_{21}, power consumption P_{DC}, third-order intercept point IIP3, input matching coefficient S_{11}, the Rollet stability factor k (if smaller than 1, the LNA is potentially unstable) and the area, which is highly important due to manufacturing costs. In mm-Wave circuits, the area of the circuits is mainly dominated by the area of the passive components. Therefore, in this work, the area is approximated as the sum of the outer diameter of the passive components used. Since the layout of mm-Wave circuits/systems is usually performed using a horizontal floorplan (across the x-axis), and, in this work the y-axis is dominated by the LNA pads, the area can be defined as the circuit length (i.e., the size in µm across the x-axis).

The LNA optimization was performed with 800 individuals, 300 generations and had four objectives: maximization of S_{21} and minimization of length, NF and P_{DC}. Other specifications were imposed as optimization constraints (e.g., lower constraint for gain or upper constraint for power), which are shown in Table I. Although this is not strictly necessary, it helps the optimizer avoiding regions of the design space that yield solutions with little interest. The ranges for all devices are defined in Table II and the result of the optimization is shown in Fig. 8, where each of the dots represents a fully sized circuit. As a comparison, the results obtained using the proposed mm-Wave synthesis methodology were compared against

TABLE I
DESIRED SPECIFICATIONS FOR THE LNA OPTIMIZATION.

LNA Performance		LNA Specifications
S_{11} @ 65-85 GHz		< -12 dB
S_{21} @ 65-85 GHz		Maximize (>7 dB)
k		> 1
P_{DC}		Minimize (< 40 mW)
Area (length)		Minimize
Gain flatness	$S_{21@65GHz} - S_{21@75GHz}$	<1.5dB
	$S_{21@85GHz} - S_{21@75GHz}$	<1.5dB
	$S_{21@70GHz} - S_{21@75GHz}$	<0.75dB
	$S_{21@80GHz} - S_{21@75GHz}$	<0.75dB
NF		Minimize (<7dB)
IIP_3		>-5 dBm

TABLE II
DESIGN VARIABLES RANGES FOR THE ALL DEVICES IN ALL OPTIMIZATIONS.

Variables	Min	Max	Step
Transistor Width (nm)	320	1280	320
Transistor Number of Fingers	2	128	2
Transistor Multiplier	1	8	1
Transistor length (nm)	30	50	5
V_{bx} (V)	0.45	0.65	0.01
Resistor lengths (µm)	1	21	1
Transformer/inductors	Selected from Library		
Capacitor Number of Fingers	2	101	2

results obtained by an actual RF/mm-Wave designer using a traditional manual design strategy. The results obtained by the designer are represented by the dot with red circle in Fig. 8a)-c). The LNA obtained with a traditional approach by an expert designer had the following performances: P_{DC}=15 mW, S_{21}=14 dB, NF=4.5 dB and length=613 µm, while complying with all

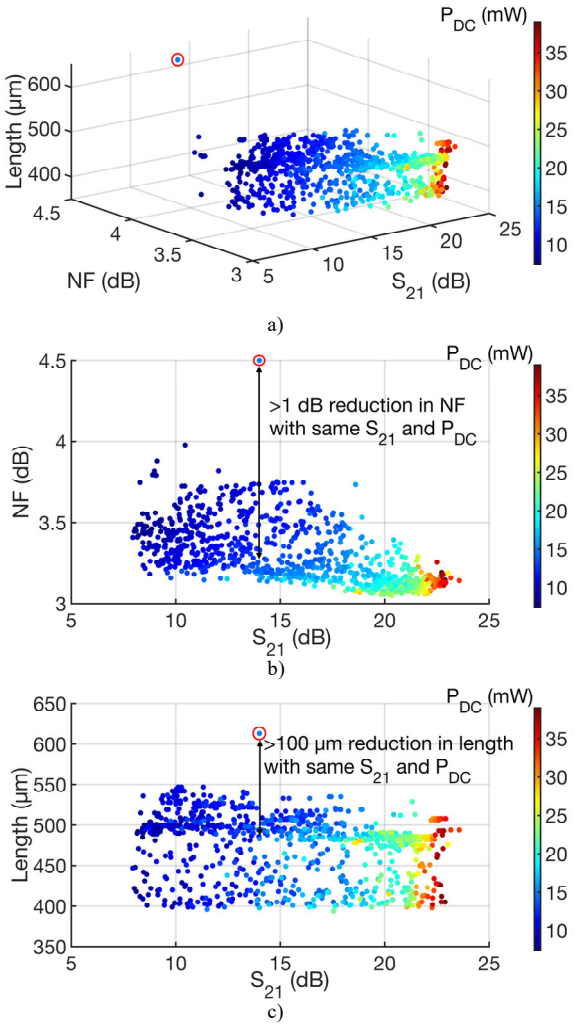


Fig. 8. a) Comparison between the obtained LNA POF using the proposed mm-Wave synthesis methodology vs. an LNA designed using a traditional design approach (dot with red circle). The color bar corresponds to the fourth objective, P_{DC}. b) 2-D projection of the POF illustrating S_{21} vs. NF vs P_{DC} (color bar). c) 2-D projection of the POF illustrating S_{21} vs. length vs P_{DC} (color bar).

the desired specifications in Table I (e.g., S_{11} and IIP_3). It is possible to see in Fig. 8b) and Fig. 8c) that the synthesis methodology proposed in this work, was capable of achieving hundreds of designs with superior performances than the design obtained with a traditional methodology. Please take into account, that the comparison was made in a fair manner, with all circuits simulated with the same level of accuracy: mm-Wave device models for transistors, resistors and capacitors and EM simulation for transformers and inductors. This comparison illustrates the strength of the methodology and the aid it can provide the designer, by being able to find optimal designs.

Regarding the MD design, the circuit topology considered is a four-stage MD, as shown in Fig. 6. The MD is a circuit whose main purpose is to amplify the signal from the PLL and adjust the voltage level in order to drive the passive mixer correctly. The first active stage of the MD is identical to the one in the LNA (shown in Fig. 7a) and the second to fourth active stages of the MD are the same as the second active stage of the LNA (shown in Fig. 6).

The MD has several important performance parameters that need to be considered during the design process: gain S_{21}, power consumption P_{DC}, input matching coefficient S_{11}, the Rollet stability factor *k,* the desired output voltage to drive the mixer V_{out} (V_{MIX2+}-V_{MIX2-}) and the power-added efficiency PAE, which is calculated as,

$$PAE(\%) = \frac{P_{OUT} - P_{IN}}{P_{DC}} \cdot 100 \quad (1)$$

where P_{OUT} is the output power of the MD and P_{IN} is the input power (during the optimization P_{IN} was set to -15 dBm).

The MD optimization was performed with 800 individuals and 300 generations and had three objectives: maximization of S_{21} and minimization of length and P_{DC}. The specifications are shown in Table III. Again, as in the LNA optimization, constraints have been imposed on some performances, some even being objectives. The search space is defined in Table II and the result of the optimization is shown in Fig. 9, where each dot represents a fully sized circuit. Again, as a comparison, the results obtained using the proposed methodology were compared against results obtained by an actual designer. The results obtained by the designer are represented by the dot with red circle in Fig. 9a)-b). The MD obtained with the traditional

TABLE III
DESIRED SPECIFICATIONS FOR THE MD OPTIMIZATION.

MD Performance		MD Specifications
S_{11} @ 65-85 GHz		< -12 dB
S_{21} @ 65-85 GHz		Maximize (>15 dB)
k		> 1
P_{DC}		Minimize (< 70 mW)
PAE		>15%
Area (length)		Minimize
Gain flatness	**$S_{21@65GHz}$ - $S_{21@75GHz}$**	<1.5dB
	$S_{21@85GHz}$ - $S_{21@75GHz}$	<1.5dB
	$S_{21@70GHz}$ - $S_{21@75GHz}$	<0.75dB
	$S_{21@80GHz}$ - $S_{21@75GHz}$	<0.75dB
V_{out} (V_{MIX2+}-V_{MIX2-})		0.9 < V_{out} < 1.1 V

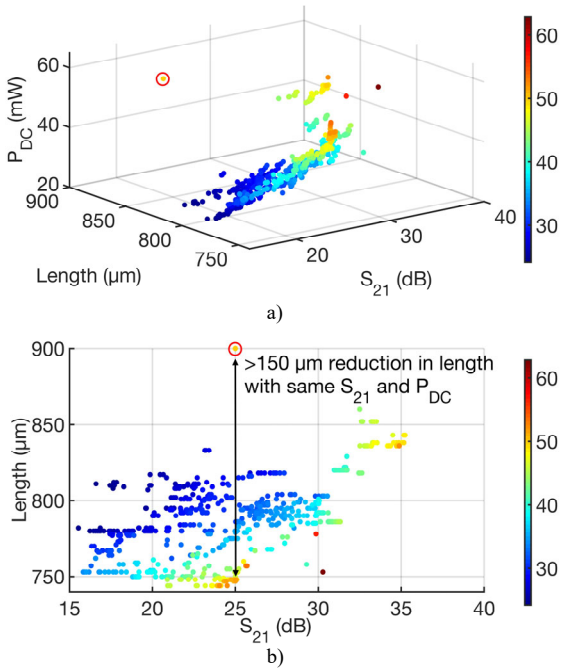


Fig. 9. a) Comparison between the obtained MD POF using the proposed mm-Wave synthesis methodology vs. an MD designed using a traditional design approach (dot with red circle). The color bar corresponds to the third objective, P_{DC}. b) 2-D projection of the POF illustrating S_{21} vs. length vs. P_{DC} (color bar).

design approach had the following performances: P_{DC}=50 mW, S_{21}=25 dB and length=900 μm, while complying with all the desired specifications in Table III. Again, it is possible to observe in Fig. 9b) that superior results were obtained using the proposed methodology.

C. System-level Synthesis

After obtaining the POF for both individual circuits (LNA and MD), the next optimization is performed in order to compose the Rx MMIC, whose specifications are shown in Table IV (the gain of the entire Rx MMIC is referred to as conversion gain, (*CG*). In this work, the passive MIX, shown in Fig. 6, is designed during the system optimization. Considering the MIX design at the same level than the LNA and MD would bring some difficulties. Since the Rx MMIC is part of a larger system, it has to be designed with a set of specifications so that it respects the full system needs (e.g., the gain of the Rx cannot be just maximized due to linearity issues, therefore, an upper constraint is established). If the MIX were optimized at the circuit level, a mandatory objective would be minimization of the noise figure. However, NF minimization in the MIX also maximizes the gain. The consequence is that the POF of the MIX would contain solutions with too high gain to meet the Rx MMIC specification in Table IV. Although this could be handled, at least partially, by introducing constraints, it is not trivial. If, on the other hand, we consider that due to the reduced number of independent design variables of the MIX, there is not a significant advantage in generating a MIX POF, the decision to handle the MIX directly at the upper level arises naturally.

The optimization was performed with 300 individuals and

TABLE IV
DESIRED SPECIFICATIONS FOR THE RX MMIC OPTIMIZATION.

Rx MMIC Performance	Rx MMIC Specifications
***CG* @ 65-85 GHz**	25 < *CG* < 35 dB
P_{DC}	Minimize (< 60 mW)
NF	Minimize (<10 dB)
Area (length)	Minimize
IIP3	> 0 dBm
V_{out} (V_{MIX2+}-V_{MIX2-})	0.9 < V_{out} < 1.1 V

100 generations. For the receiver optimization, LNA and MD candidate solutions were selected from their POFs. The ranges of the design variables of the MIX transistors were the same than in Table II. The result of the optimization is shown in Fig. 10. It is possible to observe that hundreds of fully designed Rx MMICs with a clear trade-off between P_{DC}, length and NF, are obtained. Again, as performed for the individual circuits in the previous sub-section, the system was fully designed using a traditional design approach and the results obtained are represented with the red circle in Fig. 10. The Rx MMIC obtained with a traditional methodology had the following performances: P_{DC}=65 mW, NF=7.5 dB and length=1513 μm, while complying with all the desired specifications in Table IV. Comparing with the design obtained, it is possible to observe that the proposed methodology was able to obtain designs with a reduction of 30 mW in P_{DC} and more than 250 μm in system length (while maintaining the same NF). These results clearly state that the proposed methodology can help the designers to further explore the design space, obtain optimal designs and improve the performances of mm-Wave systems, pushing

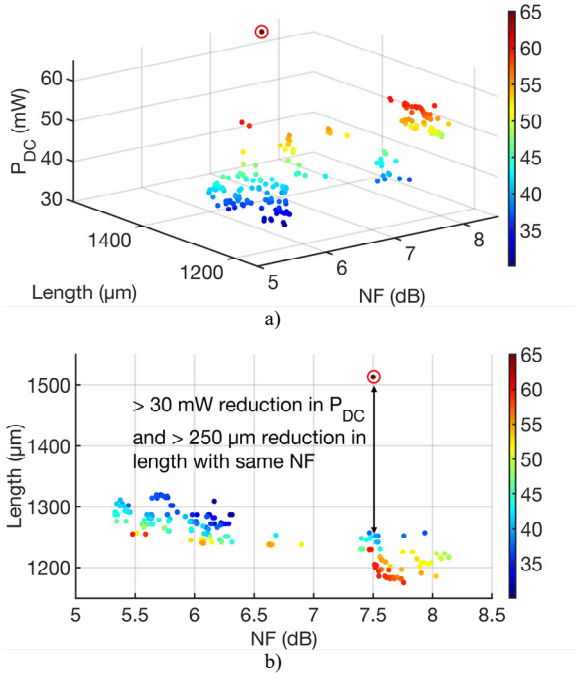


Fig. 10. a) Obtained Rx MMIC (LNA+MD+MIX) POF with all devices fully designed. The dot with the red circuit represents an Rx MMIX designed using a traditional design approach. The color bar corresponds to the third objective, P_{DC}. b) 2-D projection of the POF illustrating NF vs. length vs. P_{DC} (color bar).

forward state-of-the-art applications such as ADAS.

After all optimizations are performed and the system level POF is obtained, the designer can choose the design which best suits the needs of his/her system. In order to illustrate that, a randomly selected design, with NF=6.2 dB, P_{DC}=37.3 mW and length=1266 µm, was simulated in Cadence Virtuoso so that its performances can be visually inspected. The CG is shown in Fig. 11a), the NF in Fig. 11b), the S_{11} (at the LNA input) in Fig. 11c) and the IIP_3 in Fig. 11d). Since the passive devices are already designed, their layout is available and the passive component floorplan can be observed (see Fig. 12).

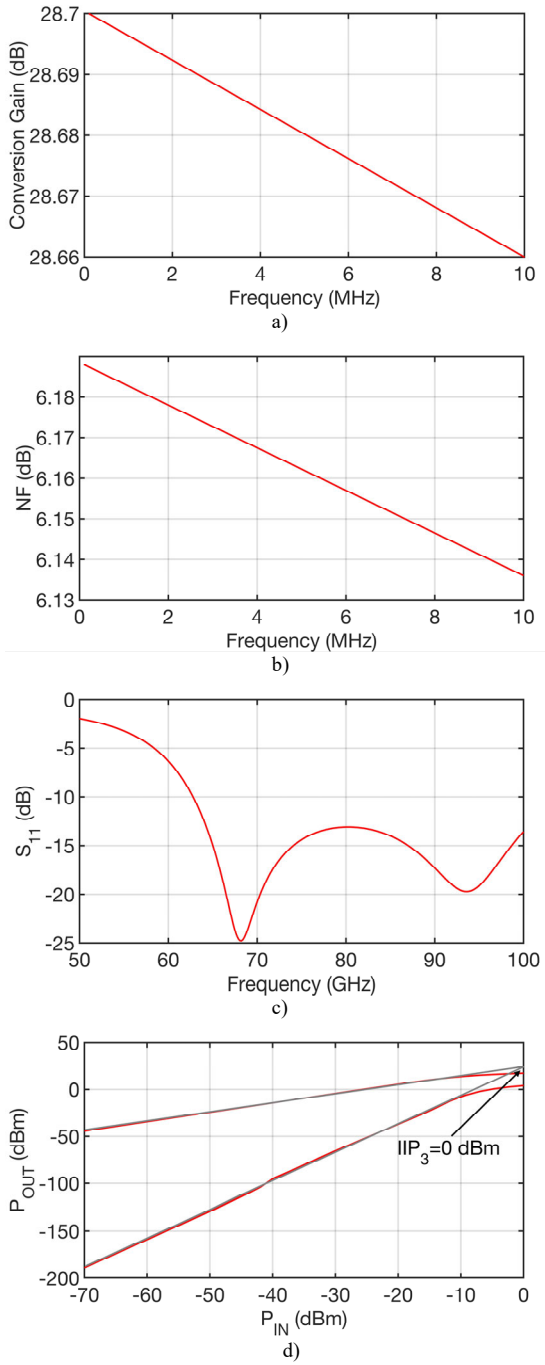


Fig.11. Performances of an obtained Rx MMIC (with all devices fully designed. a) Conversion gain. b) Noise figure c) Input matching (input of the LNA) d) third-order input intercept point.

Is has been proved in Fig. 8 to Fig. 10 that this methodology greatly improves the design quality of this type of circuits/systems. However, the methodology is also far more efficient than current traditional design methodologies. Fig. 13 shows the timeline of the optimizations performed using this methodology in order to achieve the complete Rx, which sums up to 39 hours, 24 of which are devoted to the EM simulations needed to build the passive component library, which only need to be performed once. Therefore, if an Rx MMIC needs to be designed with other circuit topologies or specifications it could be done in only 15 hours. Needless to say, this time only accounts for the computational effort. Building the complete system design strategy for the receiver requires previous development of parameterized cell layouts and tool interfacing. But these tasks only have to be performed once.

As a comparison to an actual industrial environment, it is estimated that an expert RF/mm-Wave designer needed approximately 15 days to design the LNA and the MD and another 2 days to merge the circuits as a system while designing the mixer (which amounts to 17 days) to get a single design. Therefore, it is possible to conclude that the methodology is much more efficient than the actual design process. Moreover, with the proposed methodology, optimal results are obtained by efficiently exploring the design space, reducing time-to-market.

IV. Conclusions

In this work, a methodology is presented that, by adopting an innovative strategy, allows the automatic and efficient synthesis of mm-Wave systems. A hierarchical bottom-up approach is implemented from device level up to the system level that provides a set of fully sized mm-Wave receivers with optimal trade-offs between their performances. With such new mm-Wave synthesis paradigm, each level of the hierarchy is simulated with the utmost accuracy possible: EM accuracy at device level and electrical simulations at circuit/system level. To the best of the authors' knowledge, the design of a mm-Wave system, using a BU synthesis approach, has been demonstrated for the first time in this work.

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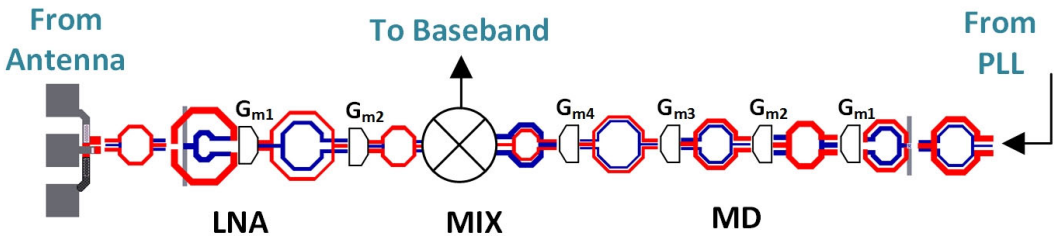

Fig. 12. Floorplan of the Rx MMIC with the performances shown in Fig. 11.

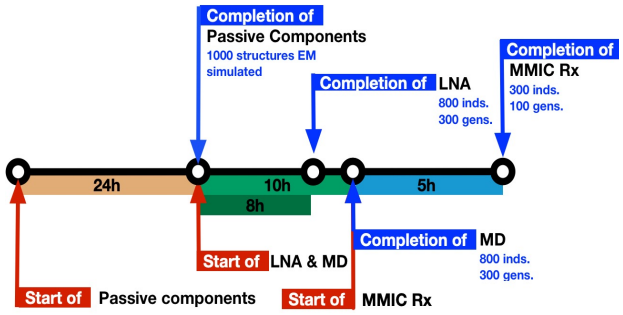

Fig.13. Timeline of the complete optimization of the MMIC Rx.

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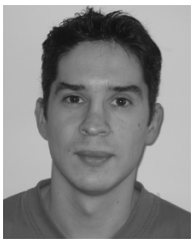

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