

A Hierarchical Performance Equation Library for Basic Op-Amp Design

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Abstract—The paper presents a new approach to automate the set-up of the design equations of the manual analog design process. Its main contribution is a comprehensive hierarchical performance equation library (HPEL) for op-amps. The HPEL makes the set-up of design equations independent of the topology. Based on the library and the functional block recognition method in [1], analytical performance models for various op-amp topologies are automatically instantiated. The method is currently designed for basic op-amps. In this paper, we use the method to size different op-amp topologies. Experimental results featuring four circuits are presented. The HPEL has also been integrated into a structural synthesis method featuring several thousand op-amp topologies [2].

Index Terms—analog circuit modeling, CMOS, operational amplifiers, circuit design, sizing

I. INTRODUCTION

Behavioral equations are a major means in the design process of analog circuits to analyze the DC-, AC-, and transient behavior of the circuit without requiring time-consuming circuit simulation. They are used for instance for structural synthesis and in the sizing process.

Structural synthesis aims at finding a suitable netlist of transistors (topology) for a given set of specifications. Behavioral equations are used to guide the topology selection and development process, e.g. [3]–[8].

Sizing is the process of finding the device sizes in an analog circuit, e.g., the widths and lengths of CMOS transistors, such that the performance specifications, e.g., for gain, power consumption, slew rate, are fulfilled. Many computer-aided approaches for sizing are equation-based, e.g., [9]–[20]. Simulation-based sizing approaches, e.g. [21]–[32], use numerical SPICE-like simulation. They are considered an alternative to or an afterburner of equation-based sizing. They deal with any type circuit, but are computationally more expensive. The optimizer and suitable constraints must be set up manually, a performance evaluation by numerical simulation is more expensive than by analytical equations and the numerical optimization process during sizing is more difficult to understand from the physical point of view.

Analog designers therefore often prefer equation-based sizing approaches. Notwithstanding the increasing significance

TABLE I
COMPARISON OF THE STATE-OF-THE-ART EQUATION-BASED SIZING TOOLS WITH THE HERE PRESENTED METHOD

Tool/author	Supported circuits	Equation set-up	Set-up time new circuit
IDAC [9]	amplifiers	topology database	months
BLADES [10]	op-amps, subblocks	subblock-based	long
OASYS [6]	op-amps	topology database	month
OPASYN [11]	op-amps	topology database	few weeks
Maulik [12]	op-amps	topology database	long
GPCAD [13]	op-amps	topology database	long
Leyn [14]	amplifiers	symbolic analysis	hours
AMGIE [15]	op-amps	topology database, symbolic analysis	8 h
Shi [16]	op-amps	symbolic analysis	seconds
Verhagen [17]	op-amps	symbolic analysis	seconds
Liu [18]	op-amps	symbolic analysis	seconds
COPRISCI [20]	op-amps	subblock-based	few days
This paper: HPEL	op-amps	subblock-based	seconds(*)

(*): new subblock 0.5-2 days

of simulation-based analog circuit design in deep submicron process technologies, an initial sizing based on analytical equations is the gold standard in analog design. It makes numerical performance evaluation within the sizing process unnecessary saving computational cost and being closer to the designer wish for physical insights. However to automatize the initial sizing process, the major obstacle is the automatic set-up of the design equations. This is where this paper presents a new approach.

Equation-based synthesis or sizing approaches (Table I) have presented fixed design plans for supported process technologies [6], [9]–[13], or apply symbolic analysis to create transfer functions automatically [14]–[18]. The methods support mainly op-amps [10]–[13], [15]–[20] and other types of amplifiers [9], [14].

Early equation-based methods [6], [9], [11]–[13] stored the equations topology-dependent. Topology libraries were developed containing a fixed equation set for every supported topology. To overcome the topology dependence, [10] splits up part of the equation-based description into subcircuits descriptions. However, only basic equations, as symmetry constraints and DC-performance constraints, are considered for the subcircuits. AC- and transient performance constraints are still restricted to a specific topology. Adding new topologies to these methods takes quite long as for every topologies a new equation-based description must be developed.

To reduce the set-up time of the equation-based description, symbolic analysis method were developed [14]–[18]. They automatically create the transfer function of a given topology. The transfer function, however, only represents the

AC-behavior of the circuit. To represent the transient and DC-behavior of the circuit, other methods are still needed. Designer knowledge is for instance used in [15] to include performance features for the transient behavior and symmetry constraints in the equation-based model.

To overcome the topology dependence, [20] presented a building block analysis to set up part of the equation-based description automatically. However, a method which allows an automatic set-up of the whole equation-based description of the circuit using the same equations as in the manual design process has not been published yet.

Such a method, called hierarchical performance equation library (HPEL), is presented in this paper. HPEL allows the automatic set-up of an equation-based description of a topology emulating the manual design process. AC-, DC- and transient behavior of a circuit are modeled in the same way as in the manual analog design process instantiating well-known model equations [33]–[36] automatically. The method supports many different op-amp topologies including several thousands of topology variants [2].

The main contributions of this paper are:

- A functional block-based hierarchical generic equation library (Sec. III - Sec. X), storing an equation set for every functional block in [1] which describes its behavior within the circuit. Compared to the state of the art, the equations are presented comprehensively, not in excerpts. The equations include hierarchically built performance equations and symmetry constraints automatically generated based on the hierarchy of a given circuit. The equation library provides a computer-oriented and hierarchical systematic of the behavior along the hierarchy the functional block composition of a circuit.
- Algorithms to automatically instantiated a behavior circuit model for a given netlist (Sec. XI). The generic equations in the library are automatically specified for a given topology. A nodal analysis model from Kirchhoff voltage and current laws analogous to circuit simulation leads to a topology-independent set-up of the comprehensive behavioral model for a given circuit netlist. Setting up the problem for a new circuit that is covered by the available equation library takes a few seconds. The circuit model can be fed into a constrained optimization solver for a fast sizing that mimics the sizing approach preferred by analog designers in practice.

The hierarchical character of the performance equation library along the functional block composition of a circuit represents a new level of generalization in equation-based design. The functional blocks and their behavioral models are general modules in analog design. They are used in advanced op-amps and other circuit classes. If such advanced design concepts for op-amps and other circuit classes are to be investigated, the performance library is not set up from scratch, but re-used and extended for new functional blocks only. Depending on the amount of additional new functionality, this is estimated to take between half a day and two days. Hence, the (manual) inclusion of new topologies into the HPEL library is fast compared to the state of the art as equation sets of functional blocks from lower levels are re-used. In topology-based approaches

HL 1: Devices	Normal transistors (nt), diode transistors (dt), capacitors (cap)
HL 2: Structures	Voltage biases (vb), current biases (cb), current mirror (cm), differential pairs (dp), analog inverter (inv)
HL 3: Amplification stage subblocks	Transconductor (tc), load (l), stage bias (b_s)
HL 4: Op-amp subblocks	Amplification stage (a), circuit bias (b_C), compensation (c_C) and load capacitor (c_L)
HL 5: Op-amps	Miller op-amp, Folded-cascode op-amp

Fig. 1. Functional blocks in op-amps

as, e.g., [15], the set-up time refers to one specific topology. Adding new functional blocks to the HPEL, however, means the inclusion of whole sets of topologies.

An application of HPEL is a sizing process described in Sec. XII. Circuits are sized in one minute without requiring much manual set-up. The HPEL sets up all constraints required for sizing fully automatically. This is different to numerical sizing approaches, which require a manual set-up of simulation, waveform postprocessing, parameters and constraints which takes around half a day of time.

Experimental results (Sec. XIII) present the circuit behavior models established through HPEL for four different circuits. Additionally, sizing results are presented obtained by the performance models.

II. FUNCTIONAL BLOCKS IN OP-AMPS

Every op-amp consists of a set of transistor blocks which can be characterized by their function and are called functional blocks in the following. These functional blocks can be hierarchically structured (Fig. 1). With every hierarchy level, the structural composition of the functional block becomes less definable however its overall function in the circuit becomes more clear. The functional block types on every hierarchy level are sketched in the following. A complete description with structural examples is given in [1].

Hierarchy level 1 consists of devices, e.g., *capacitors* (Fig. 2a cap), and transistors. Two types of transistors are distinguished by their self-connections. *Normal transistors* (nt) do not have any self-connection, e.g., Fig. 2a, nt_1 . *Diode transistors* (dt) have a gate-drain connection, e.g., Fig. 2a dt_1 .

Hierarchy level 2 consists of transistor structures: *voltage bias* vb_k (Fig. 2a vb_1, vb_3), *current bias* cb_k (Fig. 2a cb_1, cb_6), *analog inverter* inv_k (Fig. 2a inv_1), *differential pair* (Fig. 2c N_1, N_2). A voltage bias and a current bias may form a *current mirror* (cm_k), e.g., Fig. 2a cm_5 . However, cases exist where no current mirrors are formed [1], e.g., Fig. 2a, vb_2, cb_4 . Types of differential pairs are: *simple* (dp_k), *cascode* (cdp_k), e.g., Fig. 2a $P_1 - P_4$, or *folded-cascode* ($fcdp$), e.g. Fig. 2b N_1, N_2, P_1, P_2 . A cascode or folded-cascode differential pair consists of a simple differential pair connected to a *gate-connected couple* (gcc , e.g., Fig. 2a P_3, P_4 ; Fig. 2b P_1, P_2).

Hierarchy level 3 consists of the amplification stage subblocks, which are the *transconductor* tc , the *load* l and the *stage bias* b_s . For the transconductor, two main types exist: non-inverting tc_{ninv} (Fig. 2c tc_1) and inverting tc_{inv} (Fig. 2c $tc_{2,1}$). The non-inverting transconductor is further divided into three types: simple tc_s (Fig. 2c tc_1), complementary tc_c , (Fig. 2d tc_1) and common-mode feedback (CMFB) tc_{CMFB}

TABLE II
HIERARCHICAL PERFORMANCE EQUATION LIBRARY

	Symmetry constraints	Functional block behavioral constraints	Intermediate performance equations	Op-amp performance equations
HL 1: Devices			<ul style="list-style-type: none"> • Saturation drain-source voltage • Net capacitance 	<ul style="list-style-type: none"> • Area • Quiescent power
HL 2: Structures	<ul style="list-style-type: none"> • Voltage and current bias 	<ul style="list-style-type: none"> • Current mirror behavior 		
HL 3: Amplification stage subblocks	<ul style="list-style-type: none"> • Load • Non-inverting transconductor 	<ul style="list-style-type: none"> • Complementary transconductor and stage bias 	<ul style="list-style-type: none"> • Transconductance • Output conductance 	
HL 4: Op-amp subblocks	<ul style="list-style-type: none"> • Inverting stages 	<ul style="list-style-type: none"> • Output voltage offset 	<ul style="list-style-type: none"> • Stage output resistance • Stage open-loop gain • Stage non-dominate poles • Stage zeros 	<ul style="list-style-type: none"> • Common-mode input voltage • Output voltage • Common-mode rejection ratio • Unity-gain bandwidth
HL 5: Op-amps			<ul style="list-style-type: none"> • Dominant pole • Positive zero 	<ul style="list-style-type: none"> • Open-loop gain • Slew Rate • Phase margin

(Fig. 2b t_{CMFB}). The load consists of one or two load parts (l_p) (Fig. 2b). The stage bias is either of type current bias (Fig 2c, $b_{s,1}$) or of type voltage bias (Fig 2c, $b_{s,2,2}$).

Hierarchy level 4 consists of the op-amp subblocks which are the *amplification stages* a , the *circuit bias* b_O (Fig. 2d), the *compensation capacitor* (c_C) (Fig. 2c), and *load capacitor* (c_L). Two types of amplification stages exist: non-inverting a_{ninv} (Fig. 2c a_1), and inverting a_{inv} (Fig. 2c $a_{2,2}$). The non-inverting amplification stage can be further divided into simple a_s (Fig. 2c a_1) and complementary first stage a_c (Fig. 2d a_1), and common mode feedback stage a_{CMFB} (Fig. 2b a_{CMFB}).

Hierarchy level 5 consists of the op-amp itself. It is fully-differential or has a single output.

The functional blocks in an op-amp are identified as detailed in [1]. It uses a formalized structural definition of every functional block for an automatic recognition. Starting on the lowest hierarchy level, the functional blocks are hierarchically identified by analyzing the pin connections in the circuit netlist based on the structural definitions of the functional blocks. The result are the specific functional blocks of a given netlist according to the hierarchy levels in Fig. 1. Examples are the decompositions in Fig. 2. It is worth noting that the functional attribution of a group of transistors depends on its context, i.e., its connection to other circuit parts. The respective performance equations of each functional block type and their automatic set-up are presented in the following.

III. OVERVIEW OF THE HIERARCHICAL PERFORMANCE EQUATION LIBRARY

The hierarchical performance equation library uses the functional block description of op-amps to store the equation describing the op-amp behavior topology independent. It distinguishes between two main groups of equations: the basic model and the op-amp performance model.

The *basic model* describes the current and voltage flow in the circuit. It contains information gained based on the circuit netlist and an analysis of its devices. It comprises the variables of the circuit, Kirchoffs Current and Voltage Law and models for the devices. The variables can be reduced by using information from higher functional block levels, however the major set-up is based on the first hierarchy level.

The *op-amp performance model* describes the AC-, DC-, and transient behavior of the op-amp. It contains information gained from the hierarchical composition of functional

blocks. It comprises symmetry constraints, functional block constraints, intermediate performance equations and op-amp performance equations. An overview of the op-amp performance model part of the hierarchical equation library is given in Table II. For each hierarchy level, the most important equations or constraints are given. The ordering from left to right represents an abstraction from constraints to performance and it corresponds to the functional abstraction from top to bottom through the hierarchy levels. Equations based on functional blocks of low hierarchy levels highly depend on the transistor structure, e.g., the equations to describe the output conductance of a functional block. To set up the equations of the open-loop gain, the transistor structure of op-amp is ignored. This hierarchical structuring allows us to generalize the op-amp equations such that we obtain an automatic set-up of the design equations independent of the topology (Sec. XI).

In the following, variables and equations of both model types are described in detail.

IV. VARIABLES

The variables of the equation-based topology description can be divided into two groups: device specific variables and op-amp performance variables.

Device specific variables: Depending on the device type, a set of variables is automatically derived. For a transistor t_k , this set is:

$$\mathbf{t}_k^T = \{w_k, l_k, gm_k, gd_k, i_{DS,k}, v_{GS,k}, v_{DS,k}\} \quad (1)$$

w_k, l_k are the width and length of the transistor, gm_k, gd_k its transconductance and output conductance, $i_{DS,k}$ its drain-source current and $v_{GS,k}, v_{DS,k}$ its gate-source and drain-source voltage.

Op-amp performance variables: The set of characteristic performance features whose equations are automatically set up based on the HPEL is:

$$\mathbf{z}^T = \{z_D, z_{QP}, z_{v_{cm,min/max}}, z_{v_{out,min/max}}, z_{f_{GBW}}, z_{SR}, z_{AD0}, z_{CMRR}, z_{PM}\} \quad (2)$$

z_D describes the gate area of the circuit, z_{QP} its quiescent power, $z_{v_{cm,min/max}}$ is the minimal, respective maximal common-mode input voltage, $z_{v_{out,min/max}}$ the minimal/maximal output voltage of the op-amp, z_{AD0} is its open-loop gain, $z_{f_{GBW}}$ is the unity-gain bandwidth, z_{SR} the slew rate, z_{CMRR} the common-mode rejection ratio, z_{PM} is the

phase margin. The performance features describe the characteristic op-amp behavior. Additional to them, intermediate performance variables, e.g., output resistance R_{out,a_j} of a stage a_j or poles and zeros of an op-amp \mathbf{z}_P exist.

V. KIRCHOFFS CURRENT AND VOLTAGE LAW

By automatically analyzing the graph description of the netlist, Kirchoffs Current Law (KCL) is set up for every node $l \in \mathcal{N}$ in the circuit:

$$\forall l \in \mathcal{N} \sum_k i_{DS_k} = 0, \quad (3)$$

Kirchoffs Voltage Law is expressed efficiently by the voltage potentials of the circuit nodes as in circuit simulation. The voltage variables are therefore all n_N node voltages \mathbf{v}_N :

$$\begin{aligned} \mathbf{v}_N^T &= [v_{N,1}, v_{N,2}, \dots, v_{N,n_N}], v_{N,k} \in \mathbb{R}, k = 1, 2, \dots, n_N \\ [\mathbf{v}_{GS}^T \mathbf{v}_{DS}^T]^T &= \mathbf{A} \cdot \mathbf{v}_N, \text{ with } \mathbf{A} \text{ as nodal incidence matrix.} \end{aligned} \quad (4)$$

VI. TRANSISTOR BEHAVIOR MODEL

For every device in the circuit, a model is needed which describes its behavior depending on its variables. Therefore, for every device type on level 1, a behavioral model is stored in the equation library. For transistors, this is the Shichman-Hodges model [37]. It is the simplest transistor model and defines three operating regions for a transistor, off, linear, and saturation. Analytical equations exist for all operating regions. The drain-source current of an nmos transistor t_k in saturation is for instance described by:

$$i_{DS,k} = \frac{\mu_k C_{ox,k} W_k}{2 L_k} (v_{GS,k} - v_{th,k})^2 (1 + \lambda_k v_{DS,k}) \quad (5)$$

Process parameters, e.g., threshold voltage v_{th} , are specified by the underlying process technology. Equations for other operation regions are implemented analogously.

Constraints for the transistor voltages guarantee that the transistor operates in the specified region. For saturation, these are:

$$\begin{aligned} v_{GS,k} - v_{th,k} &\geq 0 \\ v_{GS,k} - v_{th,k} &< v_{DS,k} \end{aligned} \quad (6)$$

The transconductance and output conductances gm_k, gd_k of a transistor are calculated by the differentiation of the drain-source current with respect to the transistor voltages. For the saturation region, following equations are obtained:

$$gm_k = \frac{\partial i_{DS,k}}{\partial v_{GS,k}} = \sqrt{2\mu_k C_{ox,k} \frac{W_k}{L_k} i_{DS,k}} \quad (7)$$

$$gd_k = \frac{\partial i_{DS,k}}{\partial v_{DS,k}} = \lambda_k \cdot i_{DS,k} \quad (8)$$

The saturation region can be further divided into weak, moderate and strong inversion. An overview how the three inversions region are integrated into equation-based modeling is given in [38].

VII. SYMMETRY CONSTRAINTS

Symmetry constraints are crucial in analog circuits to minimize mismatch, e.g., due to channel length modulation or local manufacturing variations. Symmetry constraints are derived for structures (HL 2), subblocks of amplification stages (HL 3) and op-amp subblocks (HL 4). They reduce the number of variables of the performance model.

A. Hierarchy Level 2: Structures

For transistors in a voltage or current bias, we define that two transistors t_i, t_j connected at their gates $t_i.g, t_j.g$ must have equal lengths l_{t_i}, l_{t_j}

$$\forall t_i, t_j \in (T_{vb,\Phi} \cup T_{cb,\Phi}) t_i.g \leftrightarrow t_j.g \Rightarrow l_{t_i} = l_{t_j} \quad (9)$$

$T_{vb,\Phi}$ is the set of transistors of doping Φ being part of the voltage biases in the circuit. $T_{cb,\Phi}$ is the set of transistors of the same doping Φ being part of current biases.

B. Hierarchy Level 3: Amplification Stage Subblocks

The DC current flow must be symmetric in the subblocks of a non-inverting stage. We therefore define that the transconductor of the non-inverting stage $tc_{ninv,k}$ and its load l_k must have symmetrical geometries:

$$\begin{aligned} \forall tc_{ninv,k} \in \mathcal{M}_{tc_{ninv}} \{t_{k,i,\Phi}, t_{k,j,\Phi}\} &= tc_{ninv,k} \\ \wedge l_{t_{k,i}} = l_{t_{k,j}} \wedge w_{t_{k,i}} &= w_{t_{k,j}} \end{aligned} \quad (10)$$

$$\forall t_i, t_j \in (T_l) t_i.g \leftrightarrow t_j.g \Rightarrow (l_{t_i} = l_{t_j} \wedge w_{t_i} = w_{t_j}) \quad (11)$$

$\mathcal{M}_{tc_{ninv}}$ is the set of non-inverting transconductor in the op-amp and T_l the set of transistors forming the load.

C. Hierarchy Level 4: Op Amp Subblocks

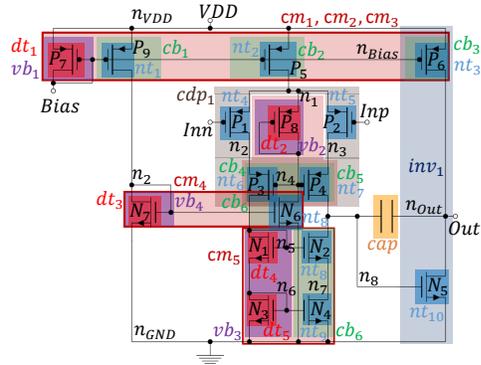
Symmetrical op-amps and fully differential two-stage op-amps have two second stages. They must be symmetrical:

$$\begin{aligned} \forall t_m \in a_{2,1}, t_n \in a_{2,2} [(t_m.pos = t_n.pos) \\ \rightarrow (w_{t_m} = w_{t_n} \wedge l_{t_m} = l_{t_n})] \end{aligned} \quad (12)$$

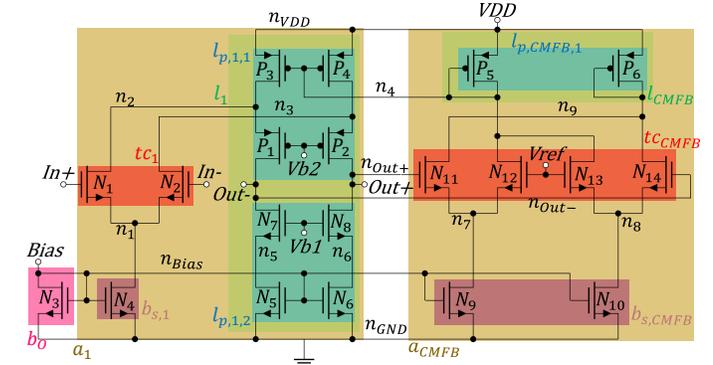
$t_k.pos$ gives the position of a transistor, e.g., n-type transistor and connected to the ground net. The transistors on equal positions should have equal geometries. In the symmetrical op-amp in Fig. 2c, the transistors N_4, N_5 have equal positions and therefore should have the same sizes. The other transistor pairs are P_5, P_6 and P_3, P_4 .

VIII. FUNCTIONAL BLOCK BEHAVIORAL CONSTRAINTS

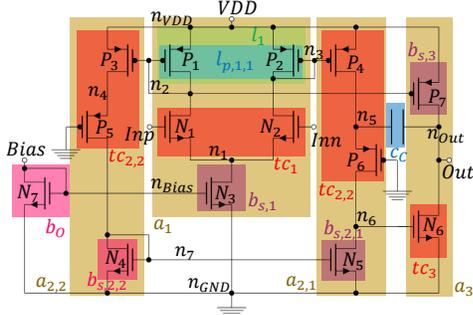
Behavioral constraints on a functional block are constraints on its transistor variables required to ensure the proper functionality of the block. Behavioral constraints are derived for structures (HL 2), amplification stage subblocks (HL 3) and op-amp subblocks (HL 4).



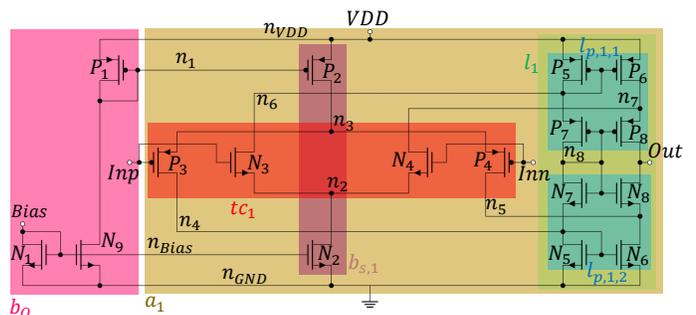
(a) Telescopic op-amp [colored background: functional blocks of HL 1 - 2]



(b) Folded-cascode op-amp with CMFB [colored background: functional blocks of HL 3 - 4]



(c) Symmetrical op-amp with high PSRR [33] [colored background: functional blocks of HL 3 - 4]



(d) Complementary op-amp [colored background: functional blocks of HL 3 - 4]

Fig. 2. Different op-amp topologies

A. Hierarchy Level 2: Structures

Behavioral constraints for specific types of current mirrors are instantiated on this level. An example is the cascode current mirror (e.g. Fig 2a, $N_1 - N_4$). In this type of current mirror, the voltage potentials of the inner nets, e.g., Fig. 2a, n_6, n_7 , must be equal to suppress the effect of the channel length modulation. To obtain equal voltages, the ratio of the widths of the transistors in the current mirror must be restricted:

$$\frac{w_{ccm,vb,d}}{w_{ccm,cb,d}} = \frac{w_{cm,vb,s}}{w_{cm,cb,s}} \quad (13)$$

$w_{ccm,vb,d}, w_{ccm,vb,s}$ are the drain and the source transistor of the voltage bias in the cascode current mirror. $w_{ccm,cb,d}, w_{ccm,cb,s}$ are the drain and the source transistor of the current bias in the cascode current mirror. Please note that the transistor length is already restricted by (9).

B. Hierarchy Level 3: Amplification Stage Subblocks

A behavioral constraint on the amplification stage subblock level exists for the complementary transconductor tc_c . The transconductance of the transistors in the n-doped differential pair $gm_{dp,n,i}|_{i=1,2}$ and p-doped differential pair $gm_{dp,p,j}|_{j=1,2}$ of tc_c must be equal.

$$gm_{dp,n,i}|_{i=1,2} = gm_{dp,p,j}|_{j=1,2} \quad (14)$$

Also the currents of the differential pairs generated with the n- and p-doped transistors in the stage bias $b_{s,c}$ must be equal:

$$|i_{DS,b_{s,c},n}| = |i_{DS,b_{s,c},p}| \quad (15)$$

C. Hierarchy Level 4: Op-Amp Subblocks

A constraint on the op-amp subblock level is the output voltage offset constraint for two stage op-amps. To suppress an offset voltage on the output voltage by equal input voltage, the voltage potentials at the first stage output nets $n_{a_1.out_1}, n_{a_1.out_2}$, e.g., Fig. 2a, $n_{a_1.out_1} = n_5, n_{a_1.out_2} = n_8$ must be equal.

$$a_2 \in \mathcal{M} \Rightarrow v_{n_{a_1.out_1}} = v_{n_{a_1.out_2}} \quad (16)$$

\mathcal{M} is the set of functional blocks of an op-amp topology.

IX. INTERMEDIATE PERFORMANCE EQUATIONS

Hierarchy levels 1, 3-5 are considered to establish all intermediate performance equations. They are only instantiated for a functional block if an op-amp performance equation requires them.

A. Hierarchy Level 1: Devices

The saturation drain-source voltage of a transistor and the net capacitance of a net in the circuit are equations generated based on the device information.

1) *Saturation Drain-Source Voltage*: The saturation drain-source voltage is the voltage at least needed to keep a transistor in saturation. According to (6), this is:

$$v_{DS,sat,i} = \begin{cases} v_{GS,i} - v_{th,i}, & t_i.type = nt \\ v_{GS,i}, & t_i.type = dt \end{cases} \quad (17)$$

considering that for a diode transistor dt_k , $v_{GS,k} = v_{DS,k}$.

2) *Net Capacitance*: The capacitance C_{n_i} of a net n_i depends on the pins P_{n_i} connected to n_i :

$$C_{n_i} = \sum_{p_j \in P_{n_i}} C_{p_j} \quad (18)$$

C_{p_j} is the capacitance arising by the pin p_j . The corresponding equations to calculate C_{p_j} are given in [36].

B. Hierarchy Level 3: Amplification Stage Subblocks

Transconductance and output conductances of the functional blocks are important properties to be described on this level.

1) *Transconductance*: The transconductance of a transconductor is defined by one of the transistors $t_{tc,i,in}$ whose gate is connected to the input signal of the stage.

$$gin_{tc,i} = gm_{t_{tc,i,in}} \quad (19)$$

In a non-inverting stage, $t_{tc,i,in}$ is one of the transistors of the differential pair. Due to symmetry, the transconductance of both transistors is equal. In an inverting stage, $t_{tc,i,in}$ is the transistor whose gate is connected to the output of the previous stage. In op-amps with two second stages, the transconductance of only one of the two stages must be calculated due to symmetry.

For the calculation of the transconductance of the complementary transconductor (Fig. 2d), the transconductances of the transistors in the pmos differential pair and the nmos differential pair must be considered:

$$gin_{tc_c} = gm_{t_{tc,in,n}} + gm_{t_{tc,in,p}} \quad (20)$$

2) *Output conductance*: The computation of $gout_i$ for a functional block m_i depends on its inner structure. It is distinguished between functional blocks consisting of one- and two-transistor stacks. A transistor stack is defined as a sequence of transistors having a drain-source connection [1]. N_1, N_3 in Fig. 2a is an example of a two-transistor stack.

$$gout_i = \begin{cases} gd_{t_{i,out}}, & \{t_{i,out}\} = ts_i \subseteq m_i \\ \frac{gd_{t_{i,out}}gd_{t_{i,supply}}}{gm_{t_{i,out}}}, & \{t_{i,out}, t_{i,supply}\} = ts_i \subseteq m_i \end{cases} \quad (21)$$

If the functional block m_i consists of one-transistor stacks, only the output conductance of the transistor in m_i connected to the stage output is relevant for the calculation. If m_i consists of two-transistor stacks, the transistor connected to the stage output and the transistor connected to the supply voltage rail are relevant. The type of functional block as load, transconductor and stage bias is irrelevant. All three types consist of one or two transistor stacks. If the functional block consists of two transistor stacks, the stacks are symmetrical. In non-symmetrical load parts [1], the output-connected transistor

stack is only relevant for calculations. Hence, in Fig. 2c, $gout_{tc_1} = gd_{N_1} = gd_{N_2}$ and $gout_{tc_2,2} = \frac{gd_{P_5}gd_{P_3}}{gm_{P_5}}$.

Further differentiation must be made for load parts including a gate-connected couple being part of a cascode or folded-cascode differential pair (Sec. II):

$$gout_i = \begin{cases} \frac{gd_{t_{i,out}}gd_{t_{c_1,1}}}{gm_{t_{i,out}}}, & \{t_{i,out}\} = ts_i \subseteq m_i \\ & \wedge \{t_{c_1,1}, t_{i,out}\} \subset cdp_k \\ \frac{gd_{t_{i,out}}(gd_{t_{i,supply}} + gd_{t_{c_1,1}})}{gm_{t_{i,out}}}, & \{t_{i,out}, t_{i,supply}\} = ts_i \subseteq m_i \\ & \wedge \{t_{c_1,1}, t_{i,out}\} \subset fcdp_k \end{cases} \quad (22)$$

The output conductance of one of the transistors of the differential pair must be included in these calculations. Thus for the load part formed by P_3, P_4 in Fig. 2a $gout_{l_{p,1,1}} = \frac{gd_{P_4}gd_{P_2}}{gm_{P_4}}$ and in Fig. 2b $gout_{l_{p,1,1}} = \frac{gd_{P_2}(gd_{P_4} + gd_{N_2})}{gm_{P_2}}$.

In symmetrical op-amp and CMFB stages, the output conductance $gout_i$ of the load part is the transconductance of one of the transistors connected with its gate to the output of the stage. The load part consists only of voltage biases [1]:

$$gout_i = gm_{t_{g,out}}, \quad m_i.type = l_p \wedge m_i = \{vb_{i,1}, vb_{i,2}\} \quad (23)$$

Hence, in Fig. 2c, $gout_{l_{p,1,1}} = gm_{P_1} = gm_{P_2}$

C. Hierarchy Level 4: Op-Amp Subblocks

The output resistance, the open-loop gain and the non-dominant poles and zeros of an amplification stage are calculated on this level.

1) *Stage Output Resistance*: The output resistance of an amplification stage is described by the output conductances of the k functional blocks of the stage, e.g. stage biases, load parts and transconductors, connected to the stage output net.

$$R_{out,i} = \frac{1}{\sum_{j=1}^k gout_j} \quad (24)$$

For the symmetrical op-amp (Fig. 2c), the output resistance of the first stage R_{out,a_1} is for example calculated by $gout_{tc_1}$ and $gout_{l_{p,1,1}}$. For the folded-cascode first stage in Fig. 2b, the output resistance is $R_{out,a_1} = \frac{1}{gout_{l_{p,1,1}} + gout_{l_{p,1,2}}}$.

2) *Stage Open-Loop Gain*: The open-loop gain of a stage $A_{D0,i}$ is calculated by the transconductance $gin_{tc,i}$ of its transconductors (Sec. IX-B1) and its output resistance $R_{out,i}$:

$$A_{D0,i} = gin_{tc,i} \cdot R_{out,i} \quad (25)$$

3) *Stage Non-Dominant Poles*: Non-dominant poles arise for every stage in the op-amp. They must be calculated for every transistor t_k on the signal path from input to output. The pole of the transistor t_k is calculated by:

$$f_{ndp,t_k} = \frac{gm_{t_k}}{2\pi C_{n_j}} \quad (26)$$

C_{n_j} is the net capacitance of the net the signal passes by before encountering t_k . It is calculated by (18) and contains the parasitics emerging from the transistor pins as well as the capacitance of the capacitors connected to the net.

If a compensation capacitor is connected between the input and the output of a stage, the equation of non-dominant pole at the input transistor of the stages changes to:

$$f_{ndp,inv,C_c} = \frac{g_{intc_{inv}}}{2\pi(C_{n_{out}} + \frac{C_{n_{tc,inv,ig}} \cdot C_{n_{out}}}{C_C} + C_{n_{tc,inv,ig}})} \quad (27)$$

$g_{intc_{inv}}$ is the transconductance of the stage. $C_{n_{tc,inv,ig}}$ is the capacitance of the gate net carrying the input signal of the stage. $C_{n_{out}}$ is the capacitance of the output net of the stage and C_C the capacitance value of the compensation capacitor.

4) *Stage zeros*: Zeros are evoked by non-dominant poles if they are a mirror pole, i.e., only half of the signal is influenced by it. They are set to occur at twice of the frequency of the mirror pole $f_{ndp,mir}$:

$$f_{z,mir} = 2 \cdot f_{ndp,mir} \quad (28)$$

D. Hierarchy Level 5: Op-Amp

The complete composition of the op-amp must be considered to calculate the dominant pole and the positive zero.

1) *Dominant Pole*: The dominant pole is the pole at the smallest frequency in an op-amp. It occurs mostly at the output net of the first stage and is calculated by:

$$f_{dp} = \frac{1}{2\pi C_{n_{out}} g_{intc_2} \prod_{i=1}^2 R_{out,i}} \quad (29)$$

$C_{n_{out}}$ is the capacitance at the output net of the first stage, g_{intc_2} the transconductance of the second stage transistor and $R_{out,j}$ the output resistance of the amplification stages. For single-stage op-amps, g_{intc_2} and $R_{out,2}$ are set to one.

In symmetrical op-amps, the dominant pole occurs at the output net of the second stage. The equation changes to:

$$f_{dp} = \frac{1}{2\pi C_{n_{out}} g_{mtc_3} \prod_{i=2}^3 R_{out,i}} \quad (30)$$

where $C_{n_{out}}$ is the capacitance at the output net of the second stage. If no third stage is part of the symmetrical op-amp, g_{mtc_3} and $R_{out,3}$ are set to one.

2) *Positive Zero*: In op-amps with compensation capacitor C_C , a positive zero exists. It is calculated by:

$$f_{pz} = \frac{1}{2\pi C_C \left(\frac{1}{g_{intc_{inv,k}}} - \frac{1}{g_{dR_C}} \right)} \quad (31)$$

$g_{intc_{inv,k}}$ is the transconductance of the inverting transistor connected by C_C to a previous stage. If a compensation resistor R_C is part of the circuit, g_{dR_C} is the output conductance of the resistor emulating the compensation resistor, otherwise $g_{dR_C} = 1$.

X. OP-AMP PERFORMANCE EQUATIONS

Analogous to the equations and constraints before, the performance features of an op-amp are ordered hierarchically. Some performance equations only need the device level information as input (HL 1). Others are based on op-amp subblocks (HL 4) or on the whole op-amp (HL 5).

A. Hierarchy Level 1: Devices

The area and quiescent power of the op-amp is calculated based on device level information.

1) *Area*: An estimation of the area of the circuit is calculated through the gate areas of all k transistors:

$$z_D = \sum_{i=1}^k W_i \cdot L_i \quad (32)$$

2) *Quiescent Power*: The quiescent power z_{QP} is the product of the positive supply voltage v_{VDD} subtracted by negative voltage v_{VSS} with the sum of the n currents flowing into the positive supply voltage net n_{VDD} . If the bias current of the circuit i_{Bias} is applied to an nmos transistor, it must be added to the currents flowing into n_{VDD} .

$$z_{QP} = (v_{VDD} - v_{VSS}) \cdot \begin{cases} \sum_{j=1}^n |i_j|, & t_{Bias} \cdot \Phi = p \\ \sum_{j=1}^n |i_j| + i_{bias}, & t_{Bias} \cdot \Phi = n \end{cases} \quad (33)$$

B. Hierarchy Level 4: Op-Amp Subblocks

Performance features determined by one amplification stage are formulated on this level. These are common-mode input voltage, output voltage, common-mode rejection ratio (CMRR) and unity-gain bandwidth.

1) *Common-mode Input Voltage*: The common-mode input voltage describes the range in which the input voltage can vary without changing the behavior of the op-amp. We can specify a maximum $z_{v_{cm,max}}$ and a minimum $z_{v_{cm,min}}$ common-mode input voltage. The two voltage loops which describe $z_{v_{cm,max}}$, $z_{v_{cm,min}}$ are either over the load of the first stage l_1 or over its stage bias $b_{s,1}$. Therefore, we can define the two limiting values by v_{cm,l_1} , $v_{cm,b_{s,1}}$.

$z_{v_{cm,max}}$, $z_{v_{cm,min}}$ are defined depending which of $v_{supply,b_{s,1}}$, v_{supply,l_1} equals v_{VDD} , v_{VSS} .

$$\begin{aligned} v_{supply,b_{s,1}} &= v_{VDD} \wedge v_{supply,l_1} = v_{VSS} \\ \Rightarrow z_{v_{cm,max}} &= v_{cm,b_{s,1}} \wedge z_{v_{cm,min}} = v_{cm,l_1} \\ v_{supply,b_{s,1}} &= v_{VSS} \wedge v_{supply,l_1} = v_{VDD} \\ \Rightarrow z_{v_{cm,max}} &= v_{cm,l_1} \wedge z_{v_{cm,min}} = v_{cm,b_{s,1}} \end{aligned} \quad (34)$$

For loads connected to both supply voltage rails, e.g. Fig. 2b, the supply voltage rail opposite to $v_{supply,b_{s,1}}$ is considered.

If the transistors in the paths are in saturation and in strong inversion, $v_{cm,b_{s,1}}$ and $v_{cm,l_{p,1,1}}$ are defined by the minimum/maximum voltage which is allowed when keeping all transistor in saturation. For a single transistor, this voltage is defined by the minimum saturation voltage (17). Hence, $v_{cm,b_{s,1}}$ is defined as:

$$v_{cm,b_{s,1}} := v_{supply,b_{s,1}} + v_{GS,tc_1} + \sum_{i=1}^{|b_1|} v_{DS,sat,i} \quad (35)$$

Determining v_{cm,l_1} is more complex, as the structure of the load highly varies [1]. Two relevant voltage paths e_1 , e_2 exist having the smallest possible number of voltage drops. Each path starts from one of the outputs of the first stage transistor tc_1 going to the supply-voltage rail of the

load n_{supply,l_1} . In the folded-cascode op-amp (Fig. 2b), $e_1 = \{P_3\}, e_2 = \{P_4\}$. In the telescopic op-amp, (Fig. 2a) $e_1 = \{P_3, N_1, N_3\}, e_2 = \{P_4, N_2, N_4\}$. For the calculation of v_{cm,l_1} the path e_k is chosen with the most diode transistors. For diode transistors, $v_{DS,sat} = v_{GS}$, such that they have a much higher impact on the input voltage range as normal transistors. If the transistors in the paths are in saturation and in strong inversion, v_{cm,l_1} is defined by:

$$v_{cm,l_1} := v_{supply,l_1} + v_{th,tc_1} + \sum_{m=1}^{|e|} \begin{cases} -(v_{DS,sat,m}), & t_m \subset gcc_m \\ v_{DS,sat,m}, & else \end{cases} \quad (36)$$

v_{th,tc_1} is the threshold voltage of a transistor of the transconductor of the first stage tc_1 . If a transistor of a gate-connected couple gcc_k is in the path e , e.g. P_3, P_4 in Fig. 2a, it introduces a negative value for $v_{DS,sat,k}$. It has a different substrate doping than the other transistors in the load relevant for e .

2) *Output Voltage*: The output voltage swing is described by the last stage of an op-amp. A maximum value $z_{v_{out,max}}$ and a minimum value $z_{v_{out,min}}$ are defined by the shortest paths from the output of the op-amp to the supply-rails e_{VDD}, e_{VSS} . The paths contain the transistors being part of transistor stacks connecting the supply-voltage rails to the output. If the transistors are supposed to be in saturation and in strong inversion, the corresponding equations are:

$$z_{v_{out,max}} = v_{VDD} + \sum_{i=1}^{|e_{VDD}|} v_{DS,sat,i} \quad (37)$$

$$z_{v_{out,min}} = v_{VSS} + \sum_{i=1}^{|e_{VSS}|} v_{DS,sat,i} \quad (38)$$

with $v_{DS,sat,i}$ described by (17).

3) *Common-mode Rejection Ratio*: For non-fully differential op-amp topologies, an analytical equation can be derived that gives a good approximation of the static systematic common-mode rejection ratio (CMRR_s). For all op-amps but symmetrical op-amps, the CMRR_s only depends on the structure of the first stage.

$$z_{CMRR} = 2A_{D0,1} \cdot \frac{gm_{l_1,g.out}}{gout_{b_{s,1}}} \quad (39)$$

$A_{D0,1}$ is the open-loop gain of the first stage of the op-amp (25). $gout_{b_{s,1}}$ the output conductance of the first stage bias calculated according to Sec. IX-B2. $gm_{l_1,g.out}$ is the transconductance of the load transistor connected with its gate to one of the output nets of the first stage. If the gates of two load transistors are connected to the output of the first stage, any of these two can be chosen. They have equal gm -values, as the load of an op-amp is symmetric. If no load transistor's gate is connected to the output of the first stage the equation to calculate the CMRR_s changes:

$$z_{CMRR} = 2 \cdot \frac{gin_{tc_1}}{gout_{b_{s,1}}} \quad (40)$$

gin_{tc_1} is the transconductance of the transconductor of the first stage calculated according to Sec. IX-B1.

The CMRR of the symmetrical op-amp is also defined by the open-loop gain of the second stage $A_{D0,2}$:

$$z_{CMRR_{sym}} = 2A_{D0,1} \cdot A_{D0,2} \cdot \frac{gm_{l_1,g.out}}{gout_{b_{s,1}}} \quad (41)$$

For fully-differential op-amps, the CMRR_s also depends on the common-mode feedback circuit and is not discussed in this paper. In complementary op-amps, the two stage bias types of the first stage, pmos and nmos, must be considered.

4) *Unity-gain bandwidth*: The unity-gain bandwidth $z_{f_{GBW}}$ is calculated by the first stage transconductor tc_1 and the capacitance of the first stage output net $C_{n_{a_1,out}}$:

$$z_{f_{GBW}} = \frac{gin_{tc_1}}{2\pi C_{n_{a_1,out}}} \quad (42)$$

The equation for $z_{f_{GBW}}$ differs slightly for symmetrical op-amps, as the second stage impacts the unity-gain bandwidth:

$$z_{f_{GBW}} = \frac{A_{D0,1} \cdot gin_{tc_2}}{2\pi C_{n_{a_2,out}}} \quad (43)$$

$A_{D0,1}$ is the first stage open-loop gain, gin_{tc_2} , the transconductance of the second stage transconductor, and $C_{n_{a_2,out}}$ the capacitance of the second stage output net connected to a capacitor.

C. Hierarchy Level 5: Op-Amp

The overall op-amp structure is considered for the calculation of open-loop gain, the slew rate and the phase margin.

1) *Open-loop Gain*: The open-loop gain of an op-amp is the product of the open-loop gains of its n stages:

$$z_{A_{D0}} = \prod_{k=0}^n A_{D0,k} \quad (44)$$

2) *Slew Rate*: The slew rate z_{SR} of a circuit is calculated from the bias currents of the n stages and the capacitances of the output nets of the stages,

$$z_{SR} = \min\left\{\frac{|i_{DS,b_{s,1}}|}{C_{n_{out,1}}}, \dots, \frac{|i_{DS,b_{s,n}}|}{C_{n_{out,n}}}\right\} \quad (45)$$

where $i_{DS,b_{s,k}}$ is the drain-source current of a transistor part of the stage bias $b_{s,k}$ of the stage k . $C_{n_{out,k}}$ is the capacitance of the stage output net calculated by (18). For symmetrical op-amps, the first stage output net does not have to be considered. However, if one of the input transistors of the first stage is shut down, the bias current of the first stage is amplified and mirrored by the current mirror forming the first stage load and the second stage transconductor, e.g., Fig. 2c P_2, P_4 . Therefore, twice the bias current of the second stage must be considered during slew rate calculations.

In a folded-cascode op-amp, the current $i_{DS,l_B,GCC}$ of the two transistors biasing the gate-connected couple, e.g., Fig. 2b P_3, P_4 , must be considered during slew rate calculation. The smallest current of $i_{DS,l_B,GCC}, i_{DS,b_{s,1}}$ restricts the slew rate.

Required Circuit netlist with devices D and nodes N , Functional block decomposition results with functional blocks FB [1]
for all $d \in D$
createDeviceVariables() (1)
createDeviceModelEquations() (5) - (8)
for all $n \in N$
createKCLEquation() (3)
createVoltageVariables() (4)
for all $fb \in FB$
createSymmetryConstraints() (9) - (12)
createFunctionalBlocksBehaviorConstraints() (13) - (16)
$z =$ createPerformanceVariables() (2)
for all $z \in z$
createPerformanceEquations() (17) - (47)
Return Analytical equation-based circuit model

Fig. 3. Automatic instantiation of an equation-based circuit model for a given topology

3) *Phase Margin*: The phase margin z_{PM} is calculated by the non-dominant poles and zeros of the circuit:

$$z_{PM} = \frac{\pi}{2} - \sum_{i=1}^m \operatorname{atan}\left(\frac{f_{GBW}}{f_{ndp_i}}\right) + \sum_{j=1}^n \operatorname{atan}\left(\frac{f_{GBW}}{f_{z_j}}\right) \quad (46)$$

f_{GBW} is the unity-gain bandwidth of the circuit. A positive zero has a negative influence on the phase margin, like non-dominant poles.

The non-dominant poles and zeros must be at least an order of magnitude larger than the dominant pole.

$$\forall_{f_i \in (F_{ndp} \cup F_z)} \frac{f_i}{f_{dp}} > 10 \quad (47)$$

XI. AUTOMATIC INSTANTIATION OF THE EQUATION-BASED CIRCUIT MODEL BASED ON HPEL

Fig. 3 shows the automatic synthesis of the equation-based circuit model for a given op-amp topology. The input of the algorithm are the circuit netlist and the results of the functional block decomposition method in [1], which automatically identifies all functional blocks described in Sec. II in a circuit netlist. The basic circuit model and the circuit performance model are automatically instantiated based on this input.

The algorithm iterates over the devices and nodes in the circuit to create the basic model. The corresponding variables and equation are automatically instantiated. This is similar to a circuit simulation tool.

Symmetry constraints, functional block behavior constraints and performance equations are automatically created to form the op-amp performance model. The symmetry and functional block behavior constraints are created by iterating over all recognized functional blocks, instantiating the corresponding constraints by selecting the corresponding variables of the basic circuit model. This is similar to the method in [39], which creates constraints for basic transistor pairs.

The performance equations are set up for every performance variable in (2). Every equation stated on a high level of abstraction in Sec. X is broken down into the circuit variables using the intermediate performance equations. Fig. 4 illustrates

Required Functional block decomposition results with functional blocks FB [1], Transistor variables
for all amplificationStages
createRoutEquation() (24)
for all $fb \in FB_{nout}$
createOutputConductance() (21) - (23)
createInputConductanceEquation() (19), (20)
createStageOpenLoopGainEquation() (25)
createOpenLoopPerformanceEquation() (44)
Return Open-loop performance equation

Fig. 4. Performance equation creation on the example of the open loop gain

this procedure with the open-loop gain. To instantiate the open-loop gain performance equation (44), the open-loop gain equations of the individual amplification stages must be created. These equations take the output resistances and the transconductances of the stages as input (25). The transconductance of a stage in turn takes the circuit variables as input (Sec. IX-B1). For the equation of the output resistance, the equations of the output conductances of all functional blocks on HL 3 FB_{nout} connected to the output net n_{out} must be created. The equations of the output conductances has the circuit variables as input (Sec. IX-B2). Thus, an overall open-loop gain equation is automatically instantiated with the circuit variables as input.

Analogously to Fig. 4, the performance equations for every supported performance feature in (2) are automatically instantiated for a given topology linking the abstract performance equations in Sec. X to the circuit variables using the intermediate performance equations (Sec. IX). Many intermediate performance equations are part of several different op-amp performance equations. The transconductance of the first stage is for example part of the open-loop gain equation as well as part of the equation for the unity-gain bandwidth. The equations are stored topology-independent but customized by the algorithms. In contrast to the presented approach, the state of the art is limited to individual topologies and their specific equation sets.

XII. APPLICATION OF THE HIERARCHICAL PERFORMANCE EQUATIONS LIBRARY IN AUTOMATIC SIZING

The circuit model automatically created for a topology with the method in Sec. XI can be applied to size the circuit for performance requirements given as lower and upper bounds and for a given process technology. Intermediate performance requirements, e.g., on poles, are automatically derived from the given op-amp specification.

The automatically created circuit model is fed into a suitable solver. We use constraint programming [40] in this work. Constraint programming is suitable for the combinatorial character of analog circuit sizing due to the manufacturing-induced discrete value range of transistor geometries. It allows all function types, as e.g., trigonometrical, polynomial. No further approximations must be made to the performance equations. A detailed description and the adaptations we made to the constraint programming solver are given in [20]. During the

sizing process, the basic model of the circuit emulates the circuit simulation, while the performance model (Secs. VII - X) describes the overall behavior of the functional blocks of the given op-amp topology providing the information needed for transistor sizing.

The tool needs a few seconds to find the first initial sizing for a circuit. The results are further improved towards higher performance safety margins by letting the optimizer run for one more minute. After one minute, the improvement slowed down significantly in the experiments, therefore the optimization loop has been set to run for one minute overall.

The runtime equals the runtime of numerical sizing methods, e.g., [27], which also have small runtimes on modern hardware due to parallelized processes. However, the lower computational cost of this method can be demonstrated by integrating the method into a synthesis tool featuring thousands of different circuits [41]. In this context, the method is twice as fast as state-of-the-art numerical approaches, e.g., [32].

Note that for the numerical optimization techniques, the constraints, parameters, performance features, simulation configuration, and waveform postprocessing, must be set up for every circuit before starting the optimization.

XIII. EXPERIMENTAL RESULTS

This section presents experimental results for the four circuits in Fig. 2. We present the performance models automatically generated with the algorithm in Sec. XI as well as transistor dimensions (Table IV) and performance values obtained with the circuit models (Tables V and VI).

A. Performance model

In the following, the important parts of the performance models of the four circuits in Fig. 2 are described. All equations were generated individually and automatically using the algorithms in Sec. XI. The generated circuit models correspond well to the models presented in analog design books [33]–[36].

1) *Symmetry Constraints*: Table III shows the symmetry constraints derived for the four circuits in Fig. 2. Eight symmetry constraints for basic structures were derived for the telescopic op-amp. This is identical to the number of current biases in the circuit. The large number of symmetry constraints for the amplification stage subblock level in the folded-cascode op-amp with CMFB results from the common-mode feedback (CMFB) stage in which both differential pairs must be identical. As the two second stages $a_{2,1}, a_{2,2}$ in the symmetrical op-amp with high PSRR must be symmetric, four symmetry constraint were derived for HL 4 for this circuit.

2) *Functional Block Constraints*: As a cascode current mirror forms one load part of the telescopic op-amp (Fig. 2a), its widths are restricted by the corresponding behavioral constraint (13). Furthermore, as the telescopic op-amp has a second stage, the output voltages of the first stage, i. e., the voltage potentials of the nets n_5, n_8 , must be equal (16).

To make the combination of folded-cascode op-amp and CMFB circuit work, a functional block constraint on the fifth hierarchy level not mentioned before must be generated for the

TABLE III
SYMMETRY CONSTRAINTS

	Telescopic op-amp	Symmetrical op-amp	Folded-cascode op-amp	Complementary op-amp
HL 2: Structures	8	5	7	7
HL 3: Amplification stage subblocks	5	3	12	8
HL 4: Op-amp subblocks	-	4	-	-

folded-cascode op-amp with CMFB (Fig. 2b). The unity-gain bandwidth of the CMFB circuit must be greater than the one of the op-amp, such that the CMFB circuit is faster.

$$f_{GBW,CMFB} > f_{GBW,op-amp} \quad (48)$$

The unity-gain bandwidth is calculated according to (42) treating the CMFB stage as a first stage.

As the complementary op-amp (Fig. 2d) has a complementary first stage, the functional block constraints for HL 3 are generated restricting the first stage transconductor to have equal transconductances, and the stages biases to produce equal currents.

3) *Performance Equations*: In the following, the performance equations of the four circuit in Fig. 2 are presented. We focus on the differences between the four circuits.

Quiescent power: For the telescopic op-amp, the currents following into the positive supply voltage rail are considered to calculate the power consumption, while for the other three circuits also the bias currents of the circuit must be considered as it is applied to nmos transistors. The equation for the quiescent power of the telescopic op-amp is:

$$z_{QP} = (v_{VDD} - v_{VSS}) \cdot (|i_{DS,P_7}| + |i_{DS,P_9}| + |i_{DS,P_5}| + |i_{DS,P_8}|) \quad (49)$$

and for the quiescent power of the symmetrical op-amp with high PSRR:

$$z_{QP} = (v_{VDD} - v_{VSS}) \cdot (|i_{DS,P_3}| + |i_{DS,P_1}| + |i_{DS,P_2}| + |i_{DS,P_4}| + |i_{DS,P_7}| + |i_{DS,N_7}|) \quad (50)$$

Common-mode input voltage: For the telescopic op-amp, the maximum input voltage is set by the path over the first stage stage bias:

$$z_{v_{cm,max}} = v_{cm,b_{s,1}} = v_{VDD} + v_{GS,P_1} + v_{GS,P_5} - v_{th,p} \quad (51)$$

For the symmetrical op-amp with PSRR and the folded-cascode op-amp, $z_{v_{cm,max}}$ is set by the path over the load. For the folded-cascode op-amp with CMFB, this is:

$$z_{v_{cm,max}} = v_{cm,l_1} = v_{VDD} + v_{th,n} + v_{GS,P_3} - v_{th,p} \quad (52)$$

In the telescopic op-amp, the load defines the minimum input voltage. As higher minimum saturation voltages must be respected, the load path with the two diode transistors N_1, N_2 is selected:

$$z_{v_{cm,min}} = v_{ss} + v_{th,p} - (v_{GS,P_3} - v_{th,n}) + v_{GS,N_1} + v_{GS,N_2} \quad (53)$$

In the other circuits, the minimum input voltage is restricted by the stage bias of the first stage, which leads to similar

equations as in (51) with the negative supply voltage as input. No equations are generated for the complementary op-amp, as it is assumed to allow all values as input voltage.

Output voltage: In the telescopic op-amp and the symmetrical op-amp with high PSRR, the output voltage is restricted by one transistor on each path of the output stage. The output voltage equations for the telescopic op-amp are:

$$\begin{aligned} z_{v_{out,max}} &= v_{VDD} + v_{GS,P_6} - v_{th,p} \\ z_{v_{out,min}} &= v_{VSS} + v_{GS,N_5} - v_{th,n} \end{aligned} \quad (54)$$

For the folded-cascode op-amp with CMFB and the complementary op-amp, the output voltage is restricted by the load parts of the first stage, as the first stage is also the output stage. For each path, two transistors must be considered. For the folded-cascode op-amp, the output voltage is restricted by:

$$\begin{aligned} z_{v_{out,max}} &= v_{VDD} + v_{GS,P_4} - v_{th,p} + v_{GS,P_2} - v_{th,p} \\ z_{v_{out,min}} &= v_{VSS} + v_{GS,N_8} - v_{th,n} + v_{GS,N_6} - v_{th,n} \end{aligned} \quad (55)$$

Common-mode rejection ratio: The common-mode rejection ratio is calculated for the telescopic op-amp and the symmetrical op-amp with high PSRR. To calculate CMRR of the telescopic op-amp, the open-loop gain of the first stage is needed. Using (25), we obtain: (21), (19):

$$A_{D0,1} = \frac{gm_{P_1}}{\frac{gd_{P_1} \cdot gd_{P_3}}{gm_{P_3}} + \frac{gd_{N_1} \cdot gd_{N_3}}{gm_{N_1}}} \quad (56)$$

N_1 is the load transistor chosen for the CMRR calculation as its gate is connected to an output of the first stage, which leads to following CMRR equation of the telescopic op-amp:

$$z_{CMRR} = 2A_{D0,1} \cdot \frac{gm_{N_1}}{gd_{P_5}} \quad (57)$$

As stated in Sec. X-B3, the first and second stage gain must be considered to calculate CMRR for symmetrical op-amps. For the symmetrical op-amp with high PSRR, these are:

$$A_{D0,1} = \frac{gm_{N_1}}{gd_{N_1} + gm_{P_1}}, \quad A_{D0,2} = \frac{gm_{P_4}}{\frac{gd_{P_6} + gd_{P_4}}{gm_{P_6}} + gd_{N_5}} \quad (58)$$

The equation of CMRR then is:

$$z_{CMRR} = 2A_{D0,1} \cdot A_{D0,2} \frac{gm_{P_2}}{gd_{N_3}} \quad (59)$$

Unity-gain bandwidth: The unity-gain bandwidth is calculated similarly for the telescopic op-amp, for the folded-cascode op-amp with CMFB and for the complementary op-amp. For the telescopic op-amp, it is:

$$z_{f_{GBW}} = \frac{gm_{P_1}}{2\pi C_{n_8}} \quad (60)$$

In the complementary op-amp, both nmos and pmos differential pairs must be considered to calculate the transconductance of the first stage transistor (Sec. IX-B1).

In the symmetrical op-amp, also the second stage must be considered to calculate the unity-gain bandwidth (43):

$$z_{f_{GBW}} = \frac{A_{D0,1} \cdot gm_{P_4}}{2\pi C_{n_5}} \quad (61)$$

Open-loop gain: The open-loop gain is calculated by the multiplication of the gain of the stages. Two stages must be

considered in the telescopic op-amp (Fig 2a), three stages in the symmetrical op-amp (Fig 2c). As the folded-cascode op-amp with CMFB consists of one stage only, its open-loop gain is the gain of the first stage.

In the complementary op-amp, two gate-connected couples exist. The open-loop gain is therefore calculated by:

$$z_{A_{D0}} = \frac{gm_{N_4} + gm_{P_4}}{\frac{gd_{P_8} \cdot (gd_{P_6} + gd_{N_4})}{gm_{P_8}} + \frac{gd_{N_8} \cdot (gd_{N_6} + gd_{P_4})}{gm_{N_8}}} \quad (62)$$

Slew rate: In the telescopic op-amp, the first stage and the second stage bias current must be considered for the slew rate:

$$z_{SR} = \min\left\{\frac{|i_{DS,P_5}|}{C_{n_8}}, \frac{|i_{DS,P_6}|}{C_{n_{out}}}\right\} \quad (63)$$

Please note that the capacitance of net n_8 is mainly influenced by the compensation capacitor c_C , the capacitance of net n_{out} by the load capacitor c_L .

In the symmetrical op-amp, the second stage and the third stage are considered for slew rate calculation as stated in Sec. X-C2. Twice the current of the second stage is considered.

$$z_{SR} = \min\left\{\frac{2 \cdot |i_{DS,N_5}|}{C_{n_5}}, \frac{|i_{DS,N_6}|}{C_{n_{out}}}\right\} \quad (64)$$

In the folded-cascode op-amp with CMFB, the bias currents of the first stage differential pair as well as the gate connected couple must be considered. This leads to:

$$z_{SR} = \frac{\min\{|i_{DS,N_4}|, |i_{DS,P_4}|\}}{C_{n_{out}}} \quad (65)$$

The same considerations must be made for the complementary op-amp. In addition, the pmos and nmos stage biases are of interest:

$$z_{SR} = \frac{\min\{(|i_{DS,N_2}| + |i_{DS,P_2}|), (|i_{DS,N_6}| + |i_{DS,P_6}|)\}}{C_{n_{out}}} \quad (66)$$

Phase margin: Two non-dominant poles are identified for the telescopic op-amp: one pole for the first stage and one for the second stage. The compensation capacitor brings a positive zero along. Hence, the automatically generated equation for the phase margin is:

$$z_{PM} = \frac{\pi}{2} - \operatorname{atan}\left(\frac{f_{GBW}}{f_{ndp,a_1}}\right) - \operatorname{atan}\left(\frac{f_{GBW}}{f_{ndp,a_2}}\right) - \operatorname{atan}\left(\frac{f_{GBW}}{f_{pz}}\right) \quad (67)$$

In the symmetrical op-amp, three non-dominant poles arise: the first stage non-dominant pole, the non-dominant pole evoked by the compensation capacitor in the third stage and the non-dominant pole of the cascode transconductors in the second stages. The compensation capacitor also leads to a positive zero. The equation for the phase margin is:

$$\begin{aligned} z_{PM} &= \frac{\pi}{2} - \operatorname{atan}\left(\frac{f_{GBW}}{f_{ndp,a_1}}\right) - \operatorname{atan}\left(\frac{f_{GBW}}{f_{ndp,a_3}}\right) \\ &\quad - \operatorname{atan}\left(\frac{f_{GBW}}{f_{ndp,a_c,2}}\right) - \operatorname{atan}\left(\frac{f_{GBW}}{f_{pz}}\right) \end{aligned} \quad (68)$$

For the folded-cascode op-amp with CMFB, the phase margins of the first stage and the CMFB circuit must be calculated. As the phase margin of the CMFB circuit is

TABLE IV
DIMENSIONS FOR THE CIRCUITS IN FIG. 2

Variable	Value
$W_{P_1} = W_{P_2}$	172 μm
$W_{P_3} = W_{P_4}$	27 μm
W_{P_5}	247 μm
W_{P_6}	515 μm
W_{P_7}	7 μm
W_{P_8}	7 μm
W_{P_9}	43 μm
$W_{N_1} = W_{N_2}$	90 μm
$W_{N_3} = W_{N_4}$	90 μm
W_{N_5}	130 μm
W_{N_6}	269 μm
W_{N_7}	166
$L_{P_1} = L_{P_2}$	9 μm
$L_{P_3} = L_{P_4} = L_{P_8}$	4 μm
$L_{P_5} = L_{P_6} =$	3 μm
$L_{P_7} = L_{P_9}$	
$L_{N_1} = L_{N_2}$	1 μm
$L_{N_3} = L_{N_4}$	1 μm
L_{N_5}	1 μm
$L_{N_6} = L_{N_7}$	9 μm
C_c	6.4pF

(a) Telescopic op-amp

Variable	Value
$W_{N_1} = W_{N_2}$	548 μm
W_{N_3}	5 μm
W_{N_4}	290 μm
$W_{N_5} = W_{N_6}$	218 μm
$W_{N_7} = W_{N_8}$	30 μm
$W_{N_9} = W_{N_{10}}$	141 μm
$W_{N_{11}} = W_{N_{12}} =$	84 μm
$W_{N_{13}} = W_{N_{14}}$	
$W_{P_1} = W_{P_2}$	175 μm
$W_{P_3} = W_{P_4}$	143 μm
$W_{P_5} = W_{P_6}$	55 μm
$L_{N_1} = L_{N_2}$	8 μm
$L_{N_3} = L_{N_4} =$	3 μm
$L_{N_5} = L_{N_6} =$	
$L_{N_9} = L_{N_{10}}$	
$L_{N_7} = L_{N_8}$	2 μm
$L_{N_{11}} = L_{N_{12}} =$	1 μm
$L_{N_{13}} = L_{N_{14}}$	
$L_{P_1} = L_{P_2}$	2 μm
$L_{P_3} = L_{P_4} =$	1 μm
$L_{P_5} = L_{P_6}$	

(b) Folded-cascode op-amp with CMFB

Variable	Value
$W_{N_1} = W_{N_2}$	8 μm
W_{N_3}	56 μm
$W_{N_4} = W_{N_5}$	205 μm
W_{N_6}	460 μm
W_{N_7}	23 μm
$W_{P_1} = W_{P_2}$	5 μm
$W_{P_3} = W_{P_4}$	15 μm
$W_{P_5} = W_{P_6}$	35 μm
W_{P_7}	287 μm
$L_{N_1} = L_{N_2}$	3 μm
$L_{N_3} = L_{N_7}$	6 μm
$L_{N_4} = L_{N_5}$	9 μm
L_{N_6}	1 μm
$L_{P_1} = L_{P_2} =$	2 μm
$L_{P_3} = L_{P_4} = L_{P_7}$	
$L_{P_5} = L_{P_6}$	2 μm
C_c	4.5pF

(c) Symmetrical op-amp with high PSRR

Variable	Value
W_{N_1}	13 μm
W_{N_2}	306 μm
$W_{N_3} = W_{N_4}$	79 μm
$W_{N_5} = W_{N_6}$	39 μm
$W_{N_7} = W_{N_8}$	32 μm
W_{N_9}	13 μm
W_{P_1}	7 μm
W_{P_2}	168 μm
$W_{P_3} = W_{P_4}$	378 μm
$W_{P_5} = W_{P_6}$	66 μm
$W_{P_7} = W_{P_8}$	104 μm
$L_{N_1} = L_{N_2} = L_{N_9}$	4 μm
$L_{N_3} = L_{N_4}$	1 μm
$L_{N_5} = L_{N_6}$	5 μm
$L_{N_7} = L_{N_8}$	5 μm
$L_{P_1} = L_{P_2}$	3 μm
$L_{P_3} = L_{P_4}$	1 μm
$L_{P_5} = L_{P_6}$	3 μm
$L_{P_7} = L_{P_8}$	3 μm

(d) Complementary op-amp

restricted by the non-dominant poles of the first stage and the CMFB stage, this phase margin is the most restrictive one.

In the complementary op-amp, two non-dominant poles of the first stage must be calculated, respecting the two differential pairs.

B. Sizing Results

The instantiated equations and constraints are automatically given to the embedded constraint programming solver GeCode [42]. Several sizings are calculated for a topology with a backtracking-search algorithm, which is based on branch-and-bound (BAB) methods. The transistor dimensions were generated using a 0.25 μm PDK. The supply voltage was 5V and the bias current 10 μA .

Sizing values (Table IV) were generated for the circuits in Fig. 2, using the specifications in Table V, VI. The performance values calculated with the performance models and

TABLE V
PERFORMANCE VALUES OF THE (A) TELESCOPIC OP-AMP (B) SYMMETRICAL OP-AMP WITH HIGH PSRR

Constraints	Spec.		Sizing tool		BSIM3v3		Average deviation
	(a)	(b)	(a)	(b)	(a)	(b)	
Gate-area ($10^3 \mu\text{m}^2$)	≤ 15	≤ 10	5.8	5.5	-	-	-
Quiescent power (mW)	≤ 10	≤ 15	5.8	4	6.1	4.5	13%
Max. common-mode input voltage (V)	≥ 3	≥ 3	3.3	4.3	4.4	4.3	-
Min. common-mode input voltage (V)	≤ 2	≤ 2	0	0.8	0.1	0.7	-
Max. output voltage (V)	≥ 4	≥ 4	4.5	4.5	4.5	4.4	-
Min. output voltage (V)	≤ 1	≤ 1	0.3	0.1	0.2	0.2	-
CMRR (dB)	≥ 90	≥ 90	130	95	146	142	11% / 33%
Unity-gain bandwidth (MHz)	≥ 7	≥ 7	10	10.3	6.5	6.8	53% / 51%
Open-loop gain (dB)	≥ 80	≥ 80	120	100	93	97	29% / 3%
Slew rate ($\frac{\text{V}}{\mu\text{s}}$)	≥ 15	≥ 10	28	15	22	11	27% / 36%
Phase Margin ($^\circ$)	≥ 60	≥ 60	60	61	67	59	10% / 3%
Average deviation of all perf. values	-	-	-	-	-	-	23% / 23%

TABLE VI
PERFORMANCE VALUES OF THE (A) FOLDED-CASCODE OP-AMP WITH CMFB (B) COMPLEMENTARY OP-AMP

Constraints	Spec.		Sizing tool		BSIM3v3		Average deviation
	(a)	(b)	(a)	(b)	(a)	(b)	
Gate-area ($10^3 \mu\text{m}^2$)	≤ 15	≤ 5	13.4	4.5	-	-	-
Quiescent power (mW)	≤ 15	≤ 5	10	5	11	4.4	10% / 14%
Max. common-mode input voltage (V)	≥ 3	-	4.5	-	4.4	-	-
Min. common-mode input voltage (V)	≤ 2	-	0.9	-	1	-	-
Max. output voltage (V)	≥ 3.5	≥ 3.5	4	3.5	4.1	3.8	-
Min. output voltage (V)	≤ 1	≤ 1.5	0.9	1.4	1	0.5	-
CMRR (dB)	≥ 80	≥ 70	122	133	118	136	3% / 2%
Unity-gain bandwidth (MHz)	≥ 10	≥ 10	10	28	10.5	19	5% / 47%
Open-loop gain (dB)	≥ 70	≥ 80	75	84	71	86	6% / 2%
Slew rate ($\frac{\text{V}}{\mu\text{s}}$)	≥ 15	≥ 15	24.5	23	19	20	29% / 15%
Phase Margin ($^\circ$)	≥ 60	≥ 60	82	62	83	57	1% / 9%
Average deviation of all perf. values.	-	-	-	-	-	-	9% / 15%

results from circuit simulation are included in these tables. The average deviations for all performance specifications are 9% - 23%. This meets the requirement of analog designers who expect a 20% - 30% deviation between the Shichman-Hodges model and full circuit simulation. The largest deviation is obtained for the unity-gain bandwidth of the telescopic op-amp and of the symmetrical op-amp. It is overestimated and is one of few performance features that do not meet the specification. The unity-gain bandwidth depends linearly on the transconductance of the input transistor of the first stage (42). This transconductance is often overestimated using the Shichman-Hodge model.

For the symmetrical and complementary op-amps, the phase margin requirement is not fulfilled. However, the deviation between the simulation and calculated value is very small, 3% respectively 9%. The equation-based model of the phase margin is quite accurate.

All other specifications are fulfilled by the calculated and simulated performance values. [2] shows additional sizing results obtained with the HPEL. The paper presents a synthesis tool featuring thousands of different op-amp topology using the HPEL to evaluate op-amp topologies. Sizing results for 100 different topologies are compared. The average deviation

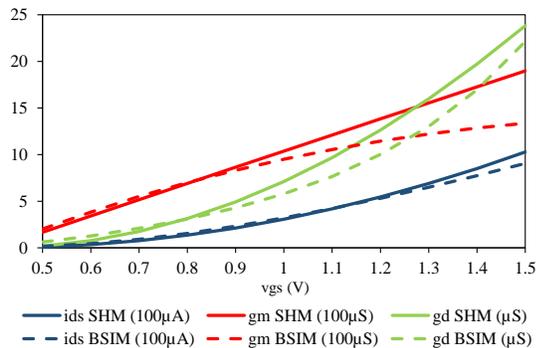


Fig. 5. Transistor parameter for different v_{GS} -values

is again between 20% - 30% and thus meets the expectation of designers. Further simulation-based optimization may be performed on the circuit to improve the performance.

Fig. 5 compares the Shichman-Hodges model used in HPEL and the BSIM3v3 model used in simulation. It shows the transconductance gm , the output conductance gd and the drain-source current i_{DS} of a transistor for different v_{GS} -values obtained with the two models. The transistor width and length are set to $10\mu\text{m}$, $1\mu\text{m}$ respectively. The drain-source voltage was set to be 1.5 V, such that the transistor operates in saturation with strong inversion, a common working region in analog circuits. For small v_{GS} values, the two transistor models correspond well. Higher v_{GS} -values lead to deviations. Keeping v_{GS} small hence leads to accurate performance results using HPEL. Future work is on integrating more complex transistor models, such as the EKV model, into HPEL. The EKV model has a low complexity compared to BSIM3v3, but features a good accuracy in all transistor regions. Integrating more advanced transistor models makes the method also usable for modern technologies with small channel lengths. Other approaches integrate the gm/Id-method based on look-up tables in the sizing tool [38].

XIV. CONCLUSIONS, LIMITATIONS, OUTLOOK

This paper presented a method to automate the set-up of an equation-based behavioral description of an op-amp and applied it to circuit sizing. A hierarchical performance equation library (HPEL) was developed, allowing the equations to be automatically set up based on a functional block analysis of the circuit. The created circuit model combines simulation and sizing as it uses KCL/KVL to simulate the currents and voltages in the circuit and performance equations to describe the circuit behavior suitable for sizing. The analytical performance equation makes the usage of numerical performance evaluation during sizing unnecessary. The method is generic in the sense that new types of circuits are not considered by setting up the equations from scratch, but by extending the HPEL with the respective new functional blocks and equations.

For the method to be applicable, an analytical description of the circuit class has to be available. While for established circuit classes, e.g., [43], [44], such descriptions exist, this may not be the case for a brandnew circuit class that just evolves.

Currently, the HPEL supports one- and two-stage op-amps with simple compensation structures. The method can be extended to advanced frequency compensation techniques as [45], [46] and multi-stage op-amps. As [43], [44] show, multi-stage op-amps are describable with analytical equations on a high level of abstraction, which can be added to the HPEL. This, e.g., needs new equations to support the arising poles and zeros of nested compensation and feedback-loops, which can be developed based on the structural studies in [43], [44]. Additionally, the concept of functional block description can be transferred to other analog circuit classes. This requires an extension of the functional block decomposition method in [1] as well as an extension of the HPEL and the corresponding algorithms. A cross-coupled pair for example is frequently part of an oscillator or comparator circuit. Its formalized structural description would be added to [1]. Its behavioral equations would be added to the HPEL.

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