# Exploring the Potential of Low-bit Training of Convolutional Neural Networks

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Abstract—Convolutional neural networks (CNNs) have been widely used in many tasks, but training CNNs is time-consuming and energy-hungry. Using the low-bit integer format has been proved promising for speeding up and improving the energy efficiency of CNN inference, while the training phase of CNNs can hardly benefit from such a technique because of following challenges: (1) The integer data format cannot meet the requirements of the data dynamic range in training, resulting in the accuracy drop; (2) The floating-point data format keeps large dynamic range with much more exponent bits, resulting in higher accumulation power than integer one; (3) There are some specially designed data formats (e.g., with group-wise scaling) that have the potential to deal with the former two problems but the common hardware can not support them efficiently.

To tackle all these challenges and make the training phase of CNNs benefit from the low-bit format, we propose a low-bit training framework for convolutional neural networks to pursue a better trade-off between the accuracy and energy efficiency. (1) We adopt element-wise scaling to improve the dynamic range of data representation, which greatly reduces the quantization error; (2) Group-wise scaling with hardware friendly factor format is designed to reduce the element-wise exponent bits without degrading the accuracy; (3) We design the customized hardware unit that implement the low-bit tensor convolution arithmetic with our multi-level scaling data format. Experiments show that our framework achieves a superior trade-off between the accuracy and the bit-width than previous low-bit training studies. For training a variety of models on CIFAR-10, using 1-bit mantissa and 2-bit exponent is adequate to keep the accuracy loss within 1%. And on larger datasets like ImageNet, using 4-bit mantissa and 2-bit exponent is adequate. Through the energy consumption simulation of the computing units, we can estimate that training a variety of models with our framework could achieve  $8.3 \sim 10.2 \times$ and  $1.9 \sim 2.3 \times$  higher energy efficiency than single-precision and 8-bit floating-point arithmetic, respectively.

Index Terms—Low-bit Training, Quantization, Convolutiuonal Neural Networks

#### I. INTRODUCTION

**C** ONVOLUTIONAL neural networks (CNNs) have achieved state-of-the-art performance in many computer vision tasks [1]–[3]. However, deep CNNs are both computation and storage-intensive. The training process could consume up to hundreds of ExaFLOPs of computations and tens of GBytes of storage [4], thus posing a tremendous challenge for training in resource-constrained environments. At present, GPU is commonly used to train CNNs and it is energy-hungry. The power of a running GPU is about 250W, and it usually

#### TABLE I

BACKWARD.

Op Name	Ор Туре	ResNet18	GoogleNet
Conv (F)	Mul&Add	1.88E+09	1.58E+09
Conv (B)	Mul&Add	4.22E+09	3.05E+09
BN	Mul&Add	3.06E+06	3.23E+06
FC	Mul&Add	5.12E+05	1.02E+06
EW-Add (F)	Add	7.53E+05	0
EW-Add (B)	Add	9.28E+05	0
SGD Update (B)	Mul&Add	1.15E+07	5.97E+06

takes more than 10 GPU-days to train one CNN model on large practical datasets like ImageNet [5]. Therefore, reducing the energy consumption of the training process has raised interest in recent years.

Reducing the precision of CNNs has drawn great attention since it can reduce both the storage and computational complexity. It is pointed out that 32-bit floating-point multiplication and addition units consumes about  $20 \sim 30 \times$  more power than 8-bit fixed-point ones [6]. Also, using 8-bit data format could save the energy consumption of memory access by roughly 4 times. Many studies [7]–[10] focus on amending the training process to acquire a reduced-precision model with higher inference efficiency. However, these methods rely on tuning from a full-precision pre-trained model, which is costly, or introduce more optimization operations into training for a better inference performance, therefore, they are not suitable for efficient training.

Besides the studies on improving inference efficiency, there are also some studies that focus on the training process. WAGE and FullINT [11], [12] implement fully fixed-point training with 8-bit and 16-bit integers to reduce the training cost. But they fail to achieve an acceptable accuracy since the dynamic range of data in training is large, and SGD algorithm needs small quantization error to ensure convergence. This contradiction between the large dynamic range requirement of training algorithm and the small representation range of high-efficiency integer data format is the first challenge of low-bit training.

Floating point format has a larger representation range than fixed-point format with the same bitwidth. FP8, HFP8 and S2FP8 [13]–[15] adopt 8-bit floating-point multiplications in

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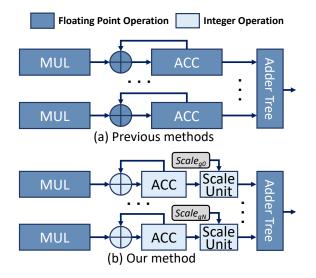


Fig. 1. The adder tree convolution hardware architecture. (a) Previous studies [14] use low-bit floating-point multiplication (FP MUL) (e.g., 8-bit), but single precision accumulations are still needed. (b) We not only makes MUL less than 8-bit, but also simplifies the local accumulator.

convolution, in which more element-wise exponent bits are used to get a larger dynamic range. However, the precision of effective number is lost and they have to use complex quantization format. On the other hand, the dynamic range of intermediate accumulation results is too large and can only be conducted in the floating-point format, which results in higher energy consumption than integer accumulation. How to realize low cost multiplications and accumulations (MACs) for high dynamic range floating-point data format is the second challenge of low-bit training.

In this work, we design a novel low-bit tensor format with multi-level scaling (MLS format) to maintain a high representation capability, which in the meantime could be manipulated by our customized hardware design with high energy efficiency. Specifically, in the MLS format: 1) Elementwise scaling is used to improve the dynamic range of data representation, which greatly reduces the quantization error; 2) A specially designed group scaling factor is used to reduce the element-wise exponent bits with smaller overhead, so that the accumulation can be simplified to integer accumulation without hurting the representational capability. Also, the specially designed group scaling could be conducted efficiently by shifting and additions instead of multiplications. Through these two techniques, we can reduce the dynamic range of most computing units while keeping the overall quantization error small, so as to achieve accurate and efficient calculation.

Common hardware (e.g., GPU) is designed to support general floating-point arithmetic and can not support most of the existing low-bit tensor format efficiently. What's more, systolic array architecture that is widely used in NN accelerator treats convolution as general matrix multiplication and can not support data format with group-wise scaling. **Hence, the third challenge of low-bit training is that common hardware does not support specially designed data formats** 

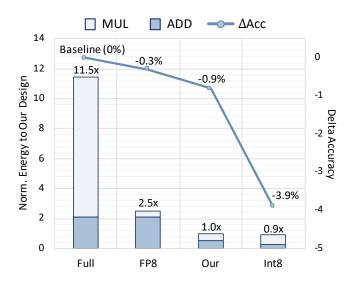


Fig. 2. The model accuracy drop (ResNet-18 on ImageNet) and energy consumption of calculating  $3 \times 3$  convolutions with different training framework, nomalized to our design. FP8: [14]; Int8: [12].

with group-wise scaling. To tackle this challenge, we design 3) the low-bit tensor convolution arithmetic unit with the MLS format to support our training framework efficiently. Our computing unit consists of low-bit multiplication, integer intra-group accumulation, group-wise scale unit, and intergroup addition tree, as shown in Fig. 1 (b). Different from previous methods with similar architecture (Fig. 1 (a)) and systolic array designs, our multiplications have smaller bitwidth and the accumulations are conducted with fixed-point arithmetic instead of floating-point arithmetic. Therefore, as shown in Fig. 2, our framework can largely reduce the energy consumption of MACs in convolution operations, compared with the full-precision and 8-bit floating-point frameworks.

- To summarize, the contributions of this paper are:
- This paper proposes the MLS tensor format to strike a superior balance between representation capability and energy efficiency. The element-wise scaling improves the dynamic range of data representation, and by using the group-wise scaling, the element-wise exponent bitwidth can be kept low, so that the intra-group accumulation can be conducted with integer accumulation units for higher energy efficiency. We elaborate the corresponding low-bit training framework to leverage the MLS tensor format, and analyze that our MLS tensor format can be manipulated efficiently with our low-bit tensor convolution arithmetic.
- 2) Experimental results demonstrate the representational capability of the MLS format: For training ResNets, VGG-16, and GoogleNet on CIFAR-10, using 1-bit mantissa and 2-bit exponent for each element can achieve an accuracy loss within 1%. For training these models on ImageNet, 4-bit mantissa and 2-bit exponent are adequate to achieve an accuracy loss within 1%.
- 3) We conduct hardware design of low-bit tensor convolution arithmetic with MLS format, and shows that our framework can indeed conduct MACs in convolutions

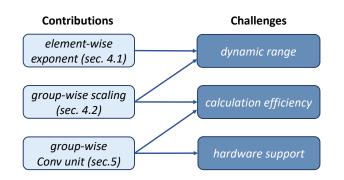


Fig. 3. Three contributions of this paper and three challenges of low-bit training.

efficiently, without degrading the model accuracy. We implement Register Transfer Language (RTL) designs of computing units with different arithmetic. And the energy consumption simulation shows that training a variety of models with our framework could achieve  $8.3 \sim 10.2 \times$  and  $1.9 \sim 2.3 \times$  higher energy efficiency than training with 32-bit and 8-bit [14] floating-point arithmetic. On the other hand, we can achieve much higher accuracy than previous fixed-point training frameworks [11], [12] with comparable energy efficiency.

The correspondences of the challenges in low-bit training and our contributions are summarized in Fig. 3. And the rest of this paper is organized as follows. Sec. II discusses the related work of low-bit training, and Sec. III gives basic knowledges on the training framework of CNNs. In Sec. IV, we explain the reason why we proposed element-wise scaling and groupwise scaling in CNN low-bit training, and summarize them in MLS tensor format. The corresponding convolution arithmetic unit design is proposed in Sec. V. The dynamic quantization method and its overhead are discussed in Sec. V-A, and the experiment results are shown in Sec. VI. Finally, we draw the conclusion in Sec. VII.

#### II. RELATED WORK

#### A. Post-Training Quantization

Earlier quantization methods like [16] focus on the posttraining quantization, and quantize the pre-trained fullprecision model using the codebook generated by clustering or other criteria (e.g., SQNR [17], entropy [18]). POST [9] and HAWQ [10] select the quantization bit-width and clipping value for each channel through the analytical investigation, but the per-channel precision allocation was not hardware-friendly. GEMMLOWP [19] propose an integer arithmetic convolution for efficient inference, but it's hard to be used in training because the scale and bias of the quantized output tensor should be known before calculation. MSFP [20] proposes a new class of data formats developed for production cloudscale inference on custom hardware. These methods show that low-bit CNN models still have adequate representation ability. However, these methods are aming to accelerate inference of a pre-trained model and can not accelerate the training process.

# B. Quantization-Aware Training

Quantization-aware training considers quantization effects in the training process to further improve the accuracy of the quantized model. It is used for training binary [21] or ternary [22] networks. Despite that the follow-up studies [23] [24] have proposed new techniques to improve the accuracy, the extremely low bit-width still causes notable accuracy degradation. Other methods seek to retain the accuracy with relatively higher precision, e.g., 8-bit [7]. [25] develop GPUbased training framework to get dynamic fixed-point models or Minifloat models. [8] parameterizes and trains the clipping value in the activation function to properly restrict the range of activation. These methods obtain quantized models that achieve better trade-off of accuracy and inference efficiency, but the training process is still full-precision.

# C. Low-Bit Training

To accelerate the training process, [26] propose to use fixedpoint arithmetic in both the forward and backward processes. [11], [12] implement full-integer training frameworks for integer-arithmetic machines. However, these methods cause notable accuracy degradation. [27] use 8-bit and 16-bit integer arithmetic [19] and achieve a better accuracy. But this arithmetic [19] is designed for accelerating inference and requires knowing the output scale before calculation. Therefore, although [27] quantize the gradients in the backward process, it is not practical for actual training acceleration. To summarize, full-integer training frameworks have high energy efficiency, but still suffer from large accuracy degradation when the bitwidth is reduced to 8 bit.

Besides the studies on full-integer training frameworks, some studies propose new low-bit formats. BFloat [28] use a 16-bit floating-point format that is more suitable for CNN training. Flexpoint [29] propose the format that contains 16bit mantissa and 5-bit tensor-shared exponent (scale), which is similar to the dynamic fixed-point format [30]. Recently, 8-bit floating-point formats [13]-[15] are used with chunk-based accumulation. However, to ensure a sufficient representation range, the exponent bit-width in their format is larger than 5, which makes the operations (especially the accumulation) using these formats inefficient. More recently, a radix-4 data format [31] is proposed along with two-stage quantization to realize 4-bit training, but the accuracy is not satisfying enough and its computation is complex. In this work, the MLS tensor format is designed to have a small exponent bit-width, such that the accumulation can be conducted using fixed-point arithmetic, while retaining the overall model accuracy.

#### III. PRELIMINARY

# A. Computation Flow for CNN Training

In this work, we denote the filter coefficient and feature map of convolution as weight and activation, respectively. In the back-propagation, the gradient of convolution results and weights are denoted as error and gradient, respectively. As shown in Fig. 4, generally, in a convolutional layer, convolution is followed by batch normalization (BN), nonlinear

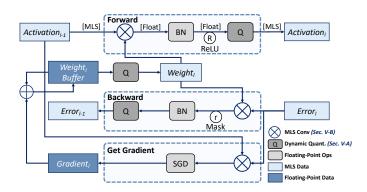


Fig. 4. Computation flow of our low-bit training framework.

activation (ReLU is used in this work) and other operations like pooling.

As shown in Table I, the MACs in convolutions are the majority of the operations in a convolution layer. Hence, conducting the MACs with low-bit arithmetic in convolutions can boost the energy efficiency of the training process. And conducting other operations (e.g., BN, weight update) using high bit-width helps to stablize training and make the accuracy higher. Therefore, we focus on the quantization before all three types of Conv (Conv of weight and activation, weight and error, activation and error). And the output data of Conv is in floating-point format for other operations like BN.

#### B. Basic Formula of Convolution

Weight, activation, and error are all 4-dimension tensors in the training process. For activation and error, the four dimensions are sample in batch (N), channel (C), feature map height  $(F_h)$ , and feature map width  $(F_w)$ . For weight, the four dimensions are output channel  $(C_o)$ , input channel  $(C_i)$ , kernel height  $(K_h)$ , kernel width  $(K_w)$ .

We take Conv(Weight, Activation) (Conv(W, A)) as the example to introduce the basic formula of convolution between two 4-dimension tensors in training, and the other two types of convolution can be implemented similarly. Denoting the input channel number as C and the kernel size as  $K = K_h = K_w$ , the original formula of convolution is:

$$\boldsymbol{Z}[n, co, x, y] = Conv(\boldsymbol{W}, \boldsymbol{A}) = \sum_{ci=0}^{C-1} \sum_{i=0}^{K-1} \sum_{j=0}^{K-1} (1)$$
$$\boldsymbol{W}[co, ci, i, j] \times \boldsymbol{A}[n, ci, x+i, y+j]$$

We can see that every element in the output 4-dimension tensor is calculated by three loops of MACs. And three dimensions of input tensors are included in this accumulation. In common training frameworks based on hardware platforms like TPU and GPU, these tensors are processed with the "image to column" transformation. Then the convolution is calculated as a general matrix multiplication, in which grouping techniques cannot be used [32]–[34]. But in many customized CNN accelerators [35], [36], parallel PE units and addition tree architecture are used. The MACs can be grouped into intra-group ones and inter-group ones, which makes it possible for us to apply group-wise scaling. Next, we will show the advantages of group-wise scaling through data format design and hardware design.

## IV. MULIT-LEVEL SCALING LOW-BIT TENSOR FORMAT

Using low-bit arithmetic in the training process is beneficial for the energy efficiency. However, retaining a good accuracy in a low-bit fixed-point training process is challenging, since that the backpropagated gradients need high precision [26]. In this work, we design a MLS low-bit tensor format to retain the representational power of low-bit representations in CNNs. It consists of three levels of scaling factors: 1) Tensor-wise scaling factor; 2) Group-wise scaling factor; 3) Element-wise exponent. By incorporating the multi-level scaling technique, the element-wise bitwidth can be largely reduced to boost the energy efficiency, while the overall dynamic range is preserved.

In this section, we give the design details of the MLS lowbit tensor format, which is the core of our low-bit training framework. And in the next section Sec. V, we will elaborate on the framework and hardware design centering around the MLS format, to demonstrate that the conversion and computation of the MLS-formatted data are energy efficient.

# A. Overall Mapping Formula of the MLS Format

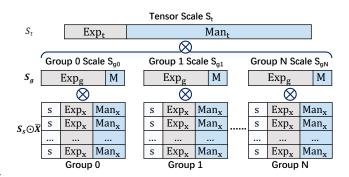


Fig. 5. The multi-level scaling (MLS) low-bit tensor format.

In a commonly used scheme [19], the mapping function from fixed-point representation and the floating-point values is  $float = scale \times (Fix + Bias)$ , in which *scale* and *Bias* are shared in one tensor. In training, however, since data distribution changes over time, one cannot simplify the *Bias* calculation as they do. Thus, we adopt an unbiased quantization scheme, and extend the scaling factor to three levels for better representation ability. The resulting MLS tensor format is illustrated in Fig. 5. Denoting a 4-dimensional tensor that is the operand of Conv (weight, activation, or error) as X, the mapping formula of the MLS tensor format is

$$\boldsymbol{X}[i,j,k,l] = \boldsymbol{S}_{\boldsymbol{s}}[i,j,k,l] \times S_t \times \boldsymbol{S}_{\boldsymbol{g}}[i,j] \times \boldsymbol{X}[i,j,k,l] \quad (2)$$

where  $[\cdot]$  denotes the indexing operation,  $S_s$  is a 1-bit sign tensor ("s" in Fig. 5),  $S_t$  is a full-precision tensor-wise scaling factor, and  $S_g$  are group-wise scaling factors shared in each group.  $S_g$  and  $\bar{X}$  use the same data format, which we refer

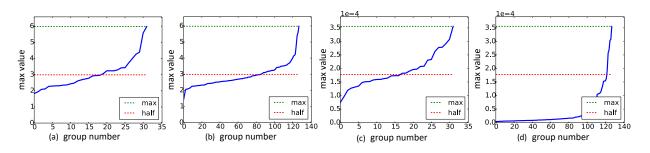


Fig. 6. Maximum value of each group of activation (a, b) and error (c, d). (a)(c): Grouped by channel; (b)(d): Grouped by sample.

to as  $\langle E, M \rangle$ , a customized floating-point format with E-bit exponent and M-bit mantissa (no sign bit). A value in the format  $\langle E, M \rangle$  is

$$float = I2F(Man, Exp) = Frac \times 2^{-Exp}$$
$$= \left(1 + \frac{Man}{2^{M}}\right) \times 2^{-Exp}$$
(3)

where Man and Exp are the M-bit mantissa and E-bit exponent, and  $Frac \in [1, 2)$  is a fraction.

#### B. Group-wise Scaling

The dynamic ranges of weight, activation and error are large in training, but we find that these values are not evenly distributed. The values in different groups have distinct dynamic ranges, as shown in Fig. 6. The blue line shows the max value in each group when activation and error are grouped by channel or sample. If we use the overall maximum value (green lines in Fig. 6) as the overall scaling, many small elements will be swamped. And usually, there are over half of the groups, in which all elements are smaller than half of the overall maximum (red line). Thus, to fully exploit the bitwidth, it is natural to use group-wise scaling factors. Our work considers three grouping dimensions: 1) the 1-st dimension of tensor, 2) the 2-nd dimension of tensor, or 3) the 1-st and the 2-nd dimensions simultaneously.

Naive floating-point group-wise scaling in previous studies [21] cannot bring actual hardware acceleration. Since when the values of different groups are accumulated, the floatingpoint scaling factors need to be multiplied back to low-bit elements, which involves floatint-point multiplications.

To facilitate a hardware-friendly low-bit training framework, we propose a special scaling format, the floating-point groupwise scaling is separate into tensor-wise and group-wise scaling factors. The first level **tensor-wise scaling factor**  $S_t$  is an ordinary floating-point number ( $\langle E_t, M_t \rangle = \langle 8, 23 \rangle$ ), to retain the precision as much as possible.

Considering the actual hardware implementation cost, there are some restrictions on the second level **group-wise scaling factor**  $S_g$ . Since calculation results of different groups need to be aggregated, using  $S_g$  in an ordinary floating-point format leads to expensive conversions in the hardware implementation. Hence, we propose two special hardware-friendly group-wise scaling schemes, whose formats can be

denoted as  $\langle E_g, 0 \rangle$ , and  $\langle E_g, 1 \rangle$ , respectively. The scaling factor in  $\langle E_g, 0 \rangle$  format is simply a power of two, which can be implemented easily as shifting on the hardware. From Eq. 3, a  $S_g = I2F(Man_g, Exp_g)$  value in the  $\langle E_g, 1 \rangle$  format can be written as

$$S_g = \left(1 + \frac{Man_g}{2}\right) \times 2^{-Exp_g}$$

$$= \begin{cases} 2^{-Exp_g} + 2^{-Exp_g-1} & Man_g = 1\\ 2^{-Exp_g} & Man_g = 0 \end{cases}$$

$$(4)$$

which is a sum of two shifting, and can also be implemented with low hardware overhead. We will see that MLS tensor convolution arithmetic benefits from group-wise scaling factor's special format with very few mantissa bits in Sec. V-B (Eq. 8).

#### C. Element-wise Scaling

The third level scaling factor  $S_x = I2F(0, Exp_x) = 2^{-Exp_x}$  is the **element-wise exponent** in  $\bar{X} = S_x(1 + \frac{Man_x}{2})$ , and we can see that the elements of  $\bar{X}$  in Eq. 2 are in a  $\langle E_x, M_x \rangle$  format. The specific values of  $E_x$  and  $M_x$  determine the cost of the MAC operation, which will be discussed in Sec. V-B. Compared with integer data format ( $E_x = 0$ ), adding element-wise exponent helps achieve a balance in the dynamic range and precision of representation. And by using group-wise scaling, the bit-width of  $\bar{X}$  can be largely reduced.

#### V. LOW-BIT TRAINING FRAMEWORK

In this section, we describe the low-bit training framework to leverage the MLS tensor format. A training iteration in our low-bit training framework is summarized in Alg. 1, and the computation flow of one layer is shown in Fig. 4. Note that, our framework is different from a quantization-aware training framework in that the convolution operands are actually quantized to the low-bit MLS format in our computation flow. In the backward propagation (Alg. 1, line 13), we use the update formula of the vanilla stochastic gradient descent (SGD) for clarity, whereas in practice, one can use other optimizers such as SGD with momentum. The t subscripts denoting the time step t are all omitted for simplicity.

In this section, we will describe two core parts of the framework to demonstrate why the conversion and computation of the format are energy efficient: Sec. V-A describes the dynamic Algorithm 1: The low-bit training framework

**Input:** L: number of layers;  $W^{1:L}$ : current float weights;  $A^0$ : inputs; T: label; lr: learning rate **Output:**  $W_{t+1}^{1:L}$ : updated float weights for the next step t+1

# /\* forward propagation \*/

**1** for l in 1 : L do  $qW^{l} = DynamicQuantization(W^{l})$ 2  $qA^{l-1} = DynamicQuantization(A^{l-1})$ 3  $\boldsymbol{Z^{l}} = LowbitConv(q\boldsymbol{W^{l}},q\boldsymbol{A^{l-1}})$ 4  $Y^{l} = BatchNorm(Z^{l})$ 5  $A^{l} = Activation(Y^{l})$ 6 7 end 8  $\frac{\partial loss}{\partial A^l} = Criterion(A^L, T)$ /\* backward propagation \*/ for l in L:1 do  $\begin{array}{l} \frac{\partial loss}{\partial \mathbf{Y}^{l}} = \frac{\partial loss}{\partial \mathbf{A}^{l}} \times Activation'(\mathbf{Y}^{l}) \\ \frac{\partial loss}{\partial \mathbf{Z}^{l}} = \frac{\partial loss}{\partial \mathbf{Y}^{l}} \times \frac{\partial \mathbf{Y}^{l}}{\partial \mathbf{Z}^{l}} \\ q\mathbf{E}^{l} = DynamicQuantization(\frac{\partial loss}{\partial \mathbf{Z}^{l}}) \\ \mathbf{G}^{l} = LowbitConv(q\mathbf{E}^{l}, q\mathbf{A}^{l-1}) \end{array}$ 9 10 11 12  $W_{t+1}^l = W^l - lr \times G^l$ 13 if l is not 1 then 14  $\frac{\partial loss}{\partial q \mathbf{A}^{l-1}} = LowbitConv(q \mathbf{E}^{l}, q \mathbf{W}^{l})$ 15

$$\frac{\partial loss}{\partial A^{l-1}} = STE(\frac{\partial loss}{\partial q A^{l-1}})$$

end

# 17 18 end

Return  $W_{t+1}^{1:L}$ 

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quantization DynamicQuantization, and Sec: V-B describes the low-bit tensor convolution arithmetic LowbitConv. They are actually FP-to-MLS conversion and the MLS MLS-to-FP conversion in the training framework.

#### A. Dynamic Quantization to MLS Tensor

The dynamic quantization converts a floating-point tensor to a MLS tensor. There are two main steps, calculating the scaling factors  $S_s, S_t, S_g$  and getting the quantized elements  $\bar{X}$ , as shown in Alg. 2. In Alg. 2, the sign tensor, overall maximun and group-wise maximums are got firstly in line  $1 \sim 3$ . And group-wise scaling factors are quantized by groupwise maximums in line  $4 \sim 8$ . Exponent( $\cdot$ ) and Fraction( $\cdot$ ) are to obtain the Exponent (an integer) and Fraction (an integer represent numberts  $\in [1, 2)$ ) of a floating-point number, which are used in the quantization of group-wise scalings and element-wise numbers in line 5 and 10. The underflow handling follows the IEEE 754 standard [37] as shown in line 11~15. When calculating the quantized elements  $\bar{X}$ , we apply the stochastic rounding [38] SRound(x,r) as shown in line 13. It is implemented with a uniformly distributed random tensor  $r \sim U[-0.5, 0.5]$  which can be generated offline as

# Algorithm 2: Dynamic Quantization

**Input:** X: float 4-d tensor; R:  $U[-\frac{1}{2}, \frac{1}{2}]$  distributed random tensor;  $\langle E_q, M_q \rangle$ : bit-width of group-wise scaling factors;  $\langle E_x, M_x \rangle$ : bit-width of each element **Output:**  $S_s$ : sign tensor;  $S_t$ : tensor-wise scaling

factor;  $S_{g}$ : group-wise scaling factors;  $\bar{X}$ : quantized elements

# /\* calculating scaling factors \*/

- 1  $S_s = Sign(X)$
- 2  $S_r = GroupMax(Abs(X))$
- $S_t = Max(S_r)$
- 4  $S_{qf} = S_r \div S_t$
- 5  $Exp_g, Frac_g = Exponent(S_{gf}), Fraction(S_{gf})$
- 6  $Exp_g = Clip(Exp_g, 1 2^{E_g}, 0)$
- 7  $Frac_{g} = Ceil(Frac_{g} \times 2^{M_{g}}) \div 2^{M_{g}}$
- 8  $S_g = Frac_q \times 2^{Exp_g}$

/\* calculating elements \*/

- 9  $X_f = Abs(X) \div S_q \div S_t$
- 10  $Exp_x, Frac_x = Exponent(X_f), Fraction(X_f)$ // quantize  $Frac_x$  to  $M_x$  bits with underflow handling
- 11  $E_{xmin} = 1 2^{E_x}$
- 12  $Frac_{xs} = Frac_x \times 2^{M_x}$  if not underflow, else  $Frac_x \times 2^{M_x E_{xmin} + E_x}$
- 13  $Frac_{xint} = Clip(SRound(Frac_{xs}, R)), 0, 2^{M_x} 1)$
- 14  $Frac_x = Frac_{xint} \times 2^{-M_x}$  if not underflow, else  $Frac_{xint} \times 2^{-M_x + E_{xmin} E_x}$
- 15  $Exp_x = Clip(Exp_x, E_{xmin}, -1)$ 16  $\bar{X} = Frac_x \times 2^{Exp_x}$
- Return  $S_s$ ,  $S_t$ ,  $S_a$ ,  $\bar{X}$

how it is done on GPU.

$$SRound(x, r) = NearestRound(x + r)$$
$$= \begin{cases} \lceil x \rceil & \text{with probability } x - \lfloor x \rfloor & (5) \\ \lvert x \rvert & \text{with probability } \lceil x \rceil - x \end{cases}$$

Note that Alg. 2 describes how we simulate the dynamic quantization process on floating-point platform. While in the hardware design, the exponent and mantissa are obtained directly, while the *Clip* operations are conducted by taking out some bits from a machine number.

# B. Low-bit Tensor Convolution Arithmetic

In this section, we describe how to do convolution with two low-bit MLS tensors.

Using the MLS tensor format and denoting the corresponding values (scaling factors S, exponents Exp and fractions Frac in the following equations) of W and A by the superscript  $^{(w)}$  and  $^{(a)}$ , one output element Z[n, co, x, y] of Conv(W, A) is calculated as:

$$\begin{aligned} \boldsymbol{Z}[n, co, x, y] &= \sum_{ci=0}^{C-1} \sum_{i=0}^{K-1} \sum_{j=0}^{K-1} \left( S_t^{(w)} \boldsymbol{S}_{\boldsymbol{g}}^{(\boldsymbol{w})}[co, ci] \bar{\boldsymbol{W}}[co, ci, i, j] \right) \\ & \left( S_t^{(a)} \boldsymbol{S}_{\boldsymbol{g}}^{(a)}[n, ci] \bar{\boldsymbol{A}}[n, ci, x+i, y+j] \right) \\ &= \left( S_t^{(w)} S_t^{(a)} \right) \sum_{ci=0}^{C-1} \left[ \left( \boldsymbol{S}_{\boldsymbol{g}}^{(\boldsymbol{w})}[co, ci] \boldsymbol{S}_{\boldsymbol{g}}^{(a)}[n, ci] \right) \\ & \sum_{i=0}^{K-1} \sum_{j=0}^{K-1} \bar{\boldsymbol{W}}[co, ci, i, j] \bar{\boldsymbol{A}}[n, ci, x+i, y+j] \right] \\ &= S_t^{(z)} \sum_{ci=0}^{C-1} \boldsymbol{S}^{(\boldsymbol{p})}[n, co, ci] \boldsymbol{P}[n, co, ci] \end{aligned}$$
(6)

Eq. 6 shows that the accumulation consist of intra-group MACs that calculates P[n, co, ci] and inter-group MACs that calculates Z.

**Intra-group MACs** The intra-group calculation of P[n, co, ci] is:

$$P[n, co, ci] = \sum_{i,j=0}^{K-1} \left( Frac^{(w)}[co, ci, i, j] Frac^{(a)}[n, ci, i, j] \right)$$

$$\times 2^{\left( Exp^{(w)}[co, ci, i, j] + Exp^{(a)}[n, ci, i, j] \right)}$$

$$(7)$$

where Frac, Exp are  $(M_x + 1)$ -bit and  $E_x$ -bit.

The intra-group calculation contains the multiplication of two  $(M_x + 1)$ -bit values and  $2 \times (2^{E_x} - 2)$ -bit shifting. The resulting  $(2M_x + 2^{E_x+1} - 2)$ -bit integer values need to be accumulated with enough bit-width to get the partial sum P. In previous 8-bit floating-point frameworks [13], [14], the accumulator has to be floating-point since they use  $E_x = 5$ . In contrast, we can use a 32-bit integer accumulator, since we adopt  $E_x = 2, M_x = 4$  in the MLS tensor format on ImageNet. See Sec. V-C for more detailed analysis.

**Inter-group MACs** As for the inter-group calculation, each element in  $S^{(p)}$  is a  $\langle E, 2 \rangle$  number obtained by multiplying two  $\langle E, 1 \rangle$  numbers. So it can be calculated by shift (multiplying the power of two) and addition as:

$$Z[co, x] = S_t^{(z)} \sum_{ci=0}^{C-1} S^{(p)}[co, ci] P[x, ci] = S_t^{(z)} \sum_{ci=0}^{C-1} \left\{ \begin{aligned} P[x, ci] 2^{-Exp^{(p)}[co, ci]} \\ P[x, ci] 2^{-Exp^{(p)}[co, ci]} + P[x, ci] 2^{-Exp^{(p)}[co, ci]-1} \\ P[x, ci] 2^{1-Exp^{(p)}[co, ci]} + P[x, ci] 2^{-Exp^{(p)}[co, ci]-2} \end{aligned} \right.$$
(8)

where the three cases correspond to  $Man^{(p)}[co, ci]=00$ ,  $Man^{(p)}[co, ci]=01/10$ , and  $Man^{(p)}[co, ci]=11$ , respectively. The index *n* is ommited for simplicity and *x* is used to denote the original 2-dimension spatial indexes *x*, *y*.

Summarize of the convolution energy efficiency of the MLS format In the MLS format, *the element-wise exponent* is 2-bit instead of 5-bit, thus the **intra-group accumulation** is simplified to use 32-bit integers. On the other hand, due to the

special format of group-wise scaling factor,  $S^{(p)}$  has a simple format, and the **inter-group accumulation** to calculate Z can be implemented efficiently on hardware without floating-point multiplication. Finally, the multiplication with the *tensor-wise* floating-point scaling factor  $S_t^{(z)}$  in Eq. 8 can usually be omitted:  $S_t^{(z)}$  only needs to be multiplied with the tensorwise floating-point scale in the following layer instead of the feature map, as long as there is no following element-wise addition on Z with another tensor.

# C. Analysis of Accumulation Bit-Width

Convolution consists of multiplication and accumulation. When different data formats are used, the results of multiplication have different dynamic ranges. As specified by the IEEE 754 standard, the gradual underflow behavior of a floating-point representation that has M-bit mantissa (Man) and E-bit exponent (Exp) is as follows. If Exp is not equal to the minimum value, the float value is not underflow, and is calculated as

$$float = Frac \times 2^{-Exp}$$
$$= \left(1 + \frac{Man}{2^M}\right) \times 2^{-Exp}.$$
(9)

If Exp is equal to the minimum value, the float value is an gradual-underflowed value, and is calculated as

$$float = Frac \times 2^{-Exp}$$
$$= \left(0 + \frac{Man}{2^M}\right) \times 2^{-Exp},$$
(10)

where Frac is (M + 1)-bit fraction, calculated by adding a 0 or 1 at the highest bit of mantissa.

The product of two numbers is calculated as

$$float_1 \times float_2 = Frac_1 \times 2^{-Exp_1} \times Frac_2 \times 2^{-Exp_1}$$
$$= (Frac_1 \times Frac_2) \times 2^{-Exp_1 - Exp_2},$$
(11)

where  $Frac_1 \times Frac_2$  is a (M+1)-bit multiplication, and the result is (2M+2)-bit. Since the minimum value of exponent is used to represent underflow, E-bit Exp represents  $2^E - 1$  levels and " $\times 2^{-Exp}$ " is  $(2^E - 2)$ -bit shifting. Therefore, " $\times 2^{-Exp_1-Exp_2}$ " is  $(2^{E+1} - 4)$ -bit shifting, and the final result of floating-point multiplication has a dynamic range of  $2M + 2 + 2^{E+1} - 4 = (2M + 2^E - 2)$ -bit. These resulting  $(2M + 2^{E+1} - 2)$ -bit integer values need to be accumulated with enough bit-width to get the partial sum. In previous 8-bit floating-point frameworks, the accumulator has to be floating-point since they use E = 5. In contrast, we can use a 32-bit integer accumulator, since we adopt  $E = 2, M = 4, (2M + 2^{E+1} - 2) = 14$  in the MLS tensor format on ImageNet.

#### VI. EXPERIMENTS

#### A. Experimental Setup

We train ResNet [39], VGG [4], and GoogleNet [40] on CIFAR-10 [41] and ImageNet [5] with our low-bit training framework. In all the experiments, the first and the last layer

#### TABLE II

COMPARISON OF LOW-BIT TRAINING METHODS ON CIFAR-10 AND IMAGENET. SINGLE NUMBER IN THE BIT-WIDTH STANDS FOR FIXED-POINT FORMAT BIT-WIDTH, WHICH IS EQUIVALENT TO  $M_x$  and the corresponding  $E_x$  is 0. "F X" indicates that X-BIT FLOATING-POINT NUMBERS are used. "ACCUM" in the "BIT-WIDTH" COLUMN STANDS FOR "ACCUMULATION", WHILE "ACC." STANDS FOR "ACCURACY".

Dataset	Method	Model	Bit-Width (W/A/E/ACCUM)	Acc.	FP baseline	Acc. Drop
	S2fFP8 [15]	ResNet-20	$\langle 5,2 \rangle \langle 5,2 \rangle \langle 5,2 \rangle$ f32	91.1%	91.5%	0.4%
	WAGE [11]	VGG-like	2 8 8 32	93.2%	94.1%	0.9%
CIFAR-10	RangeBN [27]	ResNet-20	112-	81.5%	90.36%	8.86%
		ResNet-20	4 4 4 16	92.32%	92.45%	0.13%
		ResNet-20	2 2 2 16	90.39%	92.45%	2.06%
	Ours	ResNet-20	$\langle 2,1\rangle$ $\langle 2,1\rangle$ $\langle 2,1\rangle$ 16	91.97%	92.45%	0.48%
	Ours	GoogleNet	$\langle 2,1\rangle$ $\langle 2,1\rangle$ $\langle 2,1\rangle$ 16	93.95%	94.50%	0.55%
		VGG-16	$\langle 2,1\rangle$ $\langle 2,1\rangle$ $\langle 2,1\rangle$ 16	93.34%	93.76%	0.42%
		VGG-16	$\langle 1,1\rangle$ $\langle 1,1\rangle$ $\langle 1,1\rangle$ 8	92.77%	93.76%	0.99%
	FlexPoint [29]	AlexNet	16 16 16 32	80.1% (Top5)	79.9% (Top5)	-0.2%
	DFP16 [30]	VGG-16	16 16 16 32	68.2%	68.1%	-0.1%
	DFP16 [30]	GoogleNet	16 16 16 32	69.3%	69.3%	0
	RangeBN [27]	ResNet-18	8 8 16 f32	66.4%	67.0%	0.6%
	DoReFa [26]	AlexNet	8 8 8 32	53.0%	55.9%	2.9%
	FullINT [12]	ResNet-18	8 8 8 32	64.8%	68.7%	3.9%
FullINT	FullINT [12]	ResNet-34	8 8 8 32	67.6%	72.0%	4.4%
ImagaNat	WAGE [11]	AlexNet	28832	48.4%	56.0%	7.6%
ImageNet	HFP8 [14]	ResNet-18	$\langle 5,3 \rangle \langle 5,3 \rangle \langle 5,3 \rangle$ f32	69.0%	69.3%	0.3%
	S2FP8 [15]	ResNet-18	$\langle 5,2 \rangle \langle 5,2 \rangle \langle 5,2 \rangle$ f32	69.6%	70.3%	0.7%
	Ultra-Low [31]	ResNet-18	44(3,1) f16	68.3%	69.4%	1.1%
		ResNet-18	8 8 8 32	68.5%	69.1%	0.6%
		ResNet-18	4 4 4 16	66.5%	69.1%	2.6%
		ResNet-18	$\langle 2,4\rangle$ $\langle 2,4\rangle$ $\langle 2,4\rangle$ $\langle 2,4\rangle$ 32	68.2%	69.1%	0.9%
	Ours	ResNet-34	$\langle 2, 4 \rangle \langle 2, 4 \rangle \langle 2, 4 \rangle \langle 32$	75.3%	76.1%	0.8%
		VGG-16	$\langle 2, 4 \rangle \langle 2, 4 \rangle \langle 2, 4 \rangle \langle 32$	70.8%	70.9%	0.1%
		GoogleNet	$\langle 2, 4 \rangle \langle 2, 4 \rangle \langle 2, 4 \rangle \langle 32$	69.6%	69.5%	-0.1%

are left unquantized following previous studies [14], [26], [42]. On both CIFAR-10 and ImageNet, SGD with momentum 0.9 and weight decay 5e-4 is used, and the initial learning rate is set to 0.1. We train the models for 90 epochs on ImageNet, and decay the learning rate by 10 every 30 epochs. On CIFAR-10, we train the models for 160 epochs and decay the learning rate by 10 at epoch 80 and 120. We experiment with the MLS tensor formats using different  $\langle E_x, M_x \rangle$  configurations, the group-wise scaling are in  $\langle 8, 1 \rangle$  format for all experiments in Table II. And we adopt the same quantization bit-width for weight, activation and error for a simpler hardware design.

#### B. Results on CIFAR-10 and ImageNet

The training results on CIFAR-10 and ImageNet are shown in Table II. We can see that our method can achieve a better balance between higher accuracy and lower bit-width. Previous study [26] found that quantizing error to a low bit-width hurt the accuracy, but our method can quantize error to  $M_x = 1$  on CIFAR-10, with a small accuracy drop of 0.48%, 0.55%, and 0.42% for ResNet-20, GoogleNet, and VGG-16, respectively.

On ImageNet, the accuracy degradation of our method is rather minor under 8-bit quantization (0.6% accuracy drop from 69.1% to 68.5%), which is comparable with other stateof-the-art work. In the cases with lower bit-width, our method achieves a higher accuracy (66.5%) with only 4-bit than [27] who uses 8-bit (66.4%). With  $\langle 2, 4 \rangle$  data format, for all the models including ResNet-18, ResNet-34, VGG-16, and GoogleNet, our method can achieve an accuracy loss less than

TABLE III NUMBER OF OPERATIONS AND SENSITIVITY OF RESNETS, VGG-16, AND GOOGLENET.

Model	Inference GOPs	Acc. Drop of 6-bit Training
ResNet-18	1.88	0.9%
ResNet-34	3.59	0.8%
VGG-16	15.25	0.1%
GoogleNet	1.58	-0.1%

1%. In this case, the bit-width of the intermediate results is  $2M_x+2^{E_x+1}-2 = 14$ , which means that the accumulation can be conducted using integers, instead of floating-points [14], [15], as we disscussed in Sec. V-B. Although a previous work [31] quantizes W/A/E to 4-bit, the three different types of Convs between them are different, which requires three different unit implementations. In contrast, our work unifies the W/A/E format and the Conv calculation, thus requires only one type of Conv unit.

We note that the performance of VGG and GoogleNet CNN models in low-bit training is better than ResNets. We think that this is because there are fewer channels in ResNet than VGG and GoogleNet when the network depth configuration is similar. And the smaller redundancy of ResNets makes them more sensitive to quantization errors. In fact, VGG-16 is 7 times as much as ResNet-18 in terms of computation, as shown in Table III. That means even if ResNet adopts a higher bitwidth and higher accuracy scheme for training, it still has

TABLE IV Accuracy of training ResNet-20 on CIFAR-10. "Div." means that the training failed to converge. "None" means that group-wise scaling is not used (#group=1).

#group	$M_g$	$E_x$	$M_x=4$	$M_x=3$	$M_x=2$	$M_x=1$
1	None	0	90.02	85.68	Div.	Div.
с	0	0	91.54	88.35	82.29	Div.
n	0	0	91.78	89.62	80.71	Div.
nc	0	0	92.14	91.64	88.97	76.98
nc	1	0	92.37	91.73	90.39	82.61
1	None	0	90.02	85.68	Div.	Div.
1	None	1	91.67	90.11	84.72	70.4
1	None	2	92.32	92.34	91.58	90.32
nc	1	0	92.37	91.73	90.39	82.61
nc	1	1	92.52	92.16	91.48	89.97
nc	1	2	92.37	92.65	92.05	91.97

a higher energy efficiency. In contrast, the model structure of GoogleNet class shows a higher adaptability in the face of lowbit training scenarios, which brings inspiration to the future network architecutre design for low-bit training scenarios.

# C. Ablation Studies

1) Group-wise Scaling: Group-wise scaling is beneficial as the data ranges vary across different groups. We compare the average relative quantization errors (AREs) of using the three grouping dimensions (Sec. IV-A) with  $\langle 8, 1 \rangle$  group-wise scaling format and  $\langle 0, 3 \rangle$  element format. The first row of Fig. 7 shows that the AREs are smaller when each tensor is split to  $N \times C$  groups. Furthermore, we compare these grouping dimensions in the training process. The first section of Table IV shows that when tensors are split to  $N \times C$ groups, the training accuracy is higher. This indicates that the reduction of AREs is important for the accuracy of low-bit training. And we can see that  $M_g = 1$  is important for the accuracy, especially with low  $M_x$  (e.g., when  $M_x=1$ , 76.98% V.S. 82.61%).

To show that the low-bit training is distinct from previous efficient inference studies, we add an ablation study of "error" format to further demonstrate: W/A are quantized with groupwise scaling factors consists of only exponent, when error is also quantized as this, the accuracy is 90.7%. After introducing our  $\langle 8, 1 \rangle$  group-wise scaling for error, the accuracy is 91.9%. This indicates that MLS format is better than shared exponent in [20] for a benign training.

2) Element-wise Exponent: To study the influence of the element-wise exponent, we compare the AREs of quantization with different  $E_x$  without group-wise scaling, and the results are shown in the second row of Fig. 7. Intuitively, using more exponent bits results in larger dynamic ranges and smaller AREs. And with larger  $E_x$ , the AREs of different layers are closer. Besides the ARE evaluation, Table IV shows that a larger  $E_x$  achieves a better accuracy, especially when  $M_x$  is extremely small.

As shown in Fig. 7 Row 3 and Table IV, when jointly using the group-wise scaling and the element-wise exponent, the ARE and accuracy are further improved. And we can

TABLE V The power evaluation (MW) results of MAC units with different arithmetic, simulated by Design Compiler with TSMC

Operation	MUL	LocalAcc
Full Precision	2.311	0.512
8-bit FP [14]	0.105	0.512
8-bit INT [12]	0.155	0.065
Ours	0.124	0.065

65NM PROCESS AND 1GHZ CLOCK.

see that the group-wise scaling is important for simplifying the floating-point accumulator to a fixed-point one: One can use a small element-wise exponent with group-wise scaling (#group=nc,  $M_g$ =1,  $E_x$ =0, Acc.=92.37%) to get a comparable accuracy to a configuration with larger  $E_x$ =2 without groupwise scaling (Acc.=92.32%).

#### D. Hardware Energy Consumption

Fig. 1 shows a typical convolution hardware architecture, which consists of three main components: local multiplication (MUL), local accumulation (LocalACC), and addition tree (TreeAdd). Our framework mainly improves the local multiplications and accumulations. Compared with the full-precision design, we simplify the floating-point multiplication (FP MUL) to use a bit-width less than 8 and the local floating-point (FP ACC) to use 16-bit or 32-bit integer. To evaluate the energy consumption, we implement the RTL design of the MAC unit with different arithmetic. Table V shows the hardware power results given by Design Compiler simulation with TSMC 65nm process and 1GHz clock frequency. Then, using the numbers of different operations in convolution, we can estimate our energy efficiency improvement ratio r in a single  $3 \times 3$  convolution as

$$r = [2.311(\#MUL) + 0.512(\#LocalACC) + 0.512(\#TreeAdd)]$$
  

$$\div [0.124(\#MUL) + 0.065(\#LocalACC + \#GroupwiseScale)$$
  

$$+ 0.512(\#TreeAdd)] \approx 11.5$$
(12)

where GroupwiseScale is the group-wise scaling that could be implemented efficiently as in Eq. 8. The energy estimation of  $3 \times 3$  convolutions is also shown in Fig. 2. Next, in Sec. VI-E, we present the energy analysis details of the whole network, which takes the energy consumption of different types of operations into consideration.

## E. Energy Estimation Details

For completeness, we give the detailed energy estimation of different operation types when training ResNet-34 on ImageNet in Table VI, in which all overheads introduced by our method are considered. The energy consumption is calculated by multiplying the operation amount (Table I) and the energy consumption of each operation (Table V).

Considering a convolution with  $C_i$  input channels,  $C_o$  output channels,  $K \times K$  kernel size, and  $W \times H$  feature map size, the operation amounts of floating-point multiplications and additions are  $C_i \times C_o \times K \times K \times W \times H$ , and the operation amount in the whole network is calculated by accumulating

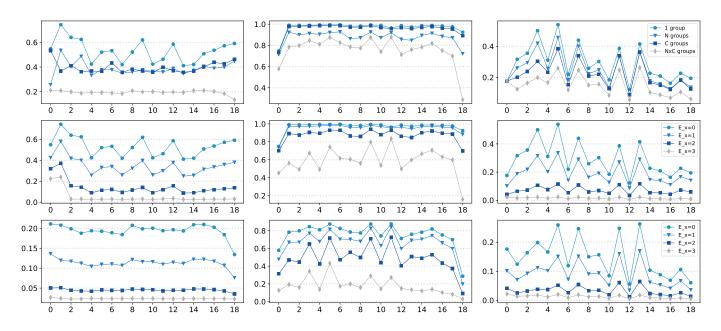


Fig. 7. Average relative quantization errors (AREs) of weight, error, activation (left, middle, right) in each layer when training a ResNet-20 on CIFAR-10. X axis: Layer index. Row 1: Different grouping dimensions ((0, 3) formatted  $\bar{X}$ , (8, 1) formatted  $S_g$ ); Row 2: Different  $E_x$  ( $\langle E_x, 3 \rangle$  formatted  $\bar{X}$ , no group-wise scaling); Row 3: Different  $E_x$  ( $\langle E_x, 3 \rangle$  formatted  $\bar{X}$ , (8, 1) formatted  $S_g$ ,  $N \times C$  groups).

TABLE VI THE COMPARISON OF THE DETAILED ENERGY ESTIMATION OF TRAINING RESNET-34 ON IMAGENET USING FULL-PRECISION TRAINING AND OUR LOW-BIT TRAINING FRAMEWORK. "DQ" MEANS DYNAMIC QUANTIZATION, WHICH IS AN ADDITIONAL OPERATION IN OUR FRAMEWORK.

Op Name	Ful	l Precision Trair	ing		Our Low-Bit Training	
	Ор Туре	Op Amount	Energy/µJ	Ор Туре	Op Amount	Energy/µJ
Conv	FloatMul	1.12E+10	25900	FP7Mul	1.12E+10	1390
	FloatAdd	1.12E+10	5740	IntAdd	1.12E+10	729
	-	0	0	FloatAdd	1.21E+09	620
BN	FloatMul	4.87E+07	101	FloatMul	4.87E+07	101
	FloatAdd	4.38E+07	24.9	FloatAdd	4.38E+07	24.9
FC	FloatMul	3.07E+06	7.1	FloatMul	3.07E+06	7.1
	FloatAdd	3.07E+06	1.57	FloatAdd	3.07E+06	1.57
SGD Update	FloatMul	5.16E+07	119	FloatMul	5.16E+07	119
	FloatAdd	5.16E+07	26.4	FloatAdd	5.16E+07	26.4
DQ	-	0	0	FloatMul FloatAdd	3.90E+7 + 6.88E+7 1.95E+6 + 3.44E+7	249 27.6
EW-Add	FloatAdd	2.88E+06	1.47	FloatAdd	2.88E+06	1.47
	-	0	0	FloatMul	2.88E+06	6.66
Sum			32000			3130

the operation amounts of each layer in both the forward and backward processes. In our low-bit training framework, floating-point additions are only reserved in the adder tree, and the amount is  $C_i \times C_o \times W \times H$ . The amount of integer accumulation is equal to the other local addition and shifting (which is the same as the adder tree). The **group-wise scaling** factors introduce additional scaling. Fortunately, when using the  $\langle E_g, 0 \rangle$  or  $\langle E_g, 1 \rangle$  format, we can implement the groupwise scaling efficiently with shifting (Eq. 4). And the energy consumption is comparable to a LocalACC operation. We have already taken this overhead into account when estimating the energy efficiency improvement ratio of convolution in Eq. 12.

For batch normalization, fully connected layer, SGD up-

date, the operation amount and energy consumption are the same for both the full-precision and our low-bit training framework. Specifically, 9 multiplications and 10 additions are performed on each element of a  $C \times W \times H$  feature map in the forward and backward processes for batch normalization.

The forward process of batch normalization is:

$$\mu = \frac{1}{M} \sum_{i=1}^{M} x_i$$

$$\sigma^2 = \frac{1}{M} \sum_{i=1}^{M} x_i^2 - \mu^2$$

$$y_i = \frac{x_i - \mu}{\sqrt{\sigma^2 + 0.00005}}$$

$$z_i = \gamma y_i + \beta.$$
(13)

We can see that in the forward process of batch normalization, for each input element, one addition is required to calculate the batch mean, and one multiplication and one addition are used to calculate the batch variance, and two multiplications and two additions are used for normalization and affine transformation.

The backward process of batch normalization is:

$$\frac{\partial L}{\partial \gamma} = \sum_{i=1}^{M} \frac{\partial L}{\partial z_i} \cdot y_i$$

$$\frac{\partial L}{\partial \beta} = \sum_{i=1}^{M} \frac{\partial L}{\partial z_i}$$

$$\frac{\partial L}{\partial y_i} = \frac{\partial L}{\partial z_i} \cdot \gamma$$

$$t_1 = \sum_{j=1}^{M} \frac{\partial L}{\partial y_j}$$

$$t_2 = \sum_{j=1}^{M} (\frac{\partial L}{\partial y_j} \cdot y_j)$$

$$\frac{\partial L}{\partial x_i} = \frac{M \frac{\partial L}{\partial y_i} - t_1 - y_i \cdot t_2}{M \cdot \sqrt{\sigma^2 + 0.00005}}.$$
(14)

There are six multiplications and six additions performed on one element in the backward process of batch normalization ("1M1A, 1A, 1M, 1A, 1M1A, 3M2A" for each formula in Eq. 14, respectively). As shown in Table I, the number of multiplication and addition operation in batch normalization is orders of magnitude smaller than that in the convolutions. Hence, the energy consumption of batch normalization is relatively smaller compared with convolution.

As for **dynamic quantization**, we consider that 4 multiplications and 2 additions are needed for one element: one addition is to calculate the max (Alg. 2 Line 2 in the original paper) and the other one is to calculate the sum of  $Frac_{xs}$  and R (Alg. 2 Line 13 in the original paper), and the four multiplications are used for the Alg. 2 Line 4 and Line 9 in the original paper. Note that other multiplications and divisions in Alg. 2 describe the simulation of the dynamic quantization process on the floating-point platform, and they do not actually introduce overhead. The number of elements is  $C \times W \times H$  for activation and error, and  $C_i \times C_o \times K \times K$  for weight, and their energy consumption are shown separately in Table VI.

For **element-wise addition** of two MLS tensors  $z_1, z_2$ , we need to multiply the ratio of their tensor-wise scales  $S_t^{z_1}/S_t^{z_2}$  to  $Z_2$ , and then the element-wise addition can be conducted.

Therefore, extra multiplications of the same amount are needed in our low-bit training framework. The last row of Table VI shows the sum of the energy consumption of previous operations, and the results are not exactly the sum of the numbers in previous rows. The results show that our low-bit training framework achieves  $32000 \div 3130 = 10.2 \times$  higher energy efficiency than full-precision training. The energy consumption calculation of other networks and 8-bit floating-point training can be conducted similarly as the above analysis, and is not discussed here.

To summarize, the introduced overhead of our framework is low compared with the reduced cost. Taking all overheads into consideration, we can estimate that our whole low-bit training framework could achieve  $8.3 \sim 10.2 \times$  higher energy efficiency than the full-precision framework when training different models on ImageNet. Compared with previous low-bit floating-point training frameworks [14], our framework can achieve  $1.9 \sim 2.3 \times$  higher energy efficiency due to the simplified integer accumulator.

#### VII. CONCLUSION

This paper proposes a low-bit training framework to enable training CNNs with lower bit-width convolution while retaining the accuracy. Specifically, we design a multi-level scaling (MLS) tensor format containing tensor-wise scaling, group-wise scaling and element-wise scaling. And we describe the corresponding quantization procedure and low-bit convolution arithmetic, and analyze why our data format and hardware design bring energy efficiency improvements. In the hardware implementation, instead of using traditional systolic array hardware architecture, we adopt an adder tree architecture hardware to support our MLS data format. Experimental results and the energy consumption simulation of the corresponding computing unit demonstrate the effectiveness of our framework. Compared with previous low-bit integer training frameworks, our framework can retain a higher accuracy for a variety of models, including ResNets, VGG, and GoogleNet. Compared with previous low-bit floating-point training frameworks, our framework can achieve much higher energy efficiency.

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