Low Jitter and Multirate Clock and Data Recovery Circuit Using a MSADLL for Chip-to-Chip Interconnection

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***Abstract*—A fully integrated clock and data recovery circuit (CDR) using a multiplying shifted-averaging delay locked loop and a rate-detection circuit is presented. It can achieve wide range and low jitter operation. A duty-cycle-insensitive phase detector is also proposed to mitigate the dependency on clock duty cycle variations. The experimental prototype has been fabricated in a 0.25-μm 1P5M CMOS technology and occupies an active area of 2.89 mm^2. The measured CDR could operate from 125 Mb/s to 2.0 Gb/s with a bit error rate better than 10^{-12} from a 2.5-V supply. Over the entire operating frequency range, the maximum rms jitter of the recovered clock is less than 4 ps.**

***Index Terms*—Clock and data recovery circuit (CDR), delay-locked loop (DLL), multirate, phase-locked loop (PLL).**

I. Introduction

DUE TO increasing computational capability of processors, the demand for high-speed interfaces to communicate information with peripheral devices has been growing dramatically. However, the speed of many digital systems is limited by the buses between different modules such as multiprocessor interconnection, and processor-to-memory, computer-to-computer, and computer-to-peripheral interfaces. Thus, considerable design efforts have focused on implementing high-speed I/O interfaces for multiple applications and standards recently. In the *mesochronous* system [1], [2], the clock is distributed through a separate clock channel as illustrated in Fig. 1. The clock and data recovery circuit (CDR) becomes much simpler since it is reduced to deal only with the timing skew between the clock and data channels. The delay locked loop (DLL)-based CDR architecture is thus suitable to implement for applications in the *source-synchronous* system. For example, the proposed CDR could be used for chip-to-chip interconnection as shown in Fig. 1.

Compared with a phase-locked loop (PLL)-based CDR, the proposed DLL-based implementation does not accumulate cycle-to-cycle jitter, allowing low jitter operation [3], [4] and simplifying the loop filter. For a conventional DLL-based CDR [4], it is difficult to extend the operating frequency range due to the limited delay range of the VCDL. The proposed CDR exhibits a wide operating range from 0.125 to 2.0 Gb/s by adopting a multiplying shifted-averaging DLL (MSADLL) and the rate-detection circuit. The MSADLL using the shifted-averaging voltage-controlled delay line (VCDL) generates precise multiphase clocks [5], [6] and synthesizes a multiplying clock with $M(= 1, 2, 4, 8, 16)$ times frequency of the reference clock to sample the data [3]. When the mismatch exists among the delay stages, it does not guarantee to have the identical delay time for every delay stage. These delay mismatches will generate the fixed pattern jitter to the multiplying clock. The MSADLL using the shifted-averaging VCDL can average the mismatch-induced timing error among the delay stages and improve jitter performance of the multiplying clock. This paper is organized as follows. The proposed CDR architecture is introduced in Section II. In Section III, the circuit descriptions are illustrated. The experimental results are shown in Section IV and the conclusions are given in Section V.

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II. Proposed CDR Architecture

A. Operation of the CDR

Fig. 2 illustrates the architecture of the proposed CDR. It is based on cascading two DLLs. The MSADLL synthesizes a multiplying clock (Mclk) with $M(= 1, 2, 4, 8, 16)$ times frequency of the reference clock to sample the data [3]. The duty-cycle-insensitive phase detector, the charge pump, and the loop filter construct another loop to align the phases between data and Mclk by increasing or decreasing the delay of the selective buffer. The rate-detection circuit compares the date rate and the frequency of Mclk dynamically and switches the operation mode of the MSADLL and selective buffer. The operation mode of the MSADLL and selective buffer corresponding to different values of M is listed in Table I.

Initially, the control voltages Vctrl2 and Vctrl1 of the selective buffer and MSADLL, are biased to half VDD and VDD [7], respectively. The delay of the VCDL in the MSADLL is set to its minimum value. The multiplication factor M of the selective buffer and the MSADLL are set to one.

The locking procedure of the proposed CDR can be divided into two steps according to the phase error of the MSADLL. In the first step, the initialization circuit keeps the delay time of the selective buffer constant. The MSADLL begins to lock to the delay, which is equal to one clock period of Ref_d. The start-control circuit [8], shown in Fig. 5, will let the down signal of the phase frequency detector (PFD) be activated first after

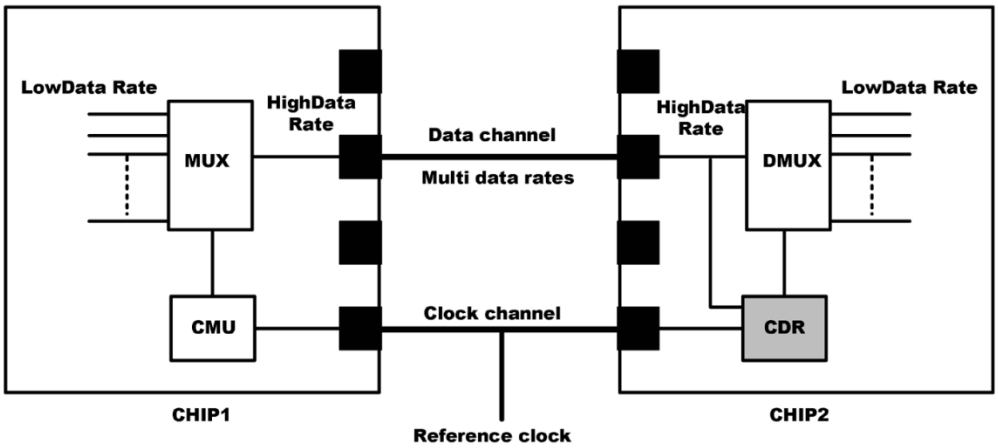

Fig. 1. CDR for chip-to-chip interconnection.

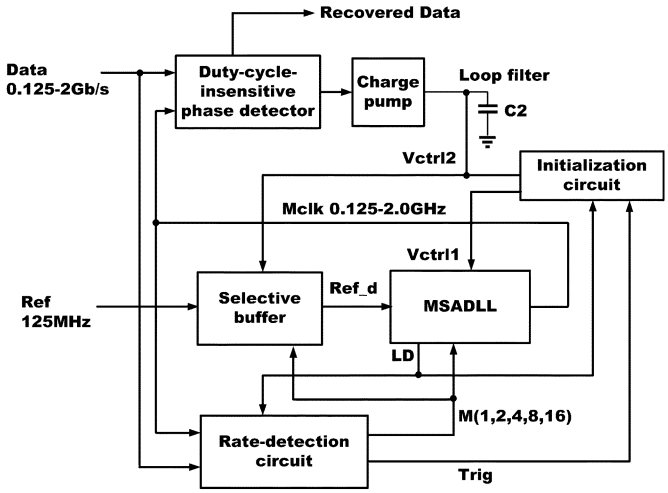

Fig. 2. Proposed multirate CDR.

TABLE I
OPERATION MODE OF MSADLL AND SELECTIVE BUFFER

	Selective Buffer (Selected Output stage)	MSADLL (Selected Output stage)
M=1	16	"set" pulse: 16 "reset" pulse: 8
M=2	8	"set" pulses: 16, 8 "reset" pulses: 12, 4
M=4	4	"set" pulses: 16, 12, 8, 4 "reset" pulses: 14, 10, 6, 2
M=8	2	"set" pulses: 16, 14, 12, 10, 8, 6, 4, 2 "reset" pulses: 15, 13, 11, 9, 7, 5, 3, 1
M=16	1	"set" pulses: 16~1 "reset" pulses: self-generated

two consecutive rising edges of clk16 causing the delay of the VCDL to increase. The start-control circuit makes the delay of the VCDL increase until its delay is equal to one clock period of the reference clock, so the MSADLL will not fall into false locking or harmonic locking even when $16T_{\rm Dmin} < 0.5T_{\rm Ref}$. $T_{\rm Dmin}$ and $T_{\rm Ref}$ represent the minimum delay of a delay cell and the period of the reference clock, respectively. When the MSADLL achieves the lock state, the delay between two successive stages will be $T_{\rm Ref}/16$. If the lock detector [9] detects the phase error of the MSADLL to be within the lock window, lock detector (LD) goes high. The locking procedure will shift to the second step. The duty-cycle-insensitive phase detector, the charge pump, and the loop filter will start to align the phases between data and $\rm Mclk$ by adjusting the delay of the selective buffer. Meanwhile, the rate-detection circuit will be activated to compare the frequencies of $\rm Mclk$ and data. Its operation is independent of the phase error of the duty-cycle-insensitive phase detector. If the data rate is higher than the frequency of $\rm Mclk$, it will increase the multiplication factor of the selective buffer and the MSADLL. The control voltage of the selective buffer is reset to half supply voltage (VDD) through the initialization circuit. The duty-cycle-insensitive phase detector, the charge pump and the loop filter will align the phase again.

In this design, the proposed CDR adjusts the reference clock into the MSADLL rather than the phase coming out the MSADLL. Adjusting the reference clock into the MASDLL, the input of the delay line is the reference clock. Since the frequency of the reference is 125 MHz, the bandwidth of delay cell could be low enough to make the reference clock pass through delay line without amplitude attenuation. However, adjusting the phase coming out of the MSADLL, the input of the delay line is the multiplying clock whose operating frequency could be varied from 125 MHz to 2 GHz. The highest operating frequency of the delay line is limited by the bandwidth of the single delay unit while the lowest operating frequency is restricted by the length of the delay line. In order to meet the maximum and minimum speed requirement at the same time, the delay line should be composed of a huge number of high bandwidth delay units. Thus, adjusting the phase coming out the MSADLL will result in a larger chip area and more power dissipations than altering the phase of the input reference clock.

B. Analysis of the CDR Stability

Cascading two loops in this CDR may lead the overall system to be unstable. It is convenient to analyze the CDR stability by adopting root locus techniques [10]. The analysis in this subsection will show that the stable condition of the proposed CDR can be easily achieved. Fig. 3 shows the z-domain model of the CDR, where $\Phi_{\rm Ref}$ and $\Phi_{\rm Data}$ represent the reference clock and

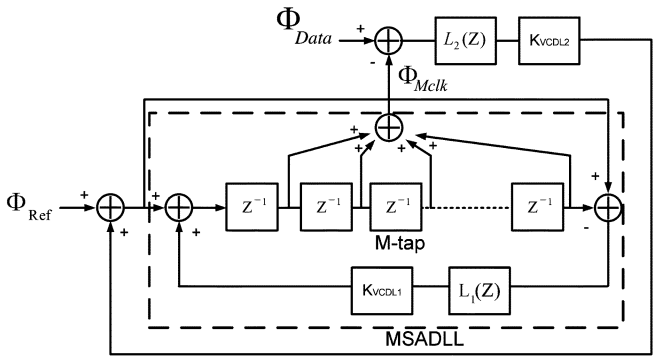

Fig. 3. Z-domain model of the proposed CDR.

data, respectively, and $\Phi_{\rm Mclk}$ is the multiplying clock [11]. Assuming the effective sampling period of this z-domain model is equal to the period of the multiplying clock, $T_{\rm Mclk}$, the function of multiplying frequency can be modeled as an M-tap finite-impulse response (FIR) filter. Each "Z^{-1}" block delays input signal by $T_{\rm Mclk}$ and then their outputs are synthesized a multiplying clock, $\Phi_{\rm Mclk}$. Since this CDR can operate in multi data rates, the operation mode of MSADLL will be varied corresponding to different values of M as shown in Table I. For example, when $M = 16$, the MASDLL combines all delayed version edges from VCDL to synthesize a clock, whose frequency is 16 times of the reference clock. In this operation mode, the MASDLL can be modeled as a 16-tap FIR. One tap delay is equal to the delay time of one unit delay stage. $K_{\rm VCDL1}$ and $K_{\rm VCDL2}$ is the gain of the delay line in the MSADLL and the selective buffer, respectively. Their units are defined as radians per cycle per volt, where a cycle refers to the corresponding sampling period. According to different multiplication factors, the selective buffer will change the number of delay stages to get gain constant, i.e., $K_{\rm VCDL2} = K_{\rm VCDL1}$. In this CDR, each loop filter consists of only a capacitor. The open-loop transfer functions, $\rm L_1(Z)$ and $\rm L_2(Z)$, in the MSADLL and CDR could be expressed, respectively, as

$$L_1(Z) = \frac{I_{\rm cp1} M T_{\rm Mclk}}{2\pi C_1} \frac{1}{1 - Z^{-M}}$$
$$L_2(Z) = \frac{I_{\rm cp2} T_{\rm Mclk} D_T}{2\pi C_2} \frac{1}{1 - Z^{-1}} \quad (1)$$

respectively. $I_{\rm CP1}$ and $I_{\rm CP2}$ are the charge pump current while C_1 and C_2 are the loop filter in the MSADLL and CDR, respectively. D_T is the data-transition density. Let $I_{\rm CP1} = I_{\rm CP2} = I_{\rm CP}$ and $C_1 = ((C_2)/(N)) \equiv C$, where N is the ratio of two loop filter capacitances. The loop gain for analyzing the CDR stability is given by

$$\text{loop gain} = \frac{1}{N}\left[\frac{I_{\rm cp} T_{\rm Mclk} D_T}{2\pi C}\frac{1}{1 - Z^{-1}} \times K_{\rm VCDL1}\frac{1 + \frac{I_{\rm cp} M T_{\rm Mclk}}{2\pi C} K_{\rm VCDL1}\frac{1}{1-Z^{-M}}}{1 + \frac{I_{\rm cp} M T_{\rm Mclk}}{2\pi C} K_{\rm VCDL1}\frac{Z^{-M}}{1-Z^{-M}}}\sum_{i=1}^{M} Z^{-i}\right] \quad (2)$$

For $I_{\rm cp} = 40$ uA, $C = 20$ pF, $K_{\rm VCDL1} = K_{\rm VCDL2} = 4.3$ radians per cycle per volt, $D_T = 0.5, M = 16, T_{\rm Mclk} = 0.5$ ns, and varying the value of $1/N$ from zero to infinite, the root locus can be shown in Fig. 4. The location of 16 open-loop poles and 16 open-loop zeros are very close and inside the unit

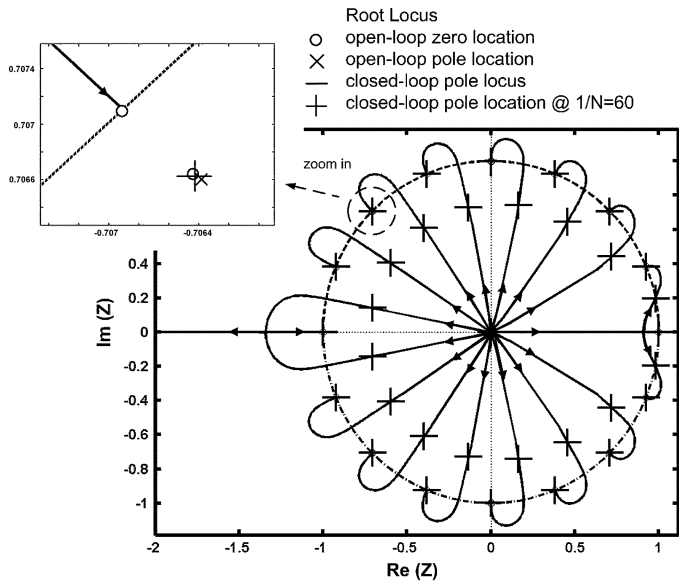

Fig. 4. Root locus of the closed-loop poles $(M = 16)$.

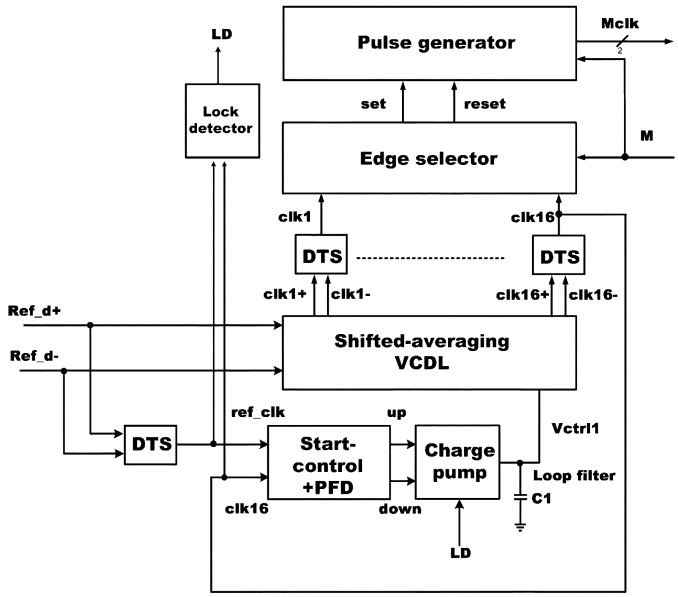

Fig. 5. Architecture of the multiplying shifted-averaging DLL.

cycle. Since the location of the closed-loop poles is a function of $1/N$, the z-domain model can predict the stable condition for this CDR of $1/N < 60$. The stable condition will be varied accordingly with different multiplication factors. To ensure CDR stability over all operating conditions, the relationship between two loop filter capacitances should be

$$C_1 < 60 C_2. \quad (3)$$

III. Circuit Description

A. MSADLL

The MSADLL is similar to a conventional DLL. The key differences are a 16-stage shifted-averaging VCDL [5], [6], an edge selector, a pulse generator, and a lock detector as shown in Fig. 5. A technique called dynamic bandwidth-adjusting is adopted here to shorten the lock time without compromising the

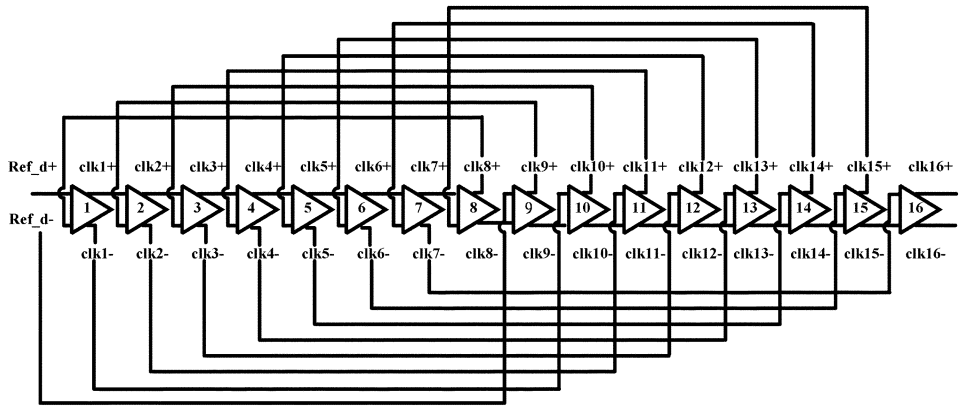

Fig. 6. Sixteen-stage shifted-averaging VCDL.

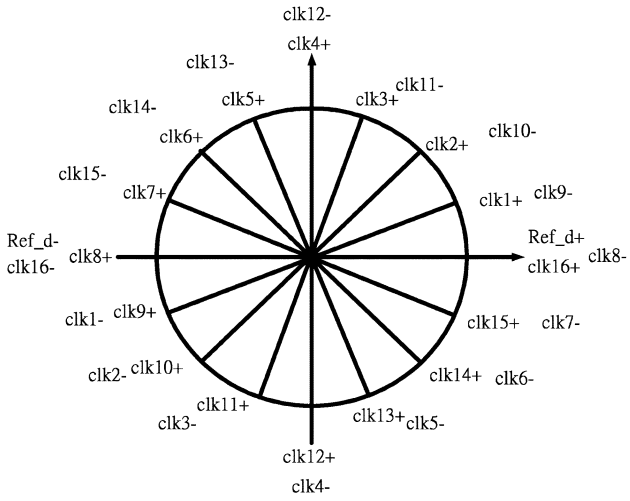

Fig. 7. Phase diagram of $N(=16)$ delay stages in the steady state.

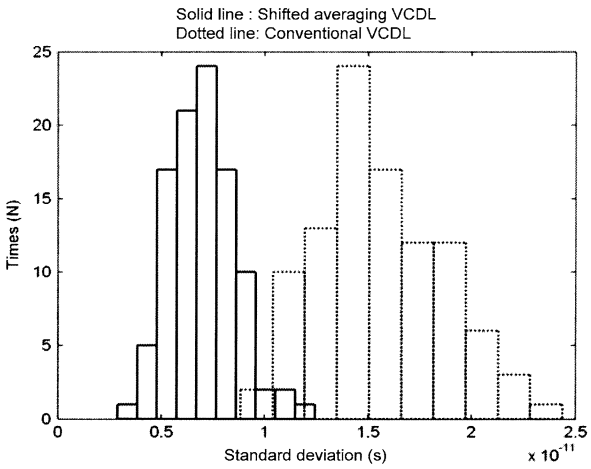

Fig. 8. Simulated results of the static timing error among delay stages.

jitter performance. Figs. 6 and 7 show the schematic and phase relation among the delay stages of the shifted-averaging VCDL, respectively (assuming that the reference clock possesses a 50% duty cycle and the DLL locks the delay with 360 degree phase

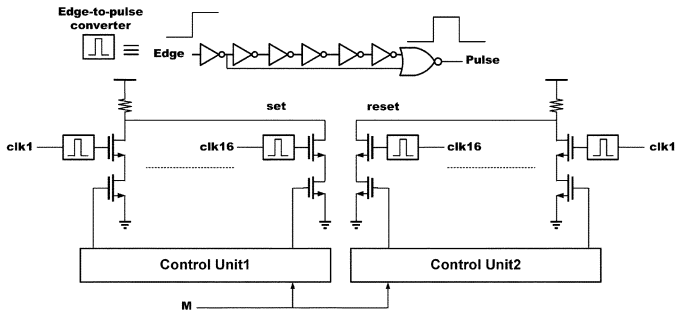

Fig. 9. Schematic of the edge selector.

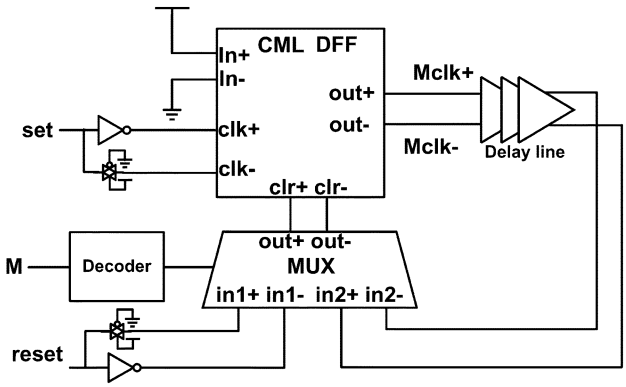

Fig. 10. Schematic of the pulse generator.

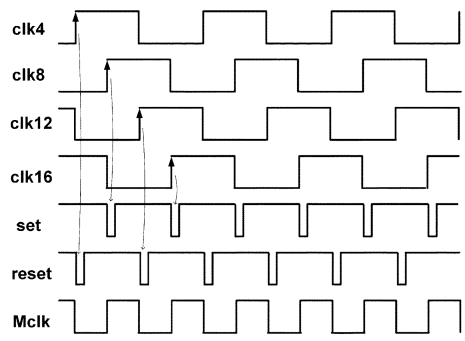

Fig. 11. Timing diagram of the edge selector $(M=2)$.

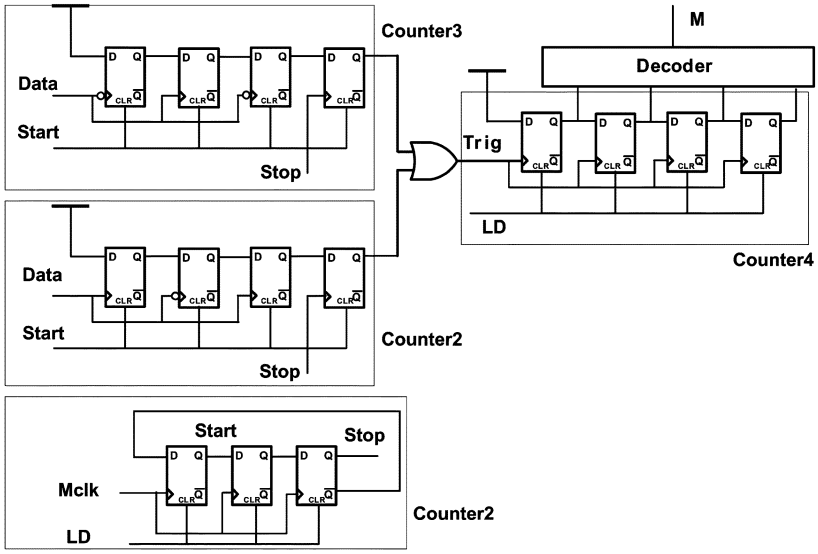

Fig. 12. Rate-detection circuit.

shift). For a 16-stage shifted-averaging VCDL, the phase relation for all outputs in the lock state can be expressed as

$$\mathrm{clk}(i)+ = \mathrm{clk}(i+8)- \quad \text{and} \quad \mathrm{clk}(i)- = \mathrm{clk}(i+8)+ \quad (4)$$

where $\mathrm{clk}(i)+$ is the positive output of the i-th stage, $\mathrm{clk}(i)-$ is the negative output of the i-th stage, and $0 \leq i \leq 8$. Utilizing the shifted-averaging technique in the multiplying DLL can reduce the fixed pattern jitter corrupted by the mismatch-induced timing error among delay stages. Fig. 8 shows one hundred points Monte Carlo simulated results for static timing errors among the delay stages, where 10% random mismatches in the aspect ratio of the delay stages are added into the conventional VCDL and the proposed one, respectively. At a given operating frequency (125 MHz), the results manifest the shifted-averaging VCDL improves phase matching. In addition, a 3-dB improvement in jitter performance can be obtained due to the mutually uncorrelated error sources at the inputs of each delay stage [5], [6].

The precise multiphase outputs are sent to the edge selector as shown in Fig. 9. Six inverters and one NOR gate form an edge-to-pulse converter. The edge selector can be divided into two parts, one of which generates the "*set*" pulses and the other produces the "*reset*" pulses. The operation mode corresponding to different values of M is summarized in Table I. Ideally, the phase difference between the "*set*" pulses and the "*reset*" pulses is 180° to ensure the duty cycle of Mclk is 50%. Fig. 10 shows the schematic of the pulse generator. The current mode logic D flip-flop (CML DFF) responds to the "set" and "reset" functions. The inverter and T-gates are used as a single-ended-to-differential converter. Fig. 11 depicts the timing diagram when the multiplication factor is 2. Control unit 1 will select clk8 and clk16 as the "*set*" pulses to set the pulse generator to high while the control unit 2 will select clk4 and clk12 as the "*reset*" pulses to reset the pulse generator to low. In order to extend further the multiplication factor from $N/2$ to N [12], where N is the number of delay stages, a multiplexer and a delay line can be inserted into the feedback loop of the pulse generator. When the

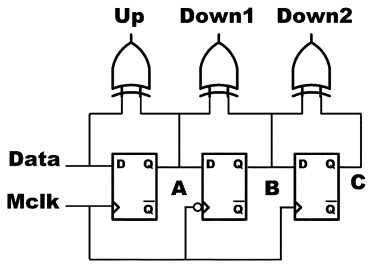

Fig. 13. Schematic of the duty-cycle-insensitive phase detector.

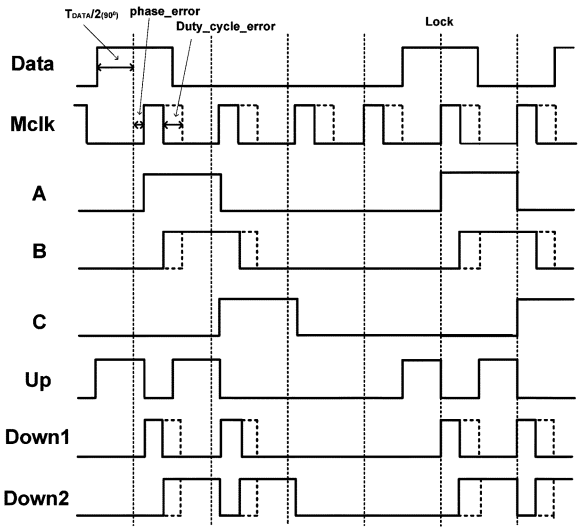

Fig. 14. Timing diagram of the phase detector.

multiplication factor is 16, control unit 1 selects all outputs from the differential-to-single-ended (DTS) converters [13] as "*set*" pulses to the pulse generator. The control unit 2 is disabled. All pulses trigger the pulse generator and then reset it.

To minimize delay mismatches among the DTS converters [13], the edge selector and the pulse generator, the layout has been carefully done to match loading of each path. However, unavoidable random mismatches still exist to diverge the duty

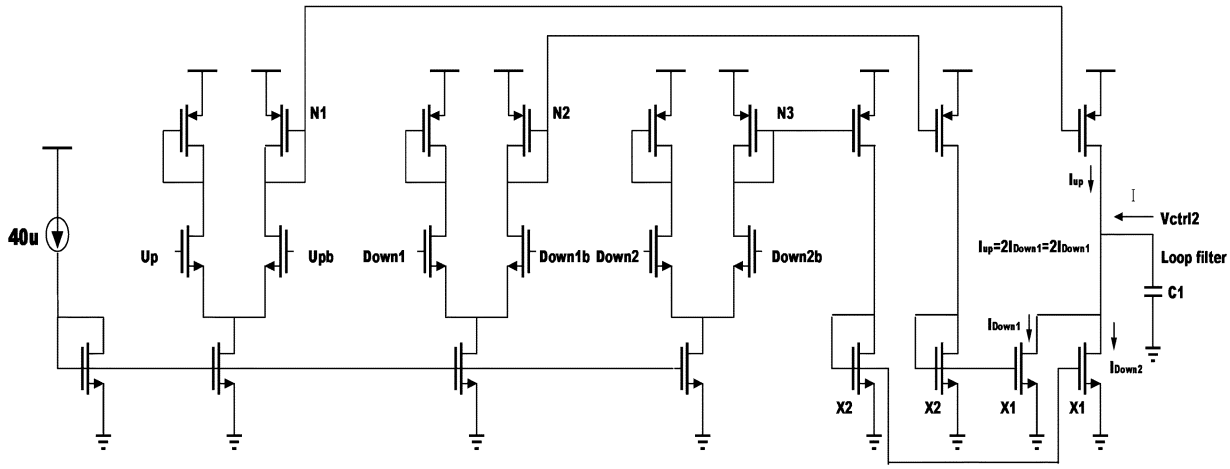

Fig. 15. Schematic of the charge pump.

cycle of Mclk from 50% [14]. Moreover, when the multiplication factor is 16, the delay of the feedback loop in the pulse generator can not be exactly controlled causing the duty cycle of Mclk deviating from 50% due to process, voltage, and temperature variations. The duty cycle variations mentioned above can be tolerated by using the proposed duty-cycle-insensitive phase detector. A dynamic logic style PFD [15] is adopted to overcome speed limitations and reduce the dead zone. The delay cell circuit is similar to [15].

B. Rate-Detection Circuit

The rate-detection circuit, shown in Fig. 12, compares the date rate and the frequency of the Mclk dynamically and switches the operation mode of the MSADLL and selective buffer accordingly. According to different M, the operation mode of the MSADLL and selective buffer is shown in Table I. The rate detection algorithm is based on the fact that if the data rate is equal to the frequency of the clock, the maximum number of the transition in the data is one during the period between two successive rising edges of the clock in a full-rate CDR architecture [16]. In order to relax the speed requirement and prevent false decisions, the rate-detection circuit detects the number of transitions in the data during the period between three successive rising edges of Mclk. Initially, the multiplication factor is set to one. After the LD goes high, the rate detection process will be activated. Its operation is independent of the phase error of the duty-cycle-insensitive phase detector. Counter 1 will generate a detection window, defined by "*start*" and "*stop*" signals, every three consecutive rising edges of the clock. If the number of transitions in the data is larger than 2 during this window, counter 4 will be triggered and then update the multiplication factor of the selective buffer and MSADLL. The frequency of Mclk will be doubled. Simultaneously, it will send a signal Trig to the initialization circuit to reset the control voltage of the selective buffer, Vctrl2, to half VDD. The duty-cycle-insensitive phase detector, the charge pump and the loop filter will attempt to align the phase again. The process will persist until the frequency of Mclk is equal to the data rate.

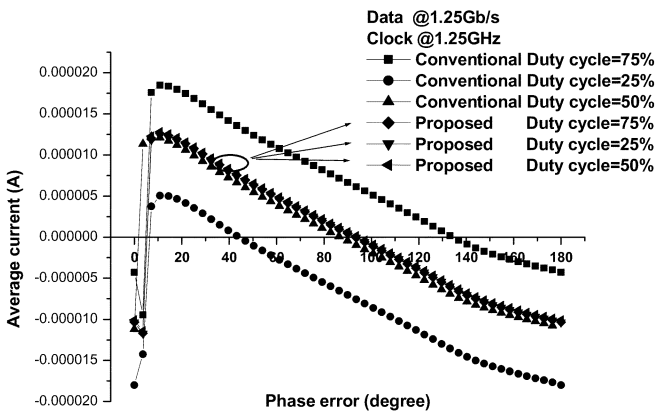

Fig. 16. Simulated results of the phase detectors with different duty cycle.

C. Duty-Cycle-Insensitive Phase Detector

Fig. 13 shows a simplified schematic of the proposed phase detector. Although it is shown as a single-ended circuit, a fully differential architecture was utilized in the implementation. Compared with the conventional Hogge phase detector [17], [18], the proposed phase detector mitigates the dependency on the clock duty cycle variation as illustrated in Fig. 14. The pulsewidth of the signals, up, down1, and down2, can be described as follows:

$$\text{Up} = \frac{T_{\text{DATA}}}{2} + \text{phase error} \tag{5}$$

$$\text{Down1} = \frac{T_{\text{DATA}}}{2} - \text{duty cycle error} \tag{6}$$

$$\text{Down2} = \frac{T_{\text{DATA}}}{2} + \text{duty cycle error} \tag{7}$$

where T_{DATA} is the period of the data. In this case, the duty cycle of Mclk is not required to be 50%. Combined with the charge pump as shown in the Fig. 15, the net current sink into the loop filter can be expressed as

$$I = \text{Up} + \frac{1}{2}[\text{Down1} + \text{Down2}] = \text{phase error}. \tag{8}$$

Equation (8) indicates the net current is directly proportional to the phase error between the data and Mclk regardless of the duty cycle of Mclk. In Fig. 16, the simulated results demonstrate the

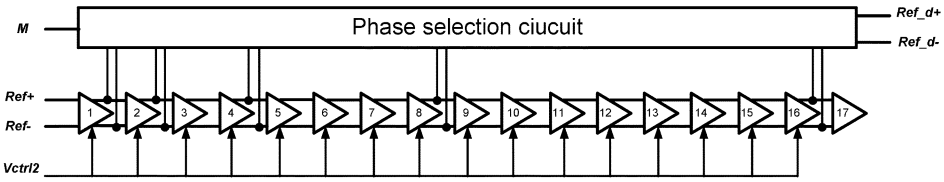

Fig. 17. Schematic of the selective buffer.

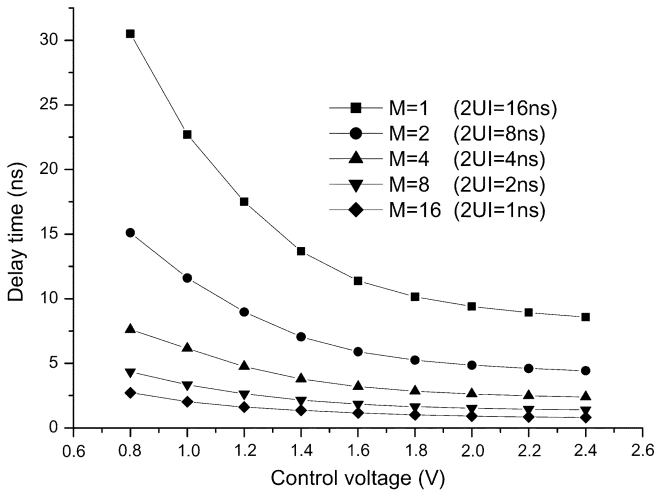

Fig. 18. Simulated transfer curve of the selective buffer.

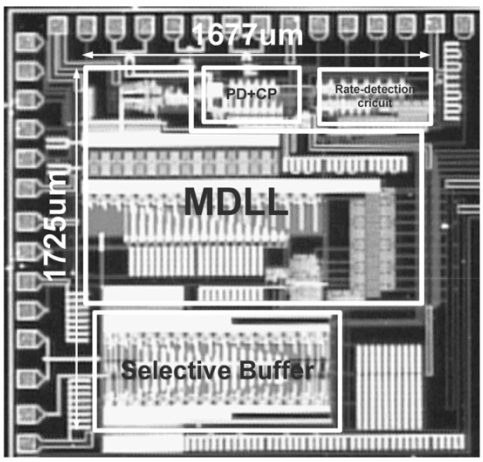

Fig. 19. CDR chip micrograph.

proposed phase detector can sample the data at center of data eye to lower bit error rate (BER) even in cases where the duty cycle of the clock deviates from 50%. The XOR circuit used in this work is similar to [19].

D. Selective Buffer

The selective buffer comprises a phase selection circuit and a 17-stage VCDL as depicted in Fig. 17. The last stage is used as a dummy stage for delay matching. The control voltage, Vctrl2, generated by the charge pump and loop filter in Fig. 2, will vary the delay of the selective buffer to accomplish the phase alignment. The number of delay stages of the selective buffer is inversely proportional to the multiplication factor M. For example, when the multiplication factor is 16, the phase selection circuit will choose the outputs of the first delay stage of the

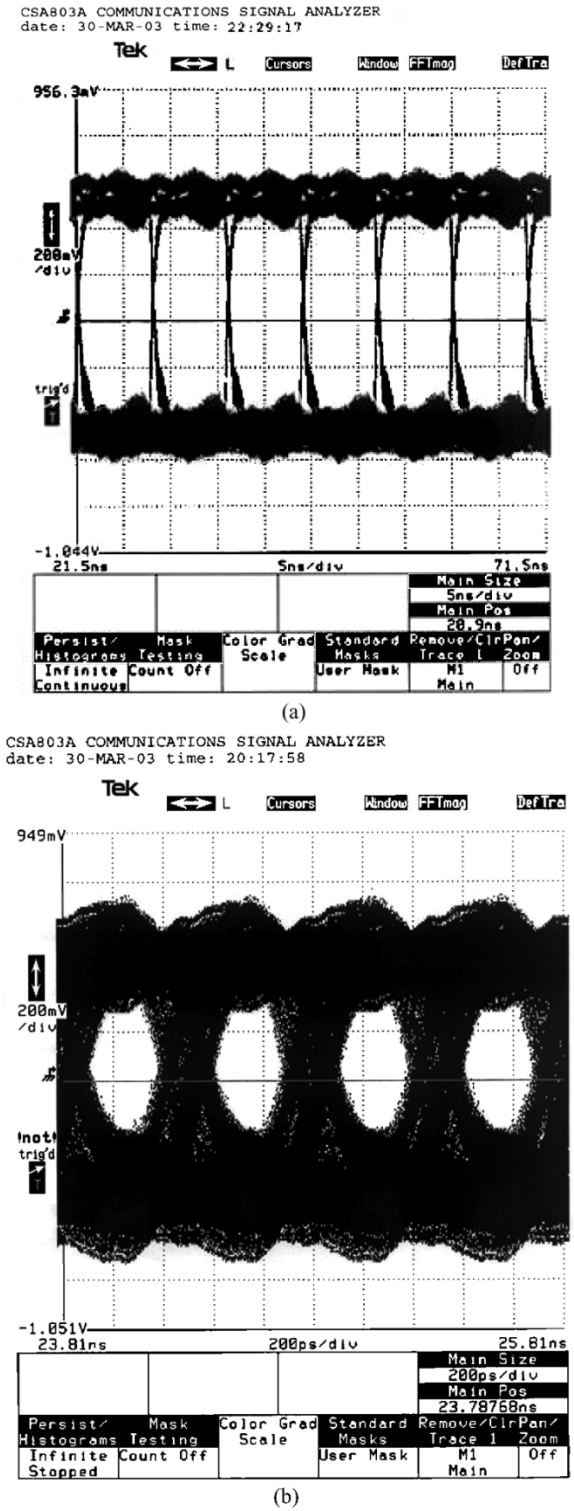

Fig. 20. Data eye diagram for (a) 0.125 Gb/s (b) 2 Gb/s ($2^7 - 1$ PRBS).

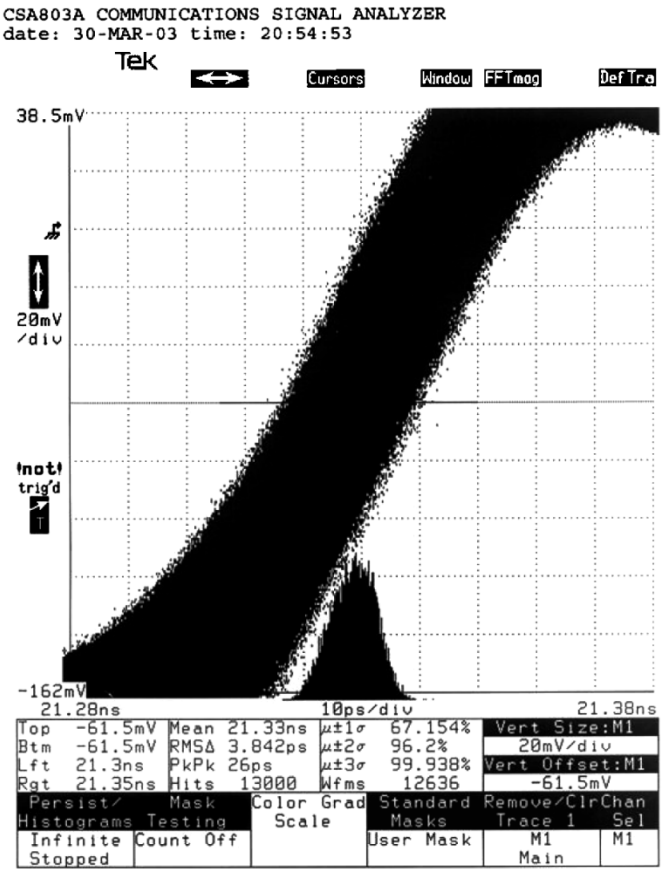

Fig. 21. Jitter histogram for the recovered clock @2 GHz ($2^7 - 1$ PRBS).

VCDL as the outputs, $\mathrm{Ref\_d+}, \mathrm{Ref\_d-}$. The operation mode corresponding to different values of M is summarized in Table I. The gain of this VCDL, K_{VCDL2} (in radians per cycle per volt), can be given by

$$K_{\mathrm{VCDL2}} = \frac{\left(\frac{16}{M}\right)K}{T_{\mathrm{Mclk}}} \times 2\pi = \frac{16K}{MT_{\mathrm{Mclk}}} \times 2\pi = \frac{16K}{T_{\mathrm{Ref}}} \times 2\pi = K_{\mathrm{VCDL1}} \tag{9}$$

where K is the gain of unit delay cell in second per volt. It also reduces the sensitivity to supply noise injection when the multiplication factor is higher. The simulated transfer curve of the selective buffer is shown in Fig. 18. The delay range of the selective buffer could be larger than 2UI (unit interval) for all data rates to provide sufficient phase shift (2π) capability.

IV. Experimental Results

The prototype chip has been fabricated in a 0.25-μm 1P5M CMOS process and occupies an active area of 1.68×1.73 mm^2. Fig. 19 shows the chip micrograph. The loop filters used in two loops are fully integrated in the chip by MIM capacitors. The MSADLL exhibits a lock range from 100 to 125 MHz. When the frequency of the reference clock is 125 MHz, the experimental results show that the CDR can operate with multi data rates, 0.125 Gb/s, 0.25 Gb/s, 0.5 Gb/s, 1 Gb/s, and 2 Gb/s, from a 2.5-V supply voltage. Fig. 20 shows the measured data eye diagrams, where the data is transmitted at 125 Mb/s and 2 Gb/s, respectively, with a pseudorandom bit sequence (PRBS) of 2^7-1. In Fig. 20(b), the peak-to-peak jitter over 200 ps may be caused from the insufficient bandwidth of output buffer. Fig. 21 shows the measured jitter histogram of the recovered clock when the CDR operates at 2 Gb/s. The measured peak-to-peak jitter and rms jitter is 26 and 3.84 ps, respectively. In the BER test for each data rate, no error was detected over 10^{12} data received. The measured CDR's BER is less than 10^{-12}. The total power consumption including I/O circuits is 455 mW when the data rate is 2 Gb/s. However, the core circuit dissipates a power of 245 mW. Fig. 22 shows the measured rms jitter of the recovered clock over different data rates. Over the entire operating frequency range, the maximum rms jitter of the recovered clock is less than 4 ps. Table II gives the performance summary.

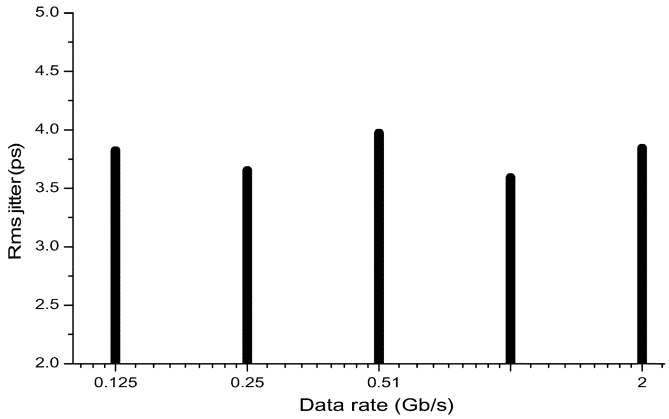

Fig. 22. Measured rms jitter of the recovered clock over different data rates.

TABLE II
Performance Summary of Proposed CDR

Technology	0.25-um 1P5M CMOS
Power supply	2.5V
Active area	1.677mm X 1.725mm
MSADLL lock range	100~125MHz
MSADLL lock time	486ns @ 125MHz (simulated)
Data rate	125Mbps/250Mbps/500Mbps/1Gbps/2Gbps
BER	$<10^{-12}$
Recovered clock	
Peak-to-peak jitter	26ps @2GHz
Rms jitter	3.84ps @2GHz
Power	455mW @2GHz (including I/O circuits)

V. Conclusion

The proposed CDR incorporating with the MSADLL and the selective buffer does not suffer from jitter accumulated problems and so achieves low jitter operation. A duty-cycle-insensitive phase detector can mitigate the dependency on clock duty cycle variations. The proposed CDR utilizes a rate-detection circuit to extend the operation range from 0.125 to 2.0 Gb/s. The measured results demonstrate the functionality of the proposed

CDR. If a more advanced process is used, the performance of the CDR such as the operating frequency range can be improved. The power consumption of the digital part of the CDR and the total chip area can be reduced.

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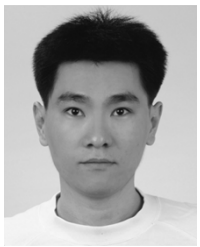

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