Visual Neuroprosthesis: A Non Invasive System for Stimulating the Cortex

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Abstract—This paper describes a complete visual neuroprosthesis wireless system designed to restore useful visual sense to profoundly blind people. This visual neuroprosthesis performs intracortical microstimulation through one or more arrays of microelectrodes implanted into the primary visual cortex. The whole system is composed by a primary unit located outside the body and a secondary unit, implanted inside the body. The primary unit comprises a neuromorphic encoder, a forward transmitter, and a backward receiver. The developed neuromorphic encoder generates the spikes to stimulate the cortex by approximating the spatio-temporal receptive fields characteristic response of ganglion cells. Power and stimuli information are carried to inside the cranium by means of a low-coupling transformer, which establishes a wireless inductive link between the two units. The secondary unit comprises a forward receiver, microelectrode stimulation circuitry and a backward transmitter that is used to monitor the implant. Address event representation is used for communicating spike events. Data is modulated with binary frequency-shift keying and differential binary phase-shift keying in the forward and in the backward directions, respectively. A prototype of the proposed system was developed and tested. Experimental results show that the spikes to stimulate the visual cortex are accurately generated and that the efficiency of the inductive link is relatively high, about 28% in average for 1 cm intercoil distance providing a power of about 50 milliwatts to the secondary implanted unit. Application specific integrated circuits were designed for this secondary unit, showing that, with current technology, it is possible to implement such a unit, respecting the power constraints.

Index Terms—Artificial retina, biomedical implant, cortical stimulation and monitoring, inductive communication link, neuromorphic encoder, smart implant, wireless neuroprosthesis.

I. INTRODUCTION

IN THE LAST FEW years, there has been a huge effort to develop implantable integrated stimulators for bio-medical applications. Most of these stimulators are in the area of muscular stimulation (for instance, for heart or limbs diseases) [1]–[5] and in the area of cortical or nerve stimulations (e.g., for blind/partially blind people or hearing diseases) [6]–[12]. In all these stimulators, information has to be coded in a format somewhat similar to the way stimulation is performed prior to the development of each of the particular diseases. Moreover, with the exception of a few applications (e.g., pacemakers), long time performance of the implanted stimulator implies the power to be furnished by the outside unit. It avoids future operations to replace old batteries, reduces the risk of infections and therefore improves the patient health level. This poses the need for wireless delivery of both power and data [10]–[12].

A lot of research has been performed in the last fifty years for understanding the structure of the mammalian visual system, its main components, and the relationship between electrical stimulation of any part of the visual pathways and the resulting visual sensations. It has been shown that electrical stimulation of individual components of the visual pathway such as the retina, the optic nerve or, directly, the visual cortex, evokes the perception of points of light spatially located, denominated by phosphenes. Based on this nuclear observation, research labs and projects have been dedicated to the study of the human visual system, researching accurate models for the visual system and developing visual prostheses capable of partially restoring vision to blind people.

Microelectronic prostheses which interact with the remaining healthy retina have been developed to restore some vision to those who suffer from eye diseases, such as retinis pigmentosa. This type of prosthesis can use sub-retinal devices [13]—to replace the photoreceptors—or more complex epi-retinal devices [14]—for capturing and processing images which are transmitted to the ganglion cells through an electrode array, but require that output neurons of the eye and the optical nerves are in a healthy state. When this is not the case, these microelectronic prostheses are not useful. The stimulation has to be performed in the primary visual cortex, directly to the neurons in higher visual regions of the brain. This is a challenge, because visual information has to be encoded in a format somewhat similar to the way stimulation was done prior to the development of total blindness. It is expected that neurons will adapt to the stimulus in a way that a blind individual will be able to extract from it information on the physical world [15].

Brindley [16] and Dobelle and Mladejovsky [17] showed that simultaneous stimulation of multiple electrodes allowed blind volunteers to recognize simple patterns. This research however also showed that a cortical prosthesis based on a relatively large number of superficial implanted electrodes requires high currents to produce phosphenes—more than 1 mA—which leads to problems such as epileptic seizures. In this cases, deep intracortical neuro-stimulation should be used, exciting the neurons

at a depth between 1 mm and 2 mm, which corresponds to the cortical layers 4 (namely, $C\alpha$ and $C\beta$), where signals from the lateral geniculate nucleus (LGN) arrive.

This paper presents a cortical visual neuroprosthesis for profoundly blind people which has been developed within the scope of the CORTIVIS project and supported by the European Commission [18], [19]. CORTIVIS started in January 2002 within the scope of the European program *Quality of Life and Management of Living Resources*, and required the work of multi-disciplinary research groups, specialised in areas such as neuro-anatomy, neuro-surgery, signal processing or microelectronics. The project aims at developing prototypes in the field of visual rehabilitation and at demonstrating the feasibility of a cortical neuroprosthesis to interface the visual cortex through intracortical microstimulation, as a means through which a limited but useful visual sense may be restored to profoundly blind people. The designation "profoundly blind" means that the output neurons of the eye, the ganglion cells, often degenerate in many retinal blindnesses and therefore a retinal prosthesis would not be helpful. It is expected that neural plasticity will help to associate phosphenes with the corresponding physical world. In parallel with the CORTIVIS project other labs and projects are performing research with the same objective namely the Meister Lab [20] which is researching models for the visual and auditive systems. The John Moran Labs in Applied Vision and Neural Sciences [21] at the University of Utah is another example of the current effort to develop an intracortical visual neuroprosthesis.

Fig. 1 illustrates the basic components of our Cortical Visual Neuroprosthesis approach. The whole system uses a bioinspired visual processing front-end, the *neuromorphic encoder*, which generates the electrical signals that are transferred to inside the skull through a radio frequency (RF) link, for stimulating an array of penetrating electrodes implanted into the primary visual cortex. Power to operate the stimulating circuitry is also provided from the outside through the RF link. This visual neuroprosthesis is expected to recreate a limited, but useful visual sense in blind individuals, by applying the electrical signals to up to about 1000 microelectrodes provided by several Utah electrode arrays (UEAs). One UEA has 100 microelectrodes, each 1.5 mm long, arranged in a square grid and contained in a package covering an area of approximately 4 mm × 4 mm (see Fig. 2). This UEA has to be priorly inserted into area 17, the primary visual cortex, by using a dedicated system developed to implant the array of microelectrodes in a manner that minimizes dimpling and compression of the subjacent structures. The microelectrode array is inserted to stimulate up to layer 4C, where the LGN axons enter. To the best of our knowledge, this paper is the first one to cover the design and implementation of all the components of an intracortical visual neuroprosthesis. It implements several innovative features, namely at the architecture level of the neuromorphic encoder and on the solutions adopted to convey data and energy through the wireless communication link to the brain.

In what concerns the neuromorphic encoder, the simplest models assume that the neural coding can be reduced to predicting the firing rate as a function of the sensory stimulus. This assumption may be justified in certain brain areas, e.g., deep in the cortex [22]. On the other hand, neurons in the early visual
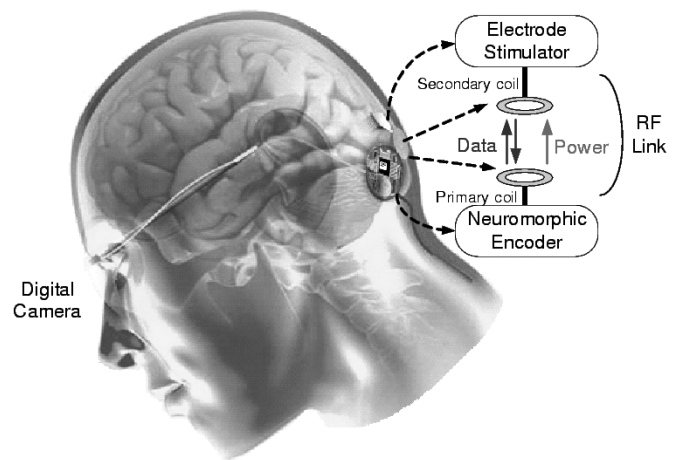

Fig. 1. Cortical visual prosthesis.

system, for example from the retina to the LGN, can deliver reproducible spike trains, whose trial-to-trial variability is clearly lower than the one predicted from the simple firing rate approach [23]. To predict individual spikes, spike patterns with higher timing accuracy and also to account for the stochastic variability of these responses other approaches have to be considered. The first retina model to provide a quantitative output was proposed in [24]. The spatial processing was modeled with a difference of Gaussians (DoG), representing the receptive field's centre and surround areas. After convolving the stimulus with this spatial kernel, the signal is processed by a temporal high-pass filter that outputs the firing rate. Another block is required to convert this firing rate into spike trains. In 2001, a new model was proposed that introduced a nonlinear feedback loop at the output of the temporal filter [25], performing a contrast gain control (CGC). The loop is composed by a temporal low-pass filter followed by a nonlinear function and feedback through a multiplier, introducing a modulation factor in the response. Also in 2001, [22] reported a stochastic model to predict the variability in the number of spikes and on its time of occurrence, introducing a spike generation block instead of using firing rate as output. It uses only temporal processing, but spatial processing can be included considering time-space separability. Stimuli are processed by a temporal filter, based on the spike triggered average—the first Wiener kernel of an expansion series of the ganglion cell response [26]. Variability in spike occurrence is done by adding two noise sources to specific points of the model.

A first experimental work comparing the performance of these models has been recently published by our research group [27]. Based on this study the model with the CGC [25] was adopted in the CORTIVIS project. Particular aspects of the retina organization are considered in this work. For example, retinotopic gradients and magnification factors are configurable parameters of the system, which allow to compensate the fact that sampling across the retina is not uniform [19].

The wireless RF link must provide both power and bidirectional transmission of data between the outside and the implant. While the visual neuroprosthesis requires a few tenths of milliwatts of power, the actual power provided from the outside must
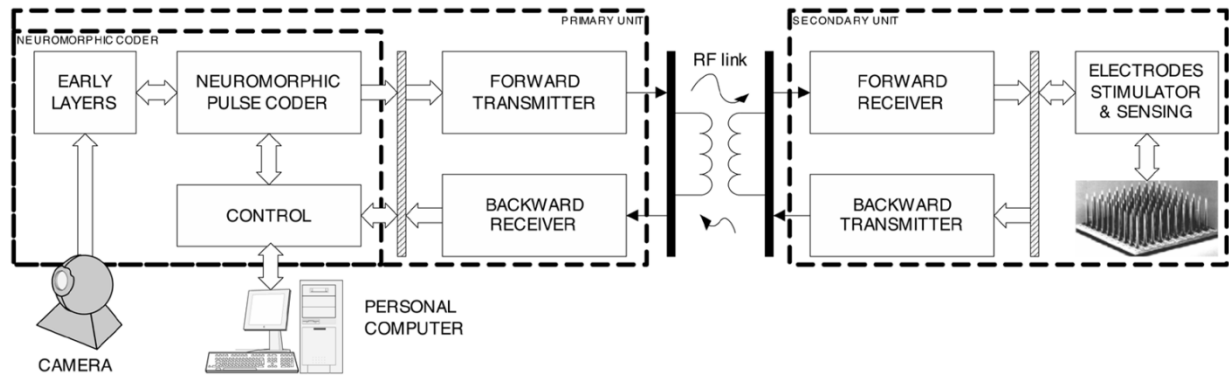
Fig. 2.   Intracortical prosthesis system architecture.

be somewhat higher, in order to account for the coupling losses. The most common solutions proposed in literature for the RF link are amplitude shift keying (ASK) modulation [28]–[33], frequency shift keying (FSK) [28], [34]–[37] and differential binary phase-shift keying (DBPSK) modulation [28], [38]. The ASK signal is usually demodulated in a noncoherent fashion, therefore requiring a very simple receiver. However, the performance of the ASK receiver is highly dependent on the amplitude of the received signal, which is unknown and may vary in time. Therefore, an ASK solution requires high-efficiency gain-monitoring and level-controlling devices. This is not the case with either FSK or DBPSK, which are constant amplitude modulations. Within reasonable limits, the FSK and DBPSK receivers are insensitive to the amplitude of the received signal, making these circuits more robust regarding the high variability of the RF channel. Demodulation of FSK and DBPSK is usually done coherently, thus requiring more complex and power consuming receivers.

The choice of the modulation format has impact on two other important features of the implant receiver, namely the requirement for wireless powering of the implant and the need for recovery of a master clock (from the incoming data signal). Carrier frequency recovery is important because it allows the digital circuitry in the implant to operate with a clock which is frequency-synchronized with the received signal. This avoids intermodulation noise components and contributes to increase the overall system performance. With ASK modulation carrier recovery is somewhat easier since, to allow for noncoherent demodulation, a fraction of the unmodulated carrier has to be sent together with the information signal. With FSK or DBPSK, the transmitted spectrum does not contain a specific carrier signal. Consequentially, carrier recovery is more difficult and requires a narrower phase-locked loop (PLL) or bandpass filter. On the other hand, power extraction is easier from the constant amplitude FSK or DBPSK signals than from the amplitude-varying ASK signal. Another important issue is that power recovery by the circuitry in the secondary system degrades the received signal, changing both its waveform and envelope amplitude therefore introducing a kind of noise dependency on the time varying power consumption of the cortical prosthesis. So, this paper proposes the use of a data modulator type that does not uses amplitude variation. After careful analysis of the different modulation characteristics, FSK was chosen as the modulation

to use in the forward link. For monitoring purposes a reverse data link has also been implemented. It uses DBPSK, which is implemented with a very simple transmitter. DBPSK was not selected for the forward link because the receiver (Costas Loop) is more complex than the FSK receiver.

This paper is organized as follows. In Section II, the main components of the system are specified and an architecture is proposed to fulfil those specifications. Sections III and IV present the neuromorphic encoder and the wireless communication link, respectively. A prototype of the system was implemented for which some experimental results are reported in Section V. Section VI concludes the paper and discusses the future work to continue the development of visual neuroprostheses.

II. System Architecture

The system architecture of the proposed visual neuroprosthesis is represented in Fig. 2. It is physically divided in two units: a primary unit located outside the body and a secondary unit consisting of an implant located inside the body. The units are connected by means of a low-coupling two-coil transformer, which establishes a magnetic RF link between the two devices. The purpose of this RF link is twofold: firstly, it is used to remotely power the secondary unit, a mandatory requirement to avoid the use of batteries; secondly to allow bidirectional data communication between the units. The primary unit interfaces with a miniature digital video camera and with a personal computer used for system configuration, patient visual training and prosthesis performance analysis purposes.

The *neuromorphic encoder* translates the visual signal captured in the miniature digital camera into a sequence of electrical pulses, a spike train, capable of being recognized by the brain. It is composed by two main modules connected in series. The *early layers*, based on models previously proposed in [25], is responsible for processing the visual signal and for its conversion into a spike rate. This rate is then taken as input by the *neuromorphic pulse coding* (NPC) module and translated into the actual spike events by using a simplified version of the integrate-and-fire spiking neuron [39]. The access to the RF link is then arbitrated by the latest module using a first-in first-out (FIFO) buffer to store the events until the link is able to send more spike events. In the visual neuroprosthesis presented in

this paper, the *neuromorphic encoder* is required to process visual images at a rate of 30 frames per second (fps), generating spikes at a rate up to 100 Hz and stimulating a number of microelectrodes equivalent to an array with up to 32×32.

The *forward transmitter* receives the multiplexed spike data from the *NPC* in a synchronous serial bit stream format at a rate of $f_b = 1$ Mbps. This data is modulated using FSK modulation with a centre frequency of $f_c = 10.333$ MHz and a frequency deviation $\Delta f = \pm 333.3$ kHz. To understand this modulation choice we need to digress briefly and characterize the communication channel between the primary and secondary units. While high level noise is not expected (either thermal or originated from magnetic disturbances), it is reasonable to assume that the channel will exhibit a high amount of attenuation and, due to the relative movement/placement between the two transformer coils, severe amplitude fluctuations. With FSK modulation, information is coded in carrier frequency changes, not in amplitude levels (it is a constant-amplitude modulation) and therefore it offers significant robustness regarding to the previous channel impairments. On the secondary unit, power is extracted from the received signal by a power supply generator circuit (considered to be part of the *forward receiver* in Fig. 2) which will be described later in Section IV. Because the integrity of brain tissue does not allow the use of high power stimuli, the secondary unit requires only tenth's of milliwatts of remotely delivered power. The spike data is recovered by the *forward receiver* which consists on an FSK demodulator, bit synchronizer and frame disassembly circuit. The recovered data and clock are then forwarded to the microelectrodes stimulator circuit.

To accomplish implant monitoring (e.g., electrode impedance measurement and calibration) a reverse data link has been developed. In the secondary unit, maintenance data is modulated and transmitted using DBPSK at a data rate of $f_b = 156.25$ kbps using low amplitude (≈ 1 V) and a carrier frequency $f_c = 5$ MHz. This modulation was chosen because the transmitter is simple and consumes very low power. Being also a constant-amplitude modulation, it exhibits the same robustness of FSK with respect to the channel adversities. In addition, for the same average bit error rate, it offers a signal-to-noise-ratio (SNR) gain of 3 dB. The disadvantage of DBPSK is that it requires a relatively complex, power-hungry receiver (significantly more complex than its FSK counterpart) and this is why DBSPK was not the chosen modulation for the forward link (note that the forward receiver is located in the remotely-powered secondary unit). In the case of the backward receiver, located on the primary unit, complexity (or, for that matter, power consumption) is not an issue and the previously mentioned advantages of DBPSK may be exploited.

The main objective of the *electrode stimulators and sensing* module is to stimulate the primary visual cortex and to measure the connectivity between the electrodes and cortex. Extensive experiments have shown that in order to safely induce phosphenes a current of 20 μA is required. However, it expected for small variations in this value to be required from microelectrode to microelectrode and patient to patient. The actual current value should therefore be set during the training phase. Electrode sensing is achieved by injecting a fixed current value to a microelectrode and then measuring the induced current value.

This allows for measuring the connectivity between the microelectrode and the visual cortex cells.

The *electrode stimulators and sensing* module is composed of a set of digital-to-analog converters (DACs), which are used to stimulate up to 32×32 microelectrodes in the visual cortex with the spike events received from the *neuromorphic encoder*. Each DAC has a current-steering type architecture, using scaled currents added at an output node, in order to ensure the desired linear digital-to-analog conversion. The main difference with respect to the common current-steering DAC is that it allows for the removal of the charge from the brain: it can inject current (positive sign) or remove current (negative sign) from the electrode. The DAC reference current is around 20 μA and the overall power consumption for stimulating and sensing the 1024 electrodes is expected to be 50 mW. The amplitude and duration of the stimulus is pre-recorded in dedicated registers on the *electrodes stimulator and sensing* module, which can be accessed by means of the RF link for both reading and writing.

The overall system is presently under development in VLSI technology. The *electrode stimulator and sending* block is to be implemented in a modular way in *Austriamicrosystems* (AMS) CMOS 0.35-μm technology: each module (except for the power supply generator) drives a 100 microelectrode array, which will be attached directly to the VLSI chip (flip chip technology). The Forward and backward emitters and receivers are also being developed using AMS CMOS 0.35-μm technology. Moreover, in order to evaluate the circuit requirements when implementing the in deep sub-micron technology, the *neuromorphic encoder* is now being synthesised using the UMC 0.13-μm CMOS technology process [40]. The UMC L130E SG-HS 1P8M process is a single poly, 8 metal layer with an operating voltage of 1.2 V.

However, to rapidly prove the concepts involved in the RF link, by using conventional integrated circuits and discrete components, a scaled frequency prototype operating 10 times slower was built: the forward data rate is 100 kbps with a carrier frequency of 1 MHz; the backward data rate is 15.625 kbps with carrier frequency of 500 kHz. Also, a neuromorphic encoder was developed using field-programmable gate array (FPGA) technology.

The visual neuroprothesis system was planed to support the driving of 1024 electrodes. However, the stimulator chip that is being developed will be flipped directly over the back of one microelectrodes array (UEA with 100 microelectrodes). This solution will solve the electrode wiring problem. Each one of the 100 ADC converters are being designed around each pad implanted in a matrix form like the UEA. Each module will be packed in a ceramic hermetic package. The set flip chip/UEA will be placed over a thin film printed circuit over the package base besides the power supply recovering circuitry. Secondary coil may be inside the ceramic package or in a separated place under the skin.

III. NEUROMORPHIC ENCODER

The *neuromorphic encoder* herein presented and shown in Fig. 3, is an approximation of the spatio-temporal receptive fields characteristic response of the retina ganglion cells. The encoder is composed of two main blocks: the *early layers*
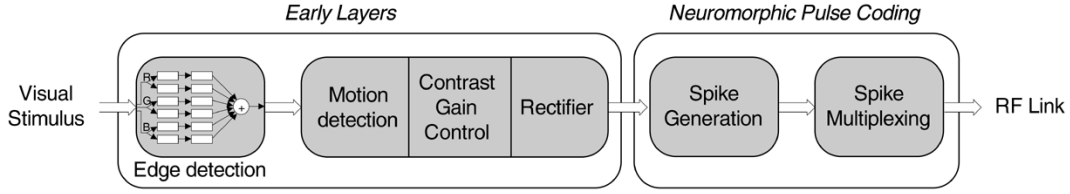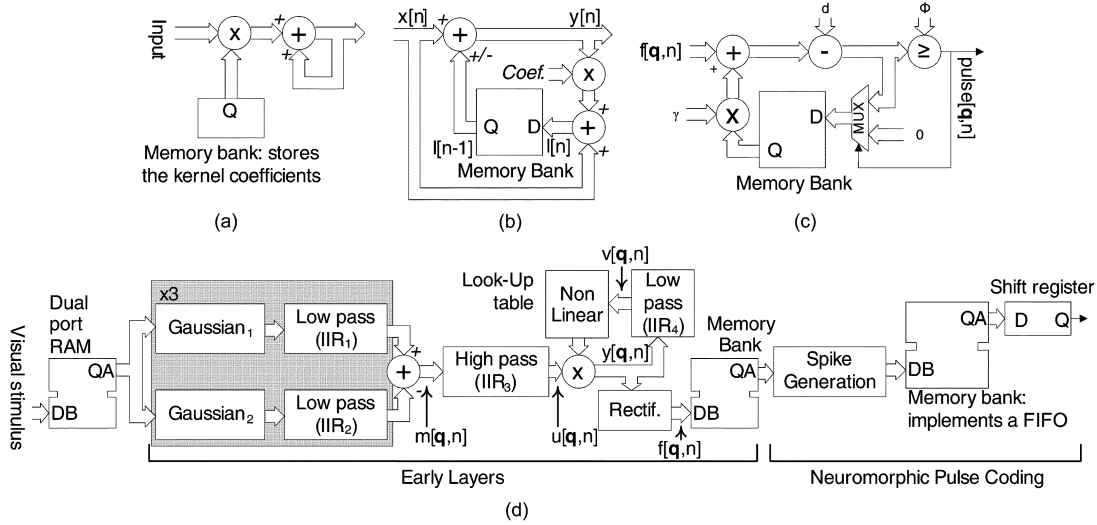
Fig. 3. Neuromorphic encoder.

Fig. 4. Detailed diagram of the visual encoder computational architecture. (a) Gaussian filter block. (b) Infinite impulse response filter. (c) Spike generation block. (d) Global architecture.

block, that performs both spatial and temporal processing of the visual signal; the *neuromorphic pulse coder* block, responsible for the conversion of the visual information to a sequence of pulses capable of being interpreted by the brain. It uses the address event representation (AER) [41] protocol to communicate information without timestamps to the microelectrode stimulator placed inside the human brain. The architecture of the system has been designed taking into account the specifications of the problem, namely the requirement of low power real-time processing of visual stimuli and stimulation of up to 1024 microelectrodes. To this end, the *neuromorphic encoder* translates a visual stimulus $\mathbf{s}(\mathbf{r}, t)$ described by the intensity of each of the three basic color components - red, green and blue - as a function of space $\mathbf{r} = [x\ y]^T$ and time t

$$\mathbf{s}(\mathbf{r}, t) = [s_R(\mathbf{r}, t) s_G(\mathbf{r}, t) s_B(\mathbf{r}, t)] \tag{1}$$

into a sequence of pulses. The encoder was designed to allow a blind individual to recognize patterns of 32×32 points.

A. Early Layers

The *early layers* block, responsible for spatio-temporal filtering, is based on research published in [25] and extended to the chromatic domain by considering independent filters for each basic color component. The first filtering element of the *early*

layers is an edge detector composed by a set of two Gaussian spatial filters per color channel [see Fig. 4(d)[1]]

$$g_{ij} = \frac{a_{ij}}{2\pi\sigma_{ij}^2} e^{-\frac{\|\mathbf{r}\|^2}{2\sigma_{ij}^2}}. \tag{2}$$

The Gaussian filters are parameterized by a gain a_{ij} and a standard deviation σ_{ij}, where i represents the color channel and j the number of the filter in the set.

In order to perform edge detection, Gaussian filters within the same color component are parameterised with opposite signs, $a_{i1} = -a_{i2}$, and different standard deviations, $\sigma_{i1} \neq \sigma_{i2}$. The output is then processed by a set of temporal first-order low-pass filters with impulse response

$$h_{ij}(t) = H(t) \cdot \beta_{ij} \cdot e^{-\beta_{ij} \cdot t} \tag{3}$$

where $H(\cdot)$ represents the Heaviside step function and β_{ij} the decay rate. The output of the edge detection module will then be as in (4), where $*$ represents the convolution operation

$$m(\mathbf{r}, t) = \sum_{i=R,G,B} \left(s_i(\mathbf{r}, t) * \sum_{j=1}^{2} (g_{ij}(\mathbf{r}) \cdot h_{ij}(t)) \right). \tag{4}$$

The $m(\mathbf{r}, t)$ signal is then convolved with the impulse response of a first-order high-pass filter with the pole at $-\alpha$ rad/s as expressed in (5), to perform motion detection

$$h_{\mathrm{HP}}(t) = \delta(t) - \alpha \cdot H(t) \cdot e^{-\alpha \cdot t}. \tag{5}$$

[1]In this figure, signals are represented in the discrete time domain where, $s[\mathbf{q}, n]$ corresponds to $s(\mathbf{r}, t)$ in the continuous-time domain.

The resulting activation function $u(\mathbf{r}, t) = m(\mathbf{r}, t) * h_{\text{HP}}(\mathbf{r}, t)$ is then modulated by the contrast gain controller (CGC) which models the strong modulatory effect exerted by stimulus contrast. The CGC nonlinear approach is also used in order to model the motion anticipation effect observed on experiments with a continuous moving bar [24]. The CGC loop works as follows. First, the CGC output $y(\mathbf{r}, t)$ is convolved with the impulse response of a low-pass temporal filter with a pole at $-\gamma$ rad/s

$$h_{LP}(t) = H(t) \cdot \gamma \cdot e^{-\gamma \cdot t}. \tag{6}$$

The resulting signal, $v(\mathbf{r}, t) = y(\mathbf{r}, t) * h_{LP}(\mathbf{r}, t)$, is then processed by a nonlinear function

$$k(v(\mathbf{r}, t)) = \frac{1}{1 + [v(\mathbf{r}, t) \cdot H(v(\mathbf{r}, t))]^4} \tag{7}$$

before being applied to modulate the amplitude of the CGC input signal as expressed in (8)

$$y(\mathbf{r}, t) = k(v(\mathbf{r}, t)) \cdot u(\mathbf{r}, t). \tag{8}$$

Finally, the last processing step of the early layers block is a rectifier operation represented in (9) which yields the firing rate f of the ganglion cells' response to the input stimuli, where Ψ and θ define the scale and baseline values of the firing rate

$$f(\mathbf{r}, t) = \Psi \cdot H(y(\mathbf{r}, t) + \theta) \cdot [y(\mathbf{r}, t) + \theta]. \tag{9}$$

Two main restrictions were taken into consideration when designing the circuits to implement the *early layers*: low power consumption and reduced circuit area. In order to comply with these restrictions, folding techniques were applied to the architecture originally obtained from the signal flow graph (SFG) [42]. The complete *early layers* circuit was folded 1024 times and the firing rate for each microelectrode is computed in series. Moreover, assuming a Gaussian kernel of 7×7, edge detecting takes a total of 98 multiplications and 98 additions. This requires the folding technique to be applied to the Gaussian filters by a factor equal to the kernel size. It allows to save computational units since only one multiply-and-accumulate (MAC) unit is needed to compute each Gaussian filter [see Fig. 4(a)].

In order to implement the temporal filters presented in (3), (5) and (6), the bilinear approximation was used, resulting in infinite impulse response (IIR) digital filters of the form

$$y[n] = b \cdot y[n-1] + c \cdot (x[n] + d \cdot x[n-1]) \tag{10}$$

where $b > 0$ and $c > 0$ represent the temporal filter coefficients, $d = 1$ for the low-pass filters in (3) and (6) and $d = -1$ for the high-pass filter in (5). Also, to reduce the amount of memory needed, the temporal filters were implemented in a transposed form where the output is calculated by adding the input $x[n]$ to a stored value $l[n]$ which is computed in the previous cycle as

$$y[n] = l[n-1] + c \cdot x[n] \tag{11a}$$
$$l[n] = b \cdot y[n] + c \cdot d \cdot x[n]. \tag{11b}$$

Fig. 4(b) shows the implementation diagram of the temporal filters. The input scaling c in (10), existent in temporal filters (3), (5) and (6), was moved and applied simultaneously with

the calculation of the Gaussian filters and with the nonlinear function, for (3) and for (5) and (6), respectively. The remaining modules, the nonlinear function presented in (7) and the rectifier shown in (9) were implemented by means of a look-up table and a comparator, respectively.

B. Neuromorphic Pulse Coding

The NPC block performs two operations. Firstly, it converts the continuous time-varying representation of the signal produced in the *early layers* of the retina into a neural pulse representation: in this representation, the signal provides information only when a new pulse begins. This block then stores the information about spike events and sends them to the implant at the maximum rate allowed by the channel. The second operation corresponds to arbitrate the access of the generated spikes to the serial bus which is located at the input of the *forward emitter* (see Fig. 3).

The model adopted for the spike generation is a simplified version of an integrate-and-fire spiking neuron [39]. The neuron accumulates input values from the respective receptive field (output firing rate determined by the *early layers*) until it reaches a threshold ϕ. Then it fires a pulse and discharges the accumulated value. A leakage term is included to force the accumulated value to diminish for low or null input values. The pulses are then generated accordingly to

$$P_{\text{acc}}[\mathbf{q}, n] = F[\mathbf{q}, n] + \gamma \cdot P_{\text{acc}}[\mathbf{q}, n-1]$$
$$- \text{pulse}[\mathbf{q}, n-1] - d \tag{12a}$$
$$\text{pulse}[\mathbf{q}, n] = H(P_{\text{acc}}[\mathbf{q}, n] - \phi) \tag{12b}$$

where P_{acc} is the accumulated value, γ sets the decay rate of $P(\text{decay} = 1 - \gamma)$, and $H(\cdot)$ represents the Heaviside step function. The implementation of the pulse generation circuit is shown in Fig. 4(c). It works in a two stage pipeline: in the first stage the input firing rate $F[\mathbf{q}, n]$ is added to the accumulated value; in the second stage, the leakage value is subtracted and, if the result is bigger than the threshold ϕ, a pulse is fired and the accumulator returns to zero. This block is connected to the *early layers* by means of a dual port memory bank. This allows for the *early layers* block to write data onto one port while the *NPC* block reads data from the other port. The *spike multiplexing* block uses a FIFO buffer to arbitrate the access of the spikes generated in the *spike generating* block to the RF link, as shown in Fig. 4(d). When a spike is generated it is stored in the buffer until the channel becomes available. The buffer allows the system to respond well to short periods in which the spike rate is high.

C. Model Evaluation

To evaluate the performance of this model, a study was made by one of the authors based on real experimental data from salamander retinal responses [27]. This study compared the performance of the presented model to the one of a recently published stochastic model which attempts to predict the temporal occurrence of spikes and spike patterns [22]. Model performance was
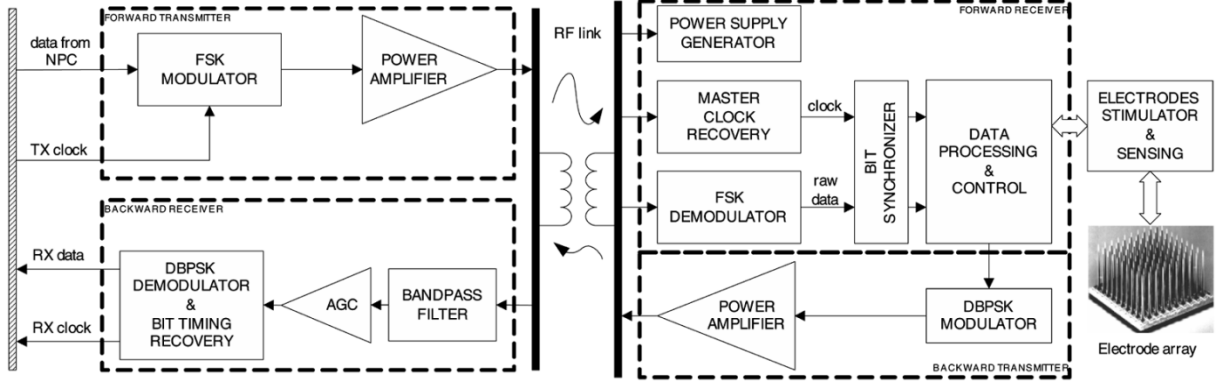
Fig. 5.   RF link circuitry diagram.

assessed based on the mean-squared error (MSE) of the firing rate. This measure is defined by [23]

$$\mathrm{MSE} = \frac{\int (f(t) - r(t))^2 dt}{\int (f(t) - \bar{r})^2 dt} \qquad (13)$$

where $f(t)$ is the firing rate produced by the model, and $r(t)$ is the firing rate obtained from the peristimulus time histogram (PSTH). This rate is calculated from the observed real data by histogramming the spike times occurrence from all experimental trials, and dividing its amplitude by the width of the time bin and by the total trials number. Formally, for a spike train described by $\rho(t)$, the firing rate in the time interval $[t_1; t_2]$ averaged amongst M trials, is given by (14).

$$r(t) = \frac{1}{M} \frac{\int_{t_1}^{t_2} \rho(t) dt}{t_2 - t_1} \qquad (14)$$

The MSE for the firing rate of the presented model is about 1.11, while for the stochastic model is 1.13 [27]. These results show that by using a deterministic model, it is possible to approximate the real neural retina response with an accuracy similar to that of the stochastic model. However, deterministic models require lower computational power, thus making them a more suitable approach for developing a visual neuroprosthesis.

D. Operating Considerations

Experiments using transcranial magnetic stimulation [43] have shown that the patterns to evoke phosphenes differ from person to person. Exciting the visual cortex by means of a microelectrode array should also require an adaptation of both the stimulation patterns and the spike amplitude and length. Thus, some level of programming is required at the encoder level. An interface with a personal computer allows changing the value of each register storing the parameters of the *neuromorphic encoder* model. It is also possible to configure the amplitude and duration of spikes at each microelectrode by sending a configuration command to the *electrode stimulator* located on the secondary unit (the detailed communication protocol in presented in Subsection IV-D).

Another operating consideration for the *neuromorphic encoder* comprises the mapping of the spike trains to the microelectrodes, which can only be made by reviewing maps after implanting the visual neuroprosthesis, during the training phase.

In this sense, full re-configuration is achieved by changing the parameters of a look-up table. Again, this configuration is made through the interface with the Personal Computer shown in Fig. 2.

IV. WIRELESS COMMUNICATION LINK

The RF link block diagram is shown in Fig. 5. The RF link circuitry can be divided into three parts: the primary RF unit (located outside the body), the secondary RF unit (located inside the body, but not necessarily inside the head) and the transformer which establishes inductive coupling between the two units (one coil in the primary unit and another in the secondary unit). This wireless communication channel implements the bidirectional RF link: 1) the forward link (the main link: data bit rate is up to 1 Mbps), in which a power/data signal is transmitted using FSK modulation with a 10 MHz frequency carrier; 2) the backward link (the secondary link: data bit rate is up to 156.25 kbps, which suffices for maintenance and initial configuration purposes) in which data is transmitted in the reverse direction using DBPSK modulation with a 5 MHz frequency carrier. To implement a very compact low-power wireless communication link, some integrated circuits were initially designed using AMS CMOS 0.8-μm technology but the new circuits, that are in development phase, use AMS CMOS 0.35-μm technology.

A. Primary RF Unit

The primary RF unit is shown in Fig. 5. The transmitter (forward link) is represented in Fig. 6 and includes a FSK modulator and a signal amplifier. FSK was chosen for its robustness to amplitude distortions [44]. The FSK modulator is implemented by means of a counter, driven by an oscillator f_{CLK}. According to the transmitted data bits, 0 or 1, the counter divides the clock signal by 16 or 15, respectively. In this way, data is modulated at $(f_{\mathrm{CLK}})/(16)$ and at $(f_{\mathrm{CLK}})/(15)$ frequencies. This signal feeds a Class-E switching-mode tuned power amplifier. The Class-E switching-mode tuned power amplifier configuration was chosen to optimize the efficiency at the transmitter [45]–[47].

The primary RF unit receiver (backward link) is a Costas-Loop [28] coherent demodulator placed after a sixth-order bandpass filter and an automatic gain control (AGC) unit.
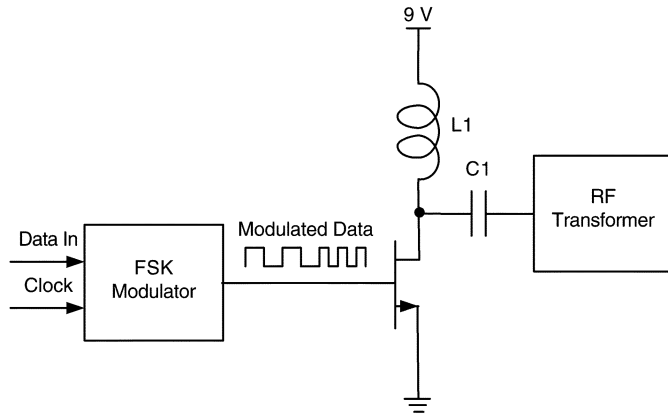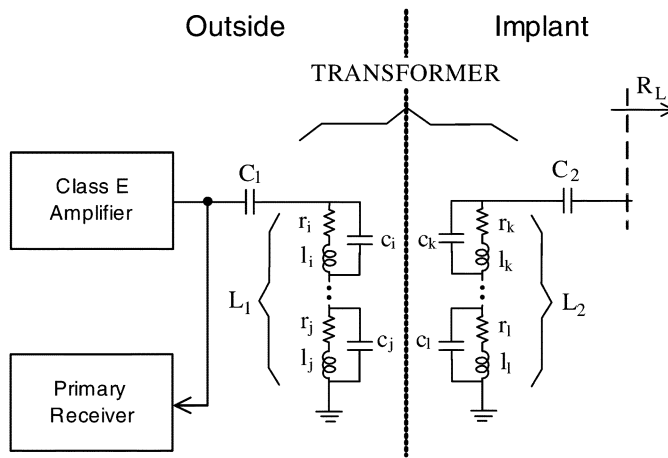
Fig. 6.   Primary RF unit transmitter.

Fig. 7.   Coupling transformer with distributed parameter model.

B. Transformer

The transformer is of major importance in the RF link since it has a strong influence on the overall performance of the secondary system. It has to be designed to allow proper system operation regardless of the intercoil distance (within reasonable limits, say 1 to 2 cm). The coupling transformer is represented in Fig. 7. It should be noticed that at the desired operation frequencies the real transformer exhibits a distributed parameter behavior (the distributed elements are represented in Fig. 7). Due to the coil separation, there is an high magnetic flux dispersion (not connected with the secondary coil), the coupling is weak and, as a consequence, a significant amount of energy is lost. To maximize the efficiency, an appropriate design of the coils is important. In order to compensate the equivalent inductances relative to the primary and secondary magnetic fluxes dispersions, capacitors (C1, C2) are placed in series with the corresponding coil, resonating at the 10-MHz carrier frequency. This originates a double tuned bandpass filter behavior for the RF transformer. Both circular coils have inside a cylindrical powerful neodymium magnet used for coil self-attracting and fixing purposes.

Experiments concerning the transformer confirmed the theoretical results with the single exception of the bandwidth centre frequency. This is explained by the fact that the transformer equivalent model used in the literature assumes a high magnetic
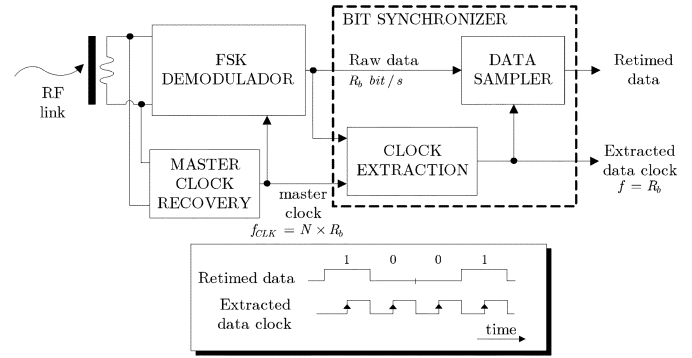

Fig. 8.   Data clock recovery and bit synchronizer.

coupling factor (parameter $k \approx 1$) and it does not take into account neither the distributed capacitance nor the skin effect. This assumption does not hold in this application because the absence of an iron core makes it impossible to have a strong magnetic coupling: the measured coupling factor was 0.3 for an intercoil distance of 1 cm using carefully designed planar coils of Litz wire with about 3 cm of diameter.

C. Secondary RF Unit

The secondary RF unit architecture is depicted in Fig. 5. The power-supply generator is comprised of a half-wave rectifier, protection circuits and a series regulator; it is able to recover the required power (stabilizing at 5 or 3.3 V dc) from the received signal with 28% power efficiency at an intercoil distance of 1 cm. The binary *FSK demodulator* is built around a PLL circuit and a comparator, and provides a stream of non-return-to-zero (NRZ) data at a bit rate of 1 Mbps. This bit stream is fed to the *bit synchronizer*, which provides a synchronized clock and retimed data to the data processing unit. The latest performs bit and frame synchronization and frame disassembly. Formatted data is then forwarded to the *electrode stimulator and sensing* block. The master clock recovery task is accomplished in the *master clock recovery* block (see Fig. 5) by means of a narrow-band PLL designed to produce a reference 10-MHz clock from the received signal.

The signal received from the primary system is used to extract the system master clock, with frequency $f_{\mathrm{CLK}} = (1)/(T_{\mathrm{CLK}}) = N \times R_b$ where $R_b = (1)/(T_b) = 10$ Mbit/s is the raw bit-rate and $N = 10$ (corresponding to a RF carrier frequency of 1 MHz). The following point is worth noting: since the master clock is derived from the transmitted signal, it follows that the data stream is frequency synchronized (i.e., frequency-locked) with the master clock; a data clock could therefore be obtained by suitable division (by a factor N) of f_{CLK}. This is because there is no frequency offset between transmitter and receiver in this system. However, the (lead or lag) *phase difference* between the positive-going clock transitions and the optimum time epoch for sampling the data, which is the central point in the time frame of each bit, is unknown and varies significantly. In fact, even small disturbances in the relative position of both coils lead to important phase offsets which have to be properly estimated and compensated by the bit synchronizer. The task performed by the bit synchronizer is thus of fundamental importance to establish a proper time
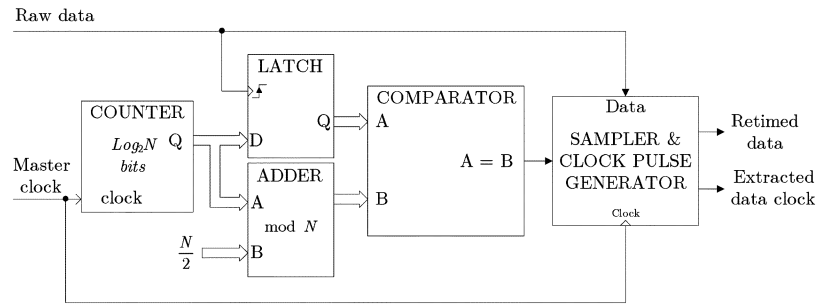
Fig. 9. Block diagram of the new feedforward bit synchronizer.

reference in the receiver. The positive-going transitions in this reference clock should accurately signal the optimum instants to sample and detect the received data bits. The part of the receiver interacting with the bit synchronizer is shown in Fig. 8.

As can be seen in Fig. 8, the new bit synchronizer has a feedforward structure; this important feature avoids the annoying loop behavior known as hang-up, typical in feedback synchronizer operation, which manifests itself has an unacceptably long synchronizer acquisition period, compromising receiver operation. The operation of the *bit synchronizer* is explained next. Suppose that we have a binary counter being driven with the master clock frequency f_{CLK}; then, it will advance N states within each bit period. If, at time t_0, the counter is in state i then, at time $t_0 + (T_b)/(2)$, it will have advanced $(T_b)/(2 \times T_{\mathrm{CLK}}) = (f_{\mathrm{CLK}})/(2 \cdot R_b) = (N)/(2)$ and be in state $i + (N)/(2)$ (on average); this is the time epoch at which the recovered clock should have a positive transition, marking the middle of the data bit. This reasoning justifies the block diagram represented in Fig. 9: the positive-going transition on the raw, unsynchronized data signal latches the counter state i, at reference time t_0, and marks the start of a bit. When the counter reaches the state $S = i + (N)/(2)$, then $(S + (N)/(2)) \mathrm{mod} N = (i + N) \mathrm{mod} N = i$ and the comparator will signal this event to the final processing block, which in turn samples the raw data and produces a clock pulse synchronized with the master clock.

Note that after a positive-going transition of the raw data, the synchronizer operates in a free-running fashion. The phase offset which eventually accumulates after this event is corrected when the next positive-going transition occurs. Thus, the raw data should not have long sequences of equal bits. This is guaranteed by the use of self-synchronising scrambler an descrambler circuits.

In summary, this new bit synchronizer has the following desirable properties: 1) due to the absence of frequency offset between transmitter and receiver the recovered clock is *jitter-free* (no dynamic phase error); 2) it has a feedforward structure that avoids the *hang-up* disabling phenomenon; and finally, 3) it is easily implemented with very simple digital logic.

A reverse link used for monitoring tasks, electrode calibration and voltage measurement is established from the secondary to the primary system at a lower data rate of 156.25 kbps, using DBPSK modulation. The DBPSK modulation format was chosen because the transmitter is very simple and requires very low power. Operation of this reverse link is in half-duplex mode i.e., while data is being sent on this link to the primary system, no useful data is transmitted in the forward link. However,

to keep the secondary system conveniently powered, the primary system continually transmits an unmodulated carrier (at 10 MHz). In the primary system, the DBPSK data is recovered by means of a Costas-Loop demodulator [28] which performs satisfactorily with intercoil distances up to 2 cm.

D. Communication Protocol

Both forward and backward communication links use the same data protocol, developed specifically for this system. The data packet structure is represented in Fig. 10(a). To transmit a set of up to 8 data values, it uses a synchronization header composed by a sequence of twelve 1's and a 3-bit type field indicating the current operation mode. Three operation modes are specified for the forward transmission. In the normal mode the RF link is being used to transmit spike information to the *electrodes stimulator and sensing* (see Fig. 2), and each data field contains the address of the electrode to be stimulated. The other operation modes are used to read/write the internal registers, for controlling the amplitude and duration of the electrical pulses. The write operation mode is accomplished by sending two pairs of data: the address of the register being configured plus the new value. The read operation is intended to measure the impedance of the microelectrodes (through the developed voltage and known drive current), in order to evaluate the microelectrode-cortex interface. It works in a two stage transmission. In the first stage, a forward transmission sends a request to the microelectrode controller for the voltage measurement of up to 8 microelectrodes (again the data fields are used as the address of the microelectrode). In the second stage, a backward transmission sends to the control module in the primary unit (see Fig. 2) the voltage information of the requested microelectrodes in the data fields. In order to increase the efficiency of the operation, the address of the microelectrodes is not repeated in the backward transmission. Instead, the measured voltage of each of the requested electrodes is sent in the exact same data field as the address was sent. Optionally, the system allows the reading of the configuration of the internal registers with the read operation mode. The verification of which data fields are valid is made by a valid bit [marked with V in Fig. 10(a)], preceding each data field. Also, in order to avoid the repetition of the synchronization header within the transmitted packages, trailing zeros are sent at the end of each packet field: header, type and data.

Four blocks were developed for implementing the described protocol: a transmitter and a receiver for both primary and secondary units. The transmitters, or data packagers, are built
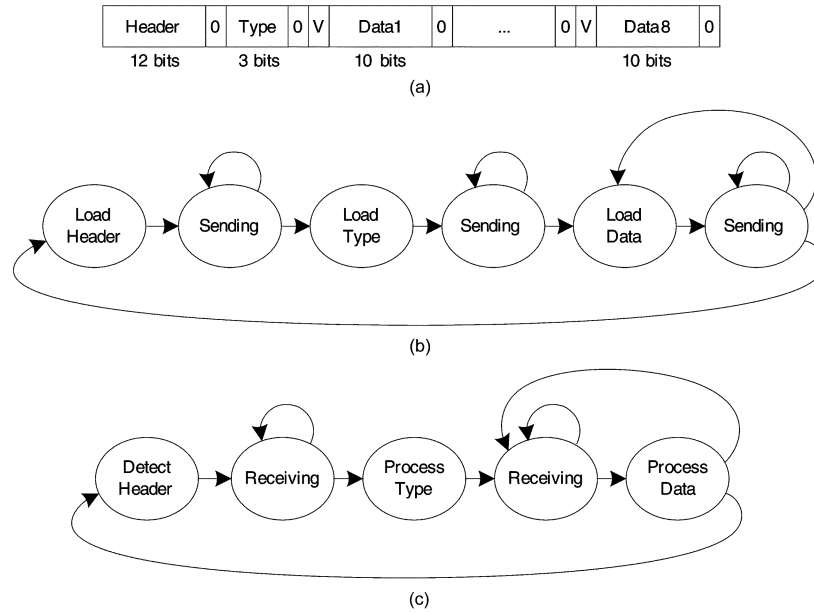
Fig. 10.   Communication protocol. (a) Structure of the transmitted packets. (b) Data packager for the transmitters. (c) Data unpackager for the receivers.

around a 13-bit shift register with parallel load and serial output. The output is sent to the RF link through a scrambler controlled by the state machine presented in Fig. 10(b). The state machine works as follows. In the *load* states, the shift-register is loaded with the `Header/Type/Data` values followed by a trailing zero. Afterwards, during the *sending* states, the loaded values and trailing zeros are transmitted. On the other side, data unpackagers for the receivers were designed. These are built around 12 bit shift registers with serial input (the bits received from the RF link, after passing by the unscrambler) and parallel output. The control of this circuit is made by a state machine as shown in Fig. 10(c). The state machine is started on *detect header* where it remains until the 12-bit header is found. Afterwards the packet information, `type` and `data`, are read in the states *process type* and *process data*, respectively. These states are preceded by *receiving* states which last while the next package field is being loaded into the shift register. After the whole package is read, a new cycle begins with the state machine returning to *detect header*.

V. EXPERIMENTAL RESULTS AND SYSTEM PROTOTYPE

In order to perform the experimental evaluation of the *neuromorphic encoder*, a system prototype was developed [48]. The processing core is based on a XILINX SPARTAN XC3S400 FPGA [49] with 400 k system gates, a total memory of 288 kbits distributed in 16 RAM blocks, 16 bit multipliers and fast carry look-ahead logic. The prototype was developed on a 4-layer printed circuit board (PCB), where the two inner layers are dedicated to the power circuit while the two outer layers are used for signal routing (see Fig. 11). This structure decreases the coupling noise between signals, therefore improving the overall performance of the prototype. The system also includes three I/O ports: 1) an I/O interface to connect to a digital camera for capturing the images to be processed by the FPGA; 2) a 40-pin digital interface to the RF link; and 3) a standard video graphics
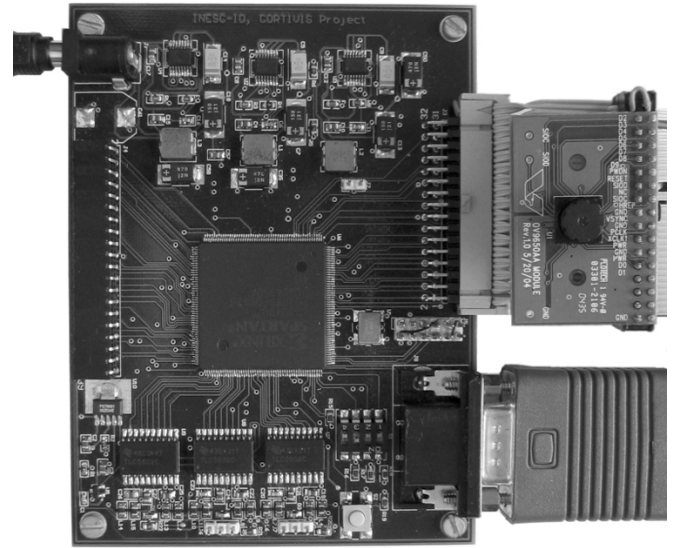

Fig. 11.   *Neuromorphic encoder* prototype.

array (VGA) output used for visualizing both input and processed images. For image capture a miniature digital camera sensor [50] is used. This sensor is capable of providing a color image with a resolution up to XVGA (1280×1024) at a frame rate of 15 fps consuming 50 mW of power. The operation of the camera and the resolution of the acquired images can be configured through the sensor internal registers, which are accessed by using the serial camera control bus (SCCB) [51] protocol.

Besides the *neuromorphic encoder*, the prototype processing core includes four other modules (Fig. 12). The *register configuration* module is used to program camera operation in order to acquire frames in YUV QVGA format at 30 fps. The *image capture and resize* module deals with the synchronization with the image sensor and with resizing the input image to a size of 32×32 pixels. This module takes the 128×128 pixels centre part of the input image and, after applying a low-pass filter based
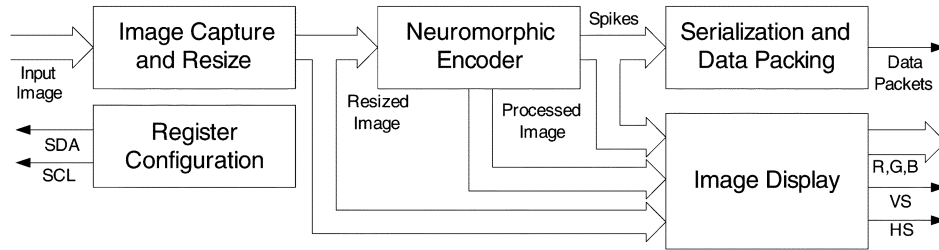
Fig. 12. Diagram of the blocks implemented in the processing core.

TABLE I
RESOURCE OCCUPANCY ON PROCESSING CORE

Modules	Slice Occupation		RAM blocks	Mult.
Total available resources	3584	100%	16	16
Image Capture and Resize	108	3%	0	2
Register Configuration	142	4%	0	0
Classic Model	420	12%	5	3
Serialization and Data Packing	60	2%	2	0
Image Display	218	6%	8	9
Complete System	948	26%	15	12

on a Gaussian kernel in the horizontal dimension, decimates the image to a size of 32×32 pixels. The *image display* module implements a standard VGA graphic interface to display any of the input or processed images on a standard monitor. It allows for the verification of the correct operation of the *neuromorphic encoder*. Finally, the *serialization and data packing* module corresponds to the forward transmitter data packager, as described in Section IV-D.

The circuits were described in VHDL and, by using the XILINX WEBPACK 6.2 tool, synthesized and mapped to the chosen XILINX SPARTAN XC3S400 FPGA. The resource occupancy of the FPGA for the implemented modules is shown in Table I. As it can be seen, the complete system was able to be mapped in the chosen FPGA using only 26% of the total resources, operating at a maximum frequency of 85 MHz. This largely exceeds the required ≈ 1.5 MHz for the implementation of the *early layers* block (processing of an image of size 32×32 at a rate of 30 fps executing 49 operations per cycle due to hardware folding) and ≈ 1 MHz for the *NPC* block (generation of spikes at a maximum rate of 100 Hz to an equivalent microelectrode array of size 32×32).

To guarantee the correct operation of all the modules, exhaustive tests were performed. In the case of the *NPC* block and the *serialization and data packing* module, the evaluation of these circuits was made by implementing: 1) a *data unpacking* block to decode the transmitted data packets and 2) an *image recovery* block responsible for the translation of a sequence of pulses into a image capable of being displayed on a standard monitor. Both these blocks were implemented on a second FPGA, a XILINX SPARTAN XC2S300 FPGA [52] connected to the prototype by a 40-pin header. The *image recovery Block* is based on a fourth-order low-pass filter where the output increases when a new spike is generated and decreases otherwise. Fig. 13 shows a photograph of the monitor on an experimental test of the *NPC* block and *serialization and data packing* module. In this test, a color image, captured directly from the camera, was presented
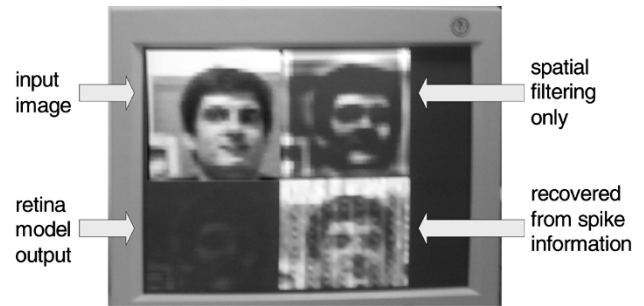

Fig. 13. Capture of the image displayed on a standard monitor.

as input to the *NPC* block (top left corner of Fig. 13). The value of each pixel, treated as a firing rate, is converted into a sequence of pulses, packed into structures as those of Fig. 12 and sent to a second FPGA by a serial communication link (which simulates the real wireless link). In the second FPGA, a SPARTAN XC2S300, the packets are decoded, and the spikes sent to the *image recovery block* which attempts to recover the initial image (bottom right corner of Fig. 13). The person in the images was moving at the time of the photo to allow displaying an image on the retina model output.

The prototype shown in Fig. 11 is operated at a frequency of 50 MHz and consumes ≈ 500 mW at 5 V, where 50 mW are due to the image sensor. The DACs only operate when images are being displayed on a standard monitor. In this case the prototype consumes an extra power of 250 mW.

In order to study the involved phenomena, in particular the important magnetic coupling issues, an RF link board level prototype was implemented [53]. This prototype is a ten times frequency scaled version of the system operating with a forward data rate 100 kbps and carrier frequency 1 MHz and with backward data rate 15.625 kbps with carrier frequency 500 kHz. The RF link results presented in this section were obtained using this prototype.

The primary RF unit maximum power consumption is 180 mW at a power supply of 9 V. Fig. 14 illustrates the amplitude response of the transformer for different intercoil distances. The transformer pass band is centred at 1 MHz, as desired. As one can see, a significant attenuation is introduced by the transformer which results from its very weak magnetic coupling [44]. However, the signal delivered to the receiver still allows satisfactory power and data recovery.

Some experiments were conducted to determine the power efficiency that is magnetically induced from the primary to the secondary system. It was determined that it is possible to obtain
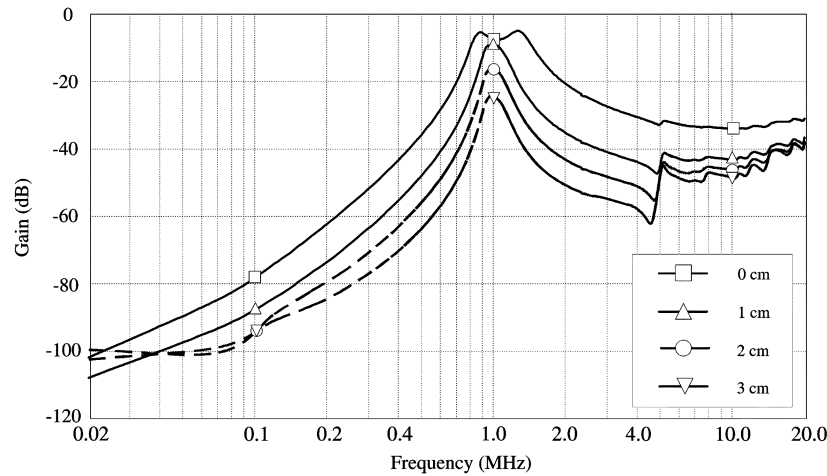
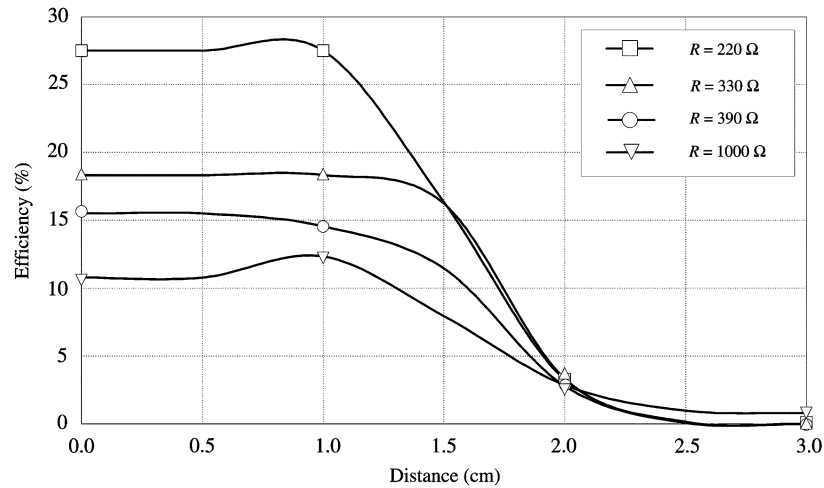Fig. 14. Amplitude characteristics for distances of 0, 1, 2, and 3 cm between primary and secondary coil.

Fig. 15. Coupling efficiency as a function of the intercoil distance and load resistor.

an efficiency of about 28% (about 50 milliwatts have been measured at the secondary receiver output and 180 milliwatts power consumption in the primary RF unit for intercoil distances up to 1 cm) as can be seen in Fig. 15.

Fig. 16 depicts the load power as a function of the intercoil distance. As can be seen, there is a degradation in power transfer between primary and secondary RF units. However, it is not significant for the equivalent load resistor values expected for a secondary RF unit with maximum power consumption of 50 mW. This degradation augments with increased distance or when the load resistances decrease. The maximum output capability occurs for intercoil distances below 1 cm (this is the target distance for which the RF transformer design was optimized). The overall transmitted and received data are illustrated in Fig. 17 (bit rate is 100 kbps and the intercoil distance is 1 cm). As one can see from this figure, scrambled data is properly recovered at the receiver after crossing all the RF link: primary modulator, RF transformer and FSK secondary demodulator. In this experiment, 50 mW of a 3.3 V dc power supply are being extracted by the secondary power recovering circuitry, simultaneously with the secondary data demodulation. The oscilloscope traces correspond to the data from the NPC and the recovered data (raw data), respectively (see Fig. 5).

VI. CONCLUSION

This paper proposes the architecture for a visual neuroprosthesis and demonstrates its feasibility using nowadays technology. The primary goal of this system is to restore a limited but useful visual sense to profoundly blind people. This neuroprosthesis is based on a *neuromorphic encoder* and a noninvasive system for intracortical stimulation of the visual cortex. The developed *neuromorphic encoder* receives the visual stimulus from a miniature digital video camera, performs the spatial and temporal processing corresponding to the "early layers" of the retina and implements a simplified version of an integrate-and-fire spiking neuron to model the spike generation.

To achieve a noninvasive system for intracortical stimulation a bidirectional RF link was designed. The system uses FSK modulation in the forward link and DBPSK modulation in the backward link. These modulation formats were chosen since, due to their constant-amplitude characteristic, they can offer significant robustness against the severe amplitude variations which are expected in this system. Because of its high efficiency, a Class-E tuned power amplifier was chosen to transmit at 1 Mbps over a 10-MHz carrier.
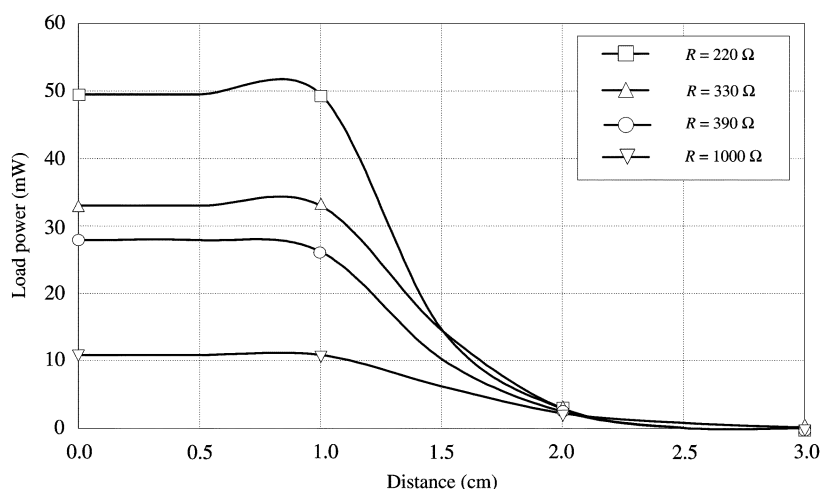
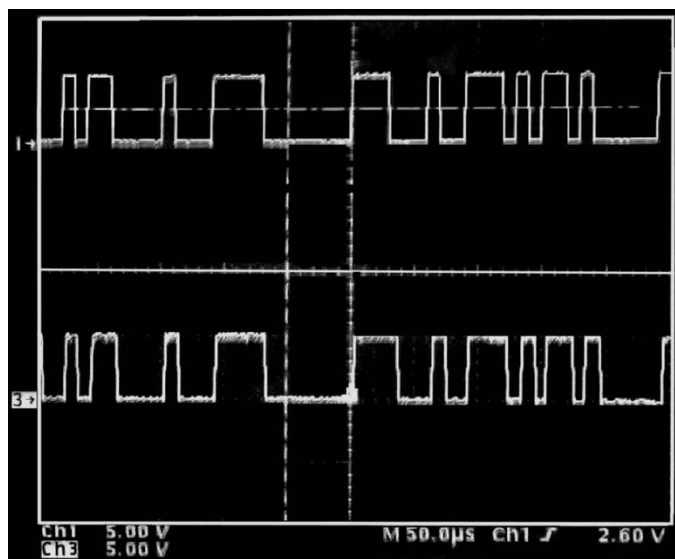Fig. 16. Load power as a function of intercoil distance and load resistor.

Fig. 17. RF link FSK demodulator operation: transmitted NRZ data (top) and recovered data (bottom).

The neuromorphic encoder, which generates the spikes delivered to the RF link, was implemented in a video processing board based on a XILINX Spartan XC3S400 FPGA. The encoder occupies about 26% of the FPGA resources, exhibiting a power consumption of about 500 mW for a clock frequency of 50 MHz. A frequency scaled prototype was also built in order to test the performance of the data and power communication system. The transmitted signal also carries the power for the secondary unit ($\approx$50 milliwatts) with an average efficiency of 28% for 1 cm intercoil distance. The system operates very well with power, data and clock recovery for distances up to 2 cm.

The *neuromorphic encoder*, which generates the spikes delivered to the RF link, was also implemented in a video processing board based on a XILINX Spartan XC3S400 FPGA. The encoder occupying about 26% of the FPGA resources and operating at 50 MHz, has a power consumption of about 500 mW.

Based on the developed prototype, a complete system is now being designed in ASIC technology. The *neuromorphic encoder* is being synthesised using the UMC 0.13-μm CMOS technology process [40]. For the *wireless communication link* and the *electrode stimulators and sensing* modules it is required a 0.35-μm AMS CMOS technology to allow for the high voltage levels being used. The work presented here contains several significative innovations. Mainly, they are as follows.

1) It is the first known complete architecture designed and implemented of the intracortical visual neuroprosthesis.
2) A new full directional RF link carrying data and power was proposed with significative contributions, namely: a new data clock feedforward bit synchronizer and a new communication protocol appropriated for cortical prosthesis.
3) A new video neuromorphic encoder system was developed.

It is expected that these innovations contribute to help the development of future practical and compact visual prosthesis.

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