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On the Static Resolution of Digitally Corrected Analog-to-Digital and Digital-to-Analog Converters With Low-Precision Components

Matthias Frey, *Member, IEEE*, and Hans-Andrea Loeliger, *Fellow, IEEE*

***Abstract*—This semi-tutorial paper considers the effect of component mismatch on the static accuracy of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with digital correction. First, it is noted that the effective static resolution of flash ADCs is not much reduced by component mismatch: with proper digital correction, the loss due to mismatch is only about 1.3 bit, virtually independently of the mismatch level unless the mismatch is very small. Second, it is noted that current steering DACs may actually benefit from component mismatch. Moreover, with proper digital correction, current steering DACs can achieve an effective static resolution of m bits with as few as $m + 2$ near-unit low-precision current sources.**

***Index Terms*—Analog-to-digital converter (ADC), calibration, digital-to-analog converter (DAC).**

I. Introduction

In this paper, we point out some basic observations on the influence of component mismatch on the static accuracy of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with digital correction. It is noted that, with proper digital correction, the effect of mismatch in flash ADCs is quite small, and mismatch may actually be beneficial in current steering DACs. These observations suggest to allow arbitrarily large mismatch in the design of such converters. While such an approach to ADCs has been suggested by several authors (as will be detailed below), its attractivity for current steering DACs does not seem to have been noticed in the literature.

This paper is semi-tutorial in that most of its substance was presented in [1] and [2]. However, the analytical results given in the Appendix are new.

We begin with ADCs. Flash ADCs consist of a bank of comparators, each with its own threshold [3]. Traditionally, such ADCs are designed to have equidistant thresholds. This is costly: in order to limit the effect of component mismatch on the thresholds, the components (mainly transistors) must be sufficiently large, which in turn requires sufficiently large currents to achieve the required speed.

However, in many applications (e.g., in communications receivers), all that is really required is a sufficient density of comparator thresholds. Moreover, the value of the individual thresholds need not be predictable at design time and may vary from chip to chip, provided they are known (with sufficient accuracy) at run time. With proper digital correction (involving some sort of measurement of each chip), it is thus possible to reduce both the area and the power consumption of the analog circuits.

ADCs designed (more or less) in this spirit have been reported in [4]–[8]. All of these papers consider flash ADCs with low-precision comparators. In [5] and [6], only a fraction of the comparators is actually used: during calibration, the comparators with suitable thresholds are identified and the others are deactivated. In [7], an effective resolution of 6 bits (at very high speed) was obtained with 255 low-precision comparators. The mathematical background of optimal ADC postcorrection was addressed in [8] and illustrated with experimental ADC data. The state of the art in error compensation in ADCs is summarized in [9].

However, a basic observation (Fig. 2, shown later) seems to be missing from the literature: with proper digital correction, the loss in effective resolution due to misplaced comparator thresholds is quite small (about 1.3 bits) and virtually independent of the mismatch level unless the mismatch is very small. In consequence, it seems attractive to deliberately use "cheap and dirty" (i.e., small) comparators that are fast without consuming much power. We illustrate this approach with measurements from an integrated flash ADC with 256 low-precision comparators that achieves an effective static resolution of almost 7 bits.

An analogous approach to DACs is perhaps even more interesting. Specifically, we will consider current steering DACs with digital correction. We will see that mismatch can actually improve the resolution of such DACs, and we will demonstrate that an effective resolution of about m bits can be achieved with as few as $m + 2$ imprecise near-unit current sources.

In this paper, we do not consider the actual calibration methods for such ADCs and DACs. Such calibration methods are a research area for themselves, for which the results of this paper give further motivation. Also, the added cost (in terms of area and power) in the digital part due to the digital correction of such converters may offset the cost reduction in the analog part in some applications; however, the balance of these two effects depends on details of the application and of the (ever-changing) technology. In contrast, the observations of this paper (except for the measurements of Section IV) are "information theoretic" and do not depend on the technology.

This paper is structured as follows. Flash ADC converters with low-precision comparators are discussed in Sections II and III. Measurements from an actual ADC chip are presented in Section IV. Current steering DACs with low-precision components are discussed in Sections V and VI. An asymptotic anal-

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M. Frey is with the Matsuzawa Laboratory, Tokyo Institute of Technology, Tokyo 152-8552, Japan (e-mail: mfrey@ieee.org).

H.-A. Loeliger is with the Department of Information Technology and Electrical Engineering, ETH Zurich, CH-8092 Zurich, Switzerland (e-mail: loeliger@isi.ee.ethz.ch).

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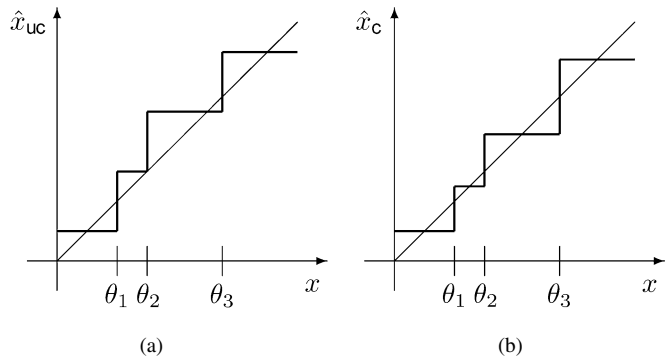


Fig. 1. ADC with comparator mismatch. (a) Standard (uncorrected) digital output. (b) Corrected digital output.

ysis of the performance of such DACs and ADCs is given in the Appendix.

II. Flash ADCs With Low-Precision Comparators

A flash ADC applies the analog input $x \in \mathbb{R}$ in parallel to K comparator circuits. Each comparator has its own threshold $\theta_k, k = 1, \ldots, K$, and computes the sign of $x - \theta_k$. In order to simplify the following discussion, we will assume $0 \leq x < 1$, and we define the two dummy thresholds $\theta_0 = 0$ and $\theta_{K+1} = 1$. An ideal m-bit flash ADC has $K = 2^m - 1$ comparators with thresholds $\theta_k = k\Delta, k = 1, \ldots, K$, with $\Delta = 2^{-m}$. However, in this paper, we allow arbitrary thresholds; we only assume that the thresholds are ordered (or reordered, if necessary) such that $\theta_k < \theta_{k+1}$ for $0 \leq k \leq K$.

If the analog input x lies in bin k, i.e., if $\theta_k \leq x < \theta_{k+1}$, the standard (uncorrected) digital output is

$$\hat{x}_{\mathrm{uc}} = k\Delta + \Delta/2 \tag{1}$$

while the corrected digital output is

$$\hat{x}_{\mathrm{c}} = (\theta_k + \theta_{k+1})/2 \tag{2}$$

the mean of the corresponding bin (see Fig. 1). For an ideal ADC, (1) and (2) coincide.

In order to assess the performance of ADCs with imprecise thresholds, we consider an ensemble of ADCs with random thresholds $\theta_k = k\Delta + E_k, k = 1, \ldots, K$, where $E_1, \ldots E_K$ are independent zero-mean Gaussian random variables with variance σ^2. The digital correction amounts to reordering the thresholds such that $\theta_k < \theta_{k+1}$ holds and then to use (2). (Thresholds outside the allowed interval $0 \leq x < 1$ are simply discarded.) We will measure the quantization distortion by the mean squared error (MSE)

$$\mathrm{MSE} = \int_0^1 (\hat{x}_{\mathrm{c}}(x) - x)^2 \, dx \tag{3}$$

and by the effective resolution (in bits) defined as

$$\mathrm{Res}_{\mathrm{eff}} = -\log_2 \sqrt{12 \cdot \mathrm{MSE}}. \tag{4}$$

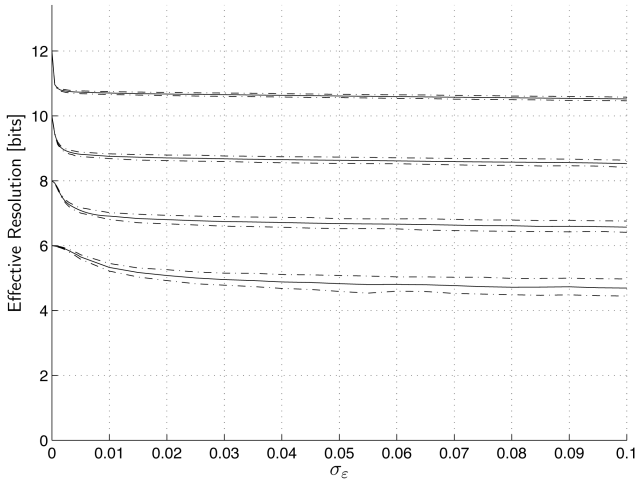


Fig. 2. Effective resolution versus σ for digitally corrected ADCs with random comparator thresholds. Solid lines: average effective resolution. Dashed lines: the best ten percentiles and the worst ten percentiles.

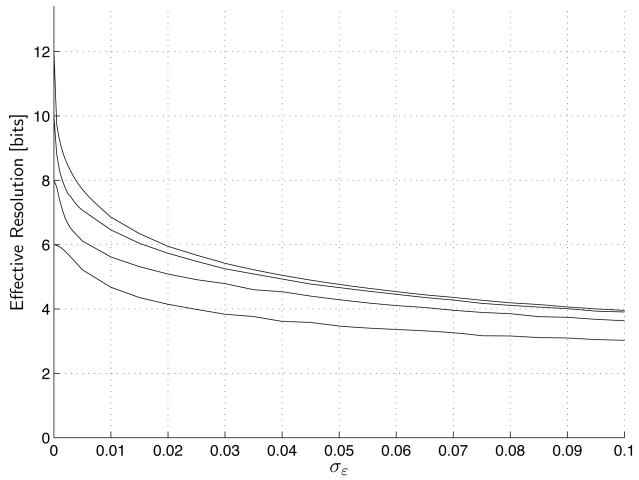


Fig. 3. Average effective resolution versus σ for uncorrected ADCs with random comparator thresholds (same thresholds as in Fig. 2).

The average performance of such random ADCs (with correction) is shown in Fig. 2. The figure shows the average effective resolution (in bits) as a function of σ^2 for $K = 2^6, K = 2^8, K = 2^{10}$, and $K = 2^{12}$. Also shown in Fig. 2 are the best ten percentiles and the worst ten percentiles of the ensemble. As claimed, the loss in effective resolution due to the threshold errors does not exceed about 1.3 bits and is virtually independent of σ unless σ is very small.

For comparison, the effective resolution of the same random ADCs without the digital correction [i.e., with output (1)] is shown in Fig. 3. Without correction, such converters are useless unless σ is very small.

Also, for comparison, Fig. 4 shows the performance of the same random ADCs as in Fig. 2, but with the different digital correction of [5] and [6]. In this example, only half of the comparators are actually used. It is remarkable that this alternative (and perhaps somewhat simpler) correction scheme achieves almost the same MSE as the optimal correction (2).

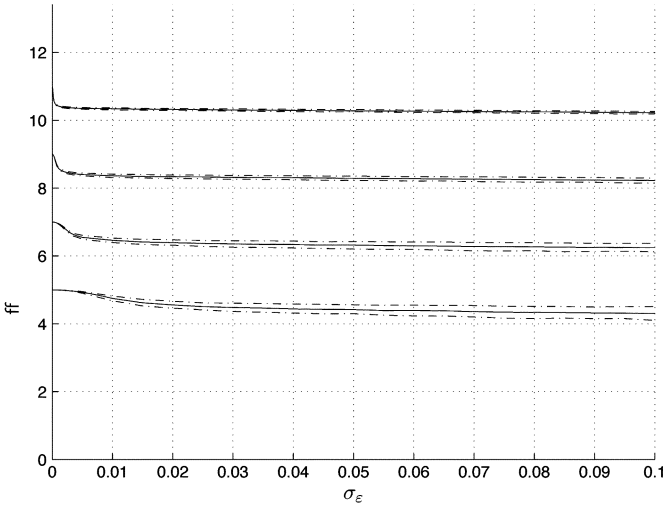


Fig. 4. Average effective resolution versus σ for "random" ADCs (with the same thresholds as in Fig. 2) with the digital correction according to Flynn *et al.* [5] and [6].

Figs. 2–4 were obtained by simulations. The limiting value (for large σ) of the effective resolution [with the optimal correction (2)] may also be obtained analytically under the assumption that the thresholds are uniformly distributed between 0 and 1. In the limit of $K \to \infty$, the effective resolution in this case is

$$\mathrm{Res}_{\mathrm{eff}} = \log_2 K - \log_2 \sqrt{6} \tag{5}$$

$$\approx \log_2 K - 1.29 \text{ bits}. \tag{6}$$

The proof of (5) is given in Appendix I.

Figs. 2 and 4 clearly suggest to design ADCs without spending resources to control the position of the individual thresholds.

III. Issues With ADC Correction

We briefly address some issues with the correction scheme of Section II.

Correction by Look-Up Table: The correction (2) can be stored in a look-up table. Digital circuitry is required to compute the index k to access the look-up table. This is a well-known issue with all flash ADCs, and it is exacerbated by the nonmonotonicity of "random" thresholds [7].

Precision of Digital Output: The corrected digital outputs $\hat{x}_{\mathrm{c}}$ should be stored (in the look-up table) with more than $\log_2 K$ bits; about $\log_2 K + 1.5$ bits should suffice in most cases (cf. Section IV). It follows that, for an effective resolution of m ($\approx \log_2 K - 1.3$) bits, it suffices to store $\hat{x}_{\mathrm{c}}$ with a precision of about $m + 2.8$ bits.

Calibration: The thresholds θ_k must be measured. This could be done, for example, by applying a ramp signal $x(t)$ to the converter input and measuring the switching times of all comparators. However, such schemes are outside the scope of this paper.

Performance Measures Beyond MSE: The nonlinearity of ADCs is usually assessed by means of the differential nonlinearity (DNL) and the integral nonlinearity (INL) [3], which measure the deviation of the thresholds from their ideal positions. These quantities do not appear to make sense for ADCs that are corrected according to (2). However, it is obvious from Fig. 1 that the linearity of such corrected ADCs is excellent.

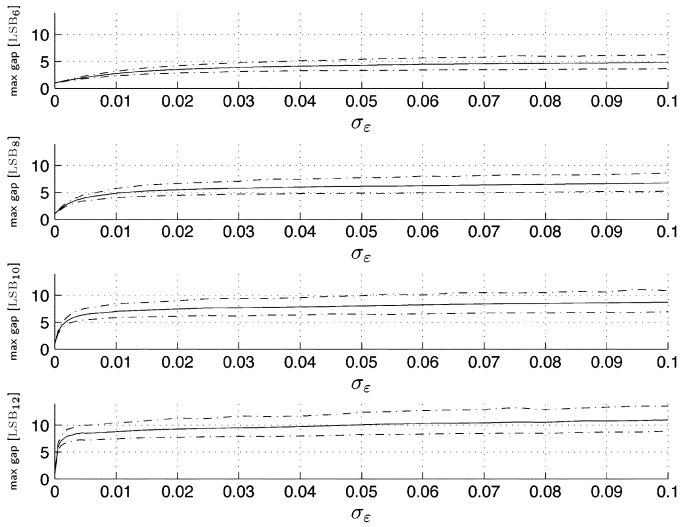


Fig. 5. Largest gap between thresholds of "random" ADCs as in Fig. 2. The gaps are measured in terms of LSB-units $= \Delta$. (In an ideal ADC, all gaps equal 1 in these units.) Solid lines: average maximum gap. Dashed lines: the best ten percentiles and the worst ten percentiles.

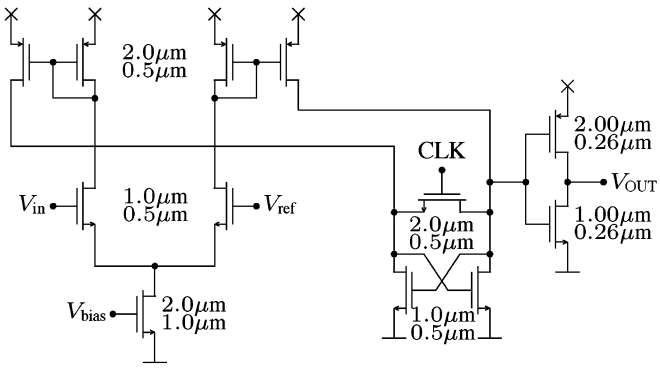


Fig. 6. Comparator circuit. The numbers indicate the width and length of the transistors.

This further suggests that the spectral distortion is very small, which is indeed confirmed by the measurements in Section IV.

However, "random" ADCs are likely to have a few large gaps, i.e., exceptionally large differences between two successive thresholds. For the ADCs of Fig. 2, the maximal gaps are plotted in Fig. 5. Note that the relative magnitude of the maximal gaps (relative with respect to the ideal threshold difference Δ) increases with K.

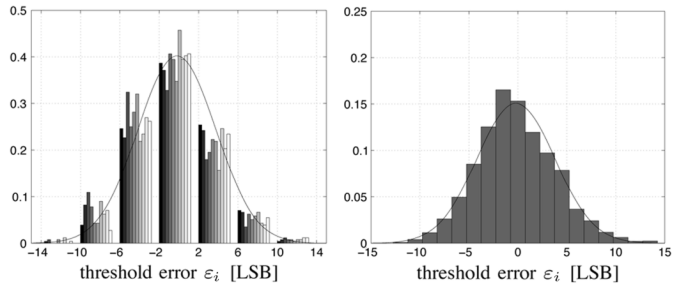
IV. ADC Design Example With Measurements

In order to demonstrate the approach of Section II, a flash ADC with 256 comparators was implemented in a 0.25-μm BiCMOS process (IBM6HP) using only CMOS transistors. The chip was designed for a supply voltage of $V_{\mathrm{dd}} = 1.8$ V. The chip also contains a 256-to-8-bit multiplexer, but the digital correction is not part of the chip.

The comparator circuit (taken from [10]) is shown in Fig. 6. Other than in [10], we use very small transistors (as indicated in Fig. 6). For example, the two input transistors of the differential pair have width $W = 1$ μm and length $L = 0.5$ μm, which is only slightly larger than the minimum transistor size of the process given by $W_{\min} = 0.3$ μm and $L_{\min} = 0.24$ μm.

TABLE I
MEAN m_ε AND STANDARD DEVIATION σ_ε OF THE THRESHOLD ERRORS FOR ALL COMPARATORS OF ONE CHIP

Chip:	m_ε $[mV]$	m_ε $[\mathrm{LSB}_8]$	σ_ε $[mV]$	σ_ε $[\mathrm{LSB}_8]$
1	1.29	0.33	14.74	3.77
2	-0.51	-0.13	16.26	4.16
3	-4.65	-1.19	16.36	4.19
4	-0.34	-0.09	15.59	3.99
5	-0.23	-0.06	14.77	3.78
6	-0.70	-0.18	14.91	3.82
7	-1.17	-0.30	15.97	4.09
8	-0.81	-0.21	15.42	3.95
9	-1.29	-0.33	15.64	4.00
10	0.64	0.16	14.84	3.80



(a) (b)

Fig. 7. Distribution of threshold errors. (a) All ten chips individually. (b) All ten chips together.

The reference voltages (V_{ref}) for the comparators are generated by a resistor ladder made of p+ polysilicon resistors. The width of each resistor is 6 μm and the length of each resistor is 3 μm. The nominal resistance of such a resistor is 143 Ω and the resistance of the whole ladder is 36.6 kΩ. In all of our measurements, the voltage across the resistor ladder is 1.0 V (with end points at 0.5 and 1.5 V, respectively). The current through the ladder is thus 27.3 μA.

Ten chips in DIL-24 packages were available for measurements.

A. Measurements of the Comparators

The thresholds of all comparators (of all ten chips) were measured with a custom-built measurement device using 12-bit ADCs. The measured thresholds θ_k were compared with the thresholds $k\Delta$ (with the appropriate Δ) of an ideal 8-bit ADC. Table I shows the mean m_ε and the standard deviation σ_ε of the threshold error $\varepsilon_k = \theta_k - k\Delta$ for each chip. These numbers are expressed both in volts and in LSB_8 (least significant bit) units $(=$ multiples of $\Delta)$. The histogram of ε_k is shown in Fig. 7, both individually for each chip (left) and over all chips (right).

Averaged over all chips, we have

$$m_\varepsilon = -0.78\ \mathrm{mV} = -0.20\ \mathrm{LSB}_8 \tag{7}$$

$$\sigma_\varepsilon = 15.51\ \mathrm{mV} = 3.97\ \mathrm{LSB}_8. \tag{8}$$

It follows that, without the digital correction, the ADCs are very bad indeed. According to a popular rule of thumb, $\sigma_\varepsilon \leq (1/6)$ LSB is required in order to achieve a reasonable yield with an uncorrected ADC [11]. From (8), the accuracy of our converters would thus be adequate for a 4-bit converter, which is consistent with Fig. 3. With digital correction, however, we expect from Fig. 2 (with $\sigma_\varepsilon = 0.0155$) to achieve an effective resolution of almost 7 bits, which is consistent with the measurements given in Section IV-B.

TABLE II
QUANTIZATION ERROR AND EFFECTIVE RESOLUTION

Chip:	Q_{raw} $[\mathrm{LSB}_8]$	Q_{calib} $[\mathrm{LSB}_8]$	eff. Res. [bits]
1	1.97	0.64	6.84
2	5.49	0.67	6.79
3	4.63	0.72	6.68
4	5.99	0.65	6.83
5	3.85	0.64	6.85
6	4.51	0.57	7.01
7	4.29	0.60	6.95
8	4.83	0.63	6.86
9	3.08	0.58	6.99
10	5.86	0.60	6.94

B. Performance of the Corrected ADC

The manufactured chips do not contain any circuitry for the digital correction: they simply provide the (digital) output of all comparators (in multiplexed form). However, from the measured thresholds (as in Section IV-A), it is straightforward to calculate the static accuracy that would be obtained with the corrected digital output (2) [cf. (16) in Appendix I]. This calculation was carried out for all 10 chips (after proper gain and offset correction, and ordering of the tresholds), and the result is shown in Table II. Also shown in Table II is the rms quantization error Q_{calib} of the ADC with corrected digital output, as well as the rms quantization error Q_{raw} of the ADC with conventional uncorrected digital output. (The rms quantization error Q is defined as the square root of the MSE (3), here in units of $\mathrm{LSB}_8 = \Delta$.) Note that the effective resolution varies from chip to chip, but is close to 7 bits for all ten chips.

More detailed information about one chip (chip 4, which is the worst chip) is shown in Figs. 8 and 9: Fig. 8 shows both the corrected digital output and the uncorrected digital output, and Fig. 9 shows the corresponding quantization error spectrum.

The effective resolution in Table II is based on a digital correction table with full measurement precision. In Table III, the effective resolution (of chip 1) is shown for a (corrected) digital output with $L = 8, 9, \ldots, 12$ bits. Note that $L = 10$ suffices to achieve virtually the full effective resolution.

V. CURRENT STEERING DACS WITH LOW-PRECISION NEAR-UNIT CURRENT SOURCES

A current steering DAC [3] consists of N current sources that produce the constant currents $c_1, \ldots, c_N$. These current sources are individually switched to form the output current

$$y = \gamma \sum_{n=1}^{N} s_n c_n \tag{9}$$

with $s_n \in \{+1, -1\}$ and with some scale factor γ. (In an alternative version, we have $s_n \in \{0, 1\}$.)

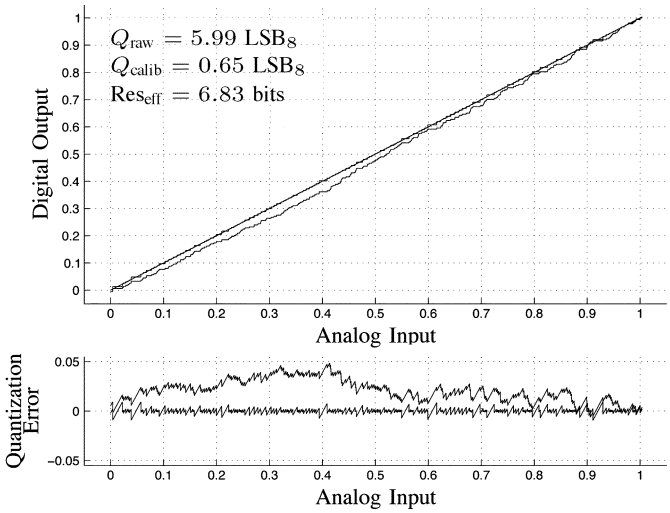


Fig. 8. Input–output characteristics (top) and quantization error (bottom) of ADC chip 4, both corrected and uncorrected.

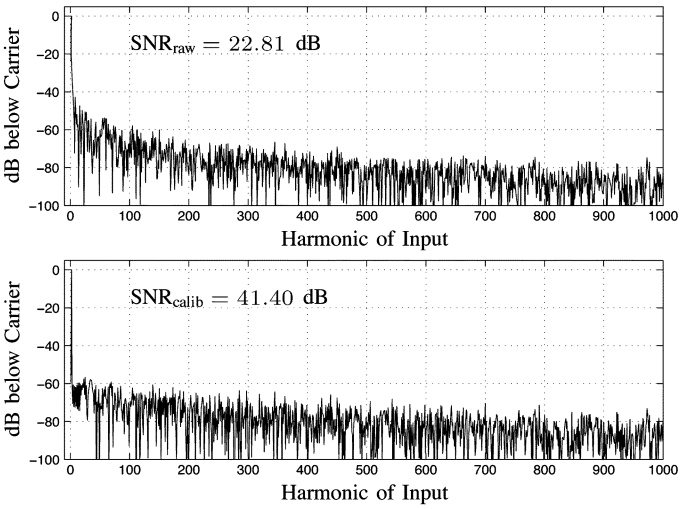


Fig. 9. Quantization error spectrum of ADC chip 4, both uncorrected (top) and corrected (bottom), under the assumption of ideal sampling.

TABLE III
RMS QUANTIZATION ERROR FOR A DIGITAL OUTPUT WITH $L = 8 \ldots 12$ BITS

Chip:	Q_{8b}	Q_{9b}	Q_{10b}	Q_{11b}	Q_{12b}	Q_{calib}
1 [LSB_8]:	0.70	0.66	0.65	0.64	0.64	0.64

Let $\mathcal{C}$ be the set of all possible output currents (9) for fixed $c_1, \ldots, c_N$ and fixed γ. In an ideal binary-scaled m-bit current steering DAC, we have $c_n = 2^{n-1}$ and $\mathcal{C} = \mathcal{C}_{\text{ideal}}$ with

$$\mathcal{C}_{\text{ideal}} = \gamma\{\pm 1, \pm 3, \pm 5, \ldots, \pm(2^m - 1)\}. \tag{10}$$

Note that the same set $\mathcal{C}$ is obtained with $N = 2^m - 1$ unit current sources $c_1 = c_2 = \ldots = c_N = 1$. However, in this paper, we allow arbitrary current sources c_n and correspondingly general sets $\mathcal{C}$.

In the most straightforward circuit realizations of current steering DACs, the relative cost (both in chip area and in power consumption) of the individual current sources $c_1, \ldots, c_N$ is proportional to their current c_n. (The cost also depends, of course, on the required precision.) If $c_2 = 2c_1$, it is quite correct to think of current source 2 as two copies of current source 1 connected in parallel. In this rough analysis, the cost of the mentioned ideal binary-scaled m-bit DAC (with $c_n = 2^{n-1}$) equals the cost of $2^m - 1$ unit current sources. (As we have seen, a DAC with $N = 2^m - 1$ ideal unit current sources also achieves a resolution of m bits.) However, we will see below that essentially the same resolution can be achieved with as few as $m + 2$ *imprecise* near-unit current sources.

Let x be the real number (available in digital form) that is to be converted into the analog output y according to (9). The conversion may be described as follows.

1) Round x to the nearest point in $\mathcal{C}$.
2) Set the switches $s_1, \ldots, s_N$ accordingly.

For an ideal m-bit DAC, both steps are trivial; for general current sources $c_1, \ldots, c_N$ (and corresponding $\mathcal{C}$), these two steps are the digital correction.

In the following, we will assume $-0.5 \leq x < 0.5$. The performance of various DACs will be measured by the MSE

$$\text{MSE} = \int_{-0.5}^{0.5} (y(x) - x)^2\, dx \tag{11}$$

or by the corresponding effective resolution $-\log_2 \sqrt{12\,\text{MSE}}$. The scale factor γ in (9) will be adjusted to obtain the smallest MSE. (This may result in unused points in $\mathcal{C}$ of magnitude larger than 0.5.)

We consider several ensembles of DACs with random source currents $c_1, \ldots, c_N$ given by $c_n = c_{n,\text{nom}}(1 + E_n)$, where $E_1, \ldots E_N$ are independent zero-mean Gaussian random variables with variance σ^2 [12].

In the first ensemble, we use only (imprecise) unit current sources: $c_{n,\text{nom}} = 1$ for all n. The performance of this ensemble as a function of σ is shown in Figs. 10 and 11 for $N = 12$ and for $N = 14$, respectively. As is obvious from these figures, the performance of these (corrected) converters is surprisingly good provided that the mismatch (measured by σ) is sufficiently *large*.

In the second ensemble of DACs, we use current sources with nominal currents $c_{n,\text{nom}} = 1.1^{n-1}$. The performance of this ensemble is shown in Figs. 12 and 13 for $N = 12$ and for $N = 14$, respectively. With this ensemble, the excellent resolution of the first ensemble is now achieved at every mismatch level.

In the third and last ensemble of DACs, we use current sources with nominal currents $c_{n,\text{nom}} = 1 + 0.1(n - 1)$. The performance of this ensemble is shown in Fig. 14 for $N = 14$.

In all of these examples, we achieve an effective resolution of about $N - 2$ bits with N imprecise current sources.

The high-σ regions in Figs. 10–14 are in good agreement with

$$\text{Res}_{\text{eff}} \approx N - 1.738\ \text{bits} \tag{12}$$

which follows from the asymptotic analysis in Appendix II. The differences in the low-σ regions of these figures can be partly understood by considering the limit of the set $\mathcal{C}$ for $\sigma \to 0$. In Figs. 10 and 11, $\mathcal{C}$ contains only $N + 1$ points for $\sigma = 0$; in Fig. 14, the cardinality of $\mathcal{C}$ is still very limited for $\sigma = 0$; but,

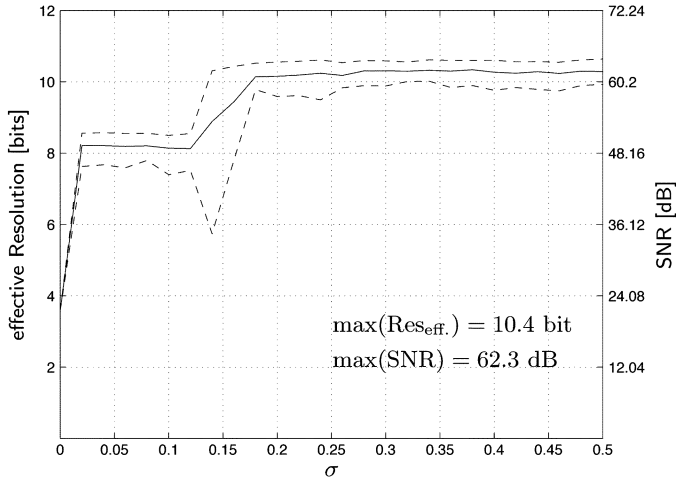


Fig. 10. Effective resolution versus σ for digitally corrected DAC with $N = 12$ random (nominally unit) current sources. Solid lines: average effective resolution. Dashed lines: ten best and ten worst percentiles.

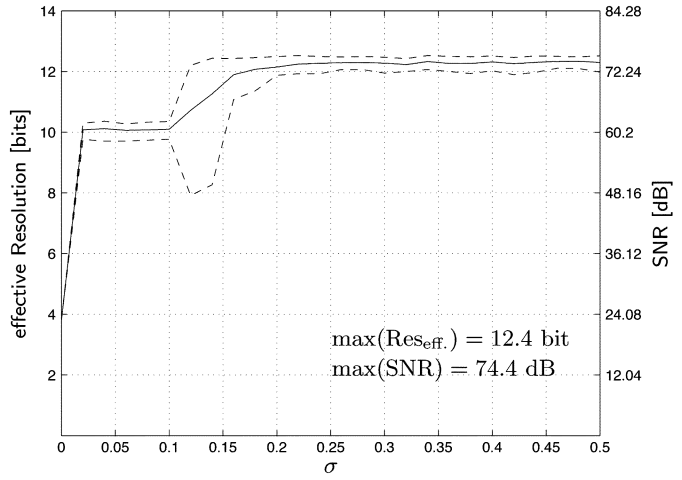


Fig. 11. Effective resolution versus σ for digitally corrected DAC with $N = 14$ random (nominally unit) current sources. Solid lines: average effective resolution. Dashed lines: ten best and ten worst percentiles.

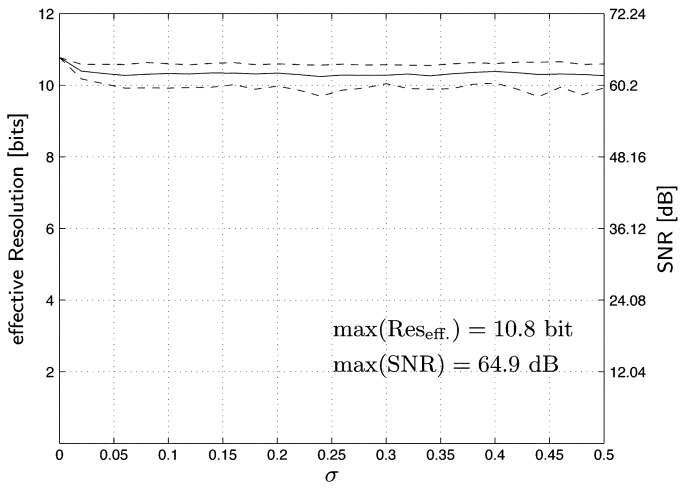


Fig. 12. Effective resolution versus σ for digitally corrected DAC with $N = 12$ random current sources with mean currents $c_{n,0} = 1.1^{n-1}, n = 1, \ldots, N$. Solid lines: average effective resolution. Dashed lines: ten best and ten worst percentiles.

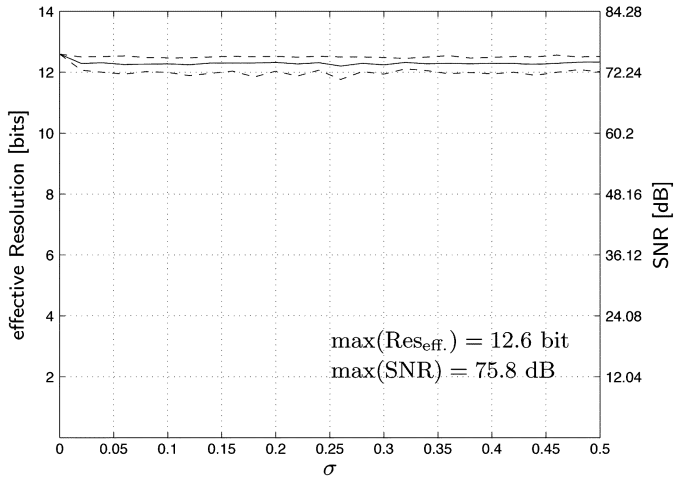


Fig. 13. Effective resolution versus σ for digitally corrected DAC with $N = 14$ random current sources with mean currents $c_{n,0} = 1.1^{n-1}, n = 1, \ldots, N$. Solid lines: average effective resolution. Dashed lines: ten best and ten worst percentiles.

in Figs. 12 and 13, $\mathcal{C}$ contains essentially 2^N different points even for $\sigma = 0$.

Figs. 10–14 were obtained by simulations. The limiting value (for large N and large σ, and with optimized scale factor γ) may also be obtained analytically: in this limit, the mean effective resolution is given by (12) independently of the particular ensemble. A semi-rigorous proof of (12) is given in Appendix II.

VI. Issues With DAC Correction

We briefly address some issues with the correction scheme of Section V.

Correction by Look-Up Table: The conversion of the real number x ($-0.5 \leq x < 0.5$, available in digital form) into the desired controls $s_1, \ldots, s_N$ of the switches may be carried out as follows. Let m be the effective resolution (in bits) to be achieved. We first round x to, say, $m + 2$ bits. From there, we use a look-up table to obtain $s_1, \ldots, s_N$.

Calibration: The following approach works in principle (although its development into a practical method is not trivial): for any given configuration of switch positions $s_1, \ldots, s_N$, the output current y may be measured by charging a capacitor and measuring the time between two fixed voltages. The calibration can also allow for the case where the output of the DAC is not y as in (9) but some (deterministic) function of it. However, the investigation of practical calibration schemes is beyond the scope of this paper.

Output Range: For "random" DACs as in Section V, the density of points in $\mathcal{C}$ is higher in the center (around zero) than at the margins. For example, Fig. 15 shows a histogram of the density of points in $\mathcal{C}$ for the DAC of Fig. 12 for $\sigma = 0.5$. (The central limit theorem may be invoked to argue that the density tends to a Gaussian distribution.) The optimization of the scale factor γ in (9) is therefore important. With an optimized scale factor, only a central region of $\mathcal{C}$ is actually used. In the example of Fig. 15, less than 40% of the total output range (containing over 80% of the points in $\mathcal{C}$) is used.

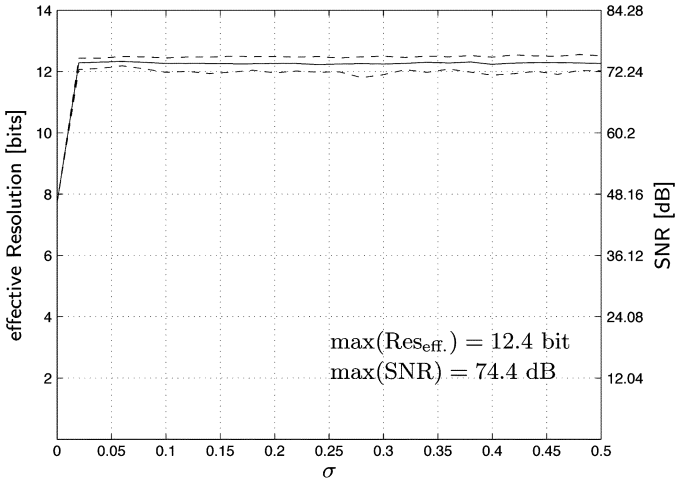


Fig. 14. Effective resolution versus σ for digitally corrected DAC with $N = 14$ random current sources with mean currents $c_{n,0} = 1 + 0.1(n-1), n = 1, \ldots, N$. Solid lines: average effective resolution. Dashed lines: ten best and ten worst percentiles.

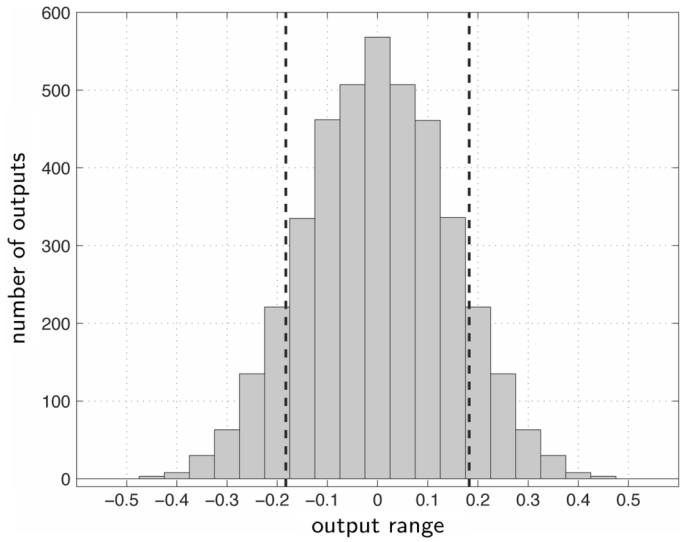


Fig. 15. Distribution of points in $\mathcal{C}$ and used range thereof for the DAC of Fig. 12 with $\sigma = 0.5$.

In the limit of large N and large σ, the analysis in Appendix II gives an optimal scale factor γ such that the standard deviation of the distribution of the points in $\mathcal{C}$ (as in Fig. 15) is

$$\sigma_{\mathcal{C}} \approx 0.361 \tag{13}$$

independently of the particular ensemble. In this case, about 83.4% of the points in $\mathcal{C}$ are used, which is in good agreement with the experimental results.

Performance Measures Beyond MSE: Both the linearity and the spectral distortion are expected to be excellent. Occasional large gaps between points in $\mathcal{C}$ may be an issue in some applications.

VII. Conclusion

There is an increasing awareness that flash ADCs can be built using low-precision comparators with virtually "random" thresholds. We have noted that the loss in the effective static resolution of such ADCs is limited to about 1.3 bits virtually independently of the mismatch level unless the mismatch is very small. This observation is confirmed by a chip with 256 low-precision comparators that achieves a static resolution of almost 7 bits.

For current steering DACs, we have shown that an effective static resolution of m bits can be achieved with as few as $m+2$ low-precision near-unit current sources. Such corrected DACs may be attractive as components inside ADCs (e.g., such as successive-approximation ADCs or sigma-delta ADCs) or for the digital calibration of other analog circuits such as OTAs [13] and analog filters made thereof.

In this paper, we have ignored the cost (in terms of chip area and power) of the digital correction, and we have not addressed practical calibration schemes. However, the promising results of this paper suggest that the study of these issues is worthwhile.

Appendix I
Asymptotic Analysis of ADCs: Proof of (5)

For fixed thresholds θ_k, the MSE (3) is

$$\mathrm{MSE} = \int_0^1 (\hat{x}(x) - x)^2 \, dx \tag{14}$$

$$= \sum_{k=0}^{K-1} \int_{\theta_k}^{\theta_{k+1}} \left(\frac{\theta_k + \theta_{k+1}}{2} - x \right)^2 dx \tag{15}$$

$$= \frac{1}{12} \sum_{k=0}^{K-1} (\theta_{k+1} - \theta_k)^3. \tag{16}$$

For an ideal quantizer with $\theta_k = k\Delta, \Delta = 1/K$, we thus obtain the textbook formula $\mathrm{MSE} = 1/(12K^2)$ which underlies (4).

For random thresholds θ_k, we define the random variables $S_k = \theta_{k+1} - \theta_k$. In the limit of very many thresholds $(K \to \infty)$ that are uniformly distributed between 0 and 1, S_k is exponentially distributed with probability density $f(s) = \lambda e^{-\lambda s}$ for $s \geq 0$ (and $f(s) = 0$ for $s < 0$) and mean $\lambda^{-1} = 1/K$ (independent of k). From (16), the expected MSE is

$$\mathrm{E}[\mathrm{MSE}] = \frac{1}{12} \sum_{k=0}^{K-1} \mathrm{E}[S_k^3] \tag{17}$$

$$= \frac{1}{12} \sum_{k=0}^{K-1} \int_0^\infty s^3 f(s) \, ds. \tag{18}$$

The integral in (18) can be computed in closed form as

$$\int_0^\infty s^3 \lambda e^{-\lambda s} \, ds = [-\lambda^{-3} e^{-\lambda s} (6 + 6\lambda s + 3\lambda^2 s^2 + \lambda^3 s^3)]_0^\infty \tag{19}$$

$$= 6\lambda^{-3}. \tag{20}$$

Inserting this into (18) yields

$$\mathrm{E}[\mathrm{MSE}] = \frac{1}{2} K \lambda^{-3} \tag{21}$$

$$= \frac{1}{2K^2}. \tag{22}$$

Inserting (22) into (4) yields (5).

APPENDIX II
ASYMPTOTIC ANALYSIS OF DACS

Recall that $\mathcal{C}$ is the set of possible values of the output current

$$y = \gamma \sum_{n=1}^{N} s_n c_n \tag{23}$$

with fixed positive currents c_n and $s_n \in \{+1, -1\}$. Let $\theta_k, k = 0, 1, 2, 3, \ldots, 2^N - 1$, be the points in $\mathcal{C}$, which we assume to be ordered such that $\theta_k \leq \theta_{k+1}$.

A. Decomposition of MSE

Recall that the MSE (11) is

$$\mathrm{MSE} = \int_{-0.5}^{0.5} (y(x) - x)^2 \, dx. \tag{24}$$

If the interval between θ_k and θ_{k+1} lies in the interval $-0.5 \leq x \leq 0.5$, then its contribution to the integral (24) is

$$\mathrm{MSE}_k \triangleq \int_{\theta_k}^{\theta_{k+1}} (y(x) - x)^2 \, dx \tag{25}$$

$$= \int_{\theta_k}^{\bar{\theta}_k} (\theta_k - x)^2 \, dx + \int_{\bar{\theta}_k}^{\theta_{k+1}} (\theta_{k+1} - x)^2 \, dx \tag{26}$$

with $\bar{\theta}_k \triangleq (\theta_k + \theta_{k+1})/2$. Straightforward computation then yields

$$\mathrm{MSE}_k = \frac{1}{12}(\theta_{k+1} - \theta_k)^3. \tag{27}$$

B. Gaussian Approximation of Point Density in $\mathcal{C}$

In the subsequent analysis, we will assume, first, that $\mathcal{C}$ has 2^N different points, and second, that the density of points in $\mathcal{C}$ is Gaussian

$$\lambda(x) \triangleq \frac{2^N}{\sqrt{2\pi}\sigma_{\mathcal{C}}} e^{-x^2/(2\sigma_{\mathcal{C}}^2)}. \tag{28}$$

The first assumption is generically satisfied for general real $c_1, \ldots, c_N$. The second assumption may be justified by the central limit theorem [applied to (23)]. The assumption thus holds rigorously in the limit $N \to \infty$, but it yields surprisingly accurate results even for the small values of N considered in Section V.

The variance $\sigma_{\mathcal{C}}$ in (28) may be computed as follows. Let $s_1, \ldots, s_N$ be independent random variables that are uniformly distributed over $\{+1, -1\}$. Then

$$\sigma_{\mathcal{C}}^2 = \mathrm{Var}[y] \tag{29}$$

$$= \gamma^2 \sum_{n=1}^{N} c_n^2 \mathrm{Var}[s_n] \tag{30}$$

$$= \gamma^2 \sum_{n=1}^{N} c_n^2. \tag{31}$$

For fixed $c_1, \ldots, c_N$, we can thus compute γ from $\sigma_{\mathcal{C}}$ and vice versa.

C. Local Uniformity Assumption for Points in DAC Ensembles

We now consider an ensemble of "random" DACs (i.e., a random choice of $c_1, \ldots, c_N$) as, e.g., in Section V, and we are interested in the mean MSE over the ensemble. The difference $G_k \triangleq \theta_{k+1} - \theta_k$ then becomes a random variable.

The key assumption in our derivation is that these random variables G_k are exponentially distributed with mean $1/\lambda$ given by (28). This assumption amounts to local application of the global assumption in Appendix I and is essentially equivalent to assuming that the points θ_k in any small bin are uniformly distributed inside the bin.

With this assumption, the contribution to the MSE (24) of some bin of width Δ around x is

$$\mathrm{E}[\text{MSE in bin}] \approx \frac{1}{12}\mathrm{E}\left[\sum_{\text{points } \theta_k \text{ in bin}} G_k^3\right] \tag{32}$$

$$\approx \frac{1}{2}\mathrm{E}[\text{number of points in bin}]\,\lambda^{-3} \tag{33}$$

$$\approx \frac{1}{2}(\Delta\lambda)\lambda^{-3} \tag{34}$$

$$= \frac{1}{2}\Delta\lambda^{-2} \tag{35}$$

where the step to (33) follows from $\mathrm{E}[G_k^3] = 6\lambda^{-3}$, which we used and proved in Appendix I.

D. Total Expected MSE and Optimal Scaling

From (35), the expected value of the total MSE is

$$\mathrm{E}[\mathrm{MSE}] \approx \frac{1}{2}\int_{-0.5}^{0.5} \lambda(x)^{-2} \, dx. \tag{36}$$

Inserting (28) then yields

$$\mathrm{E}[\mathrm{MSE}] \approx 2^{-2N} 2\pi \, \sigma_{\mathcal{C}}^2 \int_0^{0.5} e^{x^2/\sigma_{\mathcal{C}}^2} \, dx \tag{37}$$

$$= 2^{-2N} 2\pi \, \psi(\sigma_{\mathcal{C}}) \tag{38}$$

with

$$\psi(\sigma_{\mathcal{C}}) \triangleq \sigma_{\mathcal{C}}^2 \int_0^{0.5} e^{x^2/\sigma_{\mathcal{C}}^2} \, dx. \tag{39}$$

By numerical minimization, we easily obtain

$$\min \psi(\sigma_{\mathcal{C}}) \approx 0.1476 \tag{40}$$

at

$$\sigma_{\mathcal{C}} \approx 0.361. \tag{41}$$

From (38), we obtain the effective resolution

$$\mathrm{Res}_{\mathrm{eff}} = -\log_2 \sqrt{12 \cdot \mathrm{E}[\mathrm{MSE}]} \tag{42}$$

$$\approx N - \frac{1}{2}\log_2(12 \cdot 2\pi \, \psi(\sigma_{\mathcal{C}})) \tag{43}$$

and inserting (40) yields

$$\mathrm{Res}_{\mathrm{eff}} \approx N - 1.738 \text{ bits}. \tag{44}$$

The approximations in (36) and (37) become exact in the limit of large N and large σ.

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Matthias Frey (S'01–M'06) received the M.Sc. degree in electrical engineering and the Ph.D. degree from ETH Zurich, Zurich, Switzerland, in 2001 and 2006, respectively.

He is currently a JSPS Postdoctoral Fellow with the Matsuzawa Laboratory, Tokyo Institute of Technology, Tokyo, Japan. His main research interests include nonlinear analog networks for decoding error correcting codes, corrected analog-to-digital and digital-to-analog converters, as well as mixed-signal chip design.

Hans-Andrea Loeliger (S'87–M'92–SM'03–F'04) received the Diploma degree in electrical engineering and the Ph.D. degree from ETH Zurich, Zurich, Switzerland, in 1985 and 1992, respectively.

He has been a Professor with ETH Zurich since 2000. From 1992 to 1995, he was with Linköping University, Linköping, Sweden. From 1995 to 2000, he was with Endora Tech AG, Basel, Switzerland, which he cofounded. His research interests lie in the broad areas of signal processing, information theory, communications, system theory, and electronics.