Circuit-Based Characterization of Device Noise Using Phase Noise Data

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***Abstract*—A circuit-based device noise characterization technique is introduced which uses phase noise data to estimate the power spectral density (PSD) of high-frequency noise in MOSFETs. To apply this technique to a typical CMOS process, an oscillator structure is introduced which provides a predictable phase noise level for a given device noise PSD. The analytical equations governing the phase noise of this oscillator are presented and subsequently verified using circuit simulations. Three oscillators, using transistors of various channel lengths, are fabricated in a commercial 0.18 μm CMOS process technology to study short-channel excess noise. It is shown that, at equal current levels, the noise PSD in minimum-channel-length transistors is 8.7 dB larger than that in 3$\times$-minimum-channel-length devices. The proposed method is especially suitable for applying to a state-of-the-art CMOS process to provide a quantitative analysis of various noise tradeoffs which are sometimes missing in foundry-provided models.**

***Index Terms*—Device characterization, excess noise, integrated oscillator, jitter, MOSFET, noise, phase noise, ring oscillator, short-channel effects.**

I. Introduction

UNDERSTANDING noise in electronics is an important problem for integrated systems. The analysis of noise in these systems starts with a careful characterization of noise in the devices comprising them using physical and empirical models. Once these noise sources are sufficiently characterized, the analysis of noise at the circuit and system levels is performed using well-developed mathematical methods. Therefore, accurate characterization of device noise is arguably the most challenging task in noise analysis. These challenges have made physical modeling of device noise an active research topic for several decades since the pioneering work of J. B. Johnson [1].

After the commercialization of MOSFETs in the early 1960s, extensive investigations were launched that helped designers understand major MOSFET noise sources in less than a decade. These investigations revealed that there are two partially correlated noise sources in every MOSFET: channel thermal noise [2] and induced gate noise [3]. By 1970, the classical formulation of MOSFET noise was finalized [4]. In 1986, Jindal [5] and Abidi [6] suggested that the classical noise model underestimates noise power spectral density (PSD) in short-channel devices. Since then, several studies have tried to replicate those results or theoretically explain this phenomenon. These investigations have led to different (and sometimes conflicting) results for MOSFET noise behavior (see for example [7]–[9]).

One of the major difficulties in the way of reaching a unified noise model for short-channel MOSFETs is experimental verification. Measuring device noise is usually a difficult process; it requires careful de-embedding of parasitic elements as well as accurate control of environmental parameters.

Fortunately, direct device noise measurement is not the only way of estimating noise PSD in an electronic component. This paper introduces a circuit-based technique for MOSFET noise characterization based on phase noise measurement. This technique facilitates quantitative analysis of device noise tradeoffs because, when proper design prevents parasitic Q-loading effects, phase noise is simpler and faster to measure than amplitude noise. The organization of this paper is as follows. Section II introduces the proposed technique and discusses its advantages and limitations. Section III covers an actual implementation by introducing an asymmetrical ring oscillator and the analytical formulation of its phase noise which are subsequently verified using circuit simulations. Section IV concludes this paper by presenting device noise data for a commercial 0.18 μm CMOS process. Although some parts of the work have been briefly reported in [10] and [11], our work on the analytical formulation of phase noise, simulation results and interpretation of the experimental data are presented here in greater detail.

II. Circuit-Based Characterization of Device Noise

To circumvent the aforementioned difficulties in noise measurement, it is desirable to indirectly estimate noise PSD in electronic devices through characterization of a more readily measured physical quantity. One such quantity is the phase noise of an oscillator. The measurement of phase noise of an electrical oscillator is often relatively easy to perform and the results are usually quite accurate. This is because the phase noise of an oscillator is mainly set by the noise sources and electrical components "inside" the oscillation loop. Thus, most off-chip parasitic elements do not have a significant effect on the phase noise of integrated oscillators. Furthermore, phase noise measurement is a comparative measurement between the signal power at the center frequency and that at a small offset frequency [12]. Therefore, the effects of many parasitic elements such as cable loss and impedance mismatch are significantly canceled out, greatly reducing the number of non-idealities in phase noise measurement and making it faster and less costly to perform.

Manuscript received February 24, 2009; revised June 29, 2009; accepted August 16, 2009. First published December 28, 2009; current version published June 09, 2010. This work is supported under an SRC customized research project from Texas Instruments and MARCO MSD center. This paper was recommended by Associate Editor A. M. Klumperink.

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Digital Object Identifier 10.1109/TCSI.2009.2033535

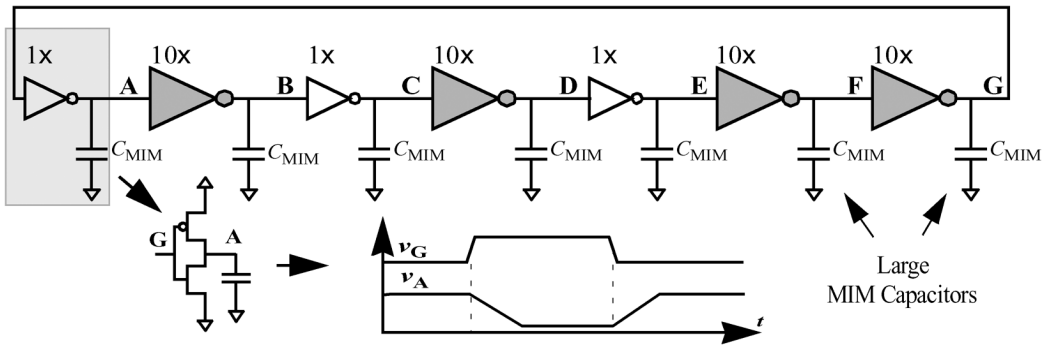

Fig. 1. An asymmetrical ring oscillator for indirect characterization of device noise through phase noise measurement.

In order to perform indirect characterization of device noise from phase noise data, it is crucial to have the relationship between device noise and phase noise for the given oscillator. In general, accurate formulation of phase noise for an arbitrary oscillator is quite complicated. Nevertheless, it is possible to design an oscillator with predictable (but not necessarily low) phase noise. The relationship between device noise and phase noise for this oscillator can then be obtained analytically. Once such an oscillator is at hand, it is straightforward to measure its phase noise using well-developed techniques and back-calculate noise PSD in the devices used in the oscillator.

The proposed technique is faster and easier to perform than direct noise measurement. However, it is worth mentioning here that the convenience provided by this indirect characterization technique comes at the cost of inferior absolute accuracy of the final numbers. Because of the indirect nature of the proposed technique, the result is sensitive to the approximations used in the formulation of phase noise. Nevertheless, as we will see shortly, this technique is quite effective for obtaining an accurate comparison between the PSD of the noise generated by various devices fabricated using the same process technology. The unfavorable effect of indirect measurement is likely to cancel out in such a comparative study. This level of accuracy suffices in many practical applications and provides practical guidelines for low-noise analog design.

In the following section, we introduce an oscillator with predictable phase noise. This oscillator is used as a vehicle for indirect device noise characterization. Note that the focus of this work is the high-frequency noise in the drain current of short-channel MOSFETs. Thus, all of the presented phase noise formulations neglect the low-frequency $1/f$ noise of the device. Parallel to that, phase noise measurements are performed at higher frequencies where phase noise drops at the rate of 20 dB per decade. It is well known that the level of phase noise in this region is fairly independent of low-frequency $1/f$ noise in the circuit [12]. Also note that the effect of the induced gate noise on the phase noise of the oscillators used in this work is negligible.

III. Implementation

A. Noise-Driven Oscillator Design

Indirect characterization of device noise through phase noise measurement calls for an oscillator with predictable phase noise. Fig. 1 shows one such oscillator designed for this study, hereafter referred to as the asymmetrical ring oscillator. Our asymmetrical ring oscillator is composed of seven inverters capacitively loaded with large metal–insulator–metal (MIM) capacitors. These capacitors are large enough to swamp the total capacitance of all internal nodes of the oscillator. Therefore the total capacitance on all internal nodes is linear, has a high quality factor and is fairly independent of temperature and device parasitic components. In order to read the signal off-chip, an inverter chain is used whose first stage is small enough to contribute negligible capacitance compared to the added MIM cap. Proper design of this inverter chain also insures that the amplitude noise is suppressed due to clamping.

The seven inverters which comprise the oscillation loop are sized differently, hence the name asymmetrical. There are three $1\times$ and four $10\times$ inverters in the oscillation loop. With the loading capacitors being the same, the voltage at the outputs of the large inverters changes much more rapidly than that at the outputs of small inverters. Thus the frequency of oscillation is mainly determined by the small inverters. Furthermore, because of the faster voltage rate of change, the noise of large inverters has a much smaller effect on the phase noise of the oscillator. This is because the variance of the switching instance at each stage is inversely proportional to the square of the voltage rate of change at its output. Therefore, even though current noise PSD at the output of the large inverters is approximately ten times larger than that at the output of the small inverters, their jitter contribution is ten times smaller because of the faster voltage rate of change.

Also note that the gate to source voltage of the transistors in small inverters is nearly constant for the duration of charging (and discharging) of the capacitors at their outputs. This is because the large inverters discharge (and charge) their output nodes much faster than the small inverters. Since these nodes are the inputs to the small inverters, the gate to source voltage of the transistors in these inverters stays relatively constant during most of the charge and discharge time. This means that the biasing condition of the transistors whose noise PSD sets oscillator's phase noise is nearly constant during their active time. This is an important virtue of this oscillator which simplifies the formulation of equations to estimate phase noise and makes it possible to characterize device noise at a given bias voltage.

B. Analytical Formulation of Phase Noise

Frequency stability in ring oscillators has been extensively studied since the introduction of these circuits (e.g. [13]–[16]).

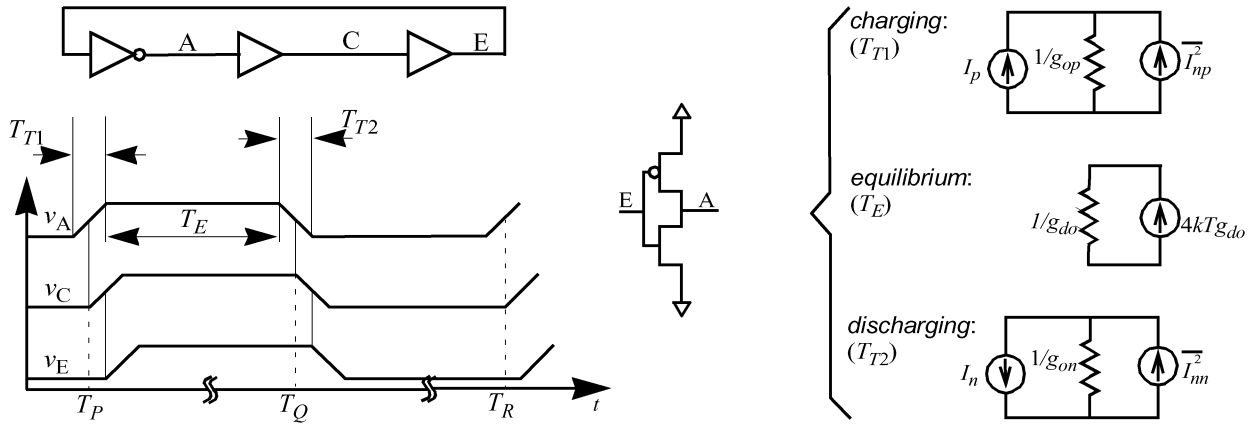

Fig. 2. Simplified model of the oscillator of Fig. 1 suitable for phase noise analysis. The length of T_E is exaggerated for better readability.

In this work, we use a method that is tailored for the oscillator of Fig. 1. To calculate the phase noise of this oscillator, we model it as a switching-based oscillator in which the energy injecting elements have a countable number of states and the transitions between these states can be considered instantaneous. Since the $10\times$ stages are significantly faster than $1\times$ stages, we neglect their effect on the oscillation frequency and phase noise. Fig. 2 shows a simplified model for the oscillator. As required by the switching-based oscillator model, each of the small inverters is assumed to have only three distinct states: *charging*, *discharging* and *equilibrium*. In its *charging* state (T_{T1}), the PMOS transistor is assumed to deliver a constant current of I_p. In this state, the inverter's output resistance and noise PSD are $1/g_{op}$ and $\overline{I_{np}^2}$, respectively. In its *discharging* state (T_{T2}), the NMOS transistor is assumed to sink a constant current of I_n. In this state, the inverters's output resistance and noise PSD are $1/g_{on}$ and $\overline{I_{nn}^2}$, respectively. During *charging* and *discharging* states, the inverter's current, output resistance and noise PSD are assumed to be independent of the output voltage.[1] In its *equilibrium* state (T_E), one of the devices in the inverter is in equilibrium while the other device is turned off. In this state, the inverter can be replaced by a noisy resistor.[2] The moment at which an inverter moves from one state to another is referred to as a switching instance.

To calculate phase noise, we use the approach presented in [11]: first we calculate jitter in the time domain and then convert that to the frequency domain to find phase noise. To calculate jitter, we first calculate the variance of each switching instance. We then add up the variances of all switching instances in one period of oscillation (assuming probabilistic independence) to find the total variance of the duration of one period, hereafter referred to as the period jitter. In order to calculate the variance of a switching instance, we first find the variance of the respective control voltage at the nominal switching moment and then divide that by the square of the voltage rate of change on that node. The rest of this subsection presents the mathematical derivations of phase noise using this approach.

There are six switching instances in each period of oscillation. In order to calculate the variance of the switching instance T_Q, we first need to calculate the variance of $v_{\rm A}$ at that time. It can be shown that the variance of the voltage across a capacitor $C_{\rm MIM}$ (C for brevity) connected in parallel with a resistor R and a current noise source with a PSD of $\overline{I_n^2}$ after time t is given by [11]

$$\overline{\Delta v_A^2(t)} = \frac{\overline{I_n^2}R}{4C}\left(1 - e^{-\frac{2t}{RC}}\right) + \sigma_o^2 e^{-\frac{2t}{RC}} \tag{1}$$

where σ_0^2 is the variance of v_A at time $t = 0$, k is Boltzmann constant and T is the absolute temperature. To calculate the variance of v_A at T_Q, we can break the time interval between T_P and T_Q into three regions: the second half of T_{T1} (*charging* state), T_E (*equilibrium* state) and the first half of T_{T2} (*discharging* state). We can then replace the inverter with its simplified model in each of these regions, assume $\overline{\Delta v_A^2(T_P)} = 0$, and use (1) consecutively to calculate $\overline{\Delta v_A^2}$ at T_Q.

Fortunately, certain approximations can be used to simplify this analysis. Namely, during the equilibrium time T_E the circuit's time constant (RC) is C/g_{dop} which is a small number since the PMOS device is in linear region. According to (1), if the equilibrium time T_E is much longer than the circuit time constant in this region (a condition which is usually satisfied), $\overline{\Delta v_A^2}$ at the end of this time interval is independent of its variance at the end of T_{T1} and is given by

$$\overline{\Delta v_A^2(T_P + T_{T1}/2 + T_E)} = \frac{\overline{I_{npTE}^2}}{4Cg_{dop}} \tag{2}$$

where $\overline{I_{npTE}^2}$ and g_{dop} are the noise PSD and output conductance of the PMOS transistor during T_E.

Other approximations are possible during the first half of T_{T2}. In this region, the output impedance of the inverter is $1/g_{on}$ which is normally a large number (the NMOS device is in saturation region). Assuming that $T_{T2}/2$ is much smaller than C/g_{on} during this time, we can replace the exponential

[1]These assumptions are best satisfied during the first half of T_{T1} and T_{T2}. These regions are indeed where we use these assumptions.

[2]The word "equilibrium" is used according to its thermodynamical definition. Based on this definition, a MOSFET is in equilibrium when $v_{bs} = v_{ds} = I_{ds} = 0$. There are, in fact, two distinguishable *equilibrium* states for the inverter: one in which the NMOS transistor conducts and one in which the PMOS transistor conducts. This fact has been taken into account in the presented formulation.

TABLE I
DESIGN PARAMETERS FOR THE SEVEN ASYMMETRICAL RING OSCILLATORS USED FOR SIMULATION-BASED VERIFICATION OF THE ACCURACY OF THE PHASE NOISE PRESENTED FORMULATION

Oscillator Number	L_{n_small} (μm)	W_{n_small} (μm)	L_{p_small} (μm)	W_{p_small} (μm)	L_{n_large} (μm)	W_{n_large} (μm)	L_{p_large} (μm)	W_{p_large} (μm)	Process
OSC1	0.18	0.28	0.18	0.56	0.18	2.8	0.18	5.6	TSMC
OSC2	0.25	0.4	0.25	0.8	0.25	4	0.25	8	
OSC3	0.18	0.28	0.18	0.56	0.18	2.8	0.18	5.6	IBM SiGe
OSC4	0.25	0.4	0.25	0.8	0.25	4	0.25	8	
OSC5	0.13	0.2	0.13	0.4	0.13	2	0.13	4	IBM CMOS
OSC6	0.18	0.28	0.18	0.56	0.18	2.8	0.18	5.6	
OSC7	0.25	0.4	0.25	0.8	0.25	4	0.25	8	

terms in (1) with their series expansion. The variance of v_A at T_Q is then given by

$$\overline{\Delta v_A^2(T_Q)} = \frac{\overline{I_{nn}^2} T_{T2}}{4C^2} + \frac{\overline{I_{npTE}^2}}{4Cg_{dop}} \tag{3}$$

where we have used $t = T_{T2}/2$, $\overline{\sigma_0^2} = \overline{I_{npTE}^2}/(4Cg_{dop})$ and $t \ll RC$ in (1). In (3), $\overline{I_{nn}^2}$ is the noise PSD of the NMOS transistor during the first half of T_{T2}. To further simplify (3), note that T_{T2} can be written as

$$T_{T2} = \left(\frac{2T_o}{3}\right) \cdot \left(\frac{I_p}{I_n + I_p}\right) \tag{4}$$

where $T_o = 1/f_o$ is the oscillation period and I_p and I_n are the dc currents of PMOS and NMOS during charging and discharging the load capacitor (C_{MIM}), respectively. Using (4) in (3) we get

$$\overline{\Delta v_A^2(T_Q)} = \frac{\overline{I_{nn}^2} I_p}{6f_o C^2 (I_n + I_p)} + \frac{\overline{I_{npTE}^2}}{4Cg_{dop}}. \tag{5}$$

To find the variance of the switching instance at T_Q, we divide $\overline{\Delta v_A^2(T_Q)}$ by the square of the voltage rate of change which is I_n/C to get

$$\overline{\Delta T_{sQ}^2} = \frac{\overline{I_{nn}^2} I_p}{6f_o I_n^2 (I_n + I_p)} + \frac{\overline{I_{npTE}^2} C}{4g_{dop} I_n^2}. \tag{6}$$

Similarly, the variance of the switching instance at T_R is given by

$$\overline{\Delta T_{sR}^2} = \frac{\overline{I_{np}^2} I_n}{6f_o I_p^2 (I_n + I_p)} + \frac{\overline{I_{nnTE}^2} C}{4g_{don} I_p^2}. \tag{7}$$

To find period jitter, we note that there are three independent switching jitters of the type of $\overline{\Delta T_{sQ}^2}$ and three independent switching jitters of the type of $\overline{\Delta T_{sR}^2}$ in each period of oscillation. Thus the total period jitter is

$$\overline{\Delta T_o^2} = \frac{1}{2f_o(I_n + I_p)} \cdot \left(\frac{\overline{I_{nn}^2} I_p}{I_n^2} + \frac{\overline{I_{np}^2} I_n}{I_p^2}\right) + \frac{3C}{4}\left(\frac{\overline{I_{npTE}^2}}{g_{dop} I_n^2} + \frac{\overline{I_{nnTE}^2}}{g_{don} I_p^2}\right). \tag{8}$$

Finally, phase noise at an offset frequency of Δf (assuming Δf is large enough to ignore the contribution of $1/f$ noise on phase noise) is given by [17]

$$PN(\Delta f) = \frac{f_o^2}{2(\Delta f)^2 (I_n + I_p)}\left(\frac{\overline{I_{nn}^2} I_p}{I_n^2} + \frac{\overline{I_{np}^2} I_n}{I_p^2}\right) + \frac{3Cf_o^3}{4(\Delta f)^2}\left(\frac{\overline{I_{npTE}^2}}{g_{dop} I_n^2} + \frac{\overline{I_{nnTE}^2}}{g_{don} I_p^2}\right). \tag{9}$$

The foregoing analysis uses several simplifying assumptions about the behavior of 1× inverter stages. Namely, the interstage noise effects are neglected. That is, variations of the voltage on node A do not affect the voltage on node B regardless of the inverter's state. Furthermore, first crossing approximation is used which assumes that each stage switches to a new state as soon as its input reaches a certain switching level for the first time [18]. For simplicity we also assumed that each inverter switches its state when its input voltage reaches $vdd/2$. This can be achieved by proper sizing of NMOS and PMOS transistors. The validity of these simplifying assumptions and the accuracy of the presented formulation is verified in the following section using circuit phase noise simulations.

C. Verification of the Model

Seven asymmetrical ring oscillators of the type shown in Fig. 1 are designed to verify the accuracy of the presented formulation using SpectreRF phase noise simulations. The design parameters are shown in Table I. Seven different fabrication process models at 0.25 μm, 0.18 μm and 0.13 μm technology nodes are utilized.

All inverters in all three oscillators are loaded by an ideal capacitor of $C_{\mathrm{MIM}} = 500$ fF which is significantly larger than the parasitic capacitance of the transistors. Thus the loading capacitance is, to the first order, the same in these oscillators. Using circuit simulation, we have estimated the parasitic capacitance at internal nodes by increasing the loading capacitance to $2C_{\mathrm{MIM}}$ and taking note of the frequency change. The effective value of the parasitic capacitance can be found using the following equation:

$$\frac{C_{parasitic} + C_{MIM}}{C_{parasitic} + 2C_{MIM}} = \frac{f_{osc-new}}{f_{osc-old}} \tag{10}$$

TABLE II
DEVICE PARAMETERS AND PHASE NOISE NUMBERS FOR THE SEVEN ASYMMETRICAL RING OSCILLATORS. PHASE NOISE IS GIVEN AT 1 MHz OFFSET FREQUENCY AT $\mathrm{T} = 60^{\circ}\mathrm{C}$

	Device Type	v_{dd} (V)	I_n, I_p (μA)	g_{do} (μS)	$\overline{I_n^2}$ in saturation (A^2/Hz)	$\overline{I_n^2}$ in triode (A^2/Hz)	Simulated f_{osc} (MHz)	Calculated Phase Noise (dBC/Hz)	Simulated Phase Noise (dBC/Hz)
OSC1 TSMC.18	NMOS	1.8	206	593	1.02e-23	1.34e-23	37.6	-127.6	-127.9
	PMOS		147	247	3.6e-24	6.11e-24			
OSC2 TSMC.25	NMOS	2.5	240	403	7.11e-24	8.74e-24	33.5	-131.1	-131.2
	PMOS		182	173	3.13e-24	5.28e-24			
OSC3 IBMSiGe.18	NMOS	1.8	192	478	1.04e-23	1.38e-23	30.1	-128.1	-128.6
	PMOS		102	179	2.61e-24	4.62e-24			
OSC4 IBMSiGe.25	NMOS	2.5	215	427	7.23e-24	8.91e-24	31.8	-130.3	-130.9
	PMOS		181	205	4.82e-24	7.0e-24			
OSC5 IBMC-MOS.13	NMOS	1.3	99	260	5.51e-24	7.25e-24	25.2	-126.3	-126.2
	PMOS		67	152	2.54e-24	4.06e-24			
OSC6 IBMC-MOS.18	NMOS	1.8	150	374	5.97e-24	7.93e-24	31.0	-128.8	-128.8
	PMOS		126	201	2.82e-24	5.01e-24			
OSC7 IBMC-MOS.25	NMOS	2.5	214	549	7.99e-24	9.35e-24	34.3	-129.9	-130.3
	PMOS		208	234	4.97e-24	7.09e-24			

TABLE III
DESIGN PARAMETERS FOR THREE FABRICATED ASYMMETRICAL RING OSCILLATORS

Oscillator Number	L_{n_small} (μm)	W_{n_small} (μm)	L_{p_small} (μm)	W_{p_small} (μm)	L_{n_large} (μm)	W_{n_large} (μm)	L_{p_large} (μm)	W_{p_large} (μm)	C_{MIM}+$C_{paras.}$ (fF)
OSC8	0.18	0.28	0.18	0.56	0.18	2.8	0.18	5.6	525
OSC9	0.38	0.56	0.38	1.12	0.38	5.6	0.38	11.2	570
OSC10	0.54	0.84	0.54	1.68	0.54	8.4	0.54	16.8	625

where $f_{osc-old}$ and $f_{osc-new}$ are the oscillation frequencies before and after increasing the loading capacitance, respectively. The calculated value of total capacitance is 525 fF for TSMC 0.18-μm process (OSC1). The same number is used for the other oscillators as the variation is small.

In order to calculate phase noise using the presented formulation, several device parameters are needed. Table II shows some of the simulated device parameters for the devices used in these oscillators. BSIM3 models are used with HSPICE simulator and v_{dd} is set to 1.3 V, 1.8 V and 2.5 V for 0.13 μm, 0.18 μm and 0.25 μm processes respectively.[3] Table II also shows the calculated phase noise obtained by using these device parameters in (9) as well as the simulated phase noise using SpectreRF.[4] In order to see the effect of white noise, the $1/f$ noise power is set to zero in the models. As can be seen in this table, phase noise numbers calculated using (9) are within 1 dB of the numbers obtained from SpectreRF phase noise simulations. This level of accuracy corresponds to 1 dB accuracy in device noise power.[5]

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Oscillator Design

Three asymmetrical ring oscillators of the type shown in Fig. 1 are fabricated in a 0.18-μm CMOS process and used to extract MOSFET noise parameters from experimental phase noise data. In order to highlight excess noise in short-channel devices, these oscillators use transistors with various channel lengths. The sizings of transistors are shown in Table III. The width-to-length ratio has been kept constant to ensure comparable oscillation frequencies. This helps to cancel out the effect of the approximations used in our phase noise formulation when the final device noise numbers are compared to each other. The transistors are built with multiple gate fingers to minimize gate resistance noise. In all cases, the noise PSD of

[3]Model parameters for these processes are obtained from MOSIS web site (publicly available). Due to a nondisclosure agreement with the foundry, we cannot present numerical values of the device parameters for the fabricated oscillators.

[4]Phase noise is calculated based on the definition of power spectral density of the signal divided by the power of the first harmonic. The simulated signal level at the first harmonic is around 1 dBV, -2 dBV and -5 dBV for the 0.25 μ, 0.18 μ and 0.13 μ oscillators, respectively. The difference is mainly due to the difference in supply voltage.

[5]The numbers in Table II are based on models that do not take into account excess noise in short-channel devices. Thus the difference between the simulated phase noise of these oscillators can be explained based on their power consumption. Similarly, the calculated phase noise numbers are based on transistor current noise power obtained from the same models and follow the same trend. This does not affect the purpose of Table II which is to validate (9).

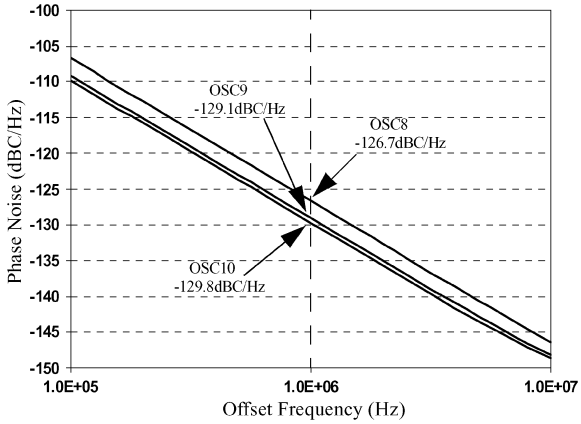

Fig. 3. Simulated phase noise of the three asymmetrical ring oscillators.

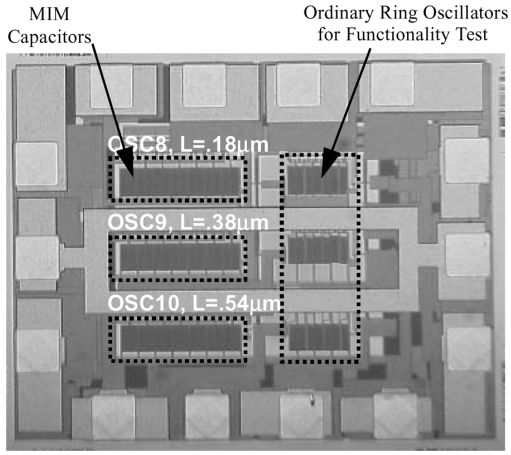

Fig. 4. Die photo of the three asymmetrical ring oscillators.

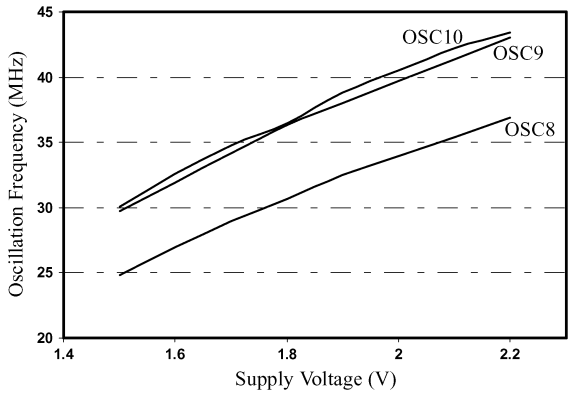

Fig. 5. Measured oscillation frequency versus supply voltage for the three fabricated oscillators.

the gate resistance is at least an order of magnitude smaller than that of the device noise, according to the models.

Inverters in all three oscillators are loaded by similar MIM capacitors of a nominal value of 500 fF which is significantly larger than the parasitic capacitance of the transistors. Using (10), we have estimated the parasitic capacitance at the internal nodes of the oscillator. The calculated values of total capacitance are given in Table III.

The simulated phase noise of the three oscillators using SpectreRF with BSIM3.3 models is shown in Fig. 3. In order to see the effect of white noise, $1/f$ noise power is set to zero in the models. That is why phase noise drops at a constant rate of 20 dB/dec.

To examine the accuracy of our assumption of neglecting large inverter stages on the phase noise of the oscillator, we simulate the phase noise once with $3\times$ more noise power on all MOS devices of OSC8 and once with $3\times$ more noise only on the MOS devices of the large inverters in this oscillator. With $3\times$ more noise on all devices, the simulated phase noise degrades by 4.8 dB as expected. With $3\times$ more noise only on the devices of the large inverters, the simulated phase noise degrades by 0.8 dB (20% increase). Therefore, the large inverters are responsible for nearly 10% of the total noise of the oscillators.

B. Measurement Results and Discussions

Fig. 4 shows a photo of the die carrying these oscillators. Fig. 5 shows the graph of oscillation frequency versus supply voltage. As can be seen in this figure, the oscillation frequency of OSC8 is nearly 20% lower than that of the other two oscillators. Unfortunately, we do not have an explanation for this result at this point (most likely caused by second order effects) but this frequency difference does not affect the final result significantly. A comparison between these measured curves and simulated oscillation frequencies reveals that the devices on this chip are best modeled by the Typical corner of the Spice model files. Later, we will use simulated drain current (using parameters from the Typical corner) to calculate device noise PSD from phase noise data.

The phase noise of the three oscillators is measured using an HP8563 spectrum analyzer equipped with a phase noise measurement module. In order to make sure that the oscillators' phase noise is not dominated by supply noise, measurements are performed once using an electronic supply generator unit and once using a battery followed by a regulator with heavy filtering. Since the change of the supply did not cause any significant change in phase noise, it was concluded that supply noise does not have a significant effect on phase noise. Figs. 6, 7 and 8 show the phase noise of the three oscillators with a typical supply voltage of 1.8 V. As can be seen in these figures, the oscillators with longer transistors have smaller phase noise. This is expected because of the smaller noise PSD in these devices [5], [6]. All of the phase noise measurements are performed at an offset frequency of 1 MHz from the center frequency. Figs. 6, 7 and 8 confirm that, for all three oscillators, this offset frequency is located in the region where phase noise drops at the rate of 20 dB per decade. The effect of $1/f$ noise is thus insignificant and the phase noise at this offset frequency is predominantly set by the power in the white region of noise spectrum.

Comparing the measured phase noise numbers presented in Figs. 6–8 to the ones presented in Fig. 3 shows that the provided BSIM3.3 model underestimates phase noise by 8.3 dBC/Hz, 7.1 dBC/Hz and 4.3 dBC/Hz for OSC8, OSC9 and OSC10, respectively. This underestimation is an indication of inaccuracy in device noise parameters especially for minimum channel length transistor. In order to quantitatively characterize noise parameters at various channel lengths using phase noise data, we use the formulation presented in Section III along with the experimental phase noise data of Figs. 6, 7 and 8. In order to simplify (9), we first take note of the fact that, according to the fluctuation-dissipation theorem of thermodynamic, during the

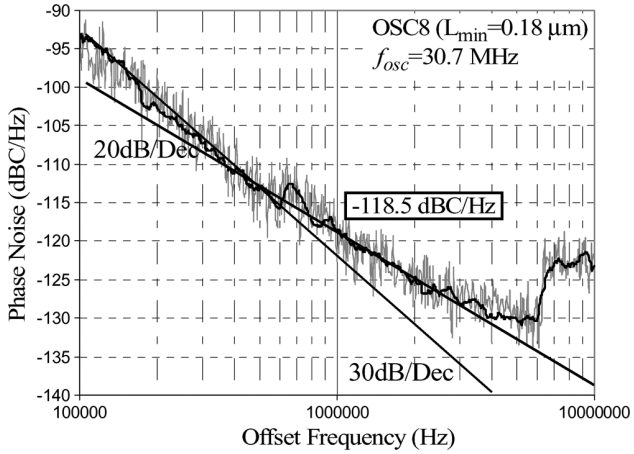

Fig. 6. Phase noise of OSC8 ($\mathrm{L_{min}} = 0.18$ m) at $v_{gs} = 1.8$ V.

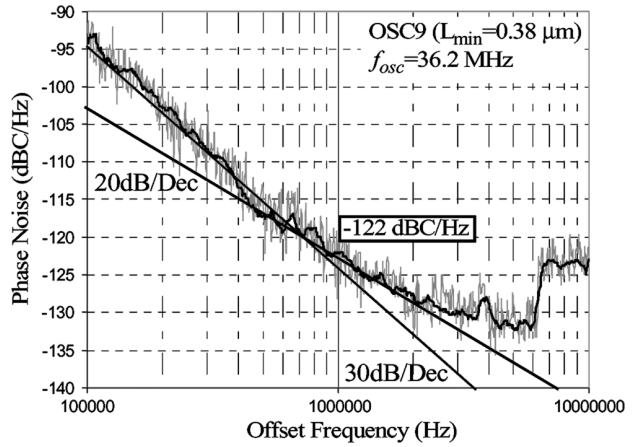

Fig. 7. Phase noise graph for OSC9 ($\mathrm{L_{min}} = 0.38$ m) at $v_{gs} = 1.8$ V.

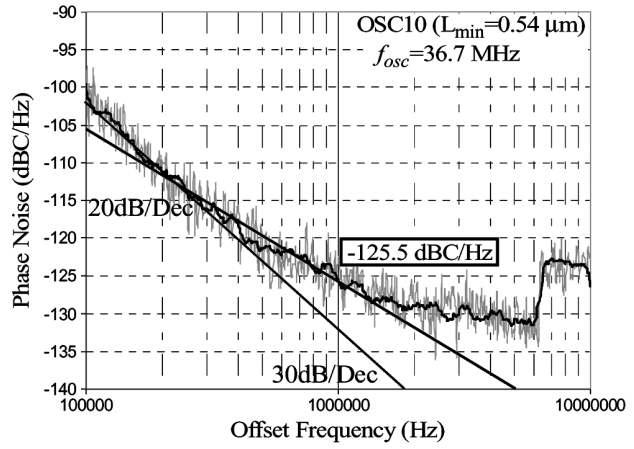

Fig. 8. Phase noise graph for OSC10 ($\mathrm{L_{min}} = 0.54\ \mu$) at $v_{gs} = 1.8$ V.

equilibrium time T_E, the noise PSD in the NMOS and PMOS devices are given by $4kTg_{don}$ and $4kTg_{dop}$, respectively. If we further assume that the current flow in NMOS and PMOS transistors are nearly equal and equal to I_{dc} ($I_n = I_p = I_{dc}$ through proper device sizing), (9) can be simplified to

$$PN(\Delta f) = \frac{f_o^2}{4I_{dc}^2(\Delta f)^2}\left(\overline{I_{nn}^2} + \overline{I_{np}^2}\right) + \frac{6kTCf_o^3}{I_{dc}^2(\Delta f)^2} \quad (11)$$

which after solving for $\overline{I_{nn}^2} + \overline{I_{np}^2}$ gives

$$\overline{I_{nn}^2} + \overline{I_{np}^2} = 4I_{dc}^2(\Delta f)^2 PN(\Delta f)/f_o^2 - 24kTCf_o. \quad (12)$$

In order to find the total noise PSD ($\overline{I_{nn}^2} + \overline{I_{np}^2}$) we use (12) along with the value of I_{dc} from simulation results (Spice models at Typical corner) and the values of f_o and $PN(\Delta f)$ from the measurements. For a supply voltage of 1.8 V ($v_{gs} = 1.8$ V), in this 0.18 μ CMOS process, total drain current noise PSD (NMOS+PMOS) is $1.14\mathrm{e}-22\ \mathrm{A}^2/\mathrm{Hz}$, $3.39\mathrm{e}-23\ \mathrm{A}^2/\mathrm{Hz}$, and $1.52\mathrm{e}-23\ \mathrm{A}^2/\mathrm{Hz}$ at 0.18 μ, 0.38 μ, and 0.54 μ channel length, respectively. Note that although the absolute accuracy of these numbers is affected by several sources of error inherent to our indirect noise measurement approach, the relative accuracy can be used with a higher confidence. This is because, most of these errors are common between the three oscillators and hence they cancel out when the numbers are compared to each other.

Although the presented experiment provides the total drain current noise PSD (NMOS+PMOS), it also possible to individually calculate the noise of NMOS and PMOS devices through a similar experiment. In such an experiment, one needs to build two asymmetrical oscillators of the type shown in Fig. 1 with different NMOS to PMOS ratios. It will then be possible to use (9) for the two oscillators and solve the two equations for $\overline{I_{nn}^2}$ and $\overline{I_{np}^2}$. Unfortunately, at the time of this submission, such structures are not available to us.

According to the presented data, in this process, total noise PSD can be reduced by nearly 5.3 dB and 8.7 dB by increasing the channel length of the transistors from minimum channel length to 2× and 3× minimum channel length, respectively (at a constant width over length ratio). Measurements of the oscillation frequency (as well as simulation results) show that the total current (hence power consumption) will stay nearly constant under this transformation.

In many applications, speed requirements limit the maximum channel length that can be used for a certain circuit. Nevertheless, if the speed requirement is not the limiting factor, long-channel transistors should be used as much as possible to minimize noise PSD. This recommendation is consistent with the general wisdom: For optimum noise operation, a circuit should be only as fast as needed and not any faster than that.

In practice, some foundries prohibit the use of transistors with longer than minimum channel length. In some cases, the accuracy of the models is not guaranteed for devices with longer-than-minimum channel lengths and/or the matching between these devices is not as well controlled as between minimum-channel-length devices. In these cases, potential circuit impairments should be carefully studied before a decision is made on using long-channel devices. In some cases, the use of stacked devices, as a way to emulate longer transistors, can be an attractive alternative.

V. Conclusions

A circuit-based method is introduced for indirect characterization of device noise using phase noise data. Compared to amplitude noise, phase noise is often easier to measure and less sensitive to measurement non-idealities and environmental conditions. We presented an asymmetrical oscillator with

predictable phase noise to back-calculate the noise PSD of MOSFETs from measured phase noise data. The analytical formulation of phase noise for this oscillator is presented and subsequently verified using circuit simulations. Using this oscillator, drain noise PSD in transistors of various channel lengths fabricated in a commercial 0.18 μ CMOS process is estimated from measured phase noise data. According to this data, the drain current noise can be reduced by nearly 8.7 dB by using 3$\times$ minimum channel length device instead of minimum-channel-length device if permitted by speed requirement and foundry rules. The introduced method can be used for in-house noise characterization of state-of-the-art devices when foundry models lack reliable noise data.

ACKNOWLEDGMENT

The authors would like to thank S. S. Mohan of Magma Design Automation for enlightening discussions.

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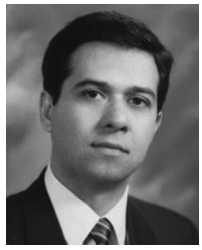

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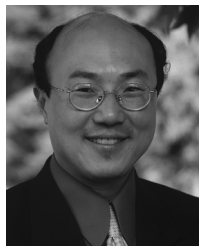

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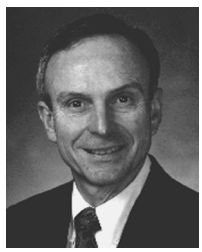

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