Guest Editorial
Special Section on the 2013 IEEE Custom Integrated Circuits Conference (CICC 2013)

THIS Special Section of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS consists of expanded versions of twelve papers presented at the Custom Integrated Circuits Conference (CICC), held in San Jose, CA, USA, in September 2013. These papers were selected among those which belong to the area of interest of TCAS-I and which demonstrated the highest quality according to the feedback and scores given by CICC TPC members. The submitted follow-up manuscripts were peer reviewed and a final selection was done based on the results of the review process. This section complements the special issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. The papers are briefly described below and organized according to their main topics. The guest editors thank the authors for their contribution and the reviewers for their prompt feedback.

I. ANALOG AND RF CIRCUITS

The first two papers of this section deal with analog modeling techniques. In the first one, Krishnapura and Rakshitdatta, from Indian Institute of Technology Madras, describe a technique for the efficient simulation of per-element distortion contributions in weakly nonlinear circuits. In the second paper, Liao and Horowitz, from Stanford University, present a Verilog piecewise-linear behavior model for an accurate and fast simulation of analog and mixed-signal circuits. Both papers show several circuit examples as demonstration vehicles.

In the third paper, Tripathi and Murmann, from Stanford University, present a test structure and mismatch characterization of metal fringe capacitors in 32-nm SOI CMOS. Measurements for these capacitors confirm area scaling according to Pelgrom's matching formula.

In the next paper, Sun *et al.*, from Carnegie Mellon University, propose a novel indirect performance sensing technique for on-chip self-healing of analog and RF circuits to accurately measure various performance metrics. A 25-GHz differential Colpitts VCO designed in 32-nm SOI CMOS is used to validate the presented method.

In the last paper of this section, Thyagarajan *et al.*, from the University of California Berkeley, describe the design of a 60 GHz drain-source neutralized wideband linear power amplifier in 28-nm CMOS. The prototype delivers a saturated output power of 16.5 dBm with a peak power added efficiency of 12.6% within an overall bandwidth of 11 GHz.

II. DATA CONVERTERS

The papers dealing with data converters report three prototypes integrated in 65-nm CMOS. In the first paper, Caldwell *et al.*, from Analog Devices Inc., present a reconfigurable continuous-time $\Delta\Sigma$ modulator, which improves the linearity of the embedded 17-level ADC by using calibration and reference shuffling technique, achieving a DR of 75.4-to-62.8 dB within a programmable 10-to-100 MHz signal bandwidth.

In the next paper, Yang and Liu, from Broadcom Corporation, propose a time-interleaved ADC with partially active flash sub-ADCs, which offers better power efficiency than conventional flash ADCs for sampling rates over 10 GS/s. The presented topology is demonstrated by a 6-bit four-way prototype with a FOM of 197 fJ/cs.

In the final paper of this section, Yu *et al.*, from KAIST, describe a second-order $\Delta\Sigma$ time-to-digital converter that uses a switched-ring oscillator and a gated switched-ring oscillator, without requiring calibration to compensate for the error from frequency difference between both oscillators. Measurements show an integrated noise of 148 fs-rms at 4-MHz bandwidth, while consuming 6.55 mW.

III. DIGITAL DESIGN AND SOC

In the first digital design paper, Das *et al.*, from ARM Ltd., present a Razor-based hardware loop-accelerator, implementing the Sobel edge-detection algorithm. A 65-nm CMOS prototype operating at 1 GHz is shown that demonstrates 34% energy-efficiency improvements on a per-device basis and 33% overall on the entire batch of devices.

In the next digital design paper, Das and Ghosh, from University of South Florida, propose an energy barrier model of SRAM that is very effective in predicting the behavior of stability and can be used as a tool to expedite the early phases of design and to optimize energy dissipation of SRAM cache.

In the third paper, Zhang *et al.*, from Harvard University, propose an adaptive-frequency clocking scheme for supply-noise resilience in battery-powered aerial microrobotic SoC. The chip, developed in 40-nm CMOS for a RoboBee microrobot, shows a $2\times$ performance improvement compared to conventional schemes.

Finally, Wachnik *et al.*, from IBM Corporation, concludes this special section with an interesting survey of measured data from five generations of CMOS technologies, showing a trend of increasing gate resistance and its effect on typical logic performance of a 20-nm replacement gate technology.

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His main research interests are in the field of analog and mixed-signal integrated circuits, especially high-performance data converters, including analysis, behavioral modeling, design and design automation of such circuits. In these topics, Dr. de la Rosa has participated in a number of National and European research and industrial projects, and has co-authored some 180 international peer-reviewed publications, including journal and conference papers, books and book chapters and recently the book *CMOS Sigma-Delta Converters: Practical Design Guide* (Wiley-IEEE Press, 2013).

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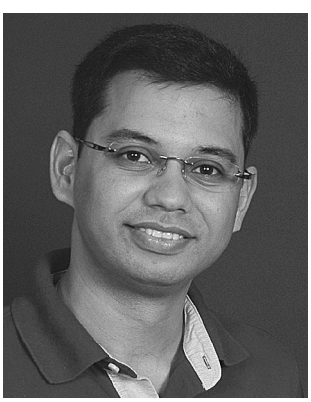
John W. M. Rogers (M'95–SM'07) received the Ph.D. degree in 2002 in electrical engineering from Carleton University, Ottawa, ON, Canada. Concurrent with his Ph.D. research he worked as part of a design team with SiGe Semiconductor that developed a cable modem IC for the DOCSIS standard.

From 2002 to 2004 he collaborated with Cognio Canada Ltd. doing research on MIMO RFICs for WLAN Applications. Since 2002 he has been a member of the faculty of engineering at Carleton University where he is now an associate professor. From 2007–2008 he was on sabbatical and working with Alereon Inc. developing ICs for UWB applications. He is the coauthor of *Radio Frequency Integrated Circuit Design* 2nd Ed. (Artech House, 2010), *Integrated Circuit Design for High Speed Frequency Synthesis* (Artech House, 2006), and *Radio Frequency System Architecture and Design* (Artech House, 2013). His research interests are in the areas of RFIC and mixed-signal design for wireless applications.

Dr. Rogers was the recipient of an IBM faculty partnership award in 2004, and an IEEE Solid-State Circuits Predoctoral Fellowship in 2002. He holds five U.S. patents and is a member of the Professional Engineers of Ontario. He has been serving as a member of the technical program committee for the Custom Integrated Circuits Conference since 2006 and the BiCMOS Circuits and Technology Meeting since 2008.



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