

Hardware Implementation Overhead of Switchable Matching Networks

Ettore Lorenzo Firrao, Anne-Johan Annema, Frank E. van Vliet, and Bram Nauta

Abstract—Nowadays, more and more RF systems include switchable matching networks to decrease the impact of the environment-dependent antenna impedance on the RF front end performance. This paper reviews the theoretical lower limit on the required number of matching states to match VSWR ranges and then presents an analysis of hardware implementations to actually implement a suitable switchable matching network. A number of matching network topologies are analyzed: PI networks, loaded transmission lines, branch line coupler based circuits, single circulators and cascaded circulators. In our investigation only narrow-band applications are targeted. For the various circuit implementations the required number of matching states for each hardware implementation is compared to the theoretical minimum number of states required for the same matching in order to benchmark their hardware implementation overhead. It appears that a matching network using cascaded circulators is the closest to the theoretical optimum for networks with a relatively low number of states: this type of matching network was implemented and analyzed in more detail.

Index Terms—Automatic antenna tuner, impedance matching, switchable matching network, tunable matching network.

I. INTRODUCTION

ANTENNA impedances are heavily dependent on their EM environment [1] [2]. As a result, antenna impedances may change significantly during operation in, e.g., handheld devices. The antenna impedance Z is usually expressed in terms of reflection coefficient $\Gamma = (Z - Z_0)/(Z + Z_0)$, where Z_0 is the characteristic impedance, or in terms of voltage standing wave ratio $VSWR = (1 + |\Gamma|)/(1 - |\Gamma|)$. For a typical antenna the VSWR can be up to 10:1 [1]–[5] which corresponds to $|\Gamma|$ values up to about 0.81.

Typically RF power amplifiers are optimized to drive a nominal load, usually 50Ω , through a fixed impedance matching network. The VSWR associated with changing antenna impedances cause serious design and performance challenges for the RF power amplifier (PA) driving the antenna. Assuming a certain lower bound on maximum transmit power, varying load impedances for the PA require robustness to both maximum voltage and maximum current levels well above those required when driving a nominal load impedance at the same power level [3]–[5]. Consequently, the PA must be designed

to operate properly for a wide load impedance range and hence the PA is necessarily overly robust at nominal conditions which results in significantly reduced efficiency at nominal conditions. On top of this, matching losses due to non-nominal load impedances decrease the efficiency and radiated power significantly.

Automatic antenna tuners are used to match an antenna impedance to an impedance close to the nominal impedance, which is typically 50Ω . An antenna tuner [6]–[25] is generally implemented through a system consisting of impedance sensing circuitry, a tunable matching network and a control loop that implements the tuning procedure [26]–[30] of the matching network. The tunable matching network can be a continuous tunable matching network or a switchable matching network; typically a switchable matching network is used [6]–[25].

In [31], the theoretical minimum number of states for switchable matching networks was derived, required to match any load impedance for which $|\Gamma_{load}| \leq |\Gamma_{load}|_{max}$ to within a smaller area for which $|\Gamma_{in}| \leq |\Gamma_{in}|_{max}$. The work in [31] targets the theoretical minimum number of required matching network states, explicitly not considering any hardware implementation.

The current paper is about the hardware overhead of implementing a switchable matching network that matches from $|\Gamma_{load}| \leq |\Gamma_{load}|_{max}$ to $|\Gamma_{in}| \leq |\Gamma_{in}|_{max}$ for a number of topologies. This hardware overhead is defined as the ratio of the number of states required for a specific (optimized) hardware implementation and the theoretical minimum number of required states to achieve the same matching performance. This is important because minimization of the hardware implementation most likely leads to easier tuning algorithms and typically results in lower losses. Lower losses directly translate in more efficient transmit systems, while in receive mode the noise figure, noise matching and losses are all relevant. In this paper, the main focus is on transmit and size and cost aspects are excluded as primary selection criterion.

For the analyses in this paper, only narrow band applications are targeted and the values of switchable reactances are assumed to be binary scalable (where every switch is controlled by one control line that corresponds to a bit). Furthermore, the passive components in the matching network are assumed to be ideal: linear and without spread. Losses and thermal noise are accounted for by resistive components associated with limited quality factors for (reactive) passive components. Note that this “ideal” is different from [31] where the expression “ideal” denoted the absence of any specific hardware implementation in order to make the theory as much general as possible.

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This paper is arranged as follows. Section II presents a short review of the theoretical minimum number of required states for switchable matching networks. Section III reports the hardware implementation overhead– in terms of required number of states– for PI networks, loaded transmission line matching networks, branch line coupler based matching networks, and for matching networks using circulators. For a low number of states, the analyses show that the cascaded circulator topology appears to have the best hardware implementation overhead. In this section the components and switches are assumed to be ideal, linear and lossless.

Section IV shows in depth analyses and measurements on the matching network that is the closest to the theoretical optimum (in required number of states): the cascaded circulator based matching network. Section V presents a short analysis of the effects of lossless components on the power efficiency and mismatch efficiency of a switchable matching network. In this section the design vehicle is a 4-bit tunable PI network for simplicity and clarity reasons. Finally, the conclusions are summarized in Section VI.

II. MINIMUM NUMBER OF STATES

In [31] it was shown that the minimum required number of states for a switchable matching network can be derived mathematically. It was shown that it is optimum to match radially equispaced circular shaped reflection areas on the Smith chart onto a circular region centered in the origin of the Smith chart. Similar results were obtained recently [25], based on a pure optimization based approach. For higher $|\Gamma_{load}|_{max}/|\Gamma_{in}|_{max}$ ratios, it was shown that cascaded simple matching networks are more efficient than more complex matching networks, in terms of the theoretical minimum required number of matching network states to match an impedance from anywhere inside $|\Gamma_{load}| \leq |\Gamma_{load}|_{max}$ to an impedance within $|\Gamma_{in}| \leq |\Gamma_{in}|_{max}$.

A. Theoretical Optimum Matching Properties

The theoretical optimum matching properties of a switchable impedance matching network are illustrated in Fig. 1, assuming $|\Gamma_{in}|_{max} = 1/3$. Fig. 1 shows the $|\Gamma_{load}|_{max}$ as a function of the numbers of states for an optimum matching network. Because the rest of this paper assumes binary controlled matching network states, the number of states is shown on a \log_2 -scale.

For a very low number for N_{states} , the optimum configuration appears to be as shown in Fig. 1(b): the $(N_{states} - 1)$ equidistant radially spaced circular regions all encircle the origin of the Smith chart, see also appendix A. For larger number for N_{states} , it is optimum to construct configurations such as shown in Fig. 1(c)–(e). In these configurations, around the center $|\Gamma_{in}| = 1/3$ circle, circular bands are constructed from circles that each can be matched to the center circle.

B. Hardware Implementation Overhead

The analyses leading to the minimum number of states to reach a certain impedance matching, as in Fig. 1, are purely mathematical: explicitly no assumption on actual hardware implementations was made. To compare actual hardware

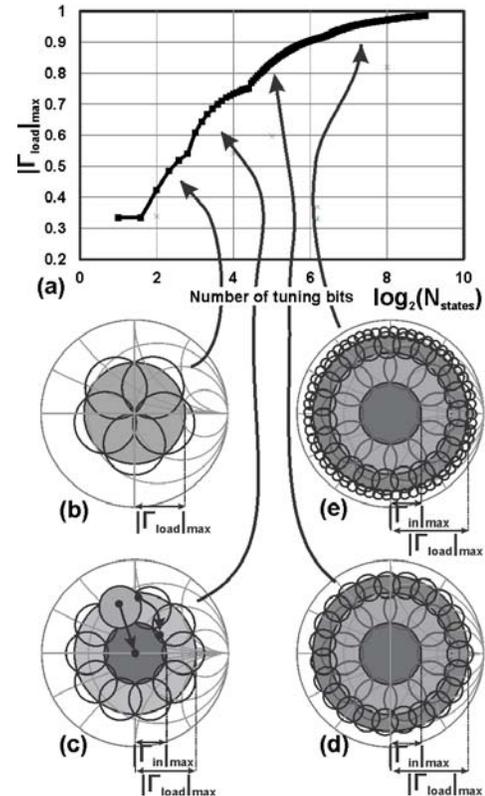


Fig. 1. Minimum number of states matching construction to match from any $|\Gamma_{load}| \leq |\Gamma_{load}|_{max}$ to within anywhere inside $|\Gamma_{in}| \leq |\Gamma_{in}|_{max}$. For $|\Gamma_{in}|_{max} = 1/3$ this yields the $|\Gamma_{load}|_{max}(N_{states})$ graph in (a) and example configurations in (b) enclosing the center of the Smith chart and in (c)–(e) having respectively 1, 2, and 3 rings of regions that can be matched to the center circle.

implementations of switchable matching networks, we defined the hardware implementation overhead in equation as:

$$\text{hardwareoverhead} = \frac{N_{states}}{N_{min}} \Big|_{\{|\Gamma_{load}| \leq |\Gamma_{load}|_{max}, |\Gamma_{in}| \leq |\Gamma_{in}|_{max}\}} \quad (1)$$

where N_{states} is the actual number of states of the switchable matching network circuit implementation and N_{min} is the theoretical minimum number of states.

In this paper we analyze and benchmark various hardware implementations of switchable matching networks. All have different ways of achieving impedance matching and consequently they all have different hardware overhead numbers. We analyze networks that are reciprocal, non-reciprocal, lumped or distributed to cover most conventional classes of switchable matching networks. We introduce a matching network using cascaded circulators because it most closely implements the theoretical optimum [31] expressed in number of states, not in size nor cost. The number of switches (equal to the number of switchable reactances) to implement N_{states} is $N_{switch} = \lceil \log_2(N_{states}) \rceil$ where the $\lceil x \rceil$ operator rounds to the nearest larger integer. Note that there is not necessarily a unique relation between N_{switch} and the total number of reactances, transmission lines and other passive matching network components.

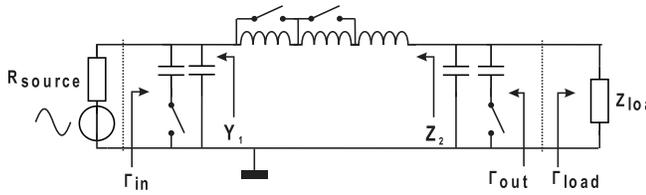


Fig. 2. Typical implementation of a (here 4 bit switchable) low-pass PI matching network.

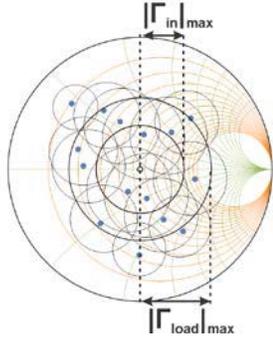


Fig. 3. An example of matchable area of a 4-bit switchable low pass PI matching network based on brute force computing on a Smith chart for $|\Gamma_{in}|_{max} = 1/3$.

III. HARDWARE IMPLEMENTATIONS

This section investigates the hardware implementation overhead for several hardware implementations. Four cases are treated, which are chosen as examples representative of particular classes. The PI networks are an example of a reciprocal lumped-element implementation. Similarly, the loaded transmission-line networks are an example of distributed matching networks, branch-line coupler networks are an example of reflection-based coupler networks and circulator networks are an example of non-reciprocal networks.

Single-stage matching networks are assumed; combinations or cascaded versions of the matching networks (such as LC-ladder networks) are not treated. Note that the cascaded circulator based matching network in Section III-E uses cascaded circulators, but is not a cascaded version of the matching network in Section III-D.

A. PI Networks

The PI network is a reciprocal and lumped-element implementation of a matching network. PI networks are widely used to implement switchable matching networks; a 4-bit switchable implementation example of a low-pass PI network is shown in Fig. 2. Its advantages over its T-network equivalent is that parasitic source and load capacitances can easily be absorbed in PI networks while a low pass PI network has advantages over its high-pass counterpart because it allows to filter harmonic content.

The switchable (banks of) reactances in the PI network implement 2^n states of this matching network. Appendix B shows the derivations of the output reflection coefficient for each state which can directly be used to determine the region on the Smith chart that can be matched to the target impedance range defined by $|\Gamma_{in}| \leq |\Gamma_{in}|_{max}$. Due to the compress-

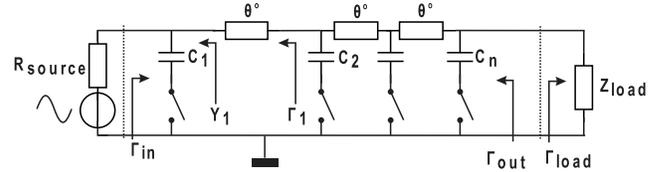


Fig. 4. Implementation of a 4-bit switchable loaded transmission line based matching network.

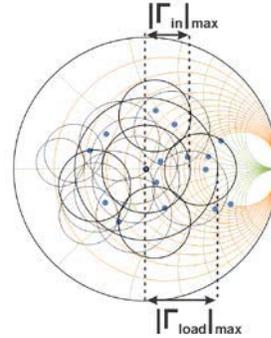


Fig. 5. Matchable area of a 4-bit switchable loaded transmission line based matching network on a Smith chart for $|\Gamma_{in}|_{max} = 1/3$.

sive nature of the Smith chart and the very non-linear equation for impedance as function of the switchable reactances, there is a considerable overhead in states, compared to the theoretical optimum [31].

An example of the matchable area on the Smith chart is shown in Fig. 3. In this figure, every dot can be matched onto the center of the Smith chart, while every circle around each dot can be mapped onto the $|\Gamma_{in}| = |\Gamma_{in}|_{max}$ circle. For this figure, the optimization to match the largest area was done using brute force computing (see appendix C for more details), here targeting $|\Gamma_{in}|_{max} = 1/3$ or equivalently $VSWR=2:1$ and assuming 4 bit settings. For this optimum tunability, the two capacitances and the inductor have 1 respectively 2 bit tunability, see Fig. 3.

For this example 4-bit PI network, for $|\Gamma_{in}|_{max} = 1/3$ the matchable region is bounded by $|\Gamma_{load}|_{max} \cong 0.54$ which corresponds to $VSWR \cong 3.3$. With (1), the hardware implementation overhead turns out to be about 2. A summary of the $|\Gamma_{load}|_{max}$ and hardware overhead, as a function of the number of bits, for all topologies considered in this paper is shown in Fig. 12 and 13.

B. Loaded Transmission Line Based Matching Networks

Another way to implement a switchable matching network is to load a transmission line with switchable capacitors [31]–[34], see Fig. 4 for a 4 bit switchable implementation. This type of impedance matching network is a reciprocal and a distributed element implementation. The advantage of this implementation is simplicity. A disadvantage is the difficulty to make it off-chip at microwave frequencies as the physical length of each transmission line becomes too short, while on-chip the length is relatively large.

Appendix D shows the derivation of the output reflection coefficient for each state in a generic loaded transmission line based impedance matching network. To get N uniformly

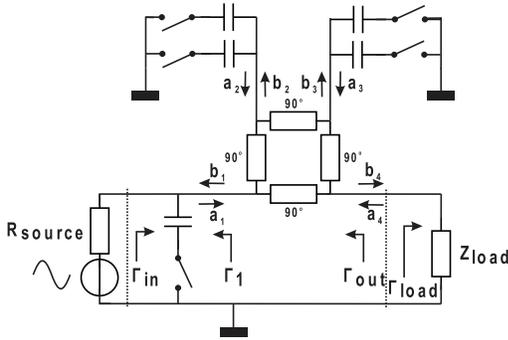


Fig. 6. Implementation of a 5-bit switchable branch line coupler based matching network.

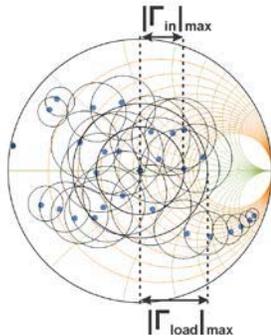


Fig. 7. Matchable area of a 5-bit branch line coupler based matching network for $|\Gamma_{in}|_{max} = 1/3$.

spaced phases of Γ_{out} , we would require N specific transmission line lengths, that directly yields significant redundancy and overhead. An example of matchable area on the Smith chart for a 4 bit switchable implementation, targeting $|\Gamma_{in}|_{max} = 1/3$ is shown in Fig. 5.

For this example the matchable region is bounded by $|\Gamma_{load}|_{max} \cong 0.54$ which corresponds to $VSWR \cong 3.3$. With (1), the hardware implementation overhead turns out to be about 2.

C. Branch Line Coupler Based Matching Networks

Branch line couplers can be used to implement impedance transformation [35], [36]–[39], yielding a reciprocal and distributed implementation. An example of a 5-bit switchable branch line coupler based impedance matching network is shown in Fig. 6; appendix E shows the derivation of its impedance matching performance. Similar to the PI-network, the very non-linear relations between Γ_{out} and the reactances yields a significant hardware implementation overhead. The advantage of this topology is that it is well suited for implementation in MMIC technologies; the disadvantage is that the losses are usually higher than that of other topologies.

Fig. 7 shows the impedance matching capabilities of a 5-bit switchable impedance matching network, for $|\Gamma_{in}|_{max} = 1/3$. Again, every dot can be matched toward the center of the Smith chart, while every circle can be mapped onto the $|\Gamma_{in}| = 1/3$ circle. For this matching network, $|\Gamma_{load}|_{max} \cong 0.45$ while the hardware implementation overhead is about 3.8 obtained using brute force optimization.

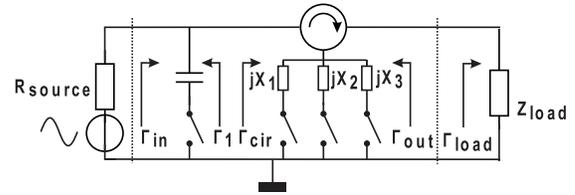


Fig. 8. Circulator-based 4-bit switchable matching network.

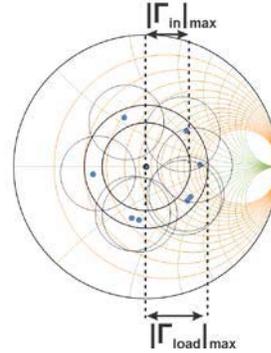


Fig. 9. Matchable area of a 4-bit switchable single circulator based matching network, for $|\Gamma_{in}| = 1/3$.

D. Single Circulator Based Matching Networks

Circulators can be used to implement (non-reciprocal) impedance matching network [35], [40]–[43]. In a three-port circulator, ideally all the power incident to a single port is coupled to only one other port, leaving the other port isolated. This property can be used to rotate the phase of the load reflection coefficient. After proper rotation, impedance matching can be achieved using a shunt capacitor. An example of a (4-bit switchable) circulator-based impedance matching network is shown in Fig. 8.

A mathematical derivation of the impedance matching properties of this type of matching network is shown in Appendix F. To get uniformly spaced mappable regions as required for the mathematical optimum [31], the appendix shows that the summed value of the switched reactances should be distributed as $X_n = R_0 \arctan(n^\pi/N)$. A hardware implementation using a minimum number of switched reactances consequently shows a significant overhead of switchable states. Other disadvantages include the size and cost of circulators.

For $|\Gamma_{in}|_{max} = 1/3$, the matching performance of a 4-bit switchable implementation is shown in Fig. 9. For this case, the maximum load VSWR is about 4.8 and the hardware overhead is about 6.

E. Cascaded Circulator Based Matching Networks

To get the closest to the theoretical optimum– in number of required matching network states, see [31]– uniformly distributed phase shifts should be implemented in the matching network in section D. The resulting implementation, showing the lowest found hardware implementation overhead in terms of required states to achieve some matching, is shown

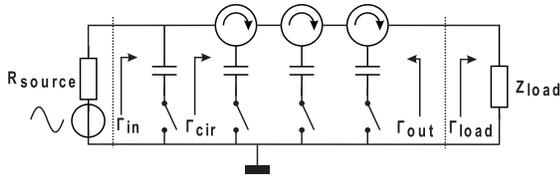


Fig. 10. Cascaded circulator based 4-bit switchable matching network implementation.

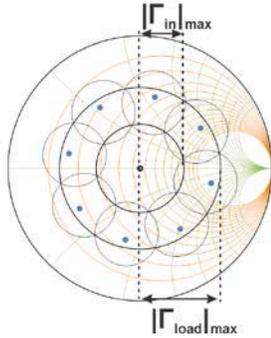


Fig. 11. Matchable area of a 4-bit switchable cascaded circulator based matching network, for $|\Gamma_{in}| = 1/3$.

in Fig. 10. Compared to the single circulator based matching networks, more circulators are required which increases cost and size. As advantage (ideal) nicely spaced phase steps can be obtained such as required for matching state configurations such as shown in Fig. 1(b) and (c). With this topology, each circulator and associated switchable component section can be designed to achieve a specific phase shift step while the leftmost shunt capacitor can match towards the center of the Smith chart.

As derived in Appendix F, the output reflection coefficient of this (4-bit switchable) network is

$$\Gamma_{out} = \Gamma_1 \Gamma_{X1} \Gamma_{X2} \Gamma_{X3} \quad (2)$$

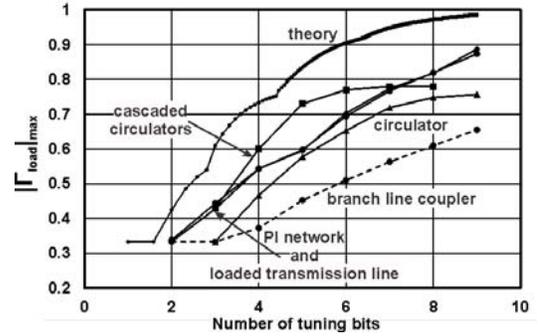
where Γ_{load} is the reflection coefficient at the output of the three circulators, Γ_{X1} , Γ_{X2} and Γ_{X3} are the reflection coefficients of the switchable jX_1 , jX_2 , jX_3 and where

$$\Gamma_1 = \frac{\frac{1}{Z_0} - Y_1}{\frac{1}{Z_0} + Y_1} \text{ and } Y_1 = \frac{1}{R_{source}} + j\omega C$$

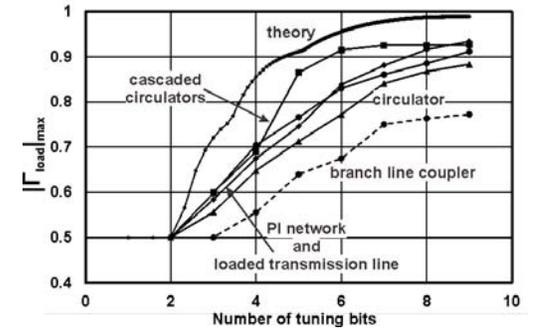
and where Z_0 is the reference impedance.

An example of the matchable area on a Smith chart for a 4-bit switchable impedance matching network using the topology in Fig. 11, for $|\Gamma_{in}|_{max} = 1/3$, is shown in Fig. 11. In this, each dot can be mapped onto the center of the Smith chart, while the dot at the center of the Smith chart is actually 8 coinciding dots, due to the nature of this network topology.

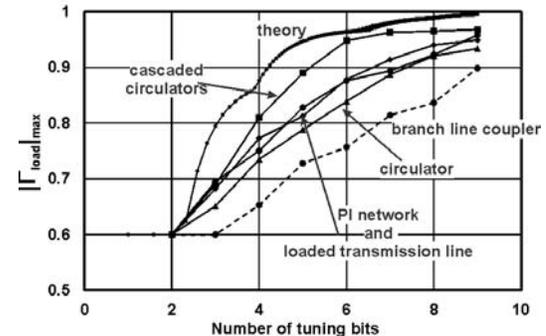
For this implementation, it can be shown that the hardware implementation overhead as defined in (1) is to 16/9 and it is the lowest achievable value for single ring optimum configurations as described in [31] and as shown in Fig. 1(b) and (c).



a)



b)



c)

Fig. 12. Magnitude of the load reflection coefficient vs. number of bits for: (a) $|\Gamma_{in}| = 1/3$; (b) $|\Gamma_{in}| = 1/2$; (c) $|\Gamma_{in}| = 3/5$.

F. Discussion

Sections III-B to III-F showed a number of hardware implementations of switchable matching networks: PI networks, loaded transmission lines, branch line couplers, single circulators and cascaded circulators. For all of these, the optimum matching performance in terms of $|\Gamma_{load}|_{max}$ as a function of the number of bits tunability for a predefined $|\Gamma_{in}|_{max}$ is plotted in Fig. 12 for $|\Gamma_{in}| = 1/3$, $|\Gamma_{in}| = 1/2$ and for $|\Gamma_{in}| = 3/5$, along with the theoretical optimum [31].

It can be seen from these plots that the branch line coupler based matching network, see Section III-D, performs worst in terms of (1). In the low-number-of-bit range the implementation based on cascaded circulators performs best in terms of hardware overhead (1). The PI-network and loaded transmission line based implementations that were described in Sections III-B and III-C have comparable matching performance in terms of required number of states to achieve some kind of impedance range matching. These two network topologies are optimum when having many states, only to be

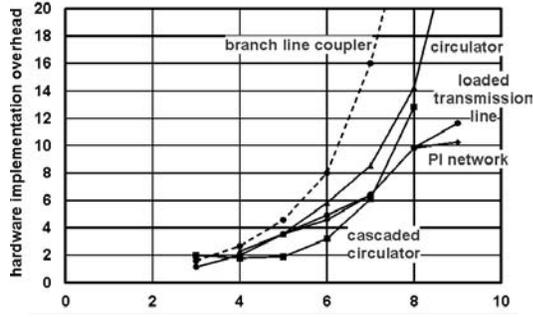


Fig. 13. Hardware implementation overhead versus number of bits for different switchable matching network topologies for $|\Gamma_{in}| = 1/3$. For 4, 5, 6, and 7 bit tunability, the cascaded circulator topology has a lower hardware overhead compared to the other switchable matching network topologies.

outperformed in terms hardware overhead at low and medium number of states by the cascaded circulator based matching network topology.

The hardware implementation overhead for the various topologies are plotted in Fig. 13, as a function of the number of bits tunability for or $|\Gamma_{in}| = 1/3$. This plot shows that the hardware implementation overhead — in terms of required number of states — increases rapidly with the number of (binary controlled) states in switchable matching networks. Especially the branch line coupler based and the single circulator based matching networks require a relatively large hardware implementation overhead in required states.

The differences in hardware overhead follow from the way states are mapped on the Smith chart, which is very different for all types we analyzed.

The lowest hardware implementation overhead, for a low number of states, is for the cascaded circulator based matching network. Its state distribution is the closest to the mathematically optimum distribution derived in [31]. This matching network is worked out in detail and experimentally in Section IV. Disadvantages of this type of matching network are the bulkiness and cost of circulators.

The second best type of matching network appears to be the PI network, which does not have the mentioned disadvantages of the cascaded circulator network. An analysis of the impact of lossy reactances (or switches) on the performance of a (4 bit tunable, for simplicity reasons) PI network is shown in Section V.

IV. CASCADED CIRCULATOR TOPOLOGY

A. Lossy Cascaded Circulators

Section III showed that the (largely unknown) cascaded circulator based switchable impedance matching network performs the closest to the theoretical optimum [31], in number of required states. In this section, this type of switchable matching network is analyzed in more detail.

The theoretical matching performance of cascaded circulator based matching networks was described in Section III-F. In that section, ideal lossless components were assumed. In case of lossy circulators, the circulators rotate phase but also decrease the signal magnitude. Assuming the same insertion

loss between ports, the reduction in magnitude is a function of the overall insertion loss of the circulators and of the interconnections and of the quality factor of the switchable reactances. Then (2) turns into

$$\Gamma_{cir} = \left(IL^{3N} \right) \Gamma_{load} \Gamma_{X_1} \Gamma_{X_2} \Gamma_{X_3} \dots \Gamma_{X_N} \quad (3)$$

where Γ_{cir} the reflection coefficient at the input of the circulators, N is the number of cascaded circulators, IL is the linear insertion loss of the circulator (assuming the same for each port and the same for every circulator), Γ_{load} the load reflection coefficient and Γ_{X_1} , Γ_{X_2} , Γ_{X_3} and Γ_{X_N} are the reflection coefficient of the reactances, see Fig. 10.

In case of a 50 Ω load, and excluding interconnect losses, the overall linear insertion loss is

$$IL_{dB} = N * 20 \log |IL|$$

The switchable matching network under investigation is linear (neglecting the non-linearity of the PIN diodes and circulators) and hence is fully characterized by its two-port S matrix (per state). For this we denote the input port as port 1 and denote the output port as port 2; there are as many S-matrices as there are number of states. For the 4-bit switchable example in Figs. 10, 16, S-matrices are needed. Once the overall S-matrices are known, the load contour can straight forwardly be derived for each state based on the required input reflection coefficient contour. Note that as the matching network is linear, load-pull measurements do not provide more information than using the S-matrix does. The input reflection coefficient Γ_{in} and load reflection coefficient Γ_{load} are related as

$$\Gamma_{load} = \frac{\Gamma_{in} - S_{11}}{S_{22}\Gamma_{in} - \Delta}$$

where

$$\Delta = S_{11}S_{22} - S_{21}S_{12}$$

The power efficiency of the switchable matching network is

$$\eta = \frac{P_{load}}{P_{in}} = \frac{(1 - |\Gamma_{load}|^2) |S_{21}|^2}{(|1 - S_{22}\Gamma_{load}|^2) (1 - |\Gamma_{in}|^2)} \quad (4)$$

where

$$\Gamma_{in} = S_{11} + \frac{S_{21}S_{12}\Gamma_{load}}{1 - S_{22}\Gamma_{load}}. \quad (5)$$

B. A practical Example

A hardware implementation of a 4-bit switchable cascaded circulator based matching network was built, see Fig. 10 for the architecture and Fig. 14 for a photo of the prototype.

The following circulator was used: CCMTH0801-915-ETL; the measurement frequency was set to 947 MHz and the PCBs were designed for this frequency. Two types of PCBs were designed: one to implement the switchable capacitors and the other to implement the switchable shunt capacitor. Although pHEMTs and MESFETs may be preferred for their lower control power, for simplicity reasons in our experimental setup we used PIN diodes to implement the switches. The switch-on current was 10 mA. The PIN diode was biased using

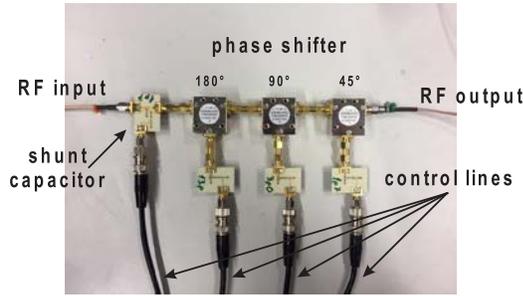


Fig. 14. Photo of the prototype implemented and measured in the lab.

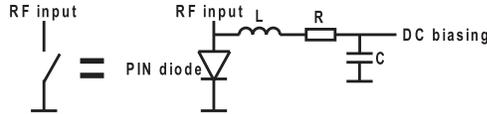


Fig. 15. Simplified schematic of the biasing circuit of the PIN diodes.

two inductors in series (for better isolation), a resistor and a shunt capacitor at the DC input, see Fig. 15.

The measurements were carried out using a Rohde & Schwarz ZVB-20 VNA at a power level of 0 dBm. The measured S-matrices for each state were then used to derive the load contour based on the required input reflection coefficient contour.

Three values for $|\Gamma_{in}|_{max}$ were chosen: 1/3, 1/5 and 1/10 for which the (measurement based) results are shown in Fig. 16(a), (b), and (c) respectively. For these $|\Gamma_{in}|_{max}$ values, the SMD shunt capacitors at the input are 1 pF, 1.7 pF and 2.7 pF. The values of the capacitors that implement X_1 , X_2 and X_3 are 13 pF, 3 pF, and 1.7 pF. The measurement results show that the theoretical and measured behavior of the switchable matching network complies nicely. Note that due to the losses, the matchable area is larger than the one derived from the theory using ideal (lossless) components.

V. THE IMPACT OF LOSSES— AN EXAMPLE

The analyses in Section III assumed ideal switches and ideal reactances, whereas Section IV presented analyses and measurement results for the network that is closest to the mathematical optimum in [31]. The results in Section IV already show that lossy components have a significant impact on, e.g., the matching performance. A major drawback of the system in Section IV is in the cost and size of circulators, which makes the cascaded circulator based network unsuitable for, e.g., handheld devices.

This section presents the impact of lossy components and switches using a 4-bit tunable PI network as vehicle, for $|\Gamma_{in}|_{max} = 1/3$, corresponding to the situation in Fig. 3. This PI network is the second best from hardware overhead point of view and does not have the cost and size disadvantages associated with the matching network in Section IV.

For, e.g., handheld devices, the matching network could be monolithically implemented on silicon, on GaAs or, e.g., using discrete SMD components, that all have losses. To show the impact of lossy components, we assume lossy reactances that

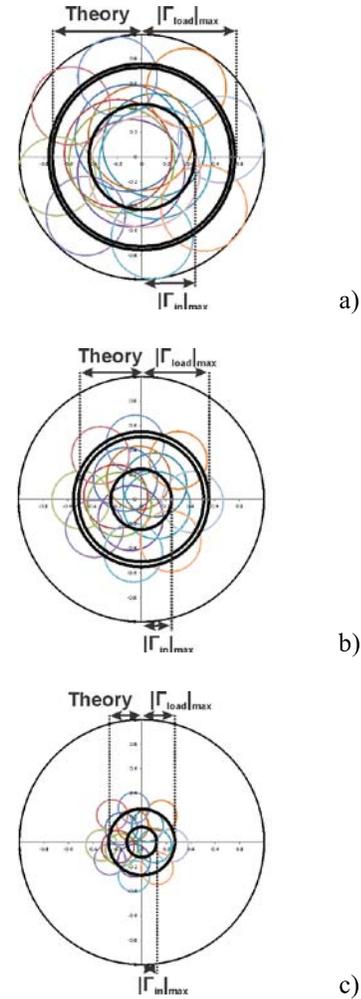


Fig. 16. Matchable area on the Smith chart for various magnitude of the input reflection coefficient: (a) $|\Gamma_{in}| = 1/3$; (b) $|\Gamma_{in}| = 1/5$; (c) $|\Gamma_{in}| = 1/10$. The black continuous circle is for ideal circulators with perfect matching at all the ports when the switch of the shunt capacitor at the input is open. Because of the non-ideal behavior of the circulators, in case the switch of the shunt capacitor at the input is open, the circles of the states do not overlap exactly.

have specific Q_L and Q_C that are the same for all inductors respectively capacitors in the switchable matching network. We assume for simplicity that this Q includes the effect of lossy switches. In the comparison, we assume ideal (lossless) implementations with fixed $Q_C = Q_L \rightarrow \infty$, implementations in silicon for which we used fixed $Q_C = 20$ and $Q_L = 10$, and implementations in GaAs for which we used $Q_C = 60$ and $Q_L = 35$. As the focus of this paper is on transmit, this section reports on power efficiency (4) and the impact of impedance matching. For the latter case a variant of (4) is used, omitting the second term in the denominator. The impact of lossy matching networks on the noise figure is briefly addressed in Appendix G

A. Constant Power Efficiency and Mismatch Contours

Below we report (for the optimized 4b PI network for $|\Gamma_{in}|_{max} = 1/3$) constant power efficiency contours and constant matching efficiency contours on the Smith chart.

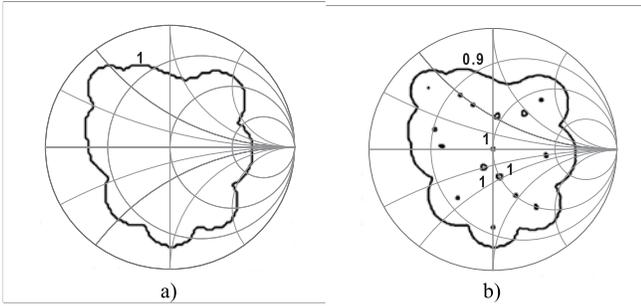


Fig. 17. For a lossless 4b-tunable PI network for $|\Gamma_{in}|_{max} = 1/3$ (a) constant power efficiency contours; (b) constant matching efficiency contours.

This is done for all three cases listed above. The power efficiency contours are relevant for cases where the matching network is driven by a non-linear source, e.g., an RF power amplifier. The constant mismatch contours assume a linear resistive signal source driving the matching network and its load. For each of the three cases, an optimization was done to reach the largest (circular) matchable region, with radius $|\Gamma_{load}|_{max}$. The resulting optimum values for the switchable reactances and the radius of the matchable region, $|\Gamma_{in}|_{max} = 1/3$, are reported below.

	value $Q_C \rightarrow \infty$ $Q_L \rightarrow \infty$	value $Q_C = 20$ $Q_L = 10$	value $Q_C = 60$ $Q_L = 35$	tunability
X_{CIN}	-41 Ω	-38 Ω	-40 Ω	1b
X_L	23 Ω	22 Ω	23 Ω	2b
X_{COUT}	-59 Ω	-43 Ω	-51 Ω	1b
$ \Gamma_{load} _{max}$	0.54	0.66	0.58	

Fig. 17(a) shows the constant power efficiency contours for a lossless PI network, where the contour demarks the matchable area. The matching efficiency contours for the same network are shown in Fig. 17(b).

Fig. 18(a) shows constant power contours for a 4-b tunable PI network for $|\Gamma_{in}|_{max} = 1/3$, implemented on low ohmic silicon ($Q_C = 20, Q_L = 10$). Due to the losses, the matchable area on a Smith chart is bigger and the power efficiency can as low as 10%. Fig. 18(b) shows the matching efficiency contours, demonstrating that matching efficiency is a little lower than the power efficiency.

Fig. 19(a) shows constant power contours and constant mismatch efficiency contours assuming implementation in GaAs. Since GaAs is a semi-isolator (not a semi-conductor like silicon) the quality factor of the passive components is higher: for this example it is assumed that the quality factor of the inductors is 35 and the quality factor of the capacitors is 60.

It can be concluded that implementing (here) PI networks using low-Q reactances as in silicon easily yields significantly decreased power and mismatch efficiencies. As a direct result, having no additional impedance matching could outperform impedance matching using low-Q reactances. To illustrate this, Fig. 20(a) and (b) show the constant matching contours of Fig. 18(b) respectively Fig. 19(b), showing only the area

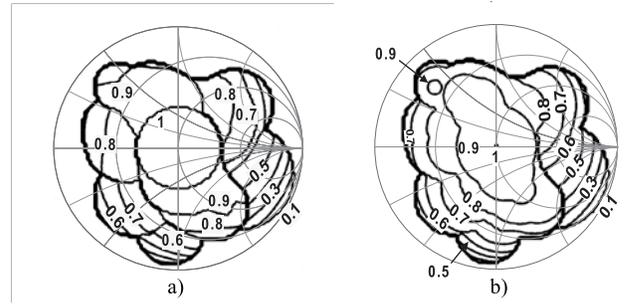


Fig. 18. For a 4b-tunable PI network for $|\Gamma_{in}|_{max} = 1/3$ in silicon ($Q_C = 20, Q_L = 10$): (a) constant power efficiency contours; (b) constant matching efficiency contours for the same case.

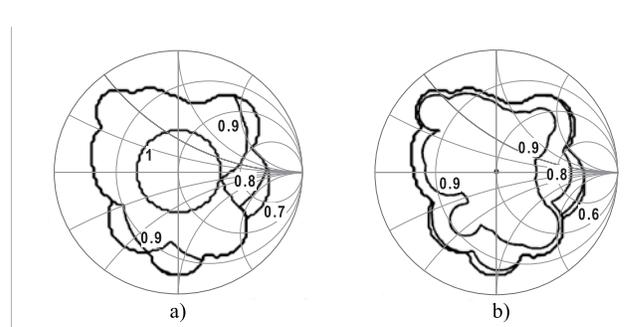


Fig. 19. For a 4b tunable PI network for $|\Gamma_{in}|_{max} = 1/3$, implemented on GaAs ($Q_C = 60, Q_L = 35$) (a) constant power efficiency contours; (b) constant matching efficiency contours for the same case.

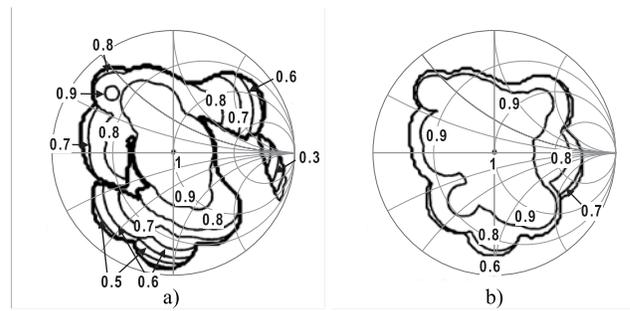


Fig. 20. Constant mismatch contours for a PI network (a) in silicon and (b) in GaAs, showing only the regions where the efficiency with a matching network is better than that without matching network.

where the matching efficiency using the matching network is higher than using no matching network at all. For the Si-case a significant part of the mappable region appears to be better off without using a (low Q) matching network.

VI. CONCLUSIONS

Hardware implementation overhead of switchable matching networks, expressed in required number of matching states to get a predefined impedance matching performance, normalized to the corresponding theoretical lower limit, was worked out in detail. For this, narrow-band applications and binary scaled component values were assumed. Several circuit topologies were investigated: switchable impedance matching networks using PI networks, based on loaded transmission lines, based on branch line couplers, using single circulators and utilizing cascaded circulators.

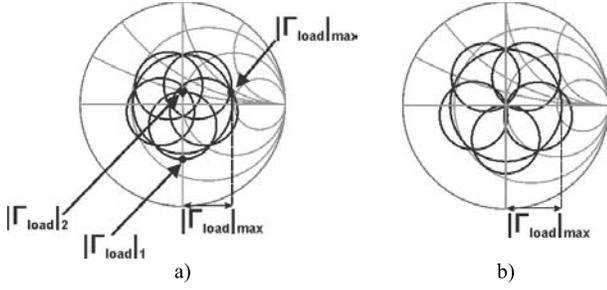


Fig. 21. (a) states enclosing the center of the Smith chart; (b) states enclosing the center of the Smith chart for $|\Gamma_{out}| = |\Gamma_{in}|$.

It follows from the types analyzed that (for not too many control bits) the cascaded circulator based topology is the closest to the theoretical optimum, in required number of matching states. This topology requires just up to 2 times the theoretical minimum number of matching states; this type of switchable matching network has been worked out as a practical example. Second best are PI network and loaded transmission line based switchable impedance matching networks that typically require up to about a factor 10 more matching states than the theoretical minimum.

Measurements on a realized cascaded circulator based matching network confirm its performance. The impact of losses on power efficiency and matching efficiency are shown using a 4-bit tunable PI matching network as vehicle.

APPENDIX A

This appendix presents an extension of the derivation of the minimum number of states for lossless switchable matching networks [31], for a low number of states. The derivations in [31] excluded the possibility that (except for the target region) matched impedance regions enclose the center of the Smith chart. In this appendix the derivation is extended to encircle the center of the Smith chart.

An example configuration with 5 circular region that can be matched to the centered circular region is shown in Fig. 21(a). The mismatch efficiency M of a matching network is [35]

$$M = \frac{(1 - |\Gamma_{out}|^2)(1 - |\Gamma_{load}|^2)}{|1 - \Gamma_{out}\Gamma_{load}|^2}$$

in terms of the output reflection coefficient Γ_{out} and of the load reflection coefficient Γ_{load} . Using this equation, it can be derived that the magnitude of intermediate load reflection coefficient $|\Gamma_{load}|_1$ and $|\Gamma_{load}|_2$ as defined in Fig. 21(a) is

$$|\Gamma_{load}|_{1,2} = \frac{\pm\beta|\Gamma_{out}| + \sqrt{\beta^2|\Gamma_{out}|^2 - (\beta|\Gamma_{out}|^2 + 1)(\beta - 1)}}{1 + \beta|\Gamma_{out}|^2}$$

where

$$\beta = \frac{M}{1 - |\Gamma_{out}|^2}$$

Using goniometric constructions, an expression for the matchable area on a Smith chart can be derived, yielding

$$|\Gamma_{load}|_{max} = c \cos\left(\frac{\pi}{N}\right) + \sqrt{r^2 - c^2 \sin^2\left(\frac{\pi}{N}\right)}$$

where

$$c = \frac{\beta|\Gamma_{out}|}{1 + \beta|\Gamma_{out}|^2} \text{ and } r = \frac{\sqrt{\beta^2|\Gamma_{out}|^2 - (\beta|\Gamma_{out}|^2 + 1)(\beta - 1)}}{1 + \beta|\Gamma_{out}|^2}$$

The expression for $|\Gamma_{load}|_{max}$ is hence a function of $|\Gamma_{in}|$, N and $|\Gamma_{out}|$. In order to maximize the matchable area, the expression should be maximized for $|\Gamma_{out}|$ which for this paper was done numerically. However, a fair estimation for this maximum can be found choosing $|\Gamma_{out}| = |\Gamma_{in}|$. For this case the states are depicted in Fig. 21(b) while for $|\Gamma_{out}| = |\Gamma_{in}|$

$$|\Gamma_{load}|_{max} = 2 \frac{|\Gamma_{in}|}{1 + |\Gamma_{in}|^2} \cos\left(\frac{\pi}{N}\right).$$

APPENDIX B

This appendix shows a mathematical derivation of the impedance matching capabilities of a low-pass PI network having binary scaled capacitors and inductor. In the derivation b_i denotes the value of control bit of the i^{th} switchable component. The output reflection coefficient of the PI network is

$$\Gamma_{out} = \frac{\frac{1}{Z_0} - Y_{out}}{\frac{1}{Z_0} + Y_{out}}$$

where

$$Y_{out} = Y_{C2} + \frac{1}{Z_2} = j\omega \sum_{i=1}^{n3} b_i C_{2,i} + \frac{1}{Z_2}$$

$$Z_2 = Z_{L1} + \frac{1}{Y_1} = j\omega \sum_{i=1}^{n2} b_i L_i + \frac{1}{Y_1}$$

$$Y_1 = Y_{C1} + \frac{1}{Z_{source}} = j\omega \sum_{i=1}^{n1} b_i C_{1,i} + \frac{1}{Z_{source}}$$

The Z_{load} for which $\Gamma_{load} = \Gamma_{out}^*$ can be matched onto Z_0 . Similarly, all load impedances that can be matched unto a circle $|\Gamma_{in}| = |\Gamma_{in}|_{max}$ can easily be derived.

APPENDIX C

This appendix describes the brute force optimization procedure used to compute the maximum mappable area on a Smith chart. In determining the mapping performance of N -bit switchable matching networks, the aim is to get the largest mappable circular Γ_{load} region, composed of 2^N circular regions that can all be mapped onto the center circle defined by $|\Gamma| \leq |\Gamma_{in}|_{max}$:

1. an initial guess for matching network components is made. In this work, the N bit tunability can be distributed across the M reactances in the switchable matching network in any way that satisfies $N = \sum_M n_M$ where n_M is the tunability (in bits) of the m^{th} tunable reactance in the matching network. In this paper we report the results that yields the largest mappable area; this follows after optimization for each possible distribution (see below).
2. the mapping of the matching network for each state of the 2^N states is determined. In each state, a circular Γ_{load} region on the Smith chart is mapped onto the center

circle defined by $|\Gamma| \leq |\Gamma_{in}|_{max}$. As each circular region is uniquely defined by 3 different points on its perimeter, it is sufficient to get a set of three Γ_{load} 's that map onto (e.g.) $\{|\Gamma_{in}|_{max}, -|\Gamma_{in}|_{max}, j|\Gamma_{in}|_{max}\}$. Then getting the circumscribed circle for the three load reflection coefficients using standard algebra yields the full Γ_{load} region that can be mapped onto $|\Gamma| \leq |\Gamma_{in}|_{max}$, per state of the switchable matching network.

3. the circular mappable areas for each the 2^N states of the switchable matching network are plotted together on the Smith chart. This plotting is a numerical/graphics step required for the next step.
4. the largest inscribed circle that only encloses mappable areas is determined graphically. As all mappable areas are plotted together on the Smith chart this is a quite straightforward numerical procedure on the graphics representation derived in the third step.

In the optimization procedure, an M-dimensional sweep of the M matching network component values is executed, starting at a coarse grid, selecting the best performing settings and (about that best point) redoing the M-dimensional sweep at increasingly higher resolution.

For *lossless* matching networks, getting the Γ_{load} for a specific Γ_{in} is described in Appendix B to E. For *lossy* matching networks, all our analyses use S-parameter descriptions to derive the matching properties. From these we can straightforwardly derive the matching efficiency and power efficiency. The derivation of the behavior of a few types of matching networks is already described in terms of S-parameters. E.g., a lossy PI-network, getting S-parameters was done by firstly deriving Y-parameters after which Y-to-S parameter conversion was done [44].

APPENDIX D

This appendix shows a mathematical derivation of the impedance matching behavior loaded transmission line based matching networks, such as shown in Fig. 4. Using the notations in Fig. 5 and working from source towards the load,

$$\Gamma_1 = \frac{\frac{1}{Z_0} - Y_1}{\frac{1}{Z_0} + Y_1} e^{-j2\theta} \text{ with } Y_1 = Y_{source} + b_1 \cdot j\omega C_1$$

where θ is the length of the leftmost transmission line, and b_n denotes the value of control bit of switchable capacitor C_n . Working towards the load impedance, the exact same relations (except for the values of θ_n and C_n) follow, recursively:

$$\Gamma_{out} = \frac{\frac{1}{Z_0} - Y_n}{\frac{1}{Z_0} + Y_n} e^{-j2\theta_n} \text{ with } Y_n = \frac{1}{Z_0} \frac{1 + \Gamma_{n-1}}{1 - \Gamma_{n-1}} + b_n \cdot j\omega C_n$$

where C_n is the n^{th} capacitor.

APPENDIX E

This appendix shows a mathematical derivation of the matching performance of a branch line coupler based matching network as shown in Fig. 6. In the derivation a_1, a_2, a_3 and a_4 are the incident waves of the four ports of the branch line coupler while b_1, b_2, b_3 and b_4 are the reflected waves.

Γ_{x2} and Γ_{x3} are the reflection coefficients of the two (switchable) reactive loads at port 2 respectively 3.

$$\begin{cases} b_1 = -\frac{j}{\sqrt{2}}a_2 - \frac{1}{\sqrt{2}}a_3 = -\frac{j}{\sqrt{2}}\Gamma_{X2}b_2 - \frac{1}{\sqrt{2}}\Gamma_{X3}b_3 \\ b_2 = -\frac{j}{\sqrt{2}}a_1 - \frac{1}{\sqrt{2}}a_4 \\ b_3 = -\frac{1}{\sqrt{2}}a_1 - \frac{j}{\sqrt{2}}a_4 \\ b_4 = -\frac{1}{\sqrt{2}}a_2 - \frac{j}{\sqrt{2}}a_3 = -\frac{1}{\sqrt{2}}\Gamma_{X2}b_2 - \frac{j}{\sqrt{2}}\Gamma_{X3}b_3 \end{cases}$$

The input and output of the matching networks are at port 1 and 4, yielding

$$\begin{cases} b_1 = \frac{1}{2}(\Gamma_{X3} - \Gamma_{X2})a_1 + j\frac{1}{2}(\Gamma_{X2} + \Gamma_{X3})a_4 \\ b_4 = j\frac{1}{2}(\Gamma_{X2} + \Gamma_{X3})a_1 + \frac{1}{2}(\Gamma_{X2} - \Gamma_{X3})a_4 \end{cases}$$

from which readily a two-port S matrix can be obtained:

$$S = \begin{pmatrix} \frac{1}{2}(\Gamma_{X3} - \Gamma_{X2}) & j\frac{1}{2}(\Gamma_{X2} + \Gamma_{X3}) \\ j\frac{1}{2}(\Gamma_{X2} + \Gamma_{X3}) & \frac{1}{2}(\Gamma_{X2} - \Gamma_{X3}) \end{pmatrix}$$

Now the output reflection coefficient of the matching network can be derived, as a function of the (switchable) Γ_{x2}, Γ_{x3} and the switchable shunt capacitor C:

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_1}{1 - S_{11}\Gamma_1}$$

with

$$\Gamma_1 = \frac{\frac{1}{Z_0} - Y_1}{\frac{1}{Z_0} + Y_1} \text{ and } Y_1 = \frac{1}{R_{source}} + j\omega C$$

APPENDIX F

This appendix shows the mathematical derivation of matching capabilities of a circulator-based impedance matching network as depicted in Fig. 8. In the expression C is the value of the shunt capacitance. A base property of a circulator is

$$\Gamma_{out} = \Gamma_1 \Gamma_X$$

where in the circuit in Fig. 10

$$\Gamma_1 = \frac{\frac{1}{Z_0} - Y_1}{\frac{1}{Z_0} + Y_1} \text{ and } Y_1 = \frac{1}{R_{source}} + j\omega C$$

and where Γ_X is the reflection coefficient of the switchable reactance X (the combined effect of jX_1, jX_2 and jX_3 with their switches). Assuming $Z_0 = R_0$, to get N uniformly distributed phase shifts $\angle\Gamma_X$, the corresponding reactances are given by $X_n = R_0 \arctan(n\pi/N)$ which are far from uniformly spaced. This results in having to have more switched reactances than required for the mathematical minimum as defined in [31] that assumes uniform spacing.

APPENDIX G

This appendix is about the noise figure of general matching networks, applied to a 4-bit tunable PI network topology.

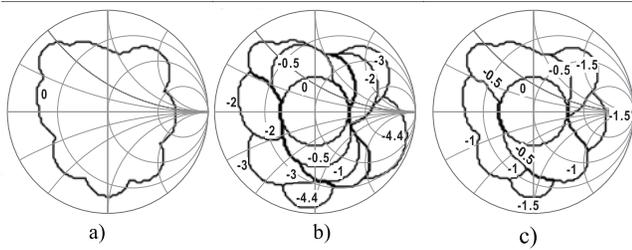


Fig. 22. Available power gain in dB for (a) a lossless 4 bit tunable PI network designed for $|\Gamma_{in}| \leq 1/3$, (b) a silicon implementation, (c) an implementation in GaAs.

According to [45], the noise figure NF of a passive lossy matching network is related to the available power gain G_{ava} by

$$NF = \frac{1}{G_{ava}}$$

where

$$G_{ava} = \frac{|S_{21}|^2}{1 - |S_{22}|^2}$$

where S_{11} , S_{21} , S_{12} and S_{22} are the S parameters of the matching network. Below are contour plots showing the available power gain G_{ava} for the PI network topology (in dB); dropping the minus sign yields the noise figure.

Three implementations are taken into account: a lossless implementation ($Q_C = Q_L \rightarrow \infty$), implementation in low ohmic silicon ($Q_C = 20$, $Q_L = 10$) and a GaAs implementation ($Q_C = 60$ and $Q_L = 35$). The quality factors are assumed to be independent from the component value and they include the switch resistor. Fig. 22(a)–(c) show the contours for G_{ava} for the three forenamed situations; the outer contours demark the matchable region.

Clearly the lossless network is noiseless; whereas the noise figure can be as high as 4.4 dB in the silicon implementation and up to 1.5 dB in GaAs, for the 4-bit tunable PI network used as vehicle.

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