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Remy Vauche, Eloi Muhr, Olivier Fourquin, Sylvain Bourdel, Jean Gaubert, et al.. A 100 MHz PRF IR-UWB CMOS Transceiver With Pulse Shaping Capabilities and Peak Voltage Detector. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64 (6), pp.1612-1625. 10.1109/TCSI.2017.2669902 . hal-01694218

HAL Id: hal-01694218

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A 100MHz PRF IR-UWB CMOS Transceiver with Pulse Shaping Capabilities and Peak Voltage Detector

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Abstract— This work presents a high rate IR-UWB transceiver chipset implemented in a 130 nm CMOS technology for WBAN and biomedical applications in the 3.1GHz-4.9GHz band. The transmitter is based on a pulse synthesizer and an analytical up-converted Gaussian pulse is used to predict its settings. Its measured peak to peak output voltage is equal to 0.9Vpp on a 100Ω load for a central frequency of 4GHz, and a supply voltage of 1.2V, which gives an emitted energy per pulse of 0.64pJ. The receiver is a non-coherent architecture based on a LNA followed by a peak voltage detector. A BER of 10^{-3} is measured for a 3.1GHz-4.9GHz input peak-to-peak pulse amplitude of 1.1mV which corresponds to a sensitivity of -85.8dBm at 1Mbps and gives a communication range estimated to 1.9m.

Index Terms— IR-UWB, Ultra-Wideband CMOS transceiver, WBAN, non-coherent receiver, Pulse shaping Capabilities

I. INTRODUCTION

Ultra-WideBand Impulse Radio (IR-UWB) is a well-known technique based on the transmission of short duration pulses. Such approach is well suited for low range, medium rate and low power applications such as Body Area Network (BAN), Wireless Sensor Network (WSN) or ranging [1][2]. Since the Federal Communications Commission (FCC) has approved UWB communications in the 3.1-10.6GHz bandwidth, many successful works have been reported showing the ease of making energy efficient systems with IR-UWB.

Recently, the research field has moved towards new challenges such as system reliability, integration and cost issues or high energy efficiency. In this context, a few meter range 100Mbps transceiver designed for BAN applications is presented. Here, the approach is to alleviate as much as possible the system constraints while allowing high tuning capabilities to ensure a successful design.

High energy efficiency is intrinsically based on the gated nature of the IR-UWB signal. To fully exploit this property, duty-cycled systems can be used. A first approach consists in duty-cycling the system at the bit rate [1] which improves the system immunity to narrow band interferers and reduces power consumption. For low bit rates (less or equal to 1Mbps), an on-time less than ten percent of the bit time can be reached with fast turn-on devices and pulse coupled oscillator based architectures for synchronization [3]. A lower on-time (close to 30ns) has been reached with a 100MHz All Digital - Clock and Data Recovery (AD-CDR) having 10ns jitter [4]. However, when a medium rate (e.g., 15.6Mbps) is considered,

the Pulse Repetition Period (PRP) is around a few tens of nanoseconds (e.g., 66.7ns) and the precision of the duty-cycling clock must be high enough (a few nanoseconds) in order to reduce efficiently the power consumption. In this case, the clock frequency of the AD-CDR must be increased up to 1GHz which impacts the system power consumption [4]. Solutions based on synchronized modulation schemes [5] have also been proposed. However, they require the transmission of additional pulses for synchronization which reduces the energy efficiency and the payload bit rate of the system.

For medium rate, a solution to reduce power consumption is to achieve a duty-cycling at burst rate. As presented in [6], this approach can reach the same energy efficiency as in a bit rate duty-cycled system, while the duty-cycling clock precision is moved towards a few tens of microseconds which releases constraints on the CDR jitter characteristics. In this case, the required idle time T_{IDLE} to maintain constant the Power Spectral Density (PSD) is equal to $T_{SWEEP} (1 - PRF_{MEAN} / PRF_{BURST})$ where T_{SWEEP} is the sweep time imposed by FCC to measure the PSD (1ms), PRF_{BURST} the Pulse Repetition Frequency (PRF) during the burst, and PRF_{MEAN} the mean PRF averaged on T_{SWEEP} . By considering PRF_{MEAN} (resp. PRF_{BURST}) is equal to 15.6MHz (resp. 100MHz), the ideal on-time T_{ON} is 156μs, the ideal idle time T_{IDLE} is 844μs, and the number of pulses per burst is 15.6k. In the context of a duty-cycled at burst level, the synchronization scheme is no more an issue and is not addressed in this paper.

However, a high rate capability (around 100MHz) is decisive to minimize the ratio PRF_{MEAN} / PRF_{BURST} and to maximize the power reduction. Such approach also requires a high data rate CDR which can be duty cycled at the burst rate like the receiver. Moreover, the acquisition time of an AD-CDR will not impact the energy efficiency because the number of pulses required for the acquisition (32 in [4]) is negligible regarding the number of pulses in the burst.

Regarding the transmitter, controlling the radiated spectrum is necessary to comply with standard masks or to reject spectrum side-lobes. Passive solutions based on external filters or integrated filters can be used [7] to shape the pulse but they dramatically impact the size and the cost. Solutions based on active devices [8][9] suite better the integration issues but need high tuning capabilities to compensate Process Voltage and Temperature (PVT) variations. In this context, several solutions have been proposed to control the shape of the

pulses [10][11][12]. Among these solutions, digital synthesis [12] is a promising approach because it operates without inductor and allows a fine tuning of the pulse shape to be obtained.

On the receiver side, Non-Coherent (NC) detection is often used to reduce complexity and save power in IR-UWB receivers. Among the different architectures, energy detectors based on super-regenerative or self-mixing coupled to integrators achieve good sensitivity performances [13][14]. However, the need for synchronization schemes operating at symbol rate increases the integration issues and reduces the maximum achievable bit rate. Another way of designing NC receivers is to use Peak Voltage Detectors (PVD). On the one hand, PVDs suffer from a lower theoretical sensitivity since the signal is not collected all along the symbol duration time as it is in energy detectors. However, using PVDs can be justified in case of a short-range transceiver. On the other hand, PVDs are intrinsically asynchronous and are well suited for a burst duty-cycled receiver.

In this paper, a high rate 3.1GHz-4.9GHz IR-UWB transceiver for WBAN applications is presented. It uses a pulse synthesizer with pulse shaping capabilities on the emitter side and a PVD at the receiver side. Section II gives a system overview and analyses the theoretical performance in terms of Bit Error Rate (BER). Since the transmitter architecture is based on pulse synthesis, an analytical pulse model is proposed to predict the required pulse shape. Next, this shape is used to estimate BER performance of the peak voltage detector implemented in the receiver. Section III and section IV present respectively the transmitter and the receiver parts of the transceiver. In Section V, measurement results obtained with the proposed transceiver are presented and compared with previous published works.

II. SYSTEM OVERVIEW

In this section, the proposed IR-UWB transmitter, which is based on pulse synthesis technique, is presented and an analytical model of Gaussian up-converted pulse is proposed to predict the waveform to generate according to the targeted bandwidth. Next, after a presentation of the proposed NC IR-UWB receiver based on a peak voltage detector, its BER performance is estimated with the help of the presented pulse model.

A. Proposed IR-UWB Transmitter

To communicate in the allocated FCC band, an IR-UWB transmitter requires a pulse generator to transmit data. Lots of approaches have been developed to generate UWB signals but they have generally few capabilities regarding spectrum shapes programmability.

Solutions based on the modulation of a carrier by an analog signal, such as a triangular waveform or a raised cosine, have

been proposed [15][16] in order to shape the envelop of the emitted pulse, to better fit standard masks, and to reduce side lobes. This approach is efficient in terms of side lobe rejection but lacks of reconfiguration and tuning capabilities. All digital architectures, which are more flexible than analog ones, have been proposed. They allow the pulse shape to be tuned in case of PVT variations [10][17]. All-digital pulse generators are generally based on Digitally Controlled Oscillator (DCO) [11], Digital Delay Line (DDL) [10], or both [17]. Compared to a DCO based generator, a DDL based pulse generator can be easily duty-cycled to reduce the power consumption since it requires shorter start-up time. Moreover, it is possible to adjust each sub-lob of the pulse to accurately tune the envelop and control the side-lobe level.

As shown in Fig. 1, an UWB pulse $p(t)$ can be seen as a linear combination of N baseband pulses ($g_n(t)$) as follows:

$$p(t) = \sum_{n=1}^N A_n \cdot g_n \left(t - \sum_{p=1}^{n-1} \tau_p \right) \quad (1)$$

where A_n and τ_n are respectively magnitude and width of the n^{th} baseband pulse. To synthesize $p(t)$, two circuits can be associated, a N baseband pulses generator and a N baseband pulses combiner, as shown in Fig. 1. The baseband pulses generator allows each baseband pulse (from $n=1$ to N) to be generated according to the targeted width (τ_n from $n=1$ to N). Next, baseband pulses are combined by the baseband pulses combiner according to the targeted magnitude (A_n from $n=1$ to N). The proposed IR-UWB transmitter is based on this approach.

To optimize the bit rate and/or the communication range with a NC receiver while the maximum mean power given by FCC is respected, it is proposed here to use a Random Alternate On-Off Keying modulation (RA-OOK) [6]. This modulation does not have discrete spectrum in its PSD but is similar to an OOK modulation from the receiver point of view. Indeed, to send a binary '0', no pulse is emitted. However, to send a binary '1', a positive pulse or a negative pulse is randomly sent.

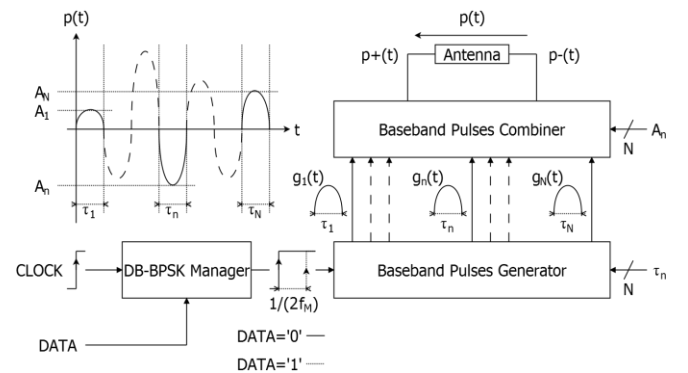


Fig. 1. Proposed IR-UWB transmitter based on pulse synthesizing technique.

To generate these positive and negative pulses, a Delay-Based Binary Phase Shift Keying (DB-BPSK) modulator can be used [7][18]. It is based on a delay cell which will softly delay or not the CLOCK triggered signal according to the DATA logical state indicated in Fig. 1. This allows positive and negative pulses of a BPSK modulation to be approximated and also allows the discrete spectrum of the emitted PSD to be suppressed which reduces the mean emitted power. To obtain the best results, the CLOCK delay ($\tau_{DB-BPSK}$) must be equal to $1/(2 \cdot f_M)$ with f_M , the frequency where the emitted power is maximum [18]. In this case, the mean emitted power can be increased until the authorized limit by increasing the bit rate and/or the energy of each pulse [7].

This DB-BPSK modulator has been implemented in the proposed IR-UWB transmitter and it is also used to obtain a Random Alternate On-Off Keying modulation [6] by using the following rules. To send a binary '0', no rising edge is provided on CLOCK and no pulse is emitted. To send a binary '1', a rising edge is provided on CLOCK and a positive or negative pulse is emitted according to the state of DATA.

B. UWB pulse waveform estimation

The use of pulse synthesizers as IR-UWB transmitters implies the definition of an UWB pulse which can match with the targeted bandwidth, in order to get an ad hoc configuration for A_n and τ_n control inputs. To define this pulse, it is possible to compute the inverse Fourier transform of the targeted frequency mask, or to analyze the impulse response of a filter which has a compliant frequency response. The fifth [19][20] and the seventh [21][22] Gaussian derivatives can also be used especially to match with FCC mask. However, these methods lead to a high number N of couples (A_n , τ_n) to synthesize when a 3.1GHz - 4.9GHz bandwidth is targeted. To address this bandwidth with a few couples (A_n , τ_n), triangular or Gaussian up-converted pulses have to be preferred. However, the Gaussian up-converted pulse has a better spectral efficiency η_{SE} than the triangular one. This spectral efficiency η_{SE} can be defined as follows:

$$\eta_{SE} = \frac{\frac{1}{Z_L} \int_{\mathbb{R}} p^2(t) \cdot dt}{E_{REF}} = \frac{BW_{-XdB}}{A^2} \int_{\mathbb{R}} p^2(t) \cdot dt \quad (2)$$

where Z_L is the impedance load of the antenna connected to the pulse generator output, and E_{REF} is the energy of a reference pulse which is here an up-converted cardinal sine having the same magnitude (A) of the emitted pulse and occupying the same bandwidth (BW_{-XdB}). In this case, it appears that the Gaussian up-converted pulse has an efficiency of 86% instead of 56% for the triangular one. Thus, to keep N low and a high emitted energy distribution, an odd Gaussian up-converted pulse is proposed here. It only requires $N/2$ values of A_n in addition to one τ_n value. Moreover, it can be easily tuned to match with different spectrum masks since the Fourier transform of a Gaussian function is another analytically computable Gaussian function.

The proposed odd Gaussian up-converted pulse can be written in time domain as follows:

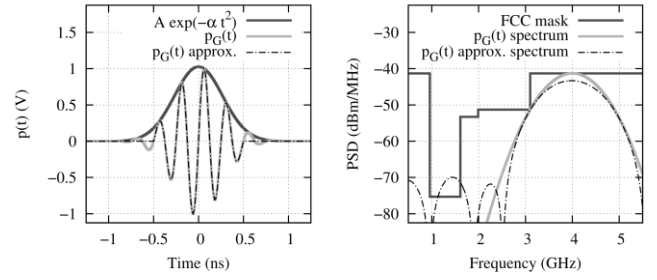


Fig. 2. Example of transient and frequency responses of the proposed Gaussian up-converted pulses with $A_{PP}=2V$, $f_M=4GHz$, and $BW_{-10dB}=1.8GHz$.

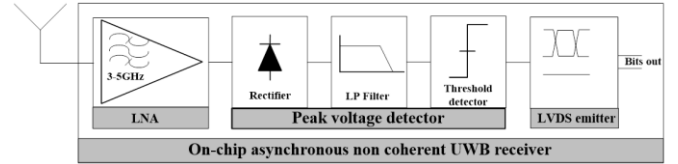


Fig. 3. Proposed IR-UWB NC receiver based on peak voltage detection.

$$p_G(t) = A \exp(-\alpha t^2) \sin(2\pi f_M t) \quad (3)$$

where A is the maximum of the Gaussian envelope and α , a parameter which sets the pulse bandwidth. In this case, the width τ_n of every baseband pulses is also equal to the optimum value of $\tau_{DB-BPSK}$ which is $1/(2 \cdot f_M)$. The maximum of the Gaussian envelope A can be related to the peak to peak magnitude A_{PP} of the pulse as follows:

$$A = \frac{A_{PP}}{2} \exp\left[\frac{\alpha}{(4f_M)^2}\right]. \quad (4)$$

The magnitude of the single side Fourier transform of $p_G(t)$ can be written as follows:

$$|\hat{p}_G(f)| = A \sqrt{\frac{\pi}{2\alpha}} \exp\left(-\frac{[2\pi(f - f_M)]^2}{4\alpha}\right) \quad (5)$$

and allows the α parameter to be computed as a function of the targeted bandwidth BW_{-XdB} defined at $-X$ dB as follows:

$$\alpha = \frac{\pi^2 BW_{-XdB}^2}{2 \ln(10^{X/10})}. \quad (6)$$

Moreover, the energy emitted per pulse E_{P-G} can be computed from (4) and is equal to:

$$E_{P-G} = \frac{A^2}{2Z_L} \sqrt{\frac{\pi}{2\alpha}} \left[1 + \exp\left(-\frac{[4\pi f_M]^2}{8\alpha}\right) \right] \quad (7)$$

This result can be approximated with an error of 5% with the following expression:

$$E_{P-G} \approx \frac{A^2}{2Z_L BW_{-XdB}} \sqrt{\frac{\ln(10^{X/10})}{\pi}} \quad (8)$$

and enables energy estimation for other works comparison with only few parameters [6].

An example of this Gaussian up-converted pulse is shown in Fig. 2 for the targeted 3-5GHz bandwidth. However, as the Gaussian envelope defined here by $A \cdot \exp(-\alpha \cdot t^2)$ is never equal to zero and that an infinite duration pulse cannot be synthesized, it is necessary to approximate $p_G(t)$. In Fig. 2, $p_G(t)$ is approximated by the height higher monocycle of the Gaussian pulse. This approximation shows a loss of 2dB in frequency domain and an unwanted side lobe around 1.5GHz. The both can be corrected thanks to pulse synthesis by using a fine tuning of A_n values.

C. Proposed Non-Coherent Receiver

Usually Non-Coherent UWB receivers use energy detection for pulse detection. In these architectures an image of the pulse energy is obtained by squaring and integrating the incoming signal during the symbol duration time. The signal amplitude at the squarer output, which varies as the square of the amplitude of the input signal, quickly becomes very small and unusable when the receiver moves away from the transmitter. Consequently, in order to obtain signals which exceed the noise floor of the stages downstream of the squarer, a large amount of amplification must be provided by the Low Noise Amplifier (LNA), whereas achieving high amplification gain with large bandwidth is difficult in low cost CMOS technologies. Although it is less efficient from a theoretical point of view, a NC receiver based on peak voltage detection could provide an interesting alternative which relaxes design constraints regarding the LNA gain, while being compatible with the requirements of many short range applications.

The proposed NC receiver architecture which uses peak voltage detection is described in Fig. 3. It is composed of a band pass type LNA that drives an asynchronous peak detector based on envelope detection. The peak detector provides a short duration (1.5ns) baseband pulse for each incoming UWB pulse. The single ended numeric signal is then converted into a Low Voltage Differential Signaling (LVDS) signal in order to provide standardized signals to the board interface.

D. Performance analysis of peak voltage detection

In this section, an estimation of the BER which can be achieved with peak voltage detection is presented by considering an OOK coding, an AWGN channel, and no multipath propagation.

As shown in [23][24], the dimensionality of the space of finite energy signals is about $2 \cdot B \cdot T + 1$ with a bandwidth B and a time spread T . From its equivalent formula in the discrete domain, it is possible to perform the BER calculation. In this work, it is then assumed that, during the symbol duration time T_s , the continuous time domain signal at the receiver input can be replaced by P discrete samples of the received signal obtained at the Nyquist rate:

$$P = 2 \cdot f_{\text{MAX}} \cdot T_s + 1. \quad (9)$$

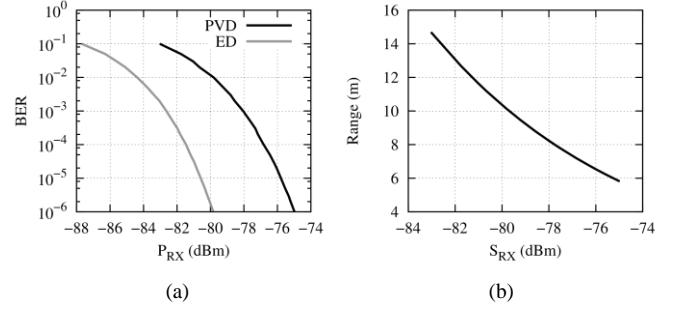


Fig. 4. Bit error rate versus the received power for OOK modulated 3.1GHz-4.9GHz pulses at a rate of 100Mbps and with $NF_{LNA} = 3\text{dB}$ for a Peak Voltage Detector (PVD) and an Energy Detector (ED) (a). Theoretical range with PVD as a function of the receiver sensitivity when a 0.52pJ (0.45V peak magnitude) pulse is emitted on a $2 \times 50\Omega$ differential antenna (b).

Given that, for the 3.1GHz-4.9GHz bandwidth UWB signal considered here, the noise bandwidth (1.8GHz) is close to the maximum spectrum frequency f_{MAX} (4.9GHz), we also assume that the noise samples are independent. The discrete samples of the received signal are the sum of the samples of the unnoisy signal and of the noise. Assuming an AWGN channel and the independence of the noise samples, the probability density function of the noise voltage for each sample is given by:

$$p_N(v) = \frac{1}{\sqrt{2\pi\sigma_N^2}} \exp\left(-\frac{v^2}{2\sigma_N^2}\right). \quad (10)$$

Assuming that the noise bandwidth is the same that the bandwidth (BW) of the signal, the noise variance σ_N at the LNA output is given by:

$$10\log\left(\frac{\sigma_N^2}{R_{LNA}}\right) = 10\log(K \cdot T \cdot BW) + G_{LNA} + NF_{LNA} \quad (11)$$

where K is the Boltzmann constant, T the absolute temperature, R_{LNA} , G_{LNA} and NF_{LNA} the input resistor, the gain, and the noise figure of the LNA.

For an OOK coding, the error probability is given by:

$$\text{Pr}_E = 0.5 \cdot \text{Pr}_{FA} + 0.5 \cdot \text{Pr}_{ND} \quad (12)$$

where Pr_{FA} is the probability of a false alarm and Pr_{ND} is the probability of a non-detection.

A false alarm occurs when the detector output switches to the high level while no pulse has been sent during the symbol duration time. So a false alarm occurs when the noise level crosses the value of the decision threshold S_D for at least one of the noisy samples during the symbol duration time. So, the probability of a false alarm is given by:

$$\text{Pr}_{FA} = 1 - \left[1 - \frac{1}{\sqrt{2\pi\sigma_N^2}} \int_{S_D}^{+\infty} \exp\left(-\frac{v^2}{2\sigma_N^2}\right) dv \right]^P \quad (13)$$

where P is the number of samples during the symbol duration time T_s given by (9).

A non-detection occurs when a pulse is sent and the magnitude of the noisy signal remains lower than the decision threshold during the symbol duration time. This corresponds for the equivalent discrete signal when no noisy signal sample crosses the value of the decision threshold S_D during the symbol duration time. So the probability of a non-detection is given by:

$$\Pr_{ND} = \prod_{i=0}^P \left[\frac{1}{\sqrt{2\pi\sigma_N^2}} \int_{-\infty}^{S_D - V_S(t_i)} \exp\left(\frac{-v^2}{2\sigma_N^2}\right) dv \right] \quad (14)$$

where $V_S(t_i)$ is the magnitude of the discrete samples of the unnoisy signal at the peak voltage detector input. The shape of $V_S(t_i)$ depends on the signal bandwidth and its magnitude depends on the received power and the LNA gain. In our case $V_S(t_i)$ is computed from (3) knowing the emitted power at the emitter side, the communication range, and the LNA gain.

For a given received power, a given data rate and a given decision threshold, the BER value is obtained with the equations (12), (13) and (14). For a given BER, there is an optimal decision threshold S_D that minimizes the received power and balances \Pr_{FA} and \Pr_{ND} . So, by using equations (12), (13), (14) and an iterative algorithm, the receiver sensitivity can be obtained for a given BER. Finally, the use of the Friis formula with this minimum received input power gives the achievable range for a given emitted power. By using the UWB pulse defined by (3) for a data rate of 100Mbps with an OOK encoding and a 1.8GHz -10dB bandwidth centered at 4GHz, the results plotted in Fig. 4 are obtained. The same analysis has been done for an ideal Energy Detector (ED) in the appendix. Results are also shown in Fig. 4 for an integration time equal to the pulse width (2ns) when a 100Mbps OOK is considered. Results are also shown in Fig. 4 and even if the peak voltage detection shows a lower theoretical sensitivity than energy detection, it is sufficient for many short range applications. Indeed, it is possible to observe in Fig. 4 that a theoretical range of 8.28m is achievable with a peak voltage detection for a BER value of 10^{-3} when a power of -78dBm is received. This range is obtained when a 0.9Vpp pulse on a $2 \times 50\Omega$ differential antenna is considered on the emitter side, which is achievable in CMOS technologies [7].

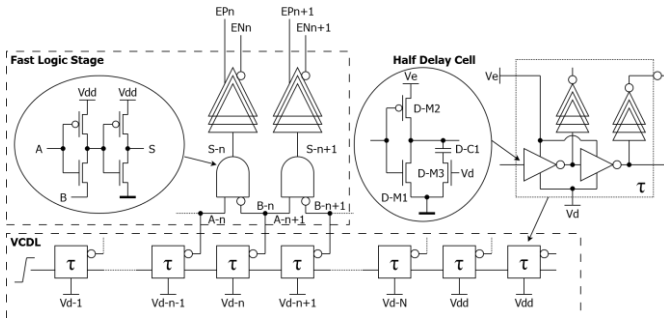


Fig. 5. Design of the proposed baseband pulses generator.

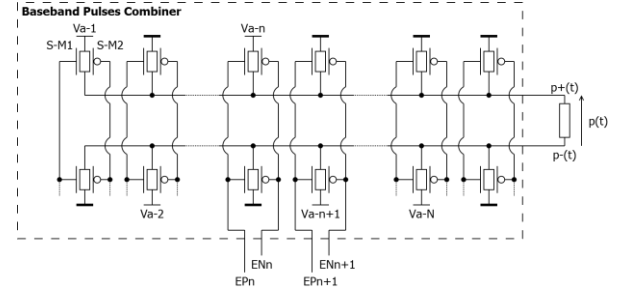


Fig. 6. Design of the proposed baseband pulses combiner.

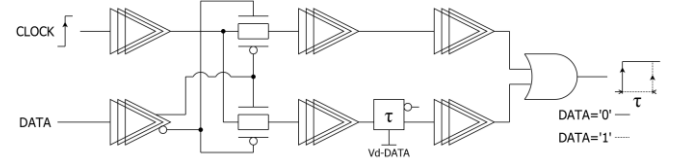


Fig. 7. Design of the proposed DB-BPSK manager.

III. TRANSMITTER DESIGN

The presented pulse synthesizer shown in Fig. 1 has been designed in order to synthesize UWB pulses for bandwidths upper than 1.5GHz centered on a frequency between 3GHz and 5GHz. To satisfy the targeted bandwidth, the designed pulse synthesizer is able to generate UWB pulses composed of 1 to 8 baseband pulses. All the baseband pulse widths τ_n are controlled by the same biasing voltage except the first and the last in order to compensate for their slower responses due to their positions. Finally, a DB-BPSK pulse manager is integrated in order to implement RA-OOK modulation which allows bit rate and/or pulse energy to be increased while legal maximum powers are respected. The design of each part shown in Fig. 1 is now presented.

A. Baseband Pulses Generator Design

The baseband pulses generator is composed of two parts, a Voltage Controlled Delay Line (VCDL), and a fast logic stage as shown in Fig. 5.

The VCDL is here a delay line where a rising edge is propagated through tunable delay cells. Each delay cell is built of two buffered stages based on a CMOS inverter loaded by a capacitor (D-C1) in series with a NMOS analog switch (D-M3) which gives a large delay tuning range. The width of each baseband pulse (τ_n) depends on the propagation delay time of the n^{th} stage of the VCDL which is set by D-M3, and D-C1 sizes and V_{d-n} value. In this implementation, all V_{d-n} are connected to the same control voltage since the proposed odd up-converted Gaussian pulse requires similar τ_n , except for the first (V_{d-1}) and the last (V_{d-N}) delay cells which are slower.

Next, the fast logic stage combines rising edges at the output of the n^{th} cell (A) and at the output of the $n+1^{\text{th}}$ cell (B) using a fast logic gate to achieve the n^{th} baseband pulse ($g_n(t)$). To increase the switching speed and also the maximum pulse central frequency, the fast logic stage has been modified from the architecture presented in [25]. Then, the number of nodes has been reduced in order to limit the parasitic capacitances due to interconnections. However, this fast logic stage is able

to generate the complementary baseband pulses required by the baseband pulses combiner (EPn and ENn).

B. Baseband Pulses Combiner Design

To generate UWB pulses with 1 to 8 baseband pulses, the baseband pulses combiner is based on 8 H-bridge paths going through the load as shown in Fig. 6. Each H-bridge path is composed of two transmission gates (S-M1 and S-M2) and is driven by the balanced baseband pulses on both sides of the load. The magnitude of the recombined baseband pulses (A_n) is controlled by applying different control voltages (V_{a-n}) at the top of each H-bridge path. An advantage of this structure is that the obtained A_n is quasi-proportional to V_{a-n} and also can be easily controlled. To alternate the sign of the baseband pulses, V_{a-n} are alternatively applied to the top and to the bottom of the paths. The baseband pulses combiner has been designed in order to be able to drive a 100Ω differential antenna with a peak-to-peak magnitude equals to the supply voltage in post-layout simulations (S-M1 and S-M2 widths are respectively equal to $200\mu\text{m}$ and $480\mu\text{m}$).

C. DB-BPSK Manager Design

As shown in Fig. 7, the DB-BPSK manager consists of two paths, one where CLOCK is delayed, and another one where CLOCK is not delayed. It uses standard CMOS logic gates as buffers, transmission gates, and an OR gate. However, it is equally composed of one delay cell which allows CLOCK rising edge to be delayed when DATA is equal to '1'. As the delay cell is the same as the one used in the VCDL, and that all baseband pulses of the synthesized pulse have the same time duration (τ_n), V_{d-DATA} has to be connected to V_{d-n} to obtain $\tau_{DB-BPSK}$ equal to $1/(2 \cdot f_M)$. In this configuration, the DB-BPSK modulation is close as much as possible to the BPSK one in terms of spectrum. To ensure the realization of this

configuration, buffers are placed on the both sides of the delay cell, and the same buffers are equally placed on the no delayed path.

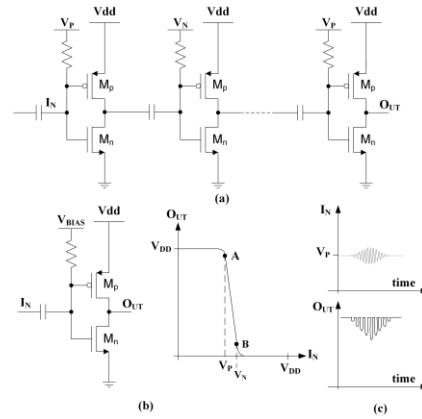


Fig. 10. Rectifier stage: (a) Schematic, (b) CMOS inverter based rectifier cell principle, (c) Simplified waveforms obtained at the rectifier input/output.

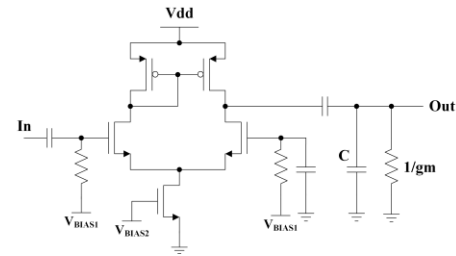


Fig. 11. First order low-pass filter schematic.

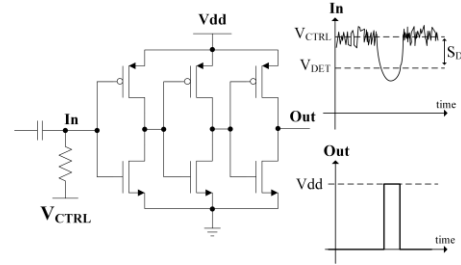


Fig. 12. Decision stage circuit.

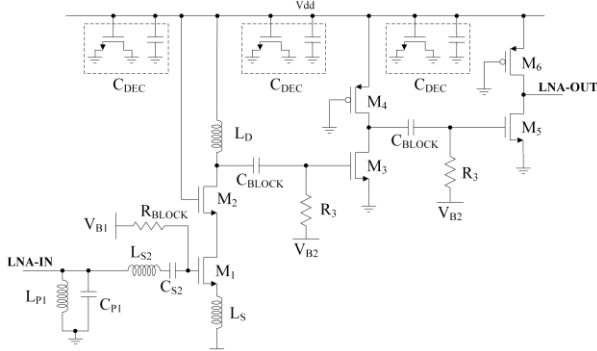


Fig. 8. Schematic of the low noise amplifier circuit.

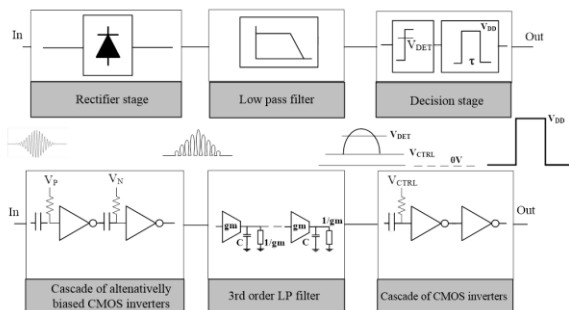


Fig. 9. Peak detector principle and architecture.

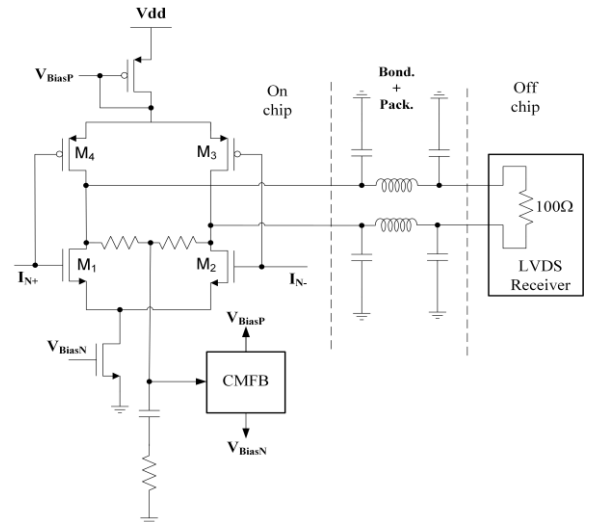


Fig. 13. LVDS transmitter schematic.

IV. NON-COHERENT RECEIVER DESIGN

The presented NC IR-UWB receiver shown in Fig. 3 has been designed to be used with 3GHz-5GHz pulses. It consists of a LNA, a voltage peak detector, and a LVDS driver, which are described in this section.

A. LNA

The LNA architecture is depicted in Fig. 8. The LNA includes three stages: a LC matched input stage and two stages with active load. The LC matched input stage (M_1 , M_2) achieves a bandpass response in the 3-5GHz bandwidth [26]. In a low-cost perspective, the use of an off-chip filter should be avoided, so the LNA bandpass response reduces both parasitic signals and equivalent noise bandwidth before the pulse detector input. The two active load stages (M_3 , M_4 and M_5 , M_6) provide an additional gain controlled by the voltage V_{GAIN} . The LNA sizing process is done to minimize the noise figure and to maximize the voltage gain as presented in [26]. For such a high gain amplifier at high frequency, signal integrity and stability are important issues. The power supply pads (V_{DD}) are decoupled by using several MIM and MOS capacitors (C_{DEC} in Fig. 8) in order to get a large on chip capacitor value (a few hundred of pF) leading to low return path ground impedance at high frequencies.

B. Peak detector

The proposed peak detector architecture is given in Fig. 9. The incoming UWB pulse is first rectified and a low-pass filter is then used to extract the pulse envelope and to reduce the noise bandwidth. Finally a decision stage based on a comparator followed by a shaping circuit provides a rectangular pulse when pulse envelope crosses the decision voltage V_{DET} .

1) Rectifier stage

The rectifier is the key element of the detector architecture. A wide bandwidth rectification is achieved by using a biased CMOS inverters chain. Part (b) of Fig. 10 depicts the operation of a biased CMOS inverter. If the biasing voltage V_{BIAS} is set to V_P , the CMOS inverter operates close to the point A of its characteristic. By using this operating point, the positive part of the input signal is amplified and inverted while the negative part of the input signal is suppressed. Conversely, if V_{BIAS} is set to V_N the point B, the CMOS inverter operates close to the point B of its characteristic. In this case, the negative part of the input signal is amplified and inverted while the positive part of the input signal is suppressed. By cascading CMOS inverters alternatively biased with V_P and V_N voltages, the input signal is rectified and also amplified. The rectifier stage uses five AC coupled CMOS inverters alternatively biased with voltage V_P and V_N . Part (c) of Fig. 10 shows the simplified waveforms obtained in the case of an even number of rectifier cells.

2) Low-pass filter

The low-pass filter consists of three cascaded AC coupled first-order filters with a cutoff frequency of 2GHz. As shown in Fig. 11, the first order low-pass cell is achieved by a single-ended transconductance loaded by a capacitor and a resistor. This simple architecture does not allow the filter cutoff

frequency to be adjusted, but avoids the implementation of a common mode feedback circuit commonly used in gm-c filters.

3) Decision stage

As shown in Fig. 12, the decision stage circuit is built from CMOS inverters. The gate of the first inverter is externally biased by a control voltage V_{CTRL} which allows the noise amplitude at its input to be maintained up the switching threshold of the inverter. A set of two other CMOS inverters follows the first one in order to generate a clean logic signal. The amplitude of the UWB pulse envelope is compared to a threshold voltage V_{DET} at a distance S_D of V_{CTRL} . If the pulse envelope crosses the threshold V_{DET} , a pulse is detected and the output signal goes to V_{DD} long enough to enable the post-detection circuits to properly process the signal. The decision threshold value is set to optimize the trade-off between the false alarm rate, due to the influence of noise, and the non-detection rate and so the receiver sensitivity.

C. LVDS transmitter

The LVDS interface allows high bit rates (up to 100Mbps⁻¹) to be achieved for chip to board interface with a low sensitivity to parasitic capacitors and inductors. The implemented LVDS transmitter circuit uses the typical architecture based on four MOS switches in a bridge configuration as shown in Fig. 13. When the pair (M_1 , M_3) is active and the pair (M_2 , M_4) is off, the polarity of the output current is positive together with the differential output voltage. Conversely, if the pair (M_1 , M_3) is off and the pair (M_2 , M_4) is active, the polarities of the output current and of the differential output voltage are reversed. The required termination resistors are provided by an off-chip standard LVDS receiver chips. With a nominal 100Ω load on the LVDS receiver side, the differential swing at the output should fall within the LVDS standard specifications (350mV). Nevertheless, since the supply voltage of the integrated circuit is 1.2V, the common mode voltage does not match with the LVDS standard specifications (1.25V). The common mode voltage is set here at $V_{DD}/2$ (0.6V) by the common mode feedback block and an external chip receiver supporting such a common mode voltage must be used.

V. MEASUREMENT RESULT

The emitter and the receiver of the presented transceiver have been realized in two separated chips using the same 130nm CMOS technology from STMicroelectronics and have a supply voltage of 1.2V. Even if the transmitter could have better performances with a more recent process due to its all-digital architecture, this technological node achieves good performances up to 5GHz and is a good tradeoff between cost and performances [2]. Emitter and receiver have been integrated on two separated chips, and measured with two different setups for a better test convenience.

A. Transmitter

As shown on part (a) of Fig. 14, the pulse synthesizer has a

die area of 1.4mm^2 and a core area of only 0.11mm^2 . To measure the pulse synthesizer, it has been packaged into a QFN32 package and three boards (represented in parts (b) of Fig. 17) have been realized: one RF-board to receive the chip, another one to generate the required supply and control voltages and an USB-board to connect with a computer. The test setup principle is given in part (a) of Fig. 17.

To generate a pulse for a given bandwidth with a pulse synthesizer, available values of A_n and τ_n have been characterized for the tuning ranges of V_{a-n} and V_{d-n} . Next, the analytical pulse model has been used to set all V_{a-n} and V_{d-n} voltages according to the targeted central frequency f_M and bandwidth $BW_{-10\text{dB}}$. Finally, all V_{a-n} are adjusted in order to optimize rejection and also respect FCC requirements. To verify that emitted pulses are well-suited to the targeted bandwidth, or to compensate for spectrum variations generally due to slow phenomenon such as temperature variations, the synthesizer can be controlled by a calibration system as described in [27].

From a Gaussian up-converted pulse with f_M and $BW_{-10\text{dB}}$ respectively equal to 4GHz and 1.8GHz, an UWB pulse has been synthesized by adjusting the control voltages and is shown in part (a) of Fig. 15. Its peak to peak voltage is about 0.9Vpp and its energy is equal to 0.64pJ on a 100Ω load (which is greater than the 0.52pJ estimated from (8) since some parts of the pulse have a magnitude greater than the model). The delayed pulses needed for RA-OOK signaling are represented in part (b) of Fig. 15.

Due to the gated nature of IR-UWB signals, the mean consumed power can be written as a function of the Pulse Repetition Frequency (PRF) as follows [28] :

$$P_C(\text{PRF}) = E_{AC} \cdot \text{PRF} + P_{DC} \quad (15)$$

where P_{DC} is the DC consumed power when no pulse is emitted and E_{AC} is the additional consumed energy when a pulse is emitted. These parameters can be extracted from two powers measured at different PRF which are here for the worst configuration $115\mu\text{W}@100\text{kHz}$ and $14.7\text{mW}@100\text{MHz}$, which give a P_{DC} equals to $100\mu\text{W}$ and an E_{AC} equals to 146pJ per pulse. At 1MHz, the pulse generator consumes $250\mu\text{W}$ which gives a 250pJ energy consumed per pulses.

Finally, the pulse shaping capabilities of the pulse generator are presented in Fig. 16. The targeted -10dB bandwidths, 3.5GHz (a) and 2.4GHz (b), are obtained in measurement thanks to the analytical pulse model given in (3). It appears that it is possible to change the central frequency from 3GHz to 5GHz by varying the delay τ in the VCDL. For a pulse centered at 4GHz, the fine tuning of V_{a-n} voltages allows A_n to be linearly controlled between 0V and 0.45V when V_{a-n} is between 0V and the supply voltage 1.2V.

The pulse generator is also able to address several bandwidths and several center frequencies with a high output dynamic as shown in Table I which gives a summary of different reported pulse generators with pulse shaping capabilities. The presented pulse generator achieves a quite

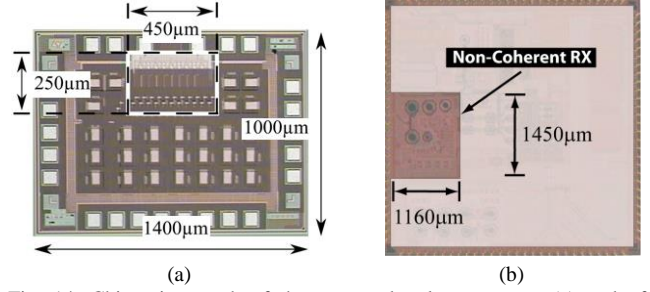


Fig. 14. Chip micrograph of the proposed pulse generator (a) and of the proposed receiver (b).

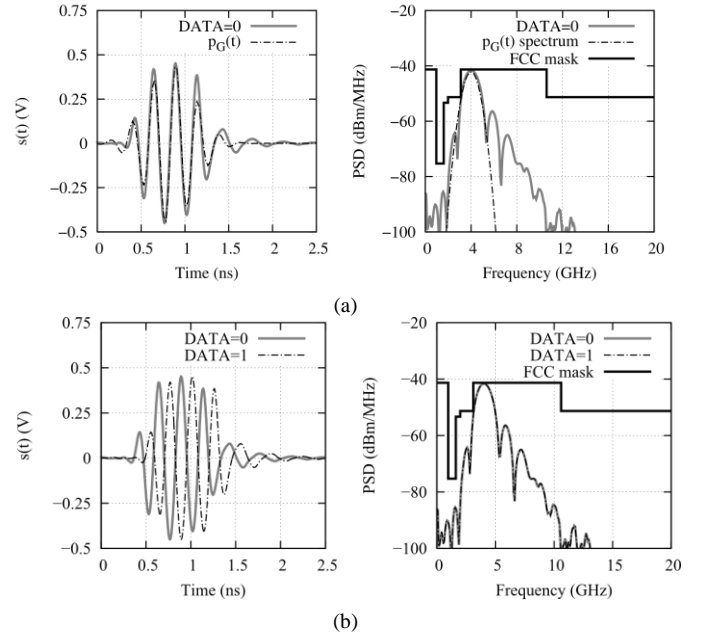


Fig. 15. Comparison of the ideal Gaussian up-converted pulse with measured transient and frequency responses of a pulse with $A=0.45\text{V}$, $f_M=4\text{GHz}$, and $BW_{-10\text{dB}}=1.8\text{GHz}$ for DATA = '0' (a). Comparison between pulses required for RA-OOK (DATA = '1' and DATA = '0') (b).

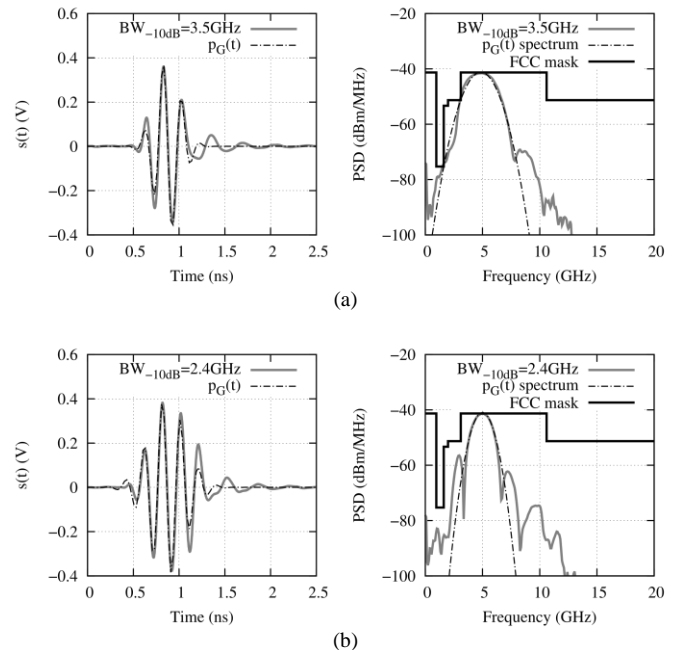


Fig. 16. Comparison of ideal Gaussian up-converted pulses with measured transient and frequency responses of a 4.85GHz centered pulse with $BW_{-10\text{dB}}=3.5\text{GHz}$ (a) and of a 5GHz centered pulse with $BW_{-10\text{dB}}=2.4\text{GHz}$ (b).

TABLE I : COMPARISON OF RECENT PULSE GENERATORS WITH PULSE SHAPING CAPABILITIES

[REF]	[9]	[11]	[16]	[17]	[32]	[33]	This Work
V_{DD} (V)	0.9	1	1	0.9	1.2	1.2	1.2
f_M (GHz)	3.5-4.5	3-5	4	3.1-5	3.1-6	4.9	3-5
BW_{-10dB} (GHz)	0.5	0.5	2	0.5-1.4	1-1.86	3.5	1.8-3.5
A (V)	0.25	0.305	0.25	0.048-0.063	0.2	0.11	0.45
E_{AC} (pJ/pulse)	N/A	2	N/A	8-12	N/A	N/A	146
P_{DC} (μ W)	2.8	105	28	170	N/A	N/A	100
$P_C@PRF$ (mW)	5.7	4.36	N/A	0.57	N/A	87.6	14.7
PRF (MHz)	0.1	15.6	32	50	<500	800	100
E_C (nJ/pulses)	0.057	0.28	0.008	0.012	0.0036-0.02	0.1	0.147
Tech. (CMOS)	90nm	90nm	65nm	90nm	90nm	130nm	130nm

good output dynamic ($A = 0.45V$) compared to other reported works. The tradeoff between output dynamic and power consumption is comparable to other all-digital synthesizers, which generally consume more power than analog pulse generators as it can be observed in Table I.

B. Receiver

The non-coherent receiver core area is 1.7 mm^2 as indicated in part (b) of Fig. 14. The chip where the receiver has been integrated includes other circuits which are out of the scope of this paper. It has been packaged in a QFN88 package. The DC power consumption of the non-coherent receiver is 30.5mW. From post-layout simulations, the LNA achieves for the 3.1GHz-4.9GHz band, a minimum voltage gain of 28dB, a maximum noise figure of 3dB, a maximum S11 of -11.5dB, and a current consumption of 17mA.

The performance of the non-coherent receiver has been measured through the BER characteristic. As it can be seen in part (c) of Fig. 17, three boards have been realized, one RF-board to receive the chip, another one to generate all the required supply voltages and control signals and a PXI-board for connection with a PC. A 2GHz bandwidth pulse centered at 4GHz is used for the measurement setup. The measurement has been done using the same considerations than in the theoretical BER calculus of the section II.D: a sequence of successive '1' is sent to measure the probability of a non-detection and a sequence of successive '0' is sent to measure the probability of a false-alarm. The detection threshold is set to obtain the same number of false-alarms and non-detections. The number of successive '1' and successive '0' used for this measurement is 10^6 . The measurement has been done for a rate of 15.6Mbps and the receiver exhibits a 10^{-3} BER for a pulse energy of 5.35 aJ. This corresponds to a -85.8dBm sensitivity at a 1Mbps rate for OOK modulations. This measured sensitivity value is much lower than the theoretical one presented in Fig. 4 (-98 dBm if downscaled to 1Mbps) since Fig. 4 gives the upper performance limit for a receiver using ideal blocks with no noise, no loss, and no bandwidth limitation. However, this sensitivity is comparable to the performances of other receivers based on energy detection.

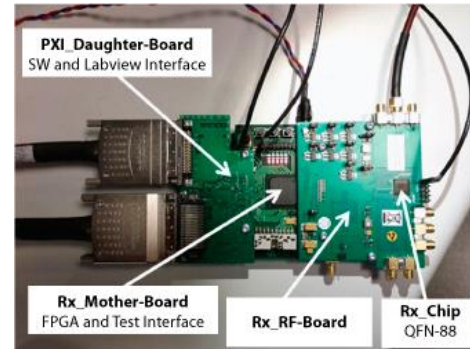
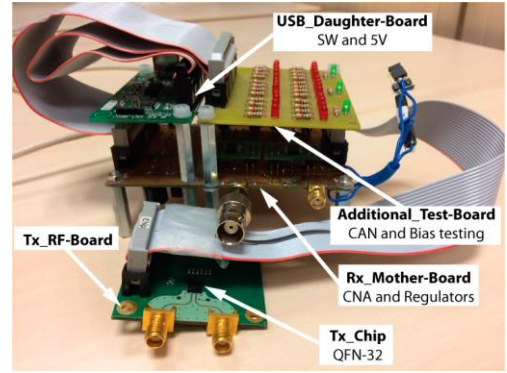
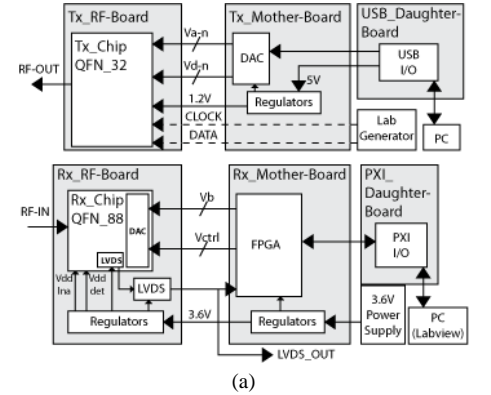


Fig. 17. Measurement setup principle (a), emitter measurement setup (b) receiver measurement setup (c).

TABLE II : FINAL LINK BUDGET

PRF _{MEAN} (MHz)	0.5
D _b (Mbps)	1
BW _{-10dB} (GHz)	1.8
E _P (pJ)	0.52***
A (V)**	0.45
A _{RX} (mV)*	1.1
E _{RX} (pJ)	5.35·10 ⁻⁶
S _{RX} @1Mbps(dBm)	-85.8
d(m)	1.9

*on a 50Ω impedance

**on a 100Ω impedance

*** estimated from (8)

C. Overview

The final budget link based on measurement results is presented in Table II and introduces A_{RX} (resp. E_{RX}) which is the peak magnitude (resp. energy) of the received pulse, and S_{RX} which is the receiver sensitivity for a given bit rate. By using the emitted pulse indicated in Fig. 15 and the measured receiver sensitivity, the range d is computed from Friis formula. Thus, the maximum communication range is estimated to 1.9m with the radiated pulse energy on a 100Ω differential load and the receiver sensitivity on a 50Ω load. In this budget link, no antenna gain and no fade margin are taken into account. This budget link shows that peak voltage detection is suitable for short range communications. The transceiver performances are compared with previous works in table III. This shows that peak voltage detection exhibits performances comparable to other type of detectors. The high output voltage of the transmitter combined with the receiver sensitivity finally gives a 1.9m communication range which is at the state of the art.

VI. CONCLUSION

A 3-5 GHz peak voltage detector based IR-UWB CMOS transceiver with pulse shaping capabilities has been presented in a 130nm CMOS technology. A non-coherent receiver based on a peak power detector has been presented. The detection is fully asynchronous. The receiver has a sensitivity of -85.8dBm for a rate of 1Mbps. This sensitivity allows detecting an input signal with a magnitude of 1.1mV which leads to a communication range of 1.9m. The receiver power consumption is about 30.5mW@100Mbps. The transmitter emits pulses with a high pulse shaping capabilities for a power consumption of 14.7mW@100Mbps.

APPENDIX

In this appendix, an estimation of the BER which can be achieved with an UWB energy detector is presented by considering an OOK coding, an AWGN channel, and no multipath propagation. The considered receiver architecture is similar to the one depicted in Fig. 3 but the peak voltage detector has been replaced by a perfect energy detector. This energy detector collects without any loss the signal energy available at the LNA output during the integration window. A perfect synchronization is assumed for the integration window.

A. Probability of error

During the integration window T_s , the continuous time domain signal at the receiver input is replaced by P discrete samples of the received signal obtained at the Nyquist rate:

$$P = 2 \cdot f_{MAX} \cdot T_s + 1. \quad (9)$$

Given that, for the 3.1GHz-4.9GHz signal bandwidth considered here, the noise bandwidth (1.8GHz) is close to the maximum spectrum frequency f_{MAX} (4.9GHz), it is assumed that the noise samples are independent. Consequently, the

TABLE III PERFORMANCE COMPARISON WITH PREVIOUS WORKS

Ref	Year	Tech. (CMOS)	size (mm ²)	Pulse BW (GHz)	f _M (GHz)	d (m)	Data Rate (bps)	Tx Power Cons. at Data Rate (mW)	Tx cons. nrj/b (pJ/b)	Rx Sensi. at Data Rate (dBm)	Rx Sensi. Scaled @ 1Mbps (dBm)	Rx Power Cons. at Data Rate (mW)	Rx cons. nrj/b (nJ/b)
This Work		130nm	1.31	0.5-2	3.5-5	1.9	100M	14.7	147	-65.8	-85.8	30.5	0.305
[3]	2013	90nm	1.7	0.5	3.5-4.5	0.5	100k	0.0085	60.7	-85	-75	0.11	0.8
[16]	2015	65nm	2.25	0.5	7.5-9.5	1.2	500M	6.9	13.8	-60	-87	5.9	0.0118
[29]	2011	90nm	0.6	3.6-4.3	2.9-3.8	1.5	1M	0.258	258	-60/-66	-60/-66	1.64-2.18	1.64
[30]	2014	180nm	4.4	1.36	3-5	N/A	20M	13.4	670	-81	-94	3.54*	3.54
[31]	2016	65nm	4.6**	0.5	3.1-10.6	1	1G	31.9***	31.9	-74	-104	27.8***	0.0278
[34]	2008	180nm	0.36	1	3	0.04	500M	0.28	0.56	N/A	N/A	11	0.022
[35]	2013	180nm	2.73	N/A	9-12	N/A	30k	0.022	747	-77	-61.7	0.037	1.2

*at 1Mbps, **with pads, ***with PLL

discrete samples of the received signal are the sum of samples of the unnoisy signal and samples of the noise.

Assuming an AWGN channel and the independence of the noise samples, the probability density function of the noise voltage for each sample is given by:

$$p_N(v) = \frac{1}{\sqrt{2\pi\sigma_N^2}} \exp\left(\frac{-v^2}{2\sigma_N^2}\right). \quad (10)$$

Assuming that the noise bandwidth is the same that the bandwidth (BW) of the signal, the noise variance σ_N at the LNA output is given by:

$$10\log\left(\frac{\sigma_N^2}{R_{LNA}}\right) = 10\log(K \cdot T \cdot BW) + G_{LNA} + NF_{LNA} \quad (11)$$

where K is the Boltzmann constant, T the absolute temperature, R_{LNA} , G_{LNA} , and NF_{LNA} the input resistor, the gain and the noise figure of the LNA respectively.

For an OOK coding, the probability of error is given by:

$$\Pr_E = 0.5 \times \Pr_{FA} + 0.5 \times \Pr_{ND} \quad (12)$$

where \Pr_{FA} is the probability of a false alarm and \Pr_{ND} is the probability of a non-detection.

B. Probability of non-detection

A non-detection occurs when the energy of the noisy signal integrated during the integration window T_S remains lower than the decision threshold. The energy collected by the energy detector is given by:

$$W = \frac{T_S}{R \cdot P} \sum_p (S_i + N_i)^2 \quad (16)$$

where S_i are the discrete samples of the unnoisy signal, N_i the discrete samples of the noise, and R is the input impedance of the energy detector which is assumed to be real.

The sum of the discrete sample of the signal S_i and of the noise N_i is a random variable X_i :

$$X_i = S_i + N_i. \quad (17)$$

The P values of X_i are P (independent) normally distributed random variables with a mean equal to the corresponding unnoisy signal sample and a variance equal to the noise variance σ_N . Consequently the random variable Y_i defined as:

$$Y_i = \frac{X_i}{\sigma_N} \quad (18)$$

has a unit variance and:

$$Y = \sum_{i=1}^P Y_i^2 = \sum_{i=1}^P \frac{X_i^2}{\sigma_N^2} \quad (19)$$

is a random variable which is distributed according to the non-central chi-squared distribution. The relation between Y and the energy (W) collected by the energy detector during T_S can be written as follows:

$$W = \frac{T_S \cdot \sigma_N^2}{R \cdot P} Y. \quad (20)$$

Y has two parameters: P the number of samples which specifies the number of degrees of freedom, and λ which is related to the mean of the random variables by:

$$\lambda = \sum_p \left(\frac{S_i}{\sigma_N}\right)^2 = \frac{R \cdot P}{T_S \cdot \sigma_N^2} W_S \quad (21)$$

where W_S is the energy of the unnoisy signal. (21) leads to:

$$W_S = \frac{T_S}{R \cdot P} \sum_p S_i^2. \quad (22)$$

The probability density function of Y is given by:

$$f_Y(x, P, \lambda) = \frac{1}{2} e^{-(x+\lambda)/2} \left(\frac{x}{\lambda}\right)^{P/4-1/2} I_{P/2-1}(\sqrt{\lambda x}) \quad (23)$$

where $I_\alpha(y)$ is α order modified first kind Bessel function which is given by:

$$I_\alpha(y) = \sum_{j=0}^{\infty} \frac{(y/2)^{2j+\alpha}}{j! \Gamma(\alpha + j + 1)} \quad (24)$$

with the Gamma function $\Gamma(z)$ defined as follows:

$$\Gamma(z) = \int_0^{\infty} x^{z-1} e^{-x} dx. \quad (25)$$

Finally the cumulative distribution function of Y is given by:

$$F_Y(x, P, \lambda) = \sum_{j=0}^{\infty} e^{-\lambda/2} \frac{(\lambda/2)^j}{j!} Q(x, P + 2j) \quad (26)$$

where $Q(x, k)$ is the cumulative distribution function of the central chi-squared distribution with k degrees of freedom, which is given by:

$$Q(x, k) = \frac{\gamma(k/2, x/2)}{\Gamma(k/2)} \quad (27)$$

where $\gamma(z, a)$ is the lower incomplete Gamma function defined as follows:

$$\gamma(z, a) = \int_0^a x^{z-1} e^{-x} dx. \quad (28)$$

A non-detection occurs when the energy collected by the energy detector is lower than the decision threshold W_D . It occurs when:

$$\frac{T_S \cdot \sigma_N^2 \cdot Y}{R \cdot P} < W_D. \quad (29)$$

which leads to:

$$Y < \frac{R \cdot P \cdot W_D}{T_S \cdot \sigma_N^2}. \quad (30)$$

So the probability of a non-detection can be obtained by using the cumulative distribution of Y :

$$\Pr_{ND} = F_Y \left(\frac{R \cdot P \cdot W_D}{T_S \cdot \sigma_N^2}, P, \frac{R \cdot P \cdot W_S}{T_S \cdot \sigma_N^2} \right). \quad (31)$$

C. Probability of false alarm

A false alarm occurs when the energy collected is greater than the decision threshold W_D while no pulse has been sent during the integration window. The mathematical expressions given in the previous part are not valid in this case because when no pulse has been sent, the parameter λ defined in (21) is equal to zero. In the case where λ is equal to zero, the random variable Y defined in (18) becomes a normal law which is called Y' in the following. Thus, Y' is a random variable which is distributed according to the central chi-squared distribution with P degrees of freedom and with a probability density function given by:

$$f_{Y'}(x, P) = \frac{x^{P/2-1} e^{-x/2}}{2^{P/2} \Gamma(P/2)}. \quad (32)$$

The cumulative distribution function of Y' is also given by:

$$F_{Y'}(x, P) = \frac{\gamma(P/2, x/2)}{\Gamma(P/2)}. \quad (33)$$

The energy collected W by the energy detector during the integration window can be computed and is given by:

$$W = \frac{T_S \cdot \sigma_N^2}{R \cdot P} Y'. \quad (34)$$

A false-alarm occurs when the energy collected by the energy detector given by W is greater than the decision threshold W_D . It occurs when:

$$\frac{T_S \cdot \sigma_N^2}{R \cdot P} Y' \geq W_D \quad (35)$$

which leads to:

$$Y' \geq \frac{R \cdot P \cdot W_D}{T_S \cdot \sigma_N^2}. \quad (36)$$

So the probability of a false alarm can be obtained by using the cumulative distribution of Y' :

$$\Pr_{FA} = 1 - F_{Y'} \left(\frac{R \cdot P \cdot W_D}{T_S \cdot \sigma_N^2}, P \right). \quad (37)$$

D. BER Calculation

Knowing the probability of a non-detection given by (31) and the probability of a false-alarm given by (37), (12) gives the probability of error for a given received power, a given integration window and a given decision threshold. Similarly as in the case of a peak voltage detection, there is an optimal decision threshold W_D that minimizes the received power and balances \Pr_{FA} and \Pr_{ND} . So, by using relations (12), (31), (37) and an iterative algorithm, the receiver sensitivity can be obtained for a given BER. Finally, the use of Friis formula with this minimum received input power gives the achievable range for a given emitted power. By using the UWB pulse

defined by (3) with a -10dB bandwidth of 1.8GHz centered at 4GHz, the theoretical BER obtained with an energy detector is given in Fig. 4 for a data rate of 100Mbps with OOK encoding, an integration window of 2ns, and a LNA noise figure of 3dB.

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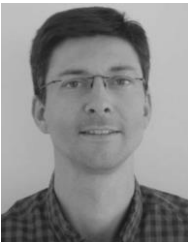
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