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An 80mV-to-1.8V Conversion-Range Low-Energy Level Shifter for Extremely Low-Voltage VLSIs

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***Abstract*—We present a low-power and low-energy level shifter (LS) circuit that can convert extremely low-voltage input into high-voltage output. The proposed LS consists of a pre-amplifier (pre-AMP) and an output latch. The pre-AMP employs a logic error correction circuit (LECC), which generates an operating current for the pre-AMP only when the logic levels of the input and output do not correspond. The pre-AMP generates complementary amplified signals, and the latch converts them into full-swing outputs. Measurement results demonstrated that the proposed LS fabricated in 0.18-μm CMOS technology was able to convert an extremely low-voltage input of 80 mV into a high-voltage output of 1.8 V. The energy of the proposed LS was 0.35 pJ when the low supply voltage, high supply voltage, and input pulse frequency were 0.4 V, 1.8 V, and 10 kHz, respectively. The static power dissipation without input was 0.12 nW.**

***Index Terms*—CMOS logic circuits, Low-power electronics, Multiple supply voltages, Level shifters, Low-voltage circuits**

I. Introduction

Low-power and low-energy circuit designs using multiple supply voltages have been widely adopted in not only modern VLSI systems but also emerging VLSI systems [1], [2]. A level shifter (LS) circuit is one of the most important circuits in such systems to correctly communicate with peripheral circuits. We present here a low-power and low-energy LS circuit that converts extremely low-voltage input into high-voltage output.

Sub-threshold (sub-$V_{\rm TH}$) and near-threshold (near-$V_{\rm TH}$) circuits have been widely used to achieve low-power and low-energy dissipation [3]–[9]. These circuits will be implemented with other peripheral circuits that operate at higher supply voltages. Because the supply voltage of sub-$V_{\rm TH}$ and near-$V_{\rm TH}$ circuits is close to or lower than the threshold voltage ($V_{\rm TH}$) of a MOS transistor (e.g., below 0.5 V) and those of the peripheral circuits are still high (e.g., 1.8 or 3.3 V), signal communications between each circuit have become difficult when conventional LSs are used [10].

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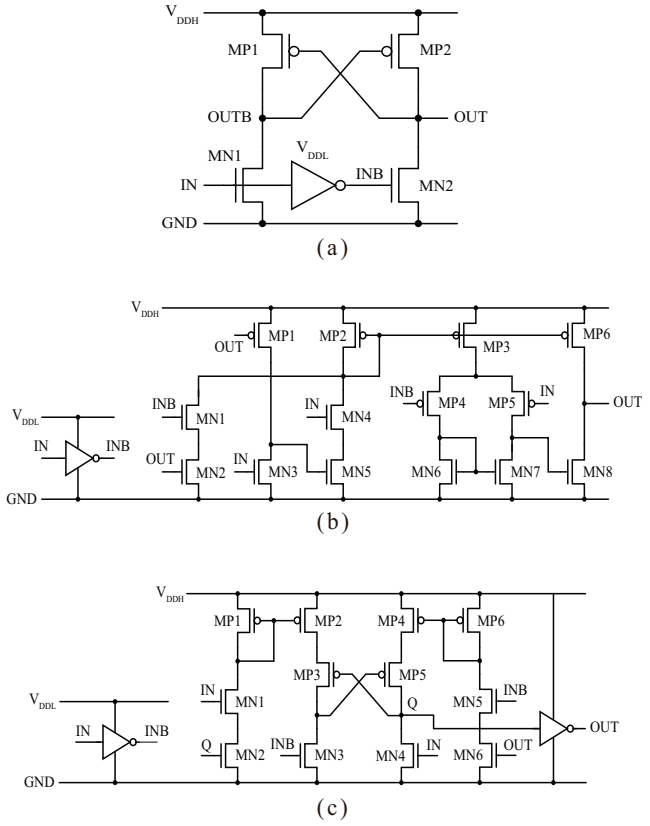

Fig. 1. Schematics of LSs. (a) cross-coupled LS, (b) LS reported by Osaki et al. [23], and (c) LS reported by Hosseini et al. [30].

Emerging applications consisting of battery-less LSI systems have been reported [11]–[18]. They obtain the necessary energy from energy harvesters. However, because the output voltages of the small harvesters are too low for VLSIs to operate (e.g., single photovoltaic (PV) cell: about 0.5 V, thermoelectric generator (TEG): several tens-of-mV), power management circuits, or voltage boost converters, are necessary to generate sufficiently high voltages. For energy harvesting systems to operate with high efficiency, they have to handle extremely low-voltage inputs together with the boosted voltages [15], [16], [19]. Because the systems are inherently multiple supply systems, an LS capable of converting those low-voltage signals is strongly required.

Fig. 1 (a) depicts a conventional LS [20]. It consists of cross-coupled pMOS transistors and two nMOS transistors driven by low-voltage inputs of IN and INB. The LS operation fails when

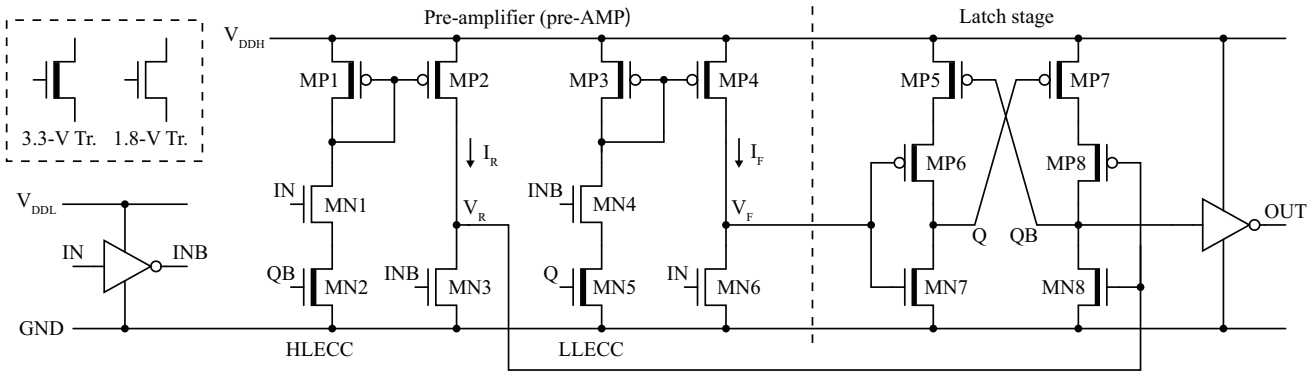

Fig. 2. Schematic of the proposed LS.

there is a large difference between the low supply voltage V_{DDL} and high supply voltage V_{DDH}. This is because the drive currents of nMOS transistors become significantly smaller than those of pMOS transistors when the V_{DDL} becomes much lower than the V_{DDH} (e.g., $V_{\mathrm{DDL}} < 0.5$ V and $V_{\mathrm{DDH}} = 1.8$ or 3.3 V).

To realize robust communications between circuits with large supply voltage differences, several LSs and remedies have been reported [21]–[30]. Osaki *et al.* proposed an LS using a logic error correction circuit (LECC) as shown in Fig. 1 (b) [22], [23]. Because the LECC operates only when the input and output logic levels do not correspond, the power dissipation of the LS itself can be minimized. However, because the LS uses a two-stage amplifier, the contention between pull-up and pull-down MOS transistors (MP6 and MN8) occurs when the input changes from High to Low. In addition, because the LS does not have a latch structure, the logic level of the output is retained by the leakage currents of MP6 and MN8. Thus, the LS was not able to ensure good retention ability. In addition, because the slew rate of the output becomes much worse due to the lack of the latch structure, CMOS gates connected to the LS dissipate large amounts of energy. Hosseini *et al.* presented a modified LS as shown in Fig. 1 (c). By combining a conventional cross-coupled LS (Fig. 1 (a)) and an LECC (Fig. 1 (b)), it achieves the short transition time and the low-power dissipation [30]. However, because pull-down nMOS transistors (MN3, MN4) and cross-coupled pMOS transistors (MP3, MP5) are still driven by V_{DDL} and V_{DDH}, respectively, the same problems as those occurring with the conventional cross-coupled LS remain to be solved.

In light of this background, this paper presents a low-power LS capable of converting extremely low-voltage inputs into high-voltage outputs [31]. In contrast to Matsuzuka *et al.* [31], we fabricated a proof-of-concept chip in a 0.18-μm CMOS process to demonstrate the low-energy and low-voltage performance of our LS architecture. The proposed LS consists of a pre-amplifier (pre-AMP) stage with an LECC and an output latch stage. The pre-AMP amplifies input signals with extremely low current dissipation. Then the output latch stage accepts the amplified voltages and converts them into full-swing output voltages. The chip's main features are a minimum input voltage (80 mV into 1.8 V), low energy per transition (0.35 pJ at 0.4-V input and 1.8-V output), and low static power dissipation (0.12 nW).

This paper is organized as follows. Section II presents the operating principles behind our proposed circuit. Section III describes simulated results of the circuit using 0.18-μm CMOS process technology. Section IV shows experimental measured results with fabricated chips. Extremely low-voltage input of 80 mV was successfully converted into high-voltage output of 1.8 V. Section V concludes the paper.

II. Proposed level shifter

Fig. 2 schematically shows our proposed LS. The LS consists of a pre-amplifier (pre-AMP) with high- and low-LECC (HLECC and LLECC), an output latch stage, and an output inverter. The pre-AMP consists of the HLECC (MN1, MN2), LLECC (MN4, MN5), current mirrors (MP1–MP2, MP3–MP4), control transistors (MN3, MN6), and an input inverter. The input inverter is used to generate INB from the input signal IN, and the output inverter is used to separate the load capacitance dependence of the latch stage. The pre-AMP generates complementary amplified signals of V_{R} and V_{F} from low-voltage inputs and high-voltage outputs of IN, INB, Q, and QB. The latch stage accepts the generated voltages (V_{R} and V_{F}) and converts them into full-swing output signals of Q and QB. Details of the circuit operation and theoretical delay analysis are discussed as follows.

A. Operation principle

When logic levels of IN and OUT correspond, neither HLECC nor LLECC generates currents of I_{R} and I_{F}. The voltages of V_{R} and V_{F} are determined by logic levels of IN and INB (when IN and INB are High and Low [or Low and High], V_{R} and V_{F} are High and Low [or Low and High]).

When logic levels of IN and OUT are High and Low (i.e., IN and QB are both High in Fig. 2), respectively, the HLECC detects the logic error of the LS and generates current of I_{R}. Because the LLECC accepts a Low signal of INB, it does not generate current of I_{F}. The current I_{R} is transferred to MN3, and node voltage of V_{R} increases. Because the V_{F} is kept at Low by MN6, complementary amplified signals of V_{R} and V_{F} are generated (V_{R} and V_{F} are High and Low, respectively).

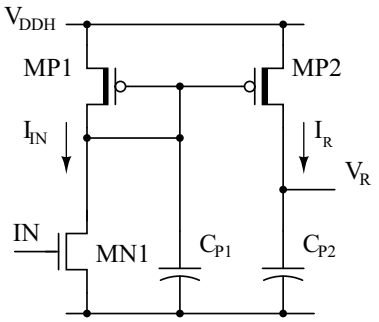

Fig. 3. Simplified schematic of the pre-AMP (HLECC).

When logic levels of IN and OUT are Low and High (i.e., INB and Q are both High in Fig. 2), respectively, the LLECC detects the logic error of the LS and generates current of $I_{\rm F}$. Because the HLECC accepts Low of IN, it does not generate current of $I_{\rm R}$. The current $I_{\rm F}$ is transferred to MN6, and node voltage of $V_{\rm F}$ increases. Because the $V_{\rm R}$ is kept at Low by MN3, complementary amplified signals of $V_{\rm F}$ and $V_{\rm R}$ are generated ($V_{\rm R}$ and $V_{\rm F}$ are Low and High, respectively).

The latch stage accepts voltages of $V_{\rm R}$ and $V_{\rm F}$ and converts them into full-swing output voltages. Because the latch stage includes a positive feedback configuration, it enhances the transition speed and keeps output logic levels stable.

Note that, as discussed earlier, when IN and OUT correspond, neither HLECC nor LLECC generate currents of $I_{\rm R}$ and $I_{\rm F}$ for the pre-AMP. This means that one of voltages to the latch stage, $V_{\rm R}$ or $V_{\rm F}$, will become a floating node when IN and OUT correspond. For example, when IN is High, $V_{\rm R}$ becomes floating ($V_{\rm F}$ is Low). This arises a concern about the operation stability due to the floating node. However, because another voltage to the latch will be kept at Low (i.e., GND) by the low-voltage input signal through MN6 or MN3, the latch can determine correct output logic of the circuit. If some unexpected noise ever changes the floating node lower than GND, the latch stage toggles internal logic incorrectly. However, the LECC detects logic errors and supplies the operating current until IN and OUT once again correspond. Therefore, the proposed LS can correct logic errors caused by the unexpected noise.

B. Theoretical delay analysis

Delay of the proposed LS is determined by those of the pre-AMP, latch stage, and output inverter. Among them, the delay of the pre-AMP becomes a dominant factor because the pre-AMP is driven by $V_{\rm DDL}$. In the following, we assume that the delay of the proposed LS is mainly determined by that of the pre-AMP.

Fig. 3 shows a simplified schematic of the HLECC in the pre-AMP when logic levels of IN and OUT correspond to Low logic level, where $C_{\rm P1}$ and $C_{\rm P2}$ are the parasitic capacitance at the PMOS gate node and output node $V_{\rm R}$, respectively. When IN changes from Low to High, $I_{\rm IN}$ flows in MN1 and is given by

$$I_{\rm IN} = I_0 e^{(V_{\rm DDL}-V_{\rm THN})/\eta V_{\rm T}}, \tag{1}$$

where $I_0 (= \mu C_{\rm OX}(W/L)(\eta-1)V_{\rm T}^2)$ is the pre-exponential factor of the subthreshold current, μ is the carrier mobility, $C_{\rm OX} (= \varepsilon_{\rm ox}/t_{\rm ox})$ is the gate-oxide capacitance, $\varepsilon_{\rm ox}$ is the oxide permittivity, $t_{\rm ox}$ is the oxide thickness, W/L is the aspect ratio, W is the channel width, L is the channel length, η is the subthreshold slope factor, $V_{\rm T} (= k_{\rm B}T/q)$ is the thermal voltage, $k_{\rm B}$ is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, and $V_{\rm THN}$ is the threshold voltage of the MOSFET [32]. The pMOS current mirror accepts $I_{\rm IN}$ and generates the output current $I_{\rm R}$. The pMOS current mirror has a single-pole transfer function and it is given by

$$\begin{aligned}\frac{I_{\rm R}(s)}{I_{\rm IN}(s)} &= \frac{g_{\rm mp2}}{g_{\rm mp1}}\frac{1}{1+sC_{\rm P1}/g_{\rm mp1}} \\ &= \frac{g_{\rm mp2}}{g_{\rm mp1}}\frac{1}{1+s\tau_p},\end{aligned} \tag{2}$$

where $g_{\rm mp1,2}$ is the transcondactance of MP1 and MP2, and τ_p is the time constant of the pMOS current mirror ($\tau_p = C_{\rm P1}/g_{\rm mp1}$). From Eq. 2, the output current $I_{\rm R}(t)$ with a step response can be derived as

$$I_{\rm R}(t) = \frac{g_{\rm mp2}}{g_{\rm mp1}}\left(1-e^{-t/\tau_{\rm p}}\right) I_{\rm IN}. \tag{3}$$

Because $I_{\rm R}$ is applied to the $C_{\rm P2}$, $I_{\rm R}$ is also expressed as

$$I_{\rm R}(t) = C_{\rm P2}\frac{dV_{\rm R}}{dt}. \tag{4}$$

From Eqs. 3 and 4, $V_{\rm R}(t)$ is given by

$$V_{\rm R}(t) = \frac{g_{\rm mp2}}{C_{\rm P2}g_{\rm mp1}}\left(t+\tau_{\rm p}(e^{-t/\tau_{\rm p}}-1)\right) I_{\rm IN}. \tag{5}$$

As shown in Eq. 5, the output voltage of the pre-AMP $V_{\rm R}$ increases with time. When $V_{\rm R}(t)$ reaches the threshold voltage of the latch at $t = t_1$, the latch stage toggles internal logic and thus we obtain the following equation:

$$\begin{aligned}V_{\rm R,TH} &= V_{\rm R}(t_1) \\ &= \frac{I_0 g_{\rm mp2}}{C_{\rm P2}g_{\rm mp1}}\left(t_1+\tau_{\rm p}(e^{-t_1/\tau_{\rm p}}-1)\right)e^{(V_{\rm DDL}-V_{\rm THN})/\eta V_{\rm T}},\end{aligned} \tag{6}$$

where $V_{\rm R,TH}$ is the threshold voltage of the latch stage. Eq. 6 can be rewritten as

$$t_1 = \frac{C_{\rm P2}V_{\rm R,TH}g_{\rm mp1}}{I_0 g_{\rm mp2}}e^{(V_{\rm THN}-V_{\rm DDL})/\eta V_{\rm T}} + \tau_{\rm p}(1-e^{-t_1/\tau_{\rm p}}). \tag{7}$$

Although Eq. 7 cannot be solved for t_1, we find that the delay t_1 increases exponentially when $V_{\rm DDL}$ becomes low. More importantly, we also find that the time constant of $\tau_{\rm p}$ should be designed as small as possible because the last term of Eq. 7, or $\tau_{\rm p}(1-e^{-t_1/\tau_{\rm p}})$, monotonically increases as $\tau_{\rm p}$ increases. Therefore, the smaller $\tau_{\rm p}$ becomes, the faster $V_{\rm R}$ increases.

III. Simulation results

The proposed LS was simulated in 0.18-μm standard CMOS technology. We designed our proposed LS using both 1.8-V and 3.3-V tolerant transistors (see Fig. 2). Threshold voltages of 1.8-V tolerant nMOS and pMOS transistors are 0.44 and –0.46 V, respectively, and those of 3.3-V tolerant nMOS and pMOS transistors are 0.72 and –0.72 V, respectively. Table I

TABLE I
TRANSISTOR SIZES OF OUR CIRCUIT

Transistor	W/L (μm)	Transistor	W/L (μm)
MN1	0.22 / 0.18	MP1	0.66 / 0.30
MN2	0.22 / 0.35	MP2	0.22 / 0.30
MN3	0.22 / 0.18	MP3	0.66 / 0.30
MN4	0.22 / 0.18	MP4	0.22 / 0.30
MN5	0.22 / 0.35	MP5	0.22 / 0.30
MN6	0.22 / 0.18	MP6	0.22 / 0.30
MN7	0.44 / 0.35	MP7	0.22 / 0.30
MN8	0.44 / 0.35	MP8	0.22 / 0.30

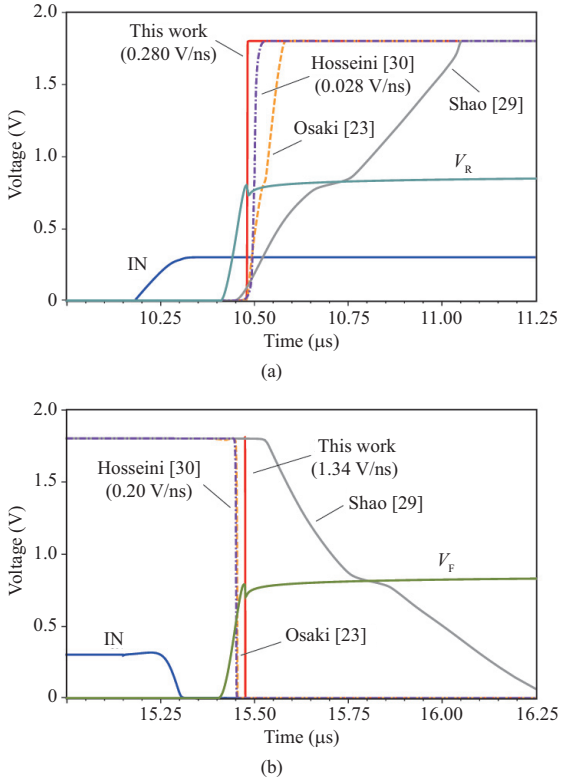

Fig. 4. Simulated waveforms. (a) Rising edge. (b) Falling edge.

lists the transistor sizes of the proposed LS. For comparison, LSs of [23], [29], [30] were also evaluated in the same technology.

The simulated waveforms are shown in Fig. 4. The V_{DDL}, V_{DDH}, and input pulse frequency f_{IN} were set to 0.3 V, 1.8 V, and 100 kHz, respectively. As a load circuit, an inverter was added. The IN, OUT, V_{R}, and V_{F} of the proposed LS are shown. The OUTs of other LSs are also shown for comparison. When the IN changed from Low to High (Fig. 4 (a)), the V_{R}

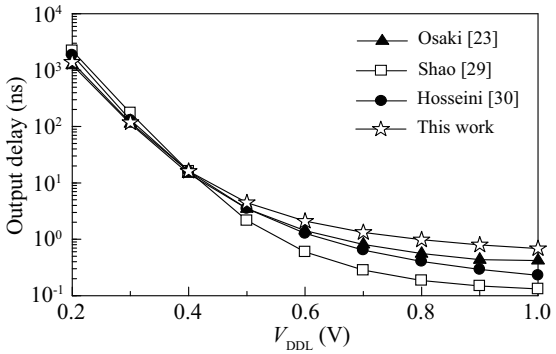

Fig. 5. Output delay time as a function of V_{DDL} at f_{IN} = 10 kHz.

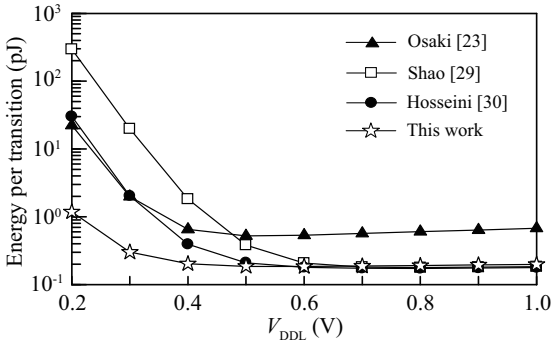

Fig. 6. Energy per transition as a function of V_{DDL} at f_{IN} = 10 kHz.

increased to around 0.8 V. Then the OUT of the proposed LS changed from Low to High with the highest slew rate and smallest delay. When the IN changed from High to Low (Fig. 4 (b)), the V_{F} increased to around 0.8 V. Then the OUT changed from High to Low. Although the proposed LS had a slightly longer delay time than the LSs of [23], [30], it achieved the highest slew rate.

The simulated output delay and energy as a function of V_{DDL} are shown in Figs. 5 and 6. The V_{DDH} and f_{IN} were set to 1.8 V and 10 kHz, respectively. As a load circuit, an inverter was added. Fig. 5 shows the simulated delay. The delay of the proposed LS in higher V_{DDL} (>0.5 V) was slower than those of other LSs. This was because the proposed LS uses two-stage architecture. The delays were increased exponentially as the V_{DDL} decreased because transistors operated in the sub-V_{TH} region of a MOS transistor. However, the delay became comparable to or even faster than those of other LSs in lower V_{DDL}. Fig. 6 shows the simulated energy. The energy per transition increased as V_{DDL} decreased. However, the proposed LS achieved the lowest energy because the latch stage changed the output nodes quickly due to the signals amplified by the pre-AMP. The proposed LS reduced energy by 86% at $V_{\mathrm{DDL}} = 0.3$ V compared with that of [30].

We investigated the circuit operation against process variation by performing 10k-run Monte Carlo statistical circuit simulations assuming die-to-die (D2D) global variations and within-die (WID) random mismatch variations in all MOS transistors using the parameters provided by the manufacturer,

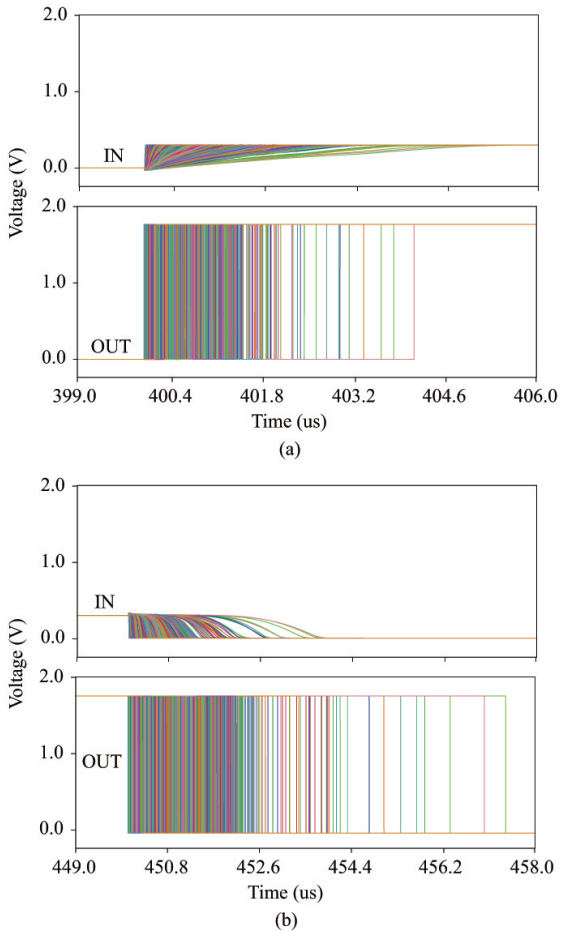

Fig. 7. Simulated waveforms (10k runs). (a) Rising edge. (b) Falling edge.

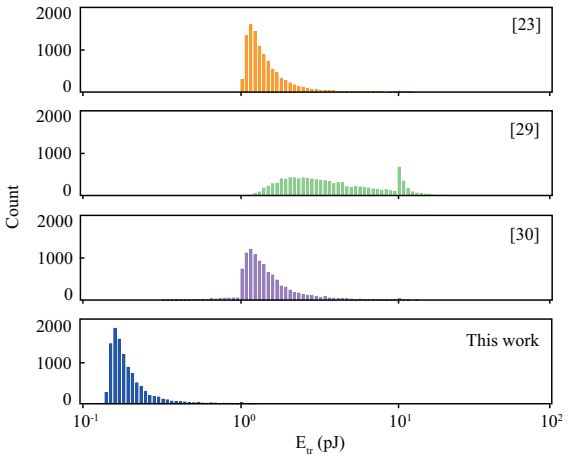

Fig. 8. Distributions of energy per transition at V_{DDH} = 1.8 V, V_{DDL} = 0.3 V, and f_{IN} = 10 kHz (10k runs).

TABLE II
SUMMARY OF MONTE CARLO SIMULATION OF THE ENERGY PER TRANSITION AT V_{DDL} = 0.3 V (10K RUNS)

Ref.	Yield (%)	μ_{E} (pJ)	σ_{E} (pJ)	$\sigma_{\mathrm{E}}/\mu_{\mathrm{E}}$ (%)
[23]	100	2.44	1.26	51.79
[29]	100	6.83	4.45	65.19
[30]	100	2.55	1.54	60.29
This work	100	0.36	0.11	31.86

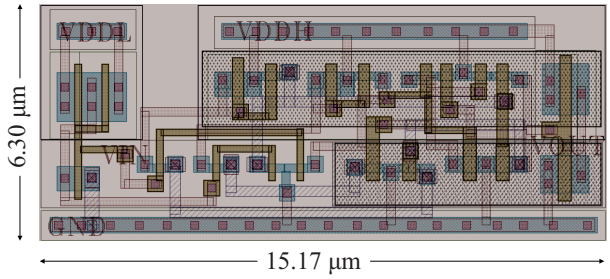

Fig. 9. Layout of the proposed LS (area: 95.6 μm^2).

which cover the slow-slow (SS) and fast-fast (FF) process corners by changing the key parameters such as threshold voltage, gate-oxide thickness, channel length and width, and carrier mobility. The V_{DDL}, V_{DDH}, and the input pulse frequency f_{IN}, were set to 0.3 V, 1.8 V, and 10 kHz, respectively. Fig. 7 shows the simulated waveforms. The IN and OUT of the proposed LS are shown. When the IN changed from Low to High as shown in Fig. 7 (a), the proposed LS successfully changed the OUT from Low to High in all cases. Then, the minimum and maximum delay times were 13.7 ns and 1.79 μs. When the IN changed from High to Low as shown in Fig. 7 (b), the proposed LS successfully changed the OUT from High to Low in all cases. Then, the minimum and maximum delay times were 18.0 ns and 4.23 μs.

We compared the energy of the proposed LS with those of other LSs [23], [29], [30]. The simulated distributions are shown in Fig. 8. The proposed LS achieved the lowest energy. Table II summarizes the results of yield and energy per transition (mean: μ_{E}, standard deviation: σ_{E}, and coefficient of variation: $\sigma_{\mathrm{E}}/\mu_{\mathrm{E}}$). Yields were evaluated to see whether the LS can successfully convert the low-voltage IN into the high-voltage OUT. The proposed LS showed the lowest μ_{E}, σ_{E}, and $\sigma_{\mathrm{E}}/\mu_{\mathrm{E}}$.

The physical design of the proposed LS is shown in Fig. 9. The area occupied 95.6 μm^2. We evaluated the circuit performance by extracting parasitic devices such as resistances and capacitances from post-layout data. The V_{DDL}, V_{DDH}, and f_{IN}, were set to 0.4, 1.8 V, and 100 kHz, respectively. The results of the energy per transition, the static power dissipation, and the delay time, were 0.24 pJ, 0.15 nW, and 21.4 ns. The simulated waveforms at V_{DDL} = 60 mV, V_{DDH} = 1.8 V, and f_{IN} = 10 Hz, are shown in Fig. 10. The proposed LS can successfully convert the extremely low-voltage signal of 60 mV into the high-voltage signal of 1.8 V.

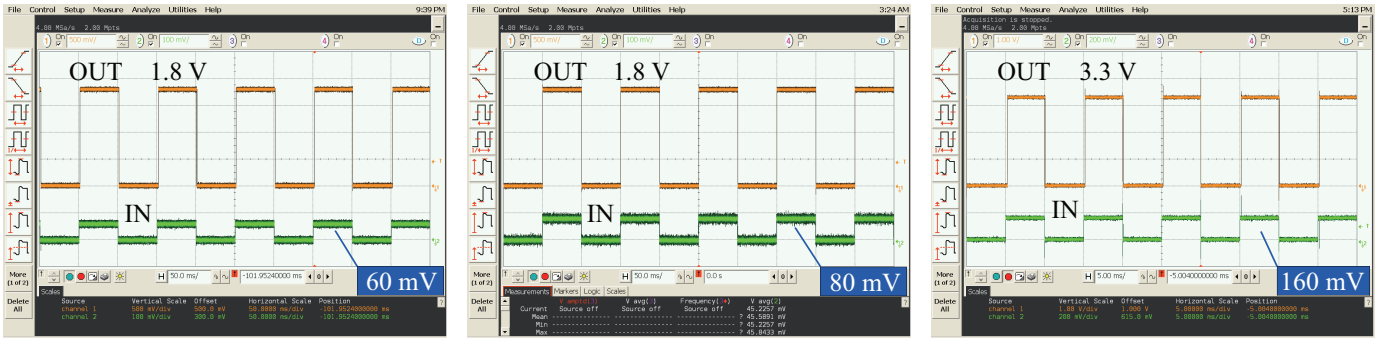

Fig. 12. Measured waveforms at different input conditions. (a) V_{DDL} = 60 mV, V_{DDH} = 1.8 V and f_{IN} = 10 Hz. (b) V_{DDL} = 80 mV, V_{DDH} = 1.8 V and f_{IN} = 10 Hz. (c) V_{DDL} = 160 mV, V_{DDH} = 3.3 V and f_{IN} = 100 Hz.

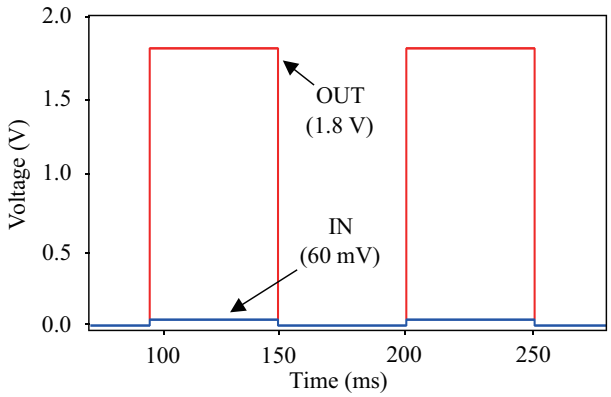

Fig. 10. Simulated waveforms at V_{DDL} = 60 mV, V_{DDH} = 1.8 V, and f_{IN} = 10 kHz.

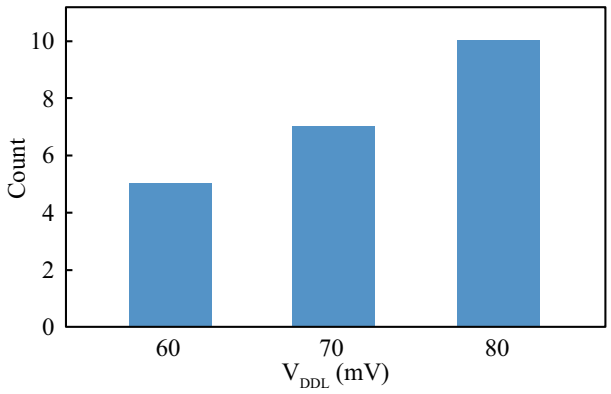

Fig. 13. Measured count that converted a low voltage input into a 1.8-V output successfully as a function of V_{DDL} (10 samples in total).

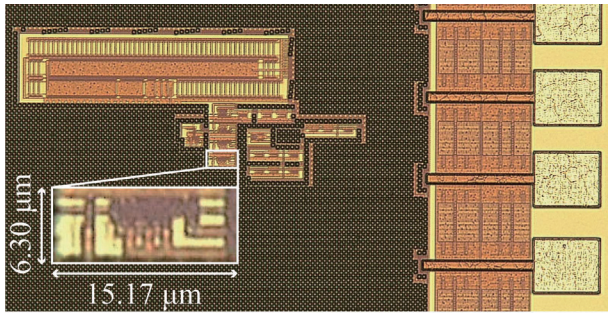

Fig. 11. Chip micrograph and its partial enlarged view.

IV. Experimental Results

We fabricated a proof-of-concept chip of the proposed LS using 0.18-μm, 1-poly, and 6-metal CMOS technology. Fig. 11 shows a micrograph of our chip and a partial enlarged view of the proposed LS. The area was 95.6 μm^2. Ten sample chips were measured.

The measured input and output waveforms of the proposed LS are shown in Fig. 12. The results at V_{DDL} = 60 mV, V_{DDH} = 1.8 V, and f_{IN} = 10 Hz are in Fig. 12 (a). The proposed LS converted an extremely low-voltage input of 60 mV into a full-swing output even though not all chips were able to operate correctly. Note that in the measurement, five out of 10 chips were able to convert the 60-mV input into a full-swing output. Fig. 13 shows measured count that was able to convert a low voltage input into a 1.8-V output successfully as a function of V_{DDL} in 10 chips. All chips successfully converted an 80-mV input into a 1.8-V full-swing output. Thus, we defined the minimum V_{DDL} as 80 mV. Fig. 12 (b) shows the results. Fig. 12 (c) shows the results at V_{DDL} = 160 mV, V_{DDH} = 3.3 V, and f_{IN} = 100 Hz. All chips were able to convert to 3.3-V output when V_{DDL} was higher than 160 mV. The minimum V_{DDL} of 160 mV was larger than that at V_{DDH} = 1.8 V. This means that the effect of the supply voltage dependence still exists in the proposed LS. However, we confirmed that the proposed LS can convert an extremely low-voltage input into a high-voltage output.

The maximum operating frequency as a function of V_{DDL} and V_{DDH} is shown in Fig. 14. As V_{DDL} and V_{DDH} increased, the maximum frequency increased. Fig. 15 shows the results at V_{DDH} = 1.8 V as a function of V_{DDL} (10 samples). The maximum operating frequency depended exponentially on V_{DDL} because the delays of the LSs exponentially depend on V_{DDL} in the sub-V_{TH} region. Although the LS can operate below 0.1 V, the maximum frequencies decreased drastically.

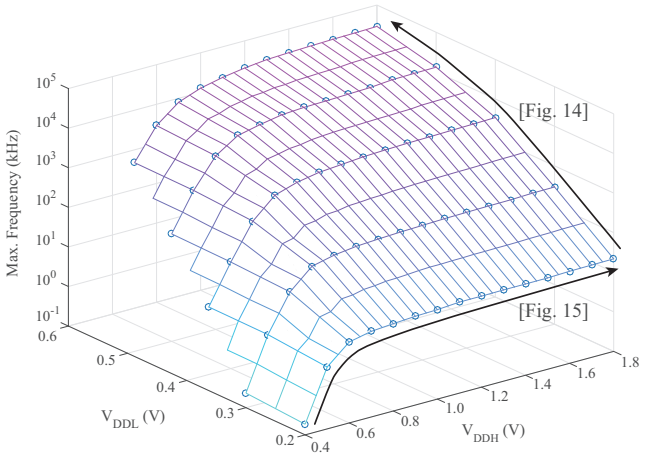

Fig. 14. Measured maximum frequency as a function of V_{DDL} and V_{DDH} (average of 10 samples).

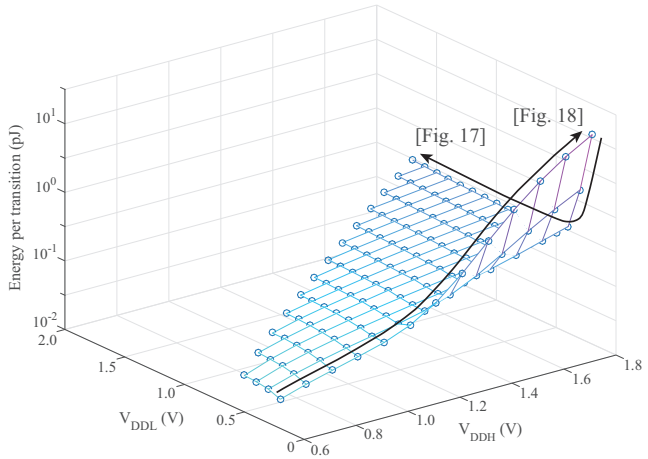

Fig. 17. Measured energy as a function of V_{DDL} and V_{DDH} (f_{IN} = 10 kHz, average of 10 samples).

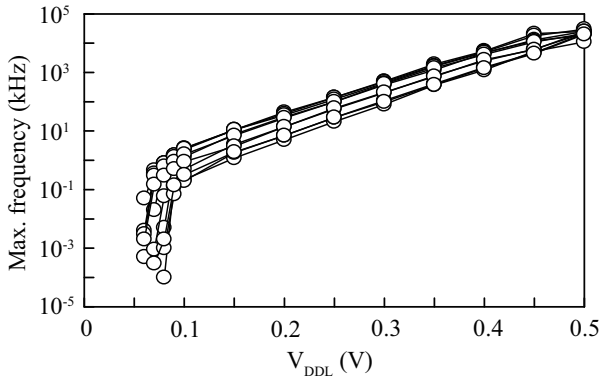

Fig. 15. Measured maximum frequency as a function of V_{DDL} (V_{DDH} = 1.8 V, 10 samples).

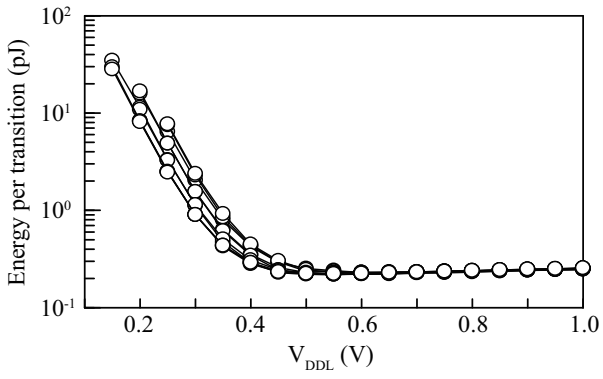

Fig. 18. Measured energy as a function of V_{DDL} (V_{DDH} = 1.8 V, f_{IN} = 10 kHz, 10 samples).

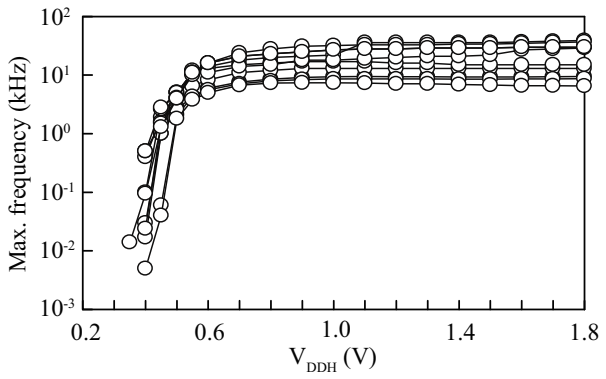

Fig. 16. Measured maximum frequency as a function of V_{DDH} (V_{DDL} = 0.2 V and 10 samples).

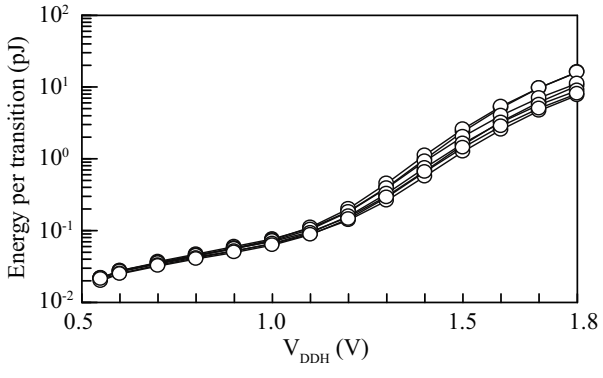

Fig. 19. Measured energy as a function of V_{DDH} (V_{DDL} = 0.2 V, f_{IN} = 10 kHz, and 10 samples).

The maximum frequencies of our 10 samples largely varied. This was because our proposed LS has a two-stage structure consisting of the pre-AMP and latch stage and is therefore susceptible to delay variation. Fig. 16 shows the results at V_{DDL} = 0.2 V as a function of V_{DDH}. Although the LS can operate below V_{DDH} = 0.5 V, the maximum operating frequency decreased drastically. This is because the delays of the LSs have exponential dependence on V_{DDH} in the sub-V_{TH} region.

Fig. 17 plots the measured energy as a function of V_{DDL} and V_{DDH} at f_{IN} = 10 kHz. The energy of the output inverter was included in the measurement. As V_{DDL} decreased and V_{DDH} increased, the energy increased. Fig. 18 shows the results at V_{DDH} = 1.8 V as a function of V_{DDL}. In the sub-V_{TH}

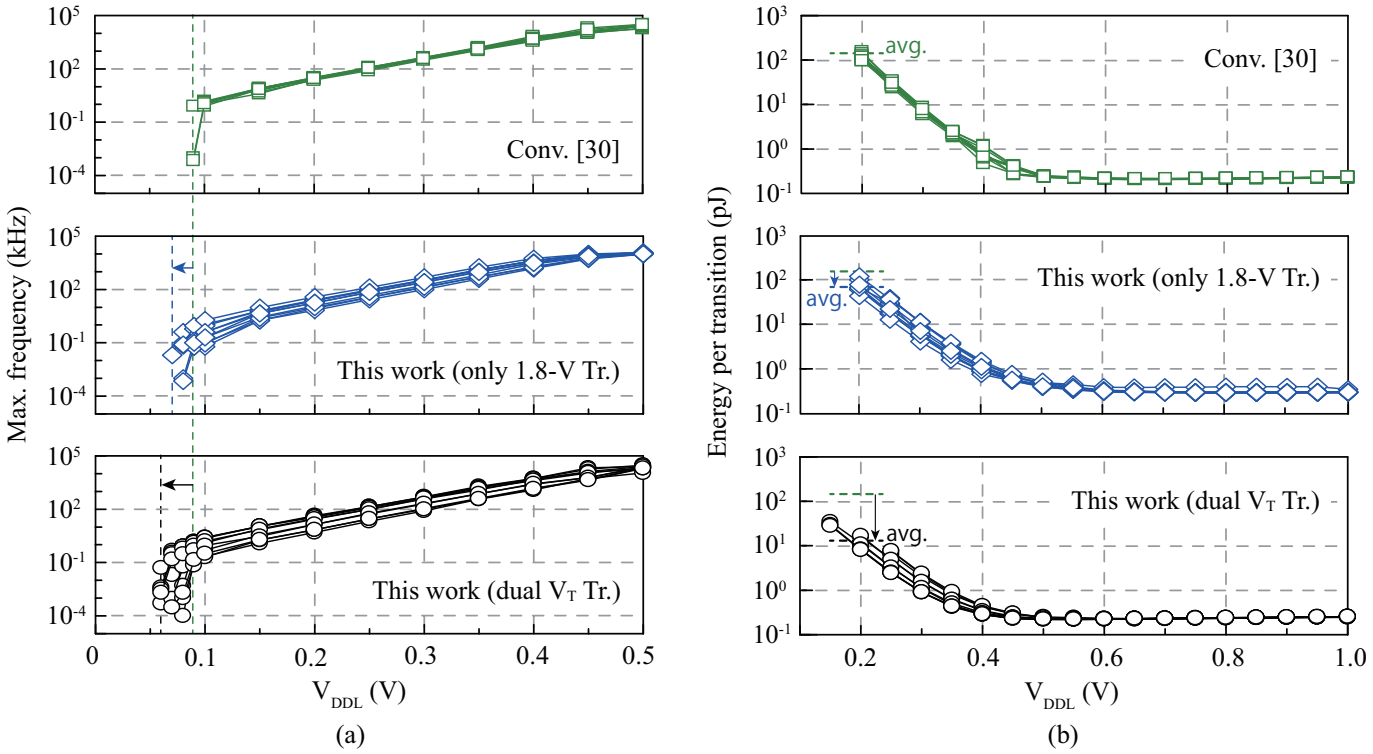

Fig. 20. Measured results of the proposed LS with 1.8-V and 3.3-V Trs., modified LS with only 1.8-V Trs. and the conventional LS [30] as a function of V_{DDL} (V_{DDH} = 1.8 V, 10 samples). (a) Maximum frequency (b) energy (f_{IN} = 10 kHz)

region, the energy increased as V_{DDL} decreased due to the leakage current. This tendency is the same as the results of the conventional LS [27], [29] and the simulation results of the proposed LS. Fig. 19 shows the results at V_{DDL} = 0.2 V as a function of V_{DDH}. Above V_{DDH} = 1.2 V, the energy depended exponentially on V_{DDH}.

For a fair comparison, a conventional LS [30] was also fabricated with the same technology and sizing. In addition, although we used dual V_{T} transistors in this work (i.e., 1.8-V and 3.3-V tolerant Trs.), the proposed LS can be composed of only 1.8-V tolerant transistors. All 3.3-V transistors in Fig. 2 were replaced with the 1.8-V tolerant transistors in the same technology and sizing. Fig. 20 shows the measured results. The maximum operating frequency as a function of V_{DDL} (V_{DDH} = 1.8 V) is shown in Fig. 20 (a). The input voltage that the proposed LS was able to convert into 1.8 V was lower than that of the conventional LS of [30]. The maximum frequency of the LS using only a 1.8-V transistor was comparable to that of the proposed LS. This was because the response time of the LS is mainly determined by the pre-AMP and 1.8-V transistors of MN1 and MN4 are the same in both cases. Fig. 20 (b) shows the measured energy at V_{DDH} = 1.8 V and f_{IN} = 10 kHz as a function of V_{DDL}. The proposed LS achieved lower energy than that of the conventional LS of [30] because the latch stage changed the output quickly due to the signals amplified by the pre-AMP. The energy of the LS using only 1.8-V transistors was larger than that of the proposed LS. This was because the leak current of a 3.3-V transistor is less than that of a 1.8-V transistor. However, because it can be composed of a single transistor, it is beneficial for cost saving.

Table III summarizes the circuit performance of the proposed LS and others [23]–[30] for comparison. Because the advanced technology is suitable for low-voltage operation, we compare our circuit with the-state-of-the-arts, which use the same and advanced technology, except for [23]. The proposed LS converted the lowest input voltage of 80 mV. The energy of the proposed LS was 0.35 pJ at V_{DDL} = 0.4 V and f_{in} = 10 kHz. The proposed LS also had the lowest static power dissipation without input pulse (0.12 nW).

In this design, we used a 0.18-μm CMOS technology for its low-leakage characteristics and high process stability to show the concept of our proposed LS design. We consider that the proposed LS architecture can be used in advanced CMOS technology nodes. This is because the functionality of our proposed LS is mainly determined by that of low-voltage digital circuits themselves, as discussed in [23]. If the low-voltage digital circuits themselves can operate correctly, the proposed LS can also operate successfully. If we choose an advanced technology, the leakage current will increase due to the lower threshold voltage. In such cases, we have to consider to use HVT transistor to reduce the leakage power.

V. Conclusion

In this paper, we proposed a low-power and low-energy LS capable of handling extremely low-voltage input signals into high-voltage output signals. Measurement results demonstrated that the proposed LS in 0.18-μm CMOS technology can convert an extremely low-voltage input of 80 mV into a

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

Reference	Process	# of devices	Min.V_{DDL} (V)	V_{DDH} (V)	E_{tr} (pJ) (@V_{DDL}, f_{IN})	P_{s} (nW)	Delay (ns)	Area (μm^2)
Osaki [23]	0.35 μm	1	0.23 (1)	3.0	5.8 (@0.4V, 10kHz)	0.23	10^4	1880
Kim [24]	0.13 μm	3	0.30 (1)	2.5	0.23 (@0.3V, N/A)	0.48	41.5	102.3
Lanuzza [25]*	90 nm	3	0.18 (2)	1.0	0.074 (@0.2V, 1MHz)	6.4	21.8	36.5
Luo [26]*	65 nm	1$^{\diamond}$	0.165 (1)	1.0 (Max. 1.2)	0.135 (@0.3V, 20kHz)	N/A	N/A	16.8
Zhao [27]	65 nm	3	0.14 (1)	1.2	0.031 (@0.3V, 1MHz)	2.5	25.1	17.6
Mohammadi [28]	65 nm	2	0.12 (1)	1.0 (Max. 1.2)	0.028 (@0.3V, 72MHz)	0.64	66.0	7.8
Shao [29]*	0.18 μm	1	0.13 (1)	1.8	1.7 (@0.4V, 100kHz)	N/A	53.0	N/A
Hosseini [30]*	0.18 μm	1	0.10 (3)	1.8	0.33 (@0.4V, 1MHz)	0.13	30.0	120.9
This work (sim.)*	0.18 μm	2	0.06 (3)	1.8	0.24 (@0.4V, 100kHz)	0.15	21.4	95.6
This work (meas. 1)	0.18 μm	2	0.08 (1)	1.8	0.35 (@0.4V, 10kHz)	0.12	N/A	95.6
This work (meas. 2)	0.18 μm	2	0.16 (1)	3.3	7.19 (@0.4V, 10kHz)	1.5	N/A	95.6

*: Sim. results. $^{\diamond}$: All low-Vt transistors. (1): Meas. results. (2): MC sim. results. (3): Typ. sim. result.

high-voltage output of 1.8 V. The energy of the proposed LS was 0.35 pJ when the V_{DDL}, V_{DDH}, and f_{IN} were set to 0.4 V, 1.8 V, and 10 kHz, respectively. The static power dissipation was 0.12 nW.

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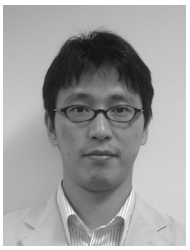

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