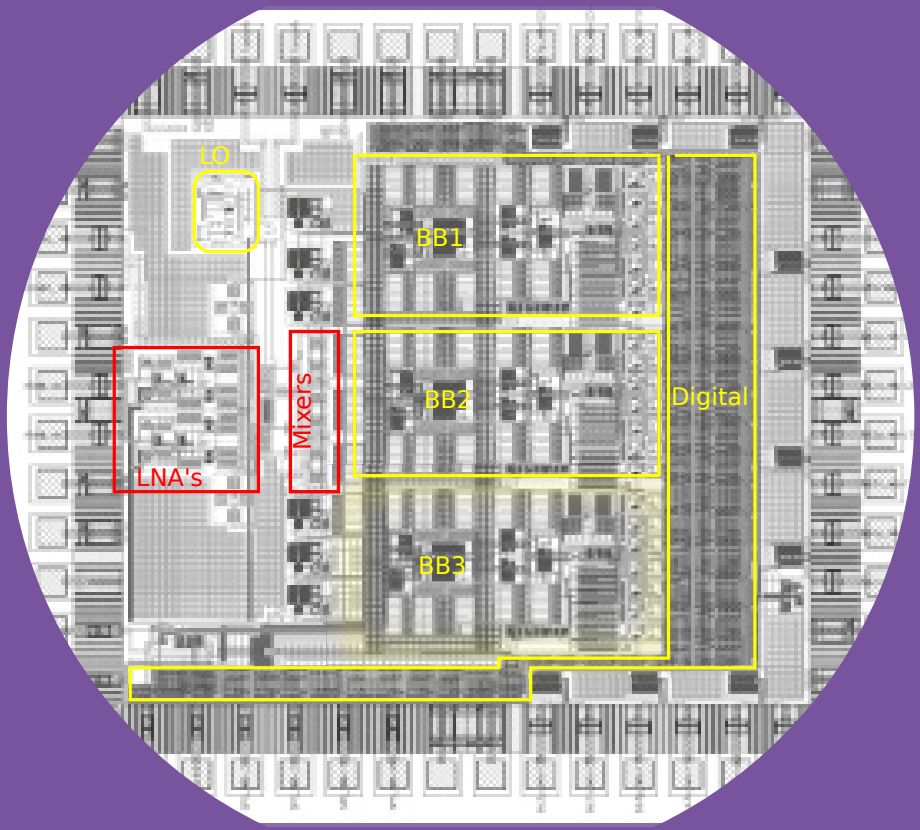
Department of Electronics and Nanoengineering

Integrated Radio-Frequency Receivers for RF-to-Digital Converters

Faizan Ul Haq



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Integrated Radio-Frequency Receivers for RF-to-Digital Converters

Faizan Ul Haq

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Abstract

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Abstract

The widespread usage of mobile communication in recent decades has crowded the frequency spectrum with multiple bands and communication standards. An ideal wireless receiver for such a scenario will need to cover all frequency bands/standards with the possibility of instant reconfigurability through software control. The receiver should also be entirely integrated to gain the advantages of mobility and cheaper production costs. The ultimate goal of an ideal receiver is encapsulated in the concept of software-defined radio (SDR).

An attractive approach to realize an SDR is an RF-to-digital converter. In best case, an RF-to-digital converter consists of an analog-to-digital converter (ADC) which is directly connected to a wideband antenna. This means that the received signal on the antenna is immediately converted in the digital domain where reconfigurability is easy to achieve. However, such a complete RF-to-digital converter has so far proved to be an elusive goal due to impractically high power consumption requirements of ADC in the GHz range. Therefore, a practical RF-to-digital converter is followed by an RF front-end which reduces the power consumption requirements of an ADC by signal amplification, filtering, and frequency down-conversion. SDR research for such a practical case is focused towards reconfigurable, wideband and digital intensive RF front-ends. It is also targetted at reducing the number of parallel receiver front-ends by implementing a single wideband and fully integrated front-end capable of receiving all frequency bands/standards. To design receiver solutions for such a practical RF-to-digital converter, new techniques are needed to overcome the design challenges.

This thesis focuses on finding new solutions to four of these design challenges related to the goal of RF-to-digital converters: 1) Blocker tolerance in wideband RF front-ends; 2) harmonic rejection RF-front ends with on-chip N-path filtering; 3) transmitter self leakage cancellation, and; 4) blocker rejection and sensitivity issues in direct delta sigma receivers.

Starting from the detailed description of these challenges, research outcomes on both theoretical and experimental fronts are presented. In particular, a harmonic-rejection receiver was fabricated in 28nm fully-depleted silicon-on-insulator (FDSOI) technology. The receiver attempts to resolve many of the above-mentioned challenges through higher-order on-chip filtering, simple local-oscillator clocking, and a two-stage harmonic-rejection implementation. The receiver front-end also includes a novel transmitter signal-leakage cancellation technique through buried-gate signaling in an FDSOI process. In addition to the fabricated receiver, the thesis incorporates two new blocker attenuation techniques at the input of the low-noise amplifier in the receiver chain. On the theoretical front, sensitivity issues in direct delta sigma receivers are analyzed with detailed theoretical modeling leading to simple design guidelines. Details of all these contributions can be found in the author's publications I-IX.

Keywords

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Preface

This dissertation is based on work that was performed in 2015-2019 in the department of electronics and nanoengineering, Aalto university Finland. The work was funded by Academy of Finland under the projects named IROC and 5GTRX. I also received a small study-exchange travel grant from the foundation TIES in 2018 for my research collaboration visit in University of Toronto, Canada.

I was honored to have professor Jussi Ryynänen as my supervising professor, who gave me the opportunity to pursue PhD degree in his research group. I especially value his friendly and encouraging attitude along with his willingness to entertain new ideas. My immediate advisor Dr. Kari Stadius deserves a strong acknowledgment for his efforts that guided me in each and every step of my PhD. He was always helpful and shedded light on many things that were previously a mystery to me. I would also like to share my warmest gratitude to my colleagues in Aalto university especially Dr. Mikko Englund with whome I started working as a group from 2015 to 2017. I sincerely value his strong knowledge in the field of receiver design. A strong collaboration, endless discussion and sharing ideas made the project a success. I would also like to thanks my other colleagues Dr. Marko Kosunen, Mr. Olli Viitala, Mr. Tero Tikka, Ms Zahra Khonsari, Mr. Yury Antonov, Dr. Enrico Roverato, Mr. Miikka Tenhunen for close coordination and support on technical matters in different phases of my PhD degree.

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Of course, none of this would have been possible without the help and

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My warmest regards to my parents who have always been there for me. It is because of their love and support that I have been able to come up to this level. I remember the countless efforts of my mother and father teaching me in my childhood days. Finally, I would like to express my deepest gratitude to my wife. Especially during the past three years she suffered due to my long working hours in university and had to take care of son single-handedly. Without your support, achieving this goal would not have been possible.

Espoo, September 5, 2019,

Faizan Ul Haq

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List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I F. Ul Haq, M. Englund, K. Stadius, M. Kosunen, K. B. Östman, K. Koli, and J. Ryynänen. A wideband blocker resilient RF front-end with selective input-impedance matching for direct delta sigma receiver architectures. In *IEEE NORCAS Conference*, pp. 1-4, Copenhagen, Denmark, November 2016.

II F. Ul Haq, M. Englund, K. Stadius, M. Kosunen, K. B. Östman, K. Koli, and J. Ryynänen. A wideband blocker resilient direct delta sigma receiver with selective input-impedance matching. In *IEEE ISCAS Conference*, pp. 1-4, Baltimore, MD USA, May 2017.

III F. Ul Haq, M. Englund, Y. Antonov, K. Stadius, M. Kosunen, K. B. Östman, K. Koli, and J. Ryynänen. Full-duplex wireless transceiver self-interference cancellation through FD-SOI buried-gate signaling. In *IEEE ISCAS Conference*, pp. 1-5, Florence, Italy, May 2018.

IV F. Ul Haq, M. Englund, Y. Antonov, K. Stadius, M. Kosunen, K. B. Östman, K. Koli, and J. Ryynänen. A blocker-tolerant two-stage harmonic-rejection RF front-End. In *IEEE RFIC symposium*, Boston, USA, June 2019.

V F. Ul Haq, K. B. Östman, M. Englund, K. Stadius, M. Kosunen, K. Koli, and J. Ryynänen. A common-gate common-source low noise amplifier

based RF front-end with selective input impedance matching for blocker-resilient receivers. *Wiley journal of circuit theory and applications*, pp. 1427-1442 Vol. 46, Issue. 8, August 2018.

VI F. Ul Haq, M. Englund, K. Stadius, M. Kosunen, K. B. Östman, K. Koli, and J. Ryynänen. Quantization noise upconversion effects in mixer first direct delta-sigma receivers. Accepted for publication in *Wiley journal of circuit theory and applications*, 2019.

VII M. Englund, F. Ul Haq, K. Stadius, M. Kosunen, K. B. Östman, K. Koli, and J. Ryynänen. A systematic design method for direct delta-sigma receivers. *IEEE transactions on Circuits and Systems I*, pp. 2389-2402 Vol. 65, Issue. 8, August 2018.

VIII F. Ul Haq, M. Englund, Y. Antonov, M. Tenhunen, K. Stadius, M. Kosunen, K. B. Östman, K. Koli, and J. Ryynänen. A blocker-tolerant two-stage harmonic-rejection receiver. Submitted to *IEEE transcations on Microwave theory and techniques*, 2019.

IX F. Ul Haq, M. Englund, K. Stadius, M. Kosunen, K. B. Östman, K. Koli, and J. Ryynänen. A wideband blocker resilient direct delta sigma receiver with selective input-impedance matching. Submitted to *Springer journal of analog integrated circuits and signal processing*, 2019.

Author's Contribution

Publication I: "A wideband blocker resilient RF front-end with selective input-impedance matching for direct delta sigma receiver architectures"

The author proposed the selective input impedance concept for blocker rejection. The author developed the idea and circuits with guidance from other authors, performed simulations, wrote the manuscript and presented the work at the conference.

Publication II: "A wideband blocker resilient direct delta sigma receiver with selective input-impedance matching"

The author further extended the selective input-impedance concept for a complete direct delta-sigma receiver. The author performed simulations, wrote the manuscript and presented the work at the conference.

Publication III: "Full-duplex wireless transceiver self-interference cancellation through FD-SOI buried-gate signaling"

The presented RF front-end was fabricated in 28nm technology. The author was responsible for the front-end design, excluding the LO chain. The author conducted all measurements, wrote the manuscript and presented the work at the conference.

Publication IV: "A blocker-tolerant two-stage harmonic-rejection RF front-End"

The presented RF front-end was designed collaboratively with the co-authors. The author was responsible for the front-end design, excluding the LO chain. The author made the prototype PCB, conducted all the measurements, wrote the manuscript and presented the work at the conference.

Publication V: "A common-gate common-source low noise amplifier based RF front-end with selective input impedance matching for blocker-resilient receivers"

The author developed the original concept of Dr. Östman, derived the theoretical analysis and design guidelines, performed simulations and wrote the manuscript.

Publication VI: "Quantization noise upconversion effects in mixer first direct delta-sigma receivers"

In co-operation with the other authors, the author developed the mixer-first DDSR model for analyzing the quantization noise upconversion effects, derived the design guidelines based on analytical and simulated results and implemented a transistor level prototype of the mixer first DDSR, except the quantizer and LO chain. The author also wrote the manuscript.

Publication VII: "A systematic design method for direct delta-sigma receivers"

The paper presents a systematic design method for gmC-based direct delta sigma receivers. The author co-developed the RF front-end specifications and circuits for the envisioned design method with the main author of paper.

Publication VIII: "A blocker-tolerant two-stage harmonic-rejection receiver"

The author was responsible for design of the RF front-end, PCB design, and measurements for the whole receiver including both analog front-end and digital quantizer output measurements. The author was the main writer of the submitted manuscript.

Publication IX: "A wideband blocker resilient direct delta sigma receiver with selective input-impedance matching"

This publication was an extended version of the previous ISCAS 2017 conference publication II. The author extended the previous work through supporting theoretical analysis, design guidelines, in-depth literature review and a gain requirement comparison between Nyquist-based ADCs and DDSR. The author was the main writer of the manuscript.

List of Abbreviations

4G	fourth generation
ADC	analog-to-digital converter
AWGN	additive white guassian noise
BAW	bulk acoustic wave
BB	baseband
BCP	blocker compression point
BER	bit error rate
BNF	blocker noise figure
CG	common gate
CMOS	complementary metal-oxide semiconductor
CS	common source
CW	continuous wave
DAC	digital-to-analog converter
DDSR	direct delta-sigma receiver
DR	dynamic range
F	noise factor
FD	full-duplex
FDD	frequency-division duplex

FDSOI	fully-depleted silicon-on-insulator
I	in-phase
IC	integrated circuit
ICP	input compression point
IDAC	current output digital-to-analog converter
IF	intermediate frequency
IFA	intermediate frequency amplifier
IIP2	input second-order intercept point
IIP3	input third-order intercept point
LNA	low-noise amplifier
LNTA	low-noise transconductance amplifier
LO	local oscillator
LTE	long-term evolution
LTE-A	long-term evolution advanced
LTI	linear time invariant
LVDS	low-voltage differential signaling
NF	noise figure
NRZ	non return to zero
NTF	noise transfer function
OB	out of band
OFDM	orthogonal frequency division multiple access
PCB	printed-circuit board
PN	phase noise
Q	quadrature
Qn	quantization noise

QPSK	quadrature phase-shift keying
RF	radio frequency
S	sensitivity
SAW	surface acoustic wave
SDR	software-defined radio
SI	self interference
SNDR	signal-to-noise and distortion ratio
SNR	signal-to-noise ratio
TRF	tuned radio-frequency receiver
TX	transmitter

List of Symbols

$AopendB$	required voltage gain of third-order integrator
A_{vRF}	RF voltage gain of proposed LNA
C_1	feedback capacitance of proposed LNA from drain to gate of common-gate transistor
C_2	feedback capacitance of proposed LNA from gate to ground of common-gate transistor
C_{F}	third-order feedback capacitor
C_{GD}	gate-to-drain parasitic capacitance
C_{in}	combined input parasitic capacitance of proposed LNA
C_{L}	gyrator capacitor
C_{NP}	N-path capacitor
C_{out}	combined output parasitic capacitance of proposed LNA
Z_{COUT}	equivalent impedance of $\mathrm{C_{out}}$
f_1	first input tone frequency
f_2	second input tone frequency
f_{BW}	baseband bandwidth
$\mathrm{F_i}$	noise factor of ith stage
$\mathrm{G_i}$	gain of ith stage
f_{LO}	local oscillator frequency
f_{ns}	noise-shaping pole frequency
f_{s}	sampling frequency
f_{z}	third-order resonance zero frequency

gm_1	common-gate amplifier transconductance
gm_2	common-source amplifier transconductance
$g_{\mathrm{m,BB}}$	baseband amplifier transconductance
$g_{\mathrm{m,FB}}$	effective transconductance of first IDAC
Z_{RF}	impedance connected to RF side of passive mixer
g_{mL}	trasnconductance of gyrator transconductors
G_{Q}	quantizer gain
G_{rel}	relative gain: ratio between gate and buried-gate input powers
H_{FB}	transfer function from DDSR output to baseband input
$H_{\mathrm{FB,upn}}$	transfer function from DDSR output to RF input at n-th harmonic
H_{I}	integrator transfer function
H_{Q}	quantizer transfer function
$IMD2$	second-order intermodulation product
$IMD3$	third-order intermodulation product
k	Boltzman's constant
L	power loss
P_1	first input test signal power
P_2	second input test signal power
P_{blocker}	blocker power
$P_{\mathrm{buriedgate}}$	input signal power at buried-gate
P_{gate}	input signal power at gate
P_{IMD3}	third-order intermodulation product power
P_{max}	maximum input power
P_{FS}	ADC full-scale input signal power

P_{S}	minimum sampling power of ADC
SNR_{tar}	target SNR
Z_{IN}	LNA input impedance
Q_{up}	upconverted quantization noise
R_{c}	complex feedback resistance to compensate N-path phase/frequency shift
R_{L}	resistance in third-order feedback
R_{in}	equivalent output impedance of mixer and LNA
R_{obb}	baseband transconductor output resistance
ro_{CG}	common-gate amplifier output resistance
ro_{CS}	common-source amplifier output resistance
R_{oL}	gyrator transconductor output impedance
R_{oLNA}	LNA output impedance
R_{S}	source resistance
R_{SH}	equivalent impedance representing mixer harmonic losses
R_{SW}	mixer switch resistance
S_{11}	input scattering parameter
$slopedB$	desired slope of third-order integrator
$\mathrm{SNR}_{\mathrm{in}}$	input signal signal-to-noise ratio
$\mathrm{SNR}_{\mathrm{min}}$	minimum signal-to-noise ratio
$\mathrm{SNR}_{\mathrm{out}}$	output signal signal-to-noise ratio
$\mathrm{SNR}_{\mathrm{peak}}$	peak signal-to-noise ratio
T	temperature
V_{DSAT}	transistor saturation voltage
V_{FS}	upper voltage swing limit
V_{out}	output voltage

V_{S}	supply voltage
Z_{BB}	baseband amplifier input impedance
Z_{CNP}	equivalent impedance of N-path capacitor C_{NP}
Z_{i}	input impedance
Z_{L}	equivalent load impedance of propose LNA
Z_{NP}	equivalent input impedance of quadrature N-path filter from RF side
Z_{o}	source impedance
β	feedback factor of proposed LNA
γ	constant mosfet noise parameter
Δ	quantization step
ζ	frequency scaling factor in N-path LTI model

1. Introduction

1.1 Background

From the very beginning of recorded time, mankind has communicated with each other in some form or another. Over time these means of communication evolved to cope with the ever-growing demand for sending information over long distances in a fast and a reliable manner. The discovery of electromagnetic waves in the late 19th century as a mean of fast and long distance communications opened a new era of wireless communications [1, 2]. Fueled by new inventions in the field on electricity, the 21st century witnessed a rapid evolution of wireless communication. Starting from the invention of the radio, right up to the development of modern fourth generation (4G) mobile phone receivers, wireless communication technology has come a long way [3]. Today's communication receivers need to operate under the presence of multiple nearby interfering signals while at the same time should be able to tune into a particular reception band. Another parallel trend that has greatly impacted the design of communication receivers has been the on-going process of electronics integration which has occurred in the past few decades. The ultimate goal is to include all needed electronics in a single integrated circuit (IC) resulting in increased speed and cheaper production costs [4]. Accelerated by the development of smaller and faster complementary metal-oxide semiconductor (CMOS) process generations that are needed to fabricate the IC's, the miniaturization trend of wireless receivers is shifting towards more digital intensive solutions. This is because the newer CMOS processes are generally more digital friendly. All these technology trends dictate that an ideal wireless receiver should be able to receive any signal frequency, while at the same time be completely integrated with no external components [5]. Such a

receiver should also be able to cope with strong interfering signals from nearby transmitters while still receiving the desired signal. Unfortunately, such a receiver does not exist in reality. Nevertheless, if we take a more practical approach to these requirements, a great deal of modern wireless receiver research focuses on making such receivers more reconfigurable, interference-tolerant, digital intensive, energy efficient and smaller [6–10].

1.2 Objectives of the work

The objective of this thesis is to find innovative solutions towards the goal of completely integrated, interference-tolerant and reconfigurable wideband receivers. First, the integration is required to increase the mobility, speed and reduce production costs of wireless receivers. Second, interference tolerance is needed when a single receiver covers a broad frequency range. Inevitably, such a receiver will pick up the desired signals as well as unwanted interferers from surrounding transmitters which needs to be filtered. Third, reconfigurability is a result of strong demand for a single receiver to be able to receive multiple frequency standards/bands. Such a receiver will eliminate the need for parallel receive chains, each dedicated to a specific standard/band.

1.3 Main scientific merits

To achieve the target objectives of this work, research was carried on both theoretical and experimental fronts. A full radio frequency (RF) receiver with two-stage harmonic rejection was fabricated and measured while, at the same time, various theoretical investigations were conducted on new innovative circuits for wireless receivers. The details of all these research outcomes are embodied in publications I-IX. The most important contributions to the scientific community are summarized below:

1. A two-stage blocker-tolerant harmonic-rejection receiver was fabricated and measured. The receiver also incorporated third-order N-path filtering for the suppression of near-band blockers. At the time of publication, the measurement results demonstrated impressive blocker rejection for blockers present at the third harmonic of the local-oscillator frequency. The results are detailed in publications IV and VIII.

2. A novel approach for transmitter signal leakage cancellation was proposed through buried-gate signaling in fully-depleted silicon-on-insulator (FDSOI) technology. A test RF front-end was fabricated and measured to validate the chosen approach. Details can be found in publication III.

3. A capacitive feedback based LNA was proposed which achieved blocker rejection both at the input and output nodes of the LNA. Detailed theoretical analysis was carried out resulting in design guidelines. Details can be found in publication V.

4. A blocker rejection positive feedback DDSR was proposed and simulated. Blocker tolerance was achieved by attenuating blockers already at the input of the receiver through selective impedance matching. Details can be found in publications I,II and IX.

5. Quantization noise upconversion effects in mixer-first DDSR on receiver sensitivity were analyzed. Systematic modeling of upconverted quantization noise was carried out in VI.

6. Design guidelines for mixer-first DDSR were formulated in VI.

7. A method to improve blocker rejection through the reduced gain method in DDSRs was proposed in II, IX, and VII.

1.4 Contents and organization of the thesis

This thesis is organized into two parts. The first part is introductory and provides an overview of the target research field with a summary of the key research findings by the author. The second part consists of a compilation of scientific publications I-IX by the author.

Chapter 2 starts with an overview of the target research field. It builds up the necessary background and technical definitions needed to understand the given research field. Once the reader is familiar with the background knowledge, it is easier to follow the research contributions by the author detailed in chapters 3 to 6.

Specifically, chapter 3 deals with new solutions for blocker-tolerant RF front-ends. Three solutions are presented here: 1) A third-order N-path

filter implementation in 28nm for near-band blocker suppression; 2) a new capacitive feedback LNA with blocker attenuation at both of its input and output nodes, and; 3) a novel transmitter leakage cancellation technique using a buried-gate in an FDSOI process.

Chapter 4 presents an implementation of a 6-phase two-stage harmonic-rejection receiver in 28nm FDSOI technology. The proposed receiver uses simpler local oscillator (LO) clocking and reduced baseband paths compared to 8-phase harmonic-rejection architectures and uses simple ± 1 gain coefficients.

Chapter 5 addresses the research outcomes in the field of direct $\Delta\Sigma$ receivers. First, a positive feedback technique from the DDSR output provides blocker attenuation at the DDSR input. Second, a reduced gain design method is proposed for blocker-tolerance in DDSRs and, third the degrading effects of quantization noise upconversion on mixer-first DDSR sensitivity are analyzed.

2. Wideband integrated receiver design

This chapter provides background information to the field of wireless receiver design. The aim is not to provide an in-depth description of the research field but rather an overview is given which will then serve as a basis for understanding the research outcomes in later chapters. The chapter starts with the overview of wireless communication in today's world and description of some of the widely used receiver architectures such as superheterodyne and direct-conversion receivers. This description is followed by an explanation of performance matrices for a receiver with a discussion on current and future research trends in wireless receiver design. At the end, an overview of current state-of-the-art blocker-tolerant and fully-integrated receivers is provided.

2.1 Overview

Imagine sitting in a room with only two people. The person who is talking is analogous to a wireless transmitter while the person listening bears a resemblance to a wireless receiver. Such a scenario is quite simple as the listing person only needs to focus his/her attention on the speaker. There are no other speaking persons in the room who can interfere with the oral communication. Therefore, the ears of the listener just need to focus on a single audio reception. On the other hand, if the same gathering would have been occupied with multiple people having a conversation, then the listener's ears will not only need to focus on the desired talking person but will also have to distinguish between strong interfering audio signals which are nearby. Today's wireless communication scenario is no different from the above analogy. Multiple wireless communications at different transmit frequencies and standards overcrowd the environment, and the wireless receiver task is to not only faithfully pick up the desired signal

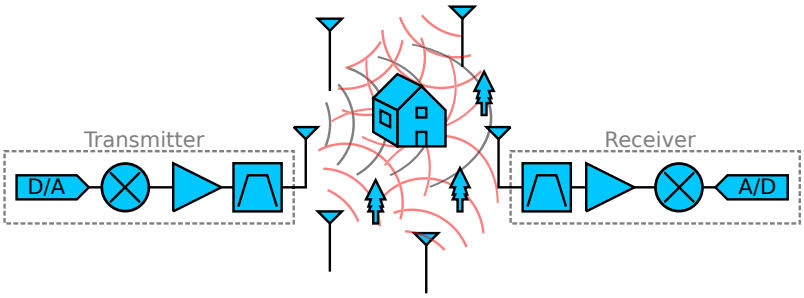

Figure 2.1. Wireless communications scenario.

but also to filter out large unwanted interferers.

Fig. 2.1 shows a simplified scenario of wireless data transmission. A transmitter does some signal processing with the transmitted signal and then radiates it through the air as electromagnetic waves from the antenna. The antenna at the receiver ends receives this electromagnetic wave and then it is the receiver's job to discriminate the desired transmitted signal from multiple other interfering signals. In this regard, the receiver should be selective in receiving the desired signal while at the same time filtering out the non-desired interferers. The receiver should also be highly sensitive to receive weak electromagnetic signals attenuated by environmental effects and obstacles. Such requirements are challenging to implement due to rapidly increasing wireless communications standards and frequency bands. Nonetheless, a few widely implemented receiver architectures which have partially served these requirements will be highlighted next.

2.2 Major receiver architectures

The following section covers some of the major wireless receiver architectures. The discussion is not meant to provide an exhaustive study. Rather, a brief overview is given which is intended to familiarize the reader with the most widely used implementations. This serves as a basis for understanding the research outcomes from the author in the later chapters. For detailed reading on receiver architectures, the reader may please refer to previous works from the author's research group [11–13].

In the beginning of wireless communications, radio receivers were just a detector connected directly to the antenna [14, 15]. Further improvements were achieved with a tuned radio-frequency receiver (TRF) which was composed of one or more tuned radio frequency amplifier stages followed

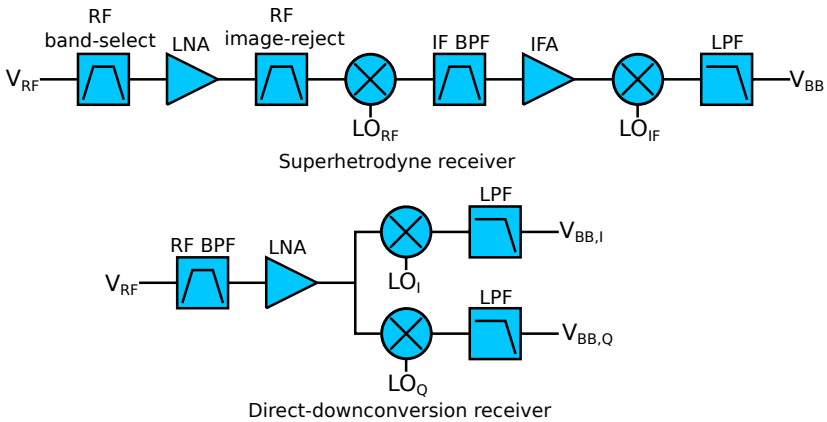

Figure 2.2. Basic block diagram of superheterodyne and direct-downconversion receivers.

by a detector. TRFs however had the drawback of tedious operation when tuning to a different station. Each receiver stage had to be individually adjusted to the station frequency.

The tuning problems related to TRF receivers were solved by the development of a revolutionary receiver architecture called the superheterodyne [16, 17]. Developed in the early 20th century by Armstrong, the superheterodyne receiver has been one of the most widely manufactured receivers to date. Fig 2.2 shows the block diagram of a superheterodyne receiver. An input signal from the antenna first passes through an RF band-select filter followed by an LNA which amplifies it. The amplified signal is then passed through an image-reject bandpass filter, a downconverting mixer to convert the RF signal to lower intermediate frequency (IF), an IF bandpass filter, and an IF amplifier. In some modified superheterodyne architectures, an additional downconverting mixer can also be used after the intermediate frequency amplifier (IFA) to relax an inherent compromise between channel-selection and image-rejection [18].

The advantages of the superheterodyne architecture are many, one of the distinct advantages being the ease of circuit design for lower IF signals in comparison to RF circuits. Downconversion to low IF also makes it possible to implement high-quality sharp filters as they are easier to implement at lower frequencies. These advantages of the superheterodyne architecture led to it becoming the commercial receiver architecture of choice for several decades. However, despite the advantages, the superheterodyne architecture has some serious problems with regard to image-rejection and integrability. The problem of integrability arises due to limitations in implementing high-quality RF bandpass filters on ICs. The need for com-

pletely integrated receivers has become even more critical with the advent of mobile cellular radio systems. Users desire every new generation of mobile receivers to be smaller yet still packed with more and more demanding functions. In addition, integration brings additional benefits of less expensive and mass-marketable user equipment. Towards this end, some major attempts to provide image-rejection without high-quality bandpass filters are the Hartley and Weaver image-rejection receivers [19–21]. Additionally, some recent attempts to implement fully-integrated superheterodyne receivers with discrete-time filtering have been reported in [22–25], while in [26] a superheterodyne receiver with an integrated high-Q bandpass filter has been presented.

Another receiver architecture which emerged as an integration-friendly alternative to the superheterodyne is known as a direct conversion or homodyne receiver architecture [18, 27, 28]. The block diagram of a typical direct-conversion receiver is shown in Fig. 2.2. An RF bandpass filter attenuates the out-of-band interferers received at the antenna. An LNA then amplifies the filtered signal which is directly down-converted to zero-IF frequency through passive mixers. The mixer and post-mixer circuits are divided into an in-phase (I) and quadrature (Q) branches with 90° phase difference. The quadrature downconversion prevents the self-corruption of downconverted spectrum for asymmetrically-modulated signals [18]. These I and Q signals are then digitized for further processing.

Downconversion to zero-IF frequency has multiple advantages. First, zero-IF downconversion eliminates the problem of image frequency as is present in superheterodyne receivers. This means that the image-rejection filter can be eliminated which would otherwise have to be implemented with non-integrated components. Further, the post-mixer IF filter is replaced from a bandpass filter to a low-pass filter which is also more straightforward to implement on IC. Therefore, apart from the first band-select filter before the LNA, all other circuits can be easily integrated on-chip.

The main benefit of integrability is counterbalanced by several problems inherent to the direct-conversion receiver [11, 18, 29]. Some of the most important ones can be mentioned as: dc offsets generated by LO frequency leakage to an antenna, flicker noise effects, and second-order intermodulation effects.

The first problem of dc-offsets can be quite severe in the direct-conversion receiver. These offsets are generated by LO signal leakage to the antenna. The leaked LO signal will then self-mix with the LO and downconvert

to dc at the input of the baseband chain. As the baseband amplifier as generally an active structure, any dc offsets present at their input when amplified with baseband gain can overload the baseband amplifiers and, consequently, the analog-to-digital converter (ADC) converter that follows it. Second, flicker noise is a type of noise exhibited by the transistors at very low frequencies. It decreases with a slope of 10dB/decade with increasing frequencies and eventually falls lower than the thermal noise level of the transistors. This noise can potentially reduce the sensitivity of the direct-conversion receiver for the lowest frequency contents of the desired signal. Finally, the second-order intermodulation products created by the interferers present at the input of the receiver can appear in the downconverted baseband signal by the direct-feedthrough of the mixers, therefore, desensitizing the receiver [30].

From the above discussion it is evident that neither the superheterodyne nor direct-conversion receiver is a clear winner over the other in terms of performance. Each architecture has its advantages and disadvantages. Nevertheless, the clear advantage of integrability has led to the widespread adoption of the direct-conversion receiver in recent years though attempts for a superheterodyne comeback have been made [22–26, 31]. Superheterodyne architecture also seems to be a more reasonable choice in millimeter-wave frequencies due to practical limitations in high-frequency quadrature local-oscillator signal generation [32–34].

In which direction is the design of wireless receiver likely to head? An attempt to answer this question requires a more thorough understanding of receiver performance parameters. In the following section, the essential performance matrix related to a wireless receiver is explained briefly. Once the reader is more familiar with this matrix, it becomes easier to attempt an explanation for current and future research trends of wireless receivers.

2.3 Performance requirements

2.3.1 Input impedance matching

Input impedance matching is an important requirement at the antenna receiver interface. The need for impedance matching arises in order to prevent the signal reflecting from the receiver input. Signal reflections can occur if the distance between the source and load is larger than $\lambda/4$ [35].

Here λ is the wavelength of the signal in question, at 5GHz and for a substrate permittivity of 4, this distance becomes 7.5mm which is easily comparable to the printed-circuit board (PCB) dimensions.

The level of input matching is usually quantified in terms of scattering parameter S_{11} which tells how well the input impedance Z_{i} is matched with the reference source impedance Z_{o} [36].

$$S_{11} = \frac{Z_i - Z_o}{Z_i + Z_o} \tag{2.1}$$

In the design process, S_{11} is usually targeted to be < -10dB at the receiver input interface. From S_{11}, the power loss L due to impedance mismatch can be defined as

$$L = 10log(1 - |S_{11}|^2) \tag{2.2}$$

2.3.2 Sensitivity and noise performance

The sensitivity (S) of the receiver is defined by the minimum signal level that can be detected by the receiver with a sufficiently low bit error rate (BER). For a proper reception, the signal received at the receiver input should be sufficiently higher than the integrated noise of the receiver. In other words, this means that there is a minimum signal-to-noise ratio $\mathrm{SNR_{min}}$ requirement which will ensure sufficiently low BER. The exact value of $\mathrm{SNR_{min}}$ is dependent on the used modulation scheme and is generally fixed for a given communication standard. Therefore, if we want to increase receiver sensitivity, then the receiver itself should ideally add no additional noise inside the reception band. In reality, however, every receiver will add some noise on top of the integrated thermal noise of the receiver, consequently decreasing the signal-to-noise ratio (SNR) at the output of the receiver.

The deterioration of receiver SNR is quantified by the noise factor (F) or noise figure (NF) given by:

$$F = \frac{SNR_{IN}}{SNR_{OUT}} = 1 + \frac{\overline{e_{out}^2}}{4kTR_S(\frac{V_{out}}{V_S})^2}, \tag{2.3}$$

$$NF = 10log(F) \tag{2.4}$$

where k is the Boltzmann constant, T is the temperature in Kelvin, R_{S} is the source resistance, V_{out} and V_{S} are the output and source voltages,

SNR_{in} and SNR_{out} are the signal-to-noise ratios at the input and output, and $\overline{e_{out}^2}$ is the output noise power density.

Generally, for a given communication standard, sensitivity and SNR_{min} are predefined. The designer need to then calculate the target NF of the receiver from these specs as:

$$NF = 174dBm - 10log(f_{BW}) - SNR_{min} + S \tag{2.5}$$

where f_{BW} is the receiver baseband bandwidth. An example of such a calculation can be given for the long-term evolution (LTE) communication standard. The LTE standard occupies a majority of its frequency bands ranging from 700MHz to 2700MHz with the channel-bandwidths from 1.4 to 20MHz. If we take 20MHz channel bandwidth as an example, then the LTE specifications [37] define a target sensitivity between -94dBm and -90dBm. This level of input power should be able sustain data throughput with a maximum BER of 5%. The BER can be linked to SNR_{min} for a given modulation scheme. For example, LTE uses orthogonal frequency division multiple access (OFDM) as a modulation scheme and for OFDM with quadrature phase-shift keying (QPSK) and additive white guassian noise (AWGN) channel, 5% BER relates to a minimum theoretical SNR_{min} of 6dB [38, 39]. For these specifications, the required NF of the receiver from Eq. 2.5 results in 4dB for a sensitivity level of -94dBm.

The overall NF of the receiver is a result of noise contribution from each receiver stage. Typically, gain is applied in the first stage of the receiver to reduce the noise contribution of later stages. In the presence of gain, the contribution of noise from later stages on overall receiver NF is characterized by the Friss equation given by [18]:

$$F_{RX} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_2} +, ... \tag{2.6}$$

where the F_i is the noise factor on ith stage while G_i represents the power gain of each stage.

2.3.3 Blocker noise figure and reciprocal mixing

The NF of the receiver, when it is exposed to a strong blocker signal of a given power $P_{blocker}$ is known as the blocker noise figure (BNF). The BNF is generally higher than NF for two reasons. First, due to reciprocal mixing and second due to 2nd and 3rd-order non-linearities [40].

Reciprocal mixing is a phenomena when a high power blocker gets do-

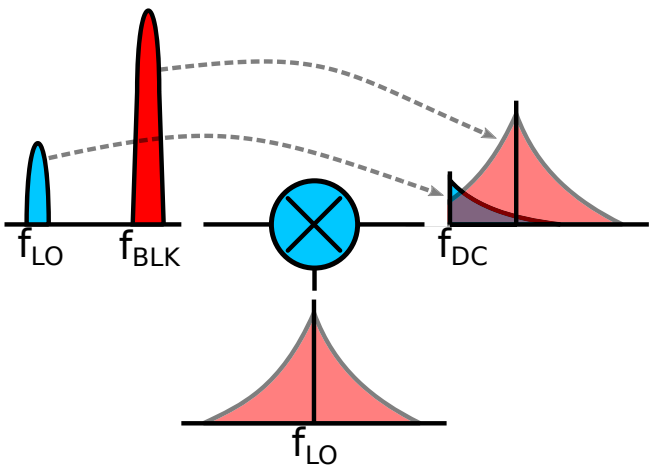

Figure 2.3. Reciprocal mixing with the blocker signal causing LO phase noise to appear inside the desired channel.

wnconverted with a noisy local-oscillator LO source to increase the NF of the receiver. Fig. 2.3 explains the reciprocal mixing where the phase noise (PN) of an LO signal mixes with the blocker and falls inside the desired band. This increases the in-band noise of the receiver. In order minimize the impact of blocker on receiver NF, the local-oscillator PN should be lower than integrated thermal noise floor of receiver. Analytically PN can be calculated as [41]:

$$PN + 10log(f_{BW}) + P_{blocker} < S - SNR_{min} \tag{2.7}$$

where P_{blocker} is the blocker input power. For example, for LTE specifications of S = -94dBm, SNR_{min} = 6dB, f_{BW} = 10MHz and $\text{P}_{\text{blocker}}$ = -15dBm at an 85MHz offset, one can derive the target LO phase-noise lower than -155dBc/Hz at the 85MHz offset.

2.3.4 Linearity: Intermodulation

The non-linear relationship between the output and input of a transistor gives rise of intermodulation products in the output spectrum. These products can cause problems in the reception of a weak desired signal and, therefore, targeted to be much lower than the thermal noise floor of the receiver. The level of these intermodulation products is defined mainly by input third-order intercept point (IIP3) and input second-order intercept point (IIP2) small signal matrices. These are obtained by exposing the

receiver input to two RF tones at f_1 and f_2. These frequencies will result in intermodulation products at $2f_1$-f_2, $2f_2$-f_1 and $|f_1 \pm f_2|$. The first two terms are used to define the third-order intermodulation product while the last term refers to the second-order intermodulation product.

When the input test signal power increases, these intermodulation products increase with the slope of three and two in comparison to the fundamental signal power. The values of IIP3 and IIP2 can then be calculated by extrapolating the slopes of the fundamental as well as second and third intermodulation products. The fictitious point where these slopes meet defines the IIP3 and IIP2 as shown in Fig. 2.4. These parameters can also be derived through calculations as:

$$IIP3 = P_1 + \frac{P_2}{2} - \frac{1}{2}(P_{IMD3} - G), \tag{2.8}$$

$$IIP2 = P_1 + P_2 - (P_{IMD2} - G), \tag{2.9}$$

where P_1 and P_2 are the test signal powers in dBm at the input, $IMD3$ is the third order intermodulation product in dBm, $IMD2$ is the second order intermodulation product in dBm, and G is the small-signal gain of the system at the frequency of the intermodulation product.

IIP3 and IIP2 specifications become more critical in certain reception scenarios. For instance, one difficult scenario where IIP3 needs to be high is when a strong signal f_1 is located between the received signal and transmitter signal f_2. This will generate third-order intermodulation tone at $2f_1$-f_2, i.e., on top of the down-converted desired signal. Another example case when IIP2 specifications need to be high can be given for a frequency-division duplex (FDD) system. In FDD systems, transmission and reception occur at same the time creating a problem of high transmitter (TX) signal leakage at the receiver input. This TX signal will cause second order distortion at the receiver output due to the intermodulation of the TX signal with itself. The generated second-order distortion may fall in the desired channel and degrade receiver sensitivity [42].

An example of deriving the receiver IIP3 specification for a communication standard, can be given for LTE specifications [37]. The standard specifies a maximum in-band input power P_{max} of -25dBm while a blocker of -15dBm can be tolerated at a 85MHz offset from the desired channel. Further, the required peak SNR for most of the modulation schemes is below 30dB [43]. Assuming a required 40dB SNR_{peak} for safety margin, the target IIP3 value of the receiver can be calculated by making sure

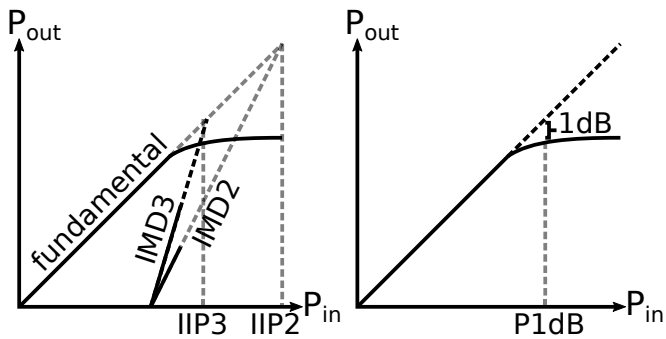

Figure 2.4. Linearity measures: IIP2, IIP3 and P1dB.

P_{IMD3} remains below the thermal noise floor. For such a case minimum IIP3 can be calculated as:

$$IIP3 = P_{max} + \frac{SNR_{peak}}{2} = -5dBm \tag{2.10}$$

Similarly, for an out-of-band maximum blocker power of -15dBm, the out-of-band IIP3 can be derived as +5dBm.

2.3.5 Linearity: Compression

When the test input signal power of the receiver increases, the output power stops increasing beyond a certain point. This is called compression, and the matrix that defines the receiver compression behavior is called the compression point. An input compression point (ICP) can be defined as the input test signal power at which the output power drops 1dB below its nominal value determined by small-signal gain. In contrast to IIP3 and IIP2 matrices, the ICP is a large-signal matrix because the input test signal power is high. The ICP can be defined for both an in-channel or out-of-channel signal. The latter is usually referred to as the blocker compression point (BCP).

The BCP is more interesting, in a wideband receiver scenario because it dictates how well the receiver is able to amplify a weak signal under the presence of a strong out-of-channel blocker. These blockers can either be from the device own transmitter or from the transmitters of other co-existing devices. These can also be from other standards in the same device. For example, coexistence of WiFi, Bluetooth and LTE transceivers in the same device [44, 45].

2.4 Research trends: From present to future

As detailed earlier, today's wireless receivers need to operate over a wide frequency range while covering multiple communication standards. The majority of the wireless receivers achieve this task by implementing parallel front-end paths each tuned to a particular reception band/standard. Obviously, this is not an optimum solution due to an increased number of components leading to higher production costs and complexity. What is ideally needed is a single wideband receiver which should be able to receive all reception bands/standards with the possibility of instant software reconfigurability. On top of it, the receiver should be completely integrated with no off-chip components to gain advantages of mobility and lower manufacturing costs. The ultimate goal of further receiver development is encapsulated by the concept of software-defined radio (SDR) [5, 46].

An attractive way to implement the SDR paradigm is an RF-to-digital converter implementation where an ADC is directly connected to a wideband antenna to immediately digitize the received signal [47]. Once the signal is in the digital domain, all functions of programmability can be attained by utilizing the inherent advantages of digital technology. However, such an RF-to-digital converter will be exposed to various high power interferers leading to very high dynamic range (DR) requirements of up to 100dB [48, 49]. Moreover, the reception frequencies in the GHz range require high GHz sampling frequencies of the ADC. Both the dynamic range and higher sampling frequency requirements of the needed ADC lead to highly impractical power consumption requirements from the ADC. For example, according to [50], the minimum sampling power P_{S} required by the ADC is given as:

$$P_S = 48kTf_s2^{2N} \tag{2.11}$$

where N is the number of bits and f_{s} is the ADC sampling frequency. [50] shows that the high speed Nyquist ADCs still burn 50-100 times more than the above limit. As a practical example, a reception frequency of 1.5GHz (f_{s} = 3GHz) and N = 13bits will lead to P_{S} of at least 2W.

Some emerging ADC architectures such as band-pass continuous-time $\Delta\Sigma$ ADC's have tried to address the problem of high power consumption. The reported band-pass $\Delta\Sigma$ ADC center frequencies extend up to a few GHz, with power consumption ranging from 40mW to 1600mW and dynamic ranges up to 73dB [51–56]. These specifications lie within the desired

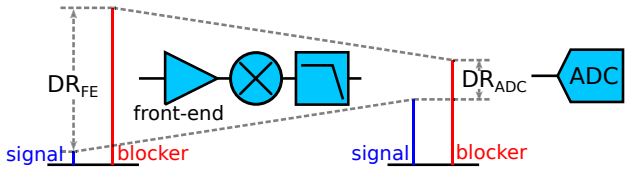

Figure 2.5. Conceptual representation of reduction in ADC dynamic range from the front-end.

range for many GHz communication standards. However, the estimated NF of such structures is quite high ranging from 20 to 40dB. Moreover, most of the band-pass $\Delta\Sigma$ ADCs are implemented with bulky on-chip inductors which makes it difficult to attain a wide tuning range.

The limitations mentioned above have so far prevented the practical implementation of complete RF-to-digital converters in the GHz range even though the SDRs in MHz range have been reported [57]. Rather, the SDR research has changed its direction towards the goal of trying to come up with solutions that serve the objective of reconfigurability, complete integration, and digital intensive receiver architectures. Towards this end, one promising digital-intensive architecture is the direct $\Delta\Sigma$ receiver DDSR [58–60]. Chapter 5 of this thesis will discuss the DDSR in little more detail.

To achieve the above mentioned goals, today's practical SDR implementations consist of an analog front-end between the antenna and the ADC [9, 10, 61]. The purpose is to relax the required specifications of ADC. This is done by front-end through amplification, downconversion and filtering. Amplification increase the signal and noise level at the input of the ADC so that it requires a lower number of bits; and downconversion brings the received signal to lower frequencies so that a lower sampling rate is required from the ADC. Finally, filtering of unwanted signals reduces the dynamic range requirements of the ADC. The reduction of ADC dyamic range requirements is visually presented in Fig. 2.5. Consequently, a typical RF front-end proceeding the ADC consists of a low-noise amplifier (LNA), downconversion mixer and baseband filtering stages. Further, it is intended that these analog front-end circuits are designed with as much digitally assisted reconfigurability as possible. This aims at the target of completely digital solutions, one step at a time, taking advantage of every new generation of digital friendly CMOS technology. At the same time, fully integrated solutions that focus on reducing the number of parallel receiver paths are desired [62–65].

Covering the details of all the research targets for RF-to-digital converters is quite broad in nature and is not within the scope of this thesis. Rather, a narrower research field is chosen, targeted towards completely integrated blocker-resilient receivers with the exception of one publication which focuses on sensitivity requirements in the mixer-first direct $\Delta\Sigma$ receivers. In following section an overview of current blocker-resilient receiver solutions will be presented. Again, this is not meant to be a comprehensive summary but rather serving to introduce the research field to the reader.

2.5 Blocker-tolerant receivers

Blocker-tolerance is needed in wireless receivers because high power blockers can cause input and output compression of active devices in the receive chain. Even if these blockers are weak, they can cause intermodulation products due to the non-linear transfer characteristics of active devices thus reducing the sensitivity of a receiver. To overcome this, receivers incorporate filtering which is mostly off-chip as it is difficult to create completely integrated high-quality bandpass filters. However, poor tunability of off-chip filters has led to the development of various on-chip filtering solutions.

One such widely studied on-chip filtering solution is N-path filtering [66,67]. The technique offers moderate quality factors with wide tunability as the center frequency of the filter can be altered by changing the LO frequency. Over the years, various N-path filtering architectures have been implemented in different configurations. For example, [59, 68–71] use N-path filtering at the output of the LNA, [72–75] implement N-path filtering in the feedback path and [76,77] show examples of N-path filtering in the feedforward path. These N-path implementations in general have certain limitations. First, the blocker filtering is limited by the mixer switch resistance which cannot be reduced indefinitely due to excessive LO power consumption. Second, N-path filtering downconverts signals present at the LO harmonics as well. To solve the second problem, various harmonic rejection N-path filtering techniques have been proposed [78–83]. However, these techniques implement harmonic rejection with a higher number of paths leading to increased area and LO power consumption. Moreover, harmonic rejection is usually implemented later in the receiver chain when gain has already been applied.

Another useful blocker-tolerant topology is a mixer-first architecture

[80, 84–87]. Mixer-first architecture achieves this resilience by completely eliminating active RF stages which are one of the main sources of receiver non-linearity. Some recent mixer-first implementations have demonstrated excellent linearity specs with an out of band (OB) IIP3 and BCP between 39-44dBm and 12-13dBm respectively [85, 88]. However, as always there are some limitations. Mixer-first receivers require the first baseband amplifier to be low-noise which leads to higher current consumption in the first baseband stage. Additionally, mixer-first receivers suffer from downconversion of the input signal around the LO harmonic and LO leakage at the RF nodes.

The LO leakage problem in a mixer-first receiver can be solved by implementing a low-noise low-noise transconductance amplifier (LNTA) [89–93]. The output of a LNTA is in the current domain thereby reducing the voltage swings at the output of an LNTA. This means that high power blockers will not be able to compress the LNTA output due to reduced voltage swings. The current signal produced by the LNTA is converted to voltage after downconversion where filtering is more easy to achieve. LNTA operation requires huge mixer switches to reduce voltage swings at the output of the LNTA. In addition, the lack of RF gain necessitates that the first baseband amplifier needs to be quite low noise. Both of these issues lead to increased power consumption in LNTA-based receivers. Table 2.1 presents performance comparison of some recent blocker tolerant wideband receivers.

For cases when the blocker frequency is known, some works have proposed an N-path notch filter response at the blocker frequencies [10, 94–96]. Other works [97–102] create a 180° version of the blocker signal and sum this with the received input for blocker cancellation. This kind of cancellation is generally implemented for transmitter signal leakage with a phase and frequency which are known a priori.

Table 2.1. Performance comparison of recent blocker-resilient receives.

Reference	Architecture	Frequency [GHz]	f_{BW} [MHz]	BCP [dBm]	BNF [dB]	OB IIP3 [dBm]	NF [dB]	Gain	Process
RFIC'17 [85]	Mixer first	0.2 to 8	20	12@4f_{BW}	4.7@0dBm	39@4f_{BW}	2.3 to 5.4	21	45nm SOI
ISSCC'17 [88]	Mixer first	0.1 to 2	13	13@6.15f_{BW}	6 to 8@0dBm	44@6.15f_{BW}	6.3	16	28nm
JSSC'12 [103]	Mixer first	0.08 to 2.7	4	-2@20f_{BW}	4.1@0dBm	13.5@20f_{BW}	1.9	72	40nm
ISSCC'15 [104]	Mixer first	0.1 to 1.5	2	-6@20f_{BW}	13.5@0dBm	13.5@20f_{BW}	1.5 to 2.9	37	65nm
JSSC'15 [105]	Mixer first	0.1 to 3.3	-	−6 to −2.5	5 to 13@0dBm	10 to 11.5	1.7 to 3	-	28nm
ESSCIRC'18 [83]	LNA first	0.7 to 1.4	10	−8.5 to 10.5 @10f_{BW}	5.8 to 8.1@-9dBm	1 to 20.5@10f_{BW}	1.5 to 15.5	20.8 to 36.8	65nm
JSSC'18 [96]	LNA first	0.7 to 1	-	9 to 12	9 to 12	26.7 to 35.1	8.7 to 11.7	1.1 to 5.5	65nm
JSSC'14 [106]	LNA first	0.4 to 6	0.5 to 50	−13 to −9	10 to 14@0dBm	3 to 8	1.8 to 3.1	58 to 70	28nm
JSSC'11 [107]	LNA first	0.4 to 0.9	-	>-8@20MHz	10 to 12@-4dBm	10@20MHz	3	70	40nm
JSSC'14 [108]	LNA first	0.05 to 2.5	0.35 to 20	-	5.1@0dBm	10	2.9	38	65nm
JSSC'18 [81]	LNA first	0.2 to 1	-	-2.4	-	9	5.4 to 6	36	65nm
ISSCC'15 [10]	LNTA first	0.5 to 3	0 to 100	-1	-	10	3.8 to 4.8	20 to 50	65nm LP
ISSCC'13 [90]	LNTA first	1.8 to 2.1	-	-1.5@20MHz offset	-	>16	1.9 to 2.7	44.5 to 45.5	40nm
ISSCC'14 [109]	LNTA first	0.3 to 1.7	2 to 76	>2 offset	-	12 to 33	4.2	19 to 34	65nm

All of the above-mentioned blocker-tolerant techniques have limitations, making no single technique a clear winner in terms of performance. The following chapters will cover some of the author's contributions in an attempt to solve the current limitations of the above blocker-tolerant techniques. Specifically, the discussion will be devoted to the following research targets: 1) To create higher-order on-chip N-path filtering for near-band blocker suppression; 2) To create simpler harmonic rejection N-path filtering which achieves harmonic rejection with a reduced number of paths and simple gain coefficients; 3) To attain blocker rejection as early as possible in the receiver chain as implementing blocker rejection later in the chain may already increase the non-linearity of the beginning stages of receiver, and; 4) To achieve transmitter leakage cancellation without adding any additional noisy circuitry at the receiver input. One exception to the above-mentioned targets of blocker resilience is the work in publication VI which addresses the sensitivity issues in the mixer-first direct $\Delta\Sigma$ receivers.

3. Blocker-tolerant RF front-ends

3.1 Overview

The widespread deployment of new communication standards and frequency bands in recent decades has resulted in the increased demand for blocker-resilient wireless receivers. This is because the communication receivers of today not only receive the desired signals but also the interfering high power blockers from nearby transmitters. One widely used technique to attenuate these high power blockers is to use pre-select bandpass filters which are implemented with either surface acoustic wave (SAW) or bulk acoustic wave (BAW) technologies [110, 111]. However, filters based on these technologies are difficult to implement on chip, and their lack of tunability has so far prevented completely integrated and tunable solutions. Rather what is done is to use multiple off-chip band-select filters to cover various communication standards/frequencies [49, 112, 113]. Obviously, this is not an efficient solution. Therefore, in order to eliminate or alleviate the performance requirements of these filters, on-chip filtering techniques need to be adopted. This chapter will focus on two on-chip blocker filtering techniques proposed by the author. The first one deals with implementing a 3rd-order tunable on-chip bandpass filter for near-band blocker suppression while the second one is related to provide blocker filtering at the LNA input interface. The presented research outcomes of these two techniques are based on publications IV, V, and VIII.

High power interfering blockers can also arise from a transmitter present on the same IC. This transmitter signal leaking to the receiver input is also known as self interference (SI). This chapter also covers a novel self-interference cancellation technique through buried-gate signaling in a fully-depleted silicon-on-insulator FDSOI process. The key measurement

results from publication III which validate the proposed approach are presented.

3.2 Third-order on-chip filtering

N-path filtering is one widely studied on-chip filtering techniques [66, 67, 73]. The technique offers widely tunable on-chip filtering with moderate quality factors. However, the majority of N-path implementations in today's receivers provide only a first-order filtering response at RF nodes [67,73,79–83,105,114]. This limits the amount of attenuation for near-band blockers. To increase the attenuation of near-band blockers, a 3rd-order baseband integrator is proposed here which acts in conjunction with N-path passive mixers. As a result, a 3rd-order filtering response is created at RF nodes which can be tuned to the desired frequency by changing mixer local-oscillator frequency.

The proposed 3rd-order N-path filtering was fabricated and measured in a 28nm FDSOI process as a part of a harmonic-rejection RF front-end. The output from the 3rd-order integrator was routed outside the IC where it was measured through an external opamp buffer. Figure 3.1 shows the implemented 3rd-order integrator with harmonic-rejection N-path filtering. The response is created by a 3rd-order impedance in the integrator feedback path that is comprised of capacitors C_{F}, R_{L}, gyrator transconductors, and C_{L}.

In order to calculate the desired values of the circuit parameters C_{F}, C_{L}, and R_{L}, a small-signal equivalent model can be used. Figure 3.2 shows the small-signal equivalent model of the proposed 3rd-order integrator together with the linear time invariant (LTI) passive mixer model [84]. The exact analysis of this small-signal model results in a complicated 3rd-order transfer function. Such a transfer function does not lead to any intuitive design guidelines. Therefore, an approximate approach, inferred from the pole-zero analysis of the exact transfer function in Matlab, was taken.

The pole-zero analysis of the 3rd-order exact transfer function reveals that the 3rd-order response is mainly due to one real and two complex poles. There is also an additional zero pair in the system whose proximity with complex poles affects the response as well. To attain the desired response, the poles should be selected at the required baseband bandwidth f_{BW}. By selecting a real pole at f_{BW}, the approximate value of C_{F} can be

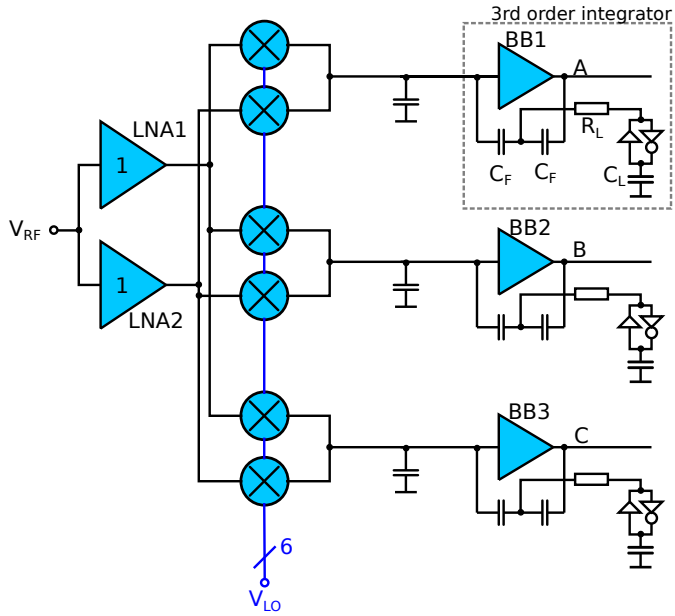

Figure 3.1. Implemented 3rd-order integrator with N-path filtering.

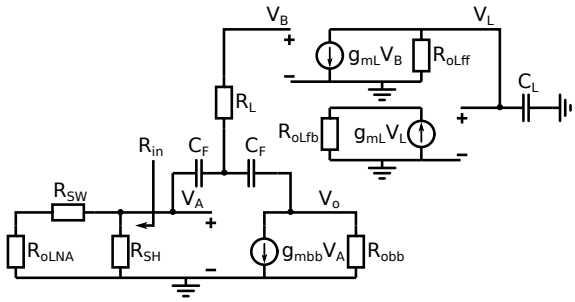

Figure 3.2. Small signal model of 3rd-order integrator and N-path filter.

calculated as:

$$C_F \approx \frac{1}{\pi f_{bw}(R_{obb} + R_{in})}, \tag{3.1}$$

where R_{obb} represents the baseband transconductor output resistance and R_{in} represents the equivalent output impedance of the mixer and LNA, as shown in Figure 3.2, given as:

$$R_{in} = \frac{R_{SH}(R_{oLNA} + R_{SW})}{R_{oLNA} + R_{SW} + R_{SH})}, \tag{3.2}$$

where R_{SH} represents the power lost due to upconversion by the harmonics of the LO. R_{SH} can be derived for our proposed 6-phase harmonic rejection

mixers as $R_{SH} = 2.65(R_{SW} + R_{LNA})$ [84].

Similarly, by selecting the complex pole pair at f_{BW}, the C_{L} value can be calculated. However, finding an exact equation for a complex pole pair is not straightforward. Therefore, we use an indirect method by tuning the complex pole-pair frequency to f_{BW} by controlling the integrator complex zero pair frequency. As these pole and zero pair frequencies lie in close proximity, changing one will also modify the other with reasonable accuracy. The complex zero pair frequency can be derived as:

$$f_z = \frac{1}{2\pi\sqrt{2C_F C_L / g_{mL}^2}}. \tag{3.3}$$

The integrator will only be able to maintain a 3rd-order slope in the frequency range located before its unity gain frequency. Therefore, if we place f_{z} around the integrator unity gain frequency then the position of the complex pole pair can be adjusted to the required f_{BW} by changing f_{z}. For such a case, the value of C_{L} can be approximated as:

$$C_L \approx \frac{g_{mL}^2}{8C_f(\pi f_{BW}(2AopendB/slopedB))^2}, \tag{3.4}$$

where g_{mL} represents the transconductance of gyrator transconductors, $AopendB$ represents the required voltage gain in dB from the integrator, and $slopedB$ is the desired 18dB/octave slope from 3rd-order integrator.

The calculated values of C_{F} and C_{L} will result in a transfer function with peaking. Therefore, a series resistor R_{L} is added with the gyrator to reduce the peaking in the transfer function. Its value can be approximated as:

$$R_L \approx 1/g_{mbb} + 1/(R_{oL} g_{mL}^2), \tag{3.5}$$

where R_{oL} = $\mathrm{R_{oLfb}}$ = $\mathrm{R_{oLff}}$ represents the gyrator transconductor output impedance.

To evaluate the above design equations, we design a 3rd-order integrator for a given f_{BW} = 10MHz. We use the extracted transconductances and output resistances of the proposed front-end as a starting point. R_{oLNA} = 500Ω, R_{SW} = 10Ω, $g_{\mathrm{m,BB}}$ = 24mS, R_{obb} = 2kΩ, g_{mL} = 2.6mS, R_{oL} = 100kΩ and $AopendB$=33dB. The baseband amplifier transconductance $g_{\mathrm{m,BB}}$ was chosen to be much higher than gyrator transconductance g_{mL} to reduce its noise contribution. On the other hand, small gyrator transconductance g_{mL} does not influence the overall input-referred noise of the integrator due to the filtering effect of C_{F} and can be chosen low for reduced power consumption. Once these transconductances have been selected, the output

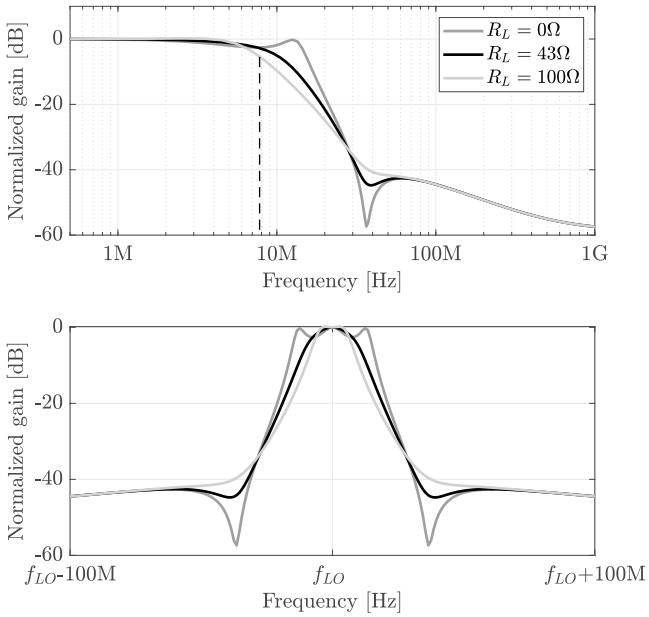

Figure 3.3. Simulated response of 3rd-order integrator for the calculated values of C_{F}, C_{L} and R_{L}. top) baseband response and bottom) upconverted RF response.

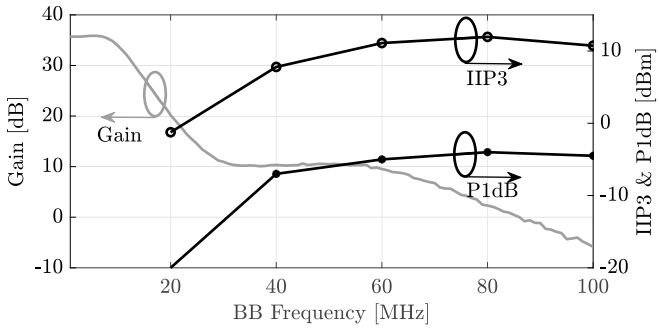

Figure 3.4. Measured baseband filtering response, IIP3 and P1dB of front-end at f_{LO} = 1.5GHz. 3rd-order baseband filtering response gets upconverted to LNA output nodes with N-path consequently helping to suppress near-band blockers.

resistance values of the transconductors are just a consequence of the amplifier structure and transistor aspect ratio in the given technology. For the remaining parameters, the value of R_{SW} should be chosen to be as small as possible for adequate blocker suppression at far-away offsets. However, a value that is too small will result in increased LO power consumption. Therefore, R_{SW} = 10Ω, is a compromise between blocker attenuation and LO power consumption.

With these chosen design variables, the values of C_{F}, C_{L} and R_{L} are

calculated to be 13.5pF, 4.75pF and 43Ω respectively. Figure 3.3 depicts the simulated 3rd order transfer function for the above calculated values. The simulated cut-off frequency of the 3rd order integrator is about 8MHz compared to our initial target of 10MHz. This much deviation is expected from the approximate design equations as they are an over-simplified form of the 3rd-order transfer function. Nevertheless, the design equations provide a simple design procedure for the 3rd order integrator and establish an initial estimate of the C_{F}, C_{L}, and R_{L} values. Once these initial values are known, the final transfer function can be tweaked in simulations to achieve the exact f_{BW}.

The proposed 3rd-order N-path filtering was fabricated and measured in an 28nm FDSOI process as a part of a harmonic-rejection RF front-end. In Figure 3.4, the measured 3rd-order baseband filtering response, IIP3 and blocker 1dB gain compression points (BCP) are plotted versus baseband frequency offset. Thanks to 3rd-order filtering, the BCP compression point for a near-band blocker located at a 40MHz offset from f_{LO} is -6.5dBm which is just 1.5dB less than the BCP measured at a 100MHz offset.

3.3 Selective input impedance for blocker rejection

As discussed earlier, N-path on-chip filtering has emerged as one of the most feasible alternatives for external off-chip filtering in recent years. However, N-path on-chip filtering is generally implemented at LNA output nodes, neglecting the filtering requirement at its input [10, 58, 59, 81, 107, 115]. Assuming that the blocker voltage gain is low at the LNA output due to filtering, the LNA input swing range limits can occur earlier than its output limits. Therefore, filtering should already start from LNA input nodes.

Some recent attempts to provide on-chip blocker attenuation at LNA input nodes are [108, 116, 117]. In [116], an active interferer reflecting feedback loop is employed while in [108, 117], miller-compensated bandpass filters, in dual-negative feedback configuration, are utilized to create blocker rejection at the LNA input. An active feedback technique has the disadvantage that the feedback path may saturate in the presence of a large blocker while the dual negative feedback together with miller-compensated bandpass filters in [108, 117] require complicated dual-feedback architecture for achieving the same goal.

3.3.1 Proposed capacitive feedback LNA

In the following section, a new feedback LNA is proposed which achieves blocker rejection both at its input and output nodes. The proposed dual attenuation is attained by designing a low intrinsic input impedance common gate (CG) common source (CS)) LNA with capacitive feedback, together with an N-path filtering load. The capacitive feedback across the LNA ensures that the selective N-path filtering profile at the LNA output is transferred to the LNA input nodes creating a selective input impedance. Consequently, the achieved front-end input impedance is low at blocker frequencies and matched to the source impedance at the desired frequencies, creating the desired voltage attenuation for blockers. This kind of capacitive feedback LNA was proposed in [118, 119] with a switchable LC load. In a wideband receiver scenario, switchable integrated LC loads consume a huge silicon area while providing only a limited frequency tunability and are therefore not a viable solution. The proposed solution instead implements this wideband tunability through the application of on-chip N-path filtering as an LNA load. The proposed solution offers the following key advantages over previously implemented approaches: First, the feedback path is entirely passive in nature, reducing chances for feedback path saturation in the presence of large blockers. Second, there are no mixers in the feedback path, reducing additional noise and local oscillator LO power consumption and simplifying the feedback design, and 3rd, the proposed design is frequency agnostic, meaning no prior information of blocker frequency is required for rejection. The proposed LNA is detailed in publication V. Below we highlight some of the main research outcomes from V.

Figure 3.5(a-c) presents the detailed diagram of the capacitive feedback CG-CS LNA, overall RF front-end, and N-path load. The LNA consists of push-pull CG and CS amplifiers where the capacitive feedback CG stage works in the same way as a typical capacitive feedback CG amplifier. A CS stage is added to increase the output impedance of the LNA as compared to resistive loads. A common-mode feedback loop is added to ensure the output common-mode voltage at OUTP/OUTN at half of the supply voltage, which creates an optimum output swing range. The LNA is loaded with quadrature passive mixers and baseband capacitive impedance. This together creates an N-path filtering response.

Complex feedback resistors R_c are added to compensate for the effect

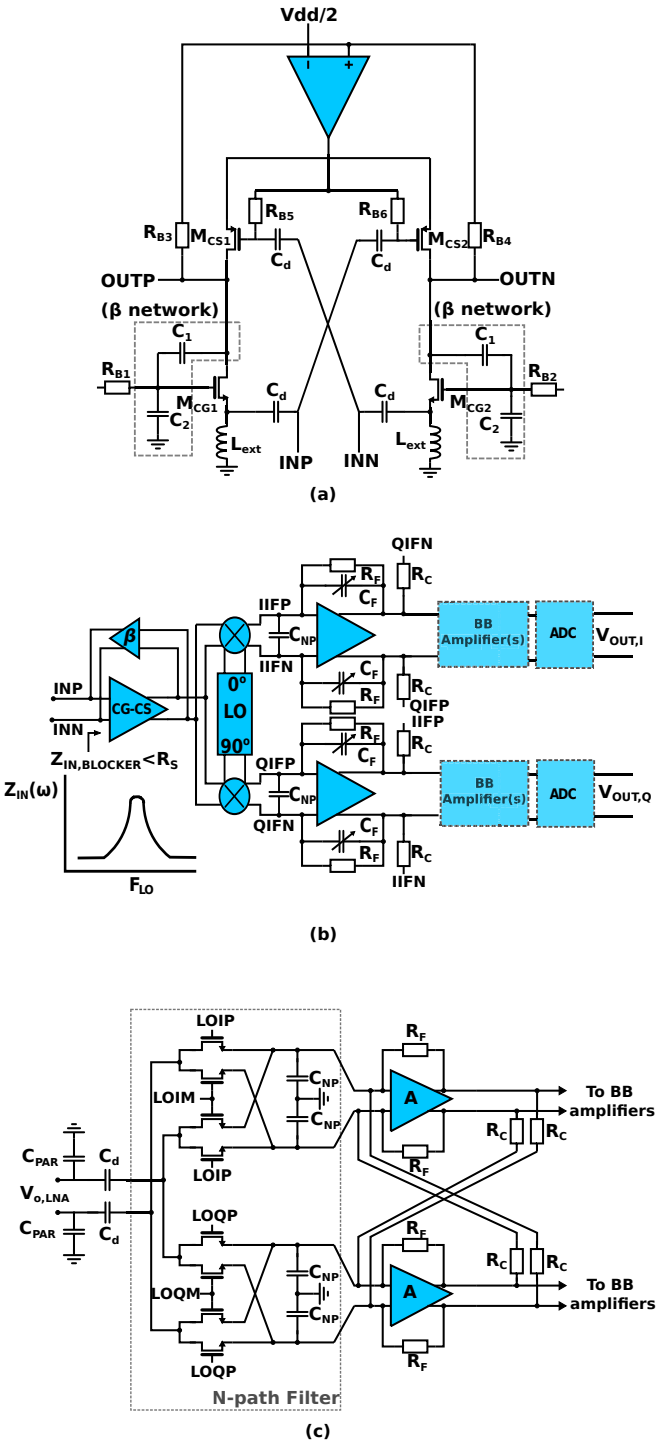

Figure 3.5. a) Proposed capacitive feedback CG-CS LNA b) Block diagram of the proposed RF front-end. c) Differential implementation of a quadrature N-path filter load with complex baseband feedback for frequency offset tuning.

of any parasitic capacitance at the LNA output. Any complex impedance present at the LNA output will manifest itself as a bandpass filter response offset from the LO. This shifts the maximum gain of the LNA away from the LO and results in non-optimal front-end performance [120]. The complex feedback resistors R_{c} overcome this problem [80, 84, 121].

3.3.2 Analysis, modeling and simulations

To gain a deeper understanding of the proposed front-end, a simplified small-signal model can be made as shown in Figure 3.6. In the model, R_{S} represents input source resistance, C_{in} is the parasitic capacitance at input nodes, gm_1 and ro_{CG} represent the CG amplifier transconductance and output resistance while gm_2 and ro_{CS} represent the CS amplifiers transconductance and output resistance. The capacitive feedback formed by capacitors C_1 and C_2 is represented through a feedback factor β. The LNA is loaded with an impedance Z_{L}, which can be represented as a parallel combination of the N-path filter input impedance $Z_{\mathrm{NP}}(\omega_{LO})$, C_{out} impedance (Z_{COUT}) and ro_{CS}.

In the N-path filter model, R_{SW} represents mixer switch resistance, $Z_{\mathrm{BB}}(\omega_{IF})$ is the baseband amplifier input impedance at the intermediate frequency IF, $Z_{\mathrm{CNP}}(\omega_{IF})$ is the impedance of the N-path capacitor at IF, and ζ represents the frequency scaling factor. For four-phase quadrature passive mixers with a 25% duty cycle, $\zeta = 2/\pi^2$. Further, $Z_{SH}(\omega_{LO})$ is virtual shunt impedance representing the power dissipation due to baseband signal upconversion. It can be expressed as [84]:

$$Z_{SH} = \Big(\sum_{n=3,7,11..}^{\infty} \frac{1}{n^2 Z^*_{OLNA}(nf_{LO})} + \sum_{n=5,9,13..}^{\infty} \frac{1}{n^2 Z_{OLNA}(nf_{LO})} \Big)^{-1}. \tag{3.6}$$

With the presented model, simplified voltage gain A_{vRF}, input impedance Z_{IN} and NF equations of the front-end can be derived as follows:

$$A_{vRF} \approx \frac{2(gm_1 + gm_2)Z_L(\omega)}{1 + gm_1[\beta Z_L(\omega) + R_S - gm_2 \beta R_S Z_L(\omega)]}, \tag{3.7}$$

$$Z_{IN} \approx \frac{1}{gm_1(1 - \beta gm_2 Z_L(\omega))} + \frac{\beta Z_L(\omega)}{1 - \beta gm_2 Z_L(\omega)}, \tag{3.8}$$

$$F \approx 1 + \Big(\frac{Z_L(\omega)^2 \gamma gm_1}{Av'^2 R_S}\Big)\Big(\frac{1 - gm_2 R_S}{\alpha}\Big)^2$$

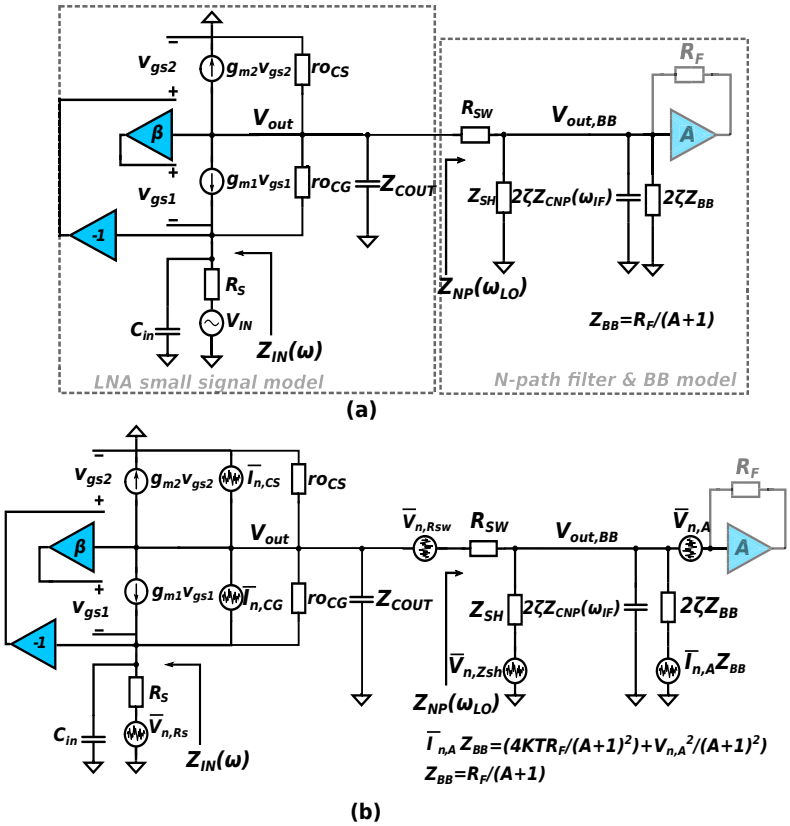

Figure 3.6. a) Small signal model of the proposed front-end with the N-path filter load. b) the noise model of the front-end.

+

$$(\frac{Z_L(\omega)^2\gamma gm_2}{Av'^2R_S})(\frac{1+gm_1R_S}{\alpha})^2+(\frac{\overline{V_{NP}^2}}{4KTR_SAv'^2})(\frac{1+gm_1R_S}{\alpha})^2, \tag{3.9}$$

$$\alpha = 1+gm_1(R_S+Z_L\beta-Z_L(\omega)R_S\beta gm_2), \tag{3.10}$$

$$\beta \approx \frac{C_1}{C_1+C_2}, \tag{3.11}$$

where factor γ accounts for a constant MOSFET noise parameter whose value is derived to be 2/3 for long channel devices. Recent submicron processes tend to exhibit values higher than 2/3. Av' and $\overline{V_{NP}^2}$ are respectively the loaded voltage gain, and the input referred noise of the N-path filter and baseband (BB) stages at ω_{IF}.

The above equations are derived by neglecting the parasitic capacitances and CG/CS amplifier output impedances. Nevertheless, they allow the designer to crudely establish circuit behavior in terms of the main design parameters. For example, Eq. 3.8 suggest that at blocker frequencies, the contribution of $Z_{\mathrm{L}}(\omega)$ to the input impedance Z_{IN} is minimal and Z_{IN} is roughly equal to $1/gm_1$. To create a selective input impedance profile, a high value of gm_1 is selected such that the input impedance at blocker frequencies is much lower than the source impedance R_{S}. On the other hand, at the desired frequency, higher $Z_{\mathrm{L}}(\omega)$ increases the Z_{IN} beyond $1/gm_1$ but can be tuned to a matched condition by proper selection of feedback factor β. For detailed equations with the parasitic effects, the reader may please refer to publication V.

Based on the analytical equations, design guidelines for the proposed LNA can be established. To arrive at these, first the NF is plotted using Equ. 3.9, at Z_{L} = 500Ω and for impedance-matched conditions. A constant Z_{L} is chosen to simplify the analysis by reducing additional variables. Later, the effect of Z_{L} on the overall front-end response will be analyzed. The result in Figure 3.7 demonstrates that a smaller value of gm_2 is desired for a reduced NF. We can achieve this smaller gm_2 value by having a smaller aspect-ratio for a CS device. However, an aspect-ration for CS device which is too small in comparison to the CG reduces the LNA linear output swing range and consequently lowers the large signal linearity. This is depicted in Figure 3.8, where the transistor-level simulation results for the NF and maximum peak output voltage swing range are plotted against CS transconductance gm_2. As expected, a smaller gm_2 leads to a reduced NF and output peak voltage swing range. The decrease in output swing range can be attributed to a higher saturation voltage V_{DSAT} of the CS devices. Consequently, gm_2 cannot be reduced significantly in comparison to gm_1, without significantly affecting the larger signal linearity of the LNA. The choice of gm_2 is thus a trade-off between NF and large signal linearity.

In the next step, the effect of $Z_{\mathrm{L}}(\omega)$ on the front-end performance is analyzed. In Figure 3.9, the required value of β for input matching at two different values of $Z_{\mathrm{L}}(\omega)$ is plotted. It can be observed that for higher values of $Z_{\mathrm{L}}(\omega)$, one needs a lower β to achieve input matching. After a certain limit, designing the LNA for lower values of β becomes impractical due to very small values of C_1. Once C_1 gets closer to the CG gate-to-drain parasitic capacitance C_{GD}, the effect of C_{GD} is significant and therefore needs

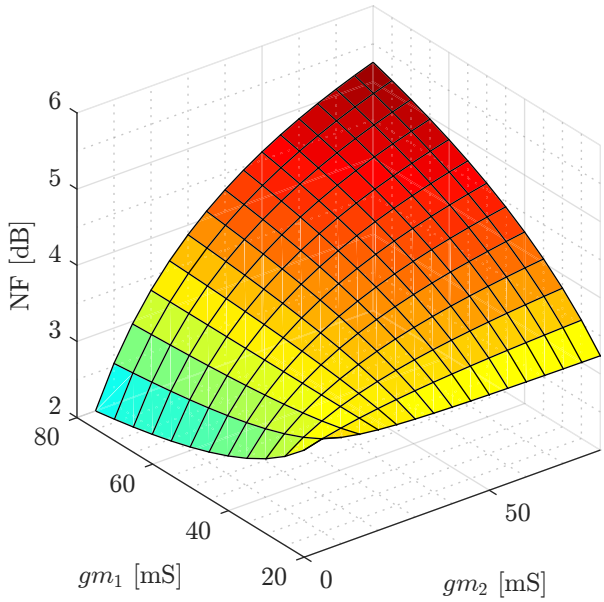

Figure 3.7. Theoretical NF, for Z_{IN} = 50Ω, for different values of gm_1 and gm_2.

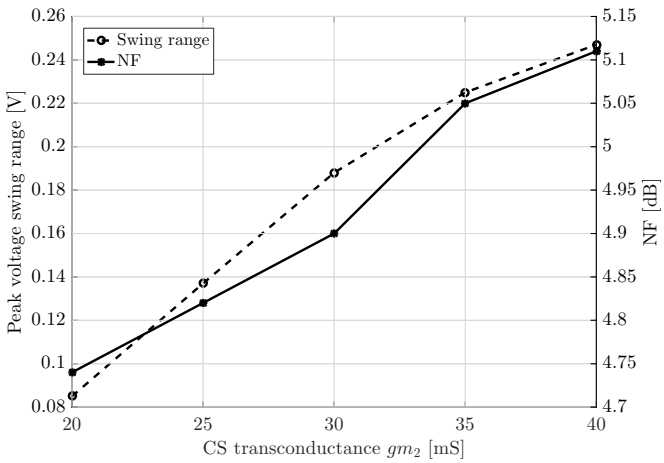

Figure 3.8. Transistor level simulations for output voltage swing range and NF, versus CS transconductance gm_2.

to be considered in the effective feedback factor β. Therefore, designing the CG-CS LNA for moderately lower values of $Z_{\mathrm{L}}(\omega_0)$ is proposed.

In conclusion, based on the above reasoning, a capacitive feedback CG-CS amplifier should be designed with $gm_2 < gm_1$ and a moderately low value of $Z_{\mathrm{L}}(\omega)$ to ensure practical values for C_1. Based on these guidelines a capacitive feedback LNA was designed with gm_1 = 80 mS and a lower gm_2

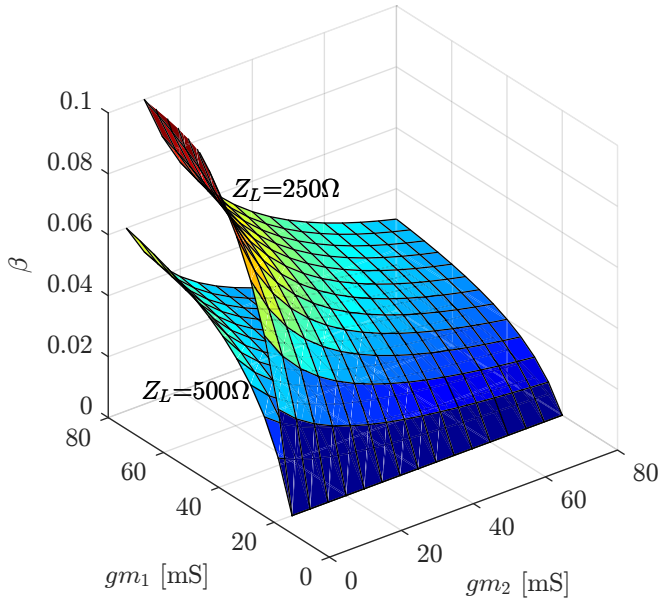

Figure 3.9. Feedback factor β, at Zin = 50Ω, for different values of gm_1 and gm_2. For higher Z_L, a lower value of β is required for input matching.

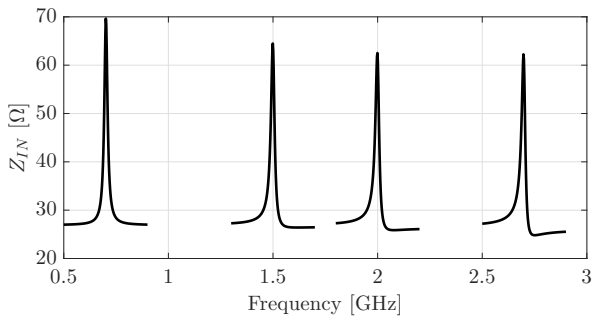

Figure 3.10. Simulated real part of the low-noise amplifier input impedance Z_{IN} around f_{LO} = 0.7,1.5,2, and 2.7 GHz.

= 30 mS. The parasitic capacitance associated with the LNA output node can shift the LNA center frequency away from the LO frequency. This was corrected by implementing a resistive complex negative feedback from the output node of the baseband differential amplifier, as depicted in Figure 3.5(c). The front-end was evaluated in a 28-nm FDSOI CMOS process with 1-V supply voltage and is configurable from 0.7 to 2.7 GHz with a baseband bandwidth of 10 MHz.

Figure 3.10 demonstrates the simulated differential Z_{IN}. As can be seen, $Z_{IN} \approx 25\Omega$ at the blocker frequencies. Assuming an antenna impedance of

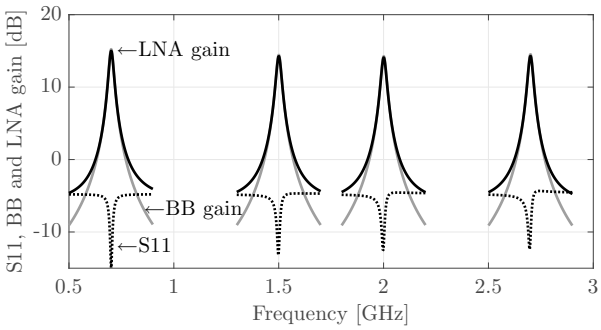

Figure 3.11. Simulated S_{11}, low-noise amplifier (LNA), and front-end downconversion gain around f_{LO} = 0.7, 1.5, 2, and 2.7 GHz.

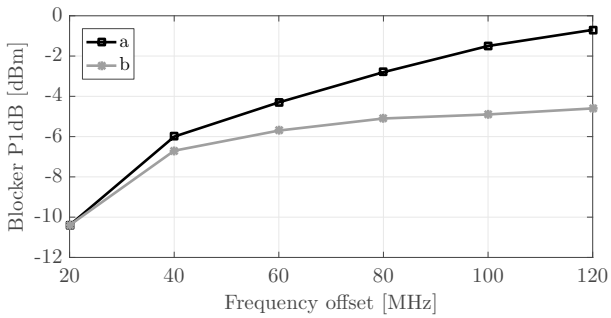

Figure 3.12. a) Simulated out-of-band blocker compression point (BCP) of the proposed radio frequency (RF) front-end and (b) BCP for CG-CS LNA-based RF front-end with wideband input matching.

100Ω (differential), this creates the required blocker voltage attenuation. Additionally, we observe a lower Z_{IN} for the upper end of the 0.7-2.7GHz band. At higher frequencies, the effect of parasitics changes the effective feedback factor β and causes a change in Z_{IN}. Figure 3.11 shows the simulated gain and S_{11} for the proposed front-end. The gain and S_{11} have been plotted at four operating frequencies in the 0.7-2.7GHz band, demonstrating the desired reconfigurability. Figure 3.12 presents the front-end blocker 1dB compression point BCP when loaded with a first order N-path response. The simulated results demonstrate the blocker tolerance of -1.5dBm at a 100MHz offset from the LO frequency.

In order to quantitatively observe the improvement of BCP due to the selective input impedance profile, a CG-CS LNA based RF front-end with flat wideband input matching was designed and simulated for the same voltage gain and baseband bandwidth. Its simulated BCP results are also plotted in the Figure 3.12. The proposed front-end demonstrates 3.5dB improvement in the BCP at a 100MHz offset from the LO frequency, thanks

to selective input impedance matching.

3.4 Self-interference cancellation in full-duplex transmission

In some receiver scenarios where the sources of blockers are present in close proximity to the receiver, achieving blocker-resilience becomes even more demanding. One such case is the full-duplex (FD) transmission when the transmission and reception are carried out simultaneously thereby potentially doubling the spectral efficiency [97, 122, 123]. One of the major issues in an FD radio is the local transmitter signal leakage to the receiver present on the same chip. This leakage is also known as SI.

In the following section, a novel approach to solve the problem of SI using buried-gate signaling in fully-depleted silicon-on-insulator (FDSOI) technology is presented. To validate the new technique, an RF front-end was fabricated and measured. Here, a summary of the proposed approach and key results are presented while for the detailed discussion, the reader may please refer to publication III

Figure 3.13 shows the simplified block diagram of the full-duplex transceiver. The transmitter and receiver operate simultaneously on frequencies separated by duplex-distance. In such a system, transmitter signal leakage will appear at the receiver input which is generally suppressed through duplexer filters or circulators [124–126]. Both of these possess limited attenuation ranging from 15-20dB for circulators and around 50dB for duplexers [127]. This level of attenuation seems to be insufficient for high transmitter leakage powers. An example can be given for long-term evolution advanced (LTE-A) band-1 with 10MHz bandwidth. The standard specifies a maximum transmitter power of 23dBm with the required sensitivity level of -97dBm [37]. Assuming 20dB attenuation from the implemented circulator, this leads to the receiver dynamic range requirement of 100dB creating an unnecessarily high burden on receiver linearity. Consequently, additional SI cancellation is required.

Over the years, various SI cancellation techniques have emerged in literature [97–102, 127]. They can be broadly categorized into digital and analog cancellation techniques. While the digital techniques offer the advantage of SI cancellation from multipath effects through complex algorithm implementation, they require huge dynamic range requirements of the receiver front-end. This is because digital SI cancellation is implemented later in the receiver chain. To overcome this problem, SI cancellation should be

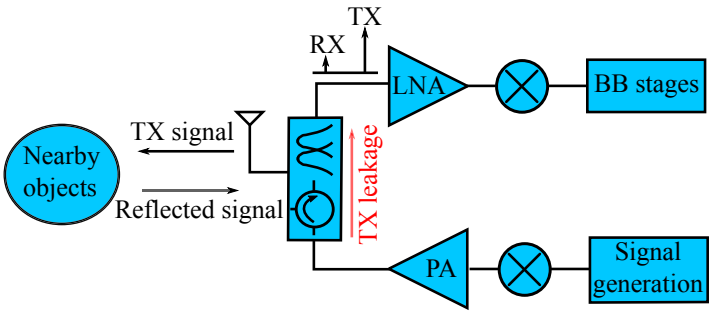

Figure 3.13. Simplified block diagram of full-duplex (FD) transceiver.

made as early as possible in the receiver chain. Various analog SI cancellation techniques serve this purpose but at the expense of an increased receiver noise figure due to added circuitry [98, 100, 101].

The proposed analog SI cancellation technique attenuates the transmitter leakage with no effect on the front-end noise figure. This is done by utilizing the buried-gate of the FDSOI transistor in a novel way. Buried-gate is an additional terminal in FDSOI which is generally used to control transistor characteristics such as threshold voltage through dc-biasing [128–132]. In contrast to the typical utilization of dc-biasing, the proposed approach uses an additional weighted and 180° phase-shifted transmitter signal fed to the buried-gate of the transistors in the low-noise amplifier of the designed front-end. Figure 3.14 shows the simulated gain and phase response of a single transistor when the signal is applied to the gate and buried-gate. There is a clear signal attenuation for a signal applied to a buried-gate preventing the use of a buried-gate terminal as an amplifier input. Nevertheless, it can be inferred that if the buried-gate signal is sufficiently higher than the signal at the transistor gate, then it can be utilized to cancel the transmitter self-interference. In transceivers, this high power signal is easily available from the TX output.

To validate the proposed technique, an RF front-end was fabricated on 28nm FDSOI technology, consisting of an LNA, downconverting passive mixers and baseband amplifier. The baseband signal was then routed outside the IC where and an external opamp based buffer was used to avoid loading from the spectrum analyzer. Figure 3.15 shows the implemented LNA with buried-gate signaling while the key measurement results from the fabricated prototype are presented in Figures 3.16-3.19.

In Figure 3.16 a test continuous wave (CW) TX leakage signal is given

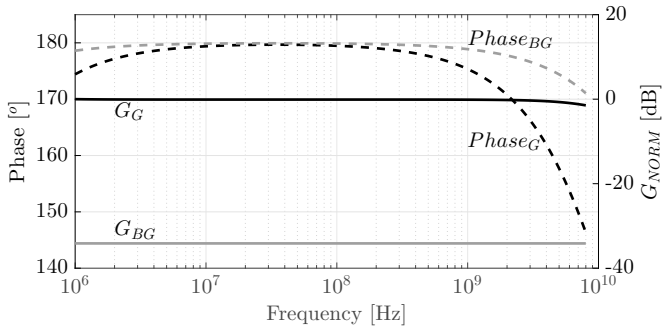

Figure 3.14. Comparison of normalized gain and phase when the signal is applied on transistor gate and buried-gate.

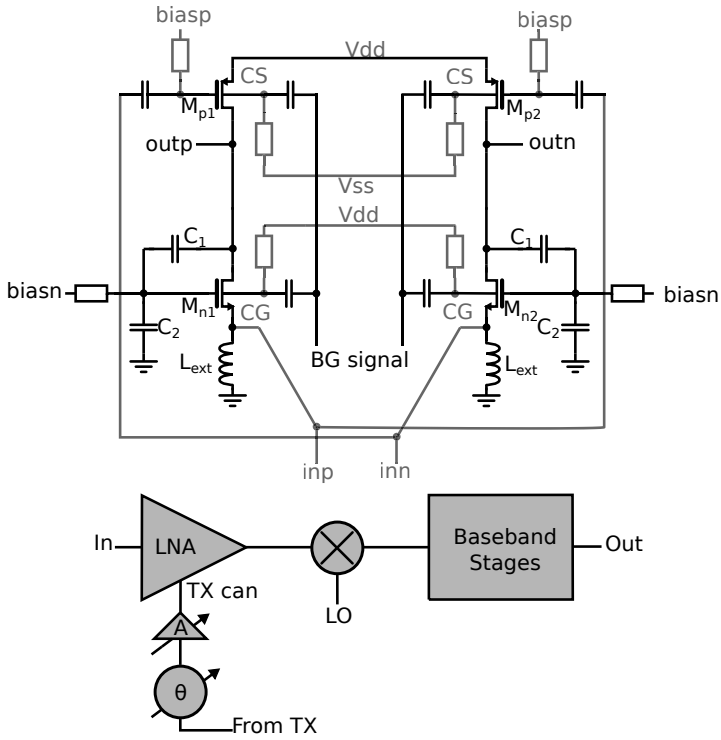

Figure 3.15. Designed LNA with buried-gate signaling.

at a duplex distance of 30MHz. A desired in-band CW signal of -65dBm is provided at a 1MHz offset from the LO and a TX signal of -40dBm is provided at a 30MHz offset from the LO. The following key points can be observed: First, the TX signal is attenuated by 40dB when TX cancellation is on. Second the desired in-band signal gain remains the same, and third, no increase in the in-band noise floor is observed.

In Figures 3.17 and 3.18, the measured normalized front-end gain is plotted for different phase and G_{rel} settings. Here, G_{rel} is defined as the

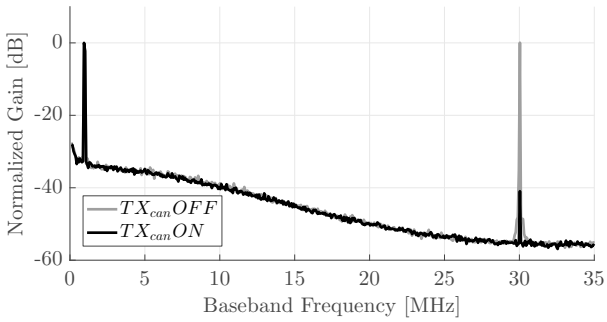

Figure 3.16. Comparison between measured BB spectrum when SI cancellation is turned on and turned off. The BB bandwidth is set to 10MHz for an LTE-A use case, with TX leakage at the shortest duplex distance of 30MHz. Around 40dB SI cancellation is observed.

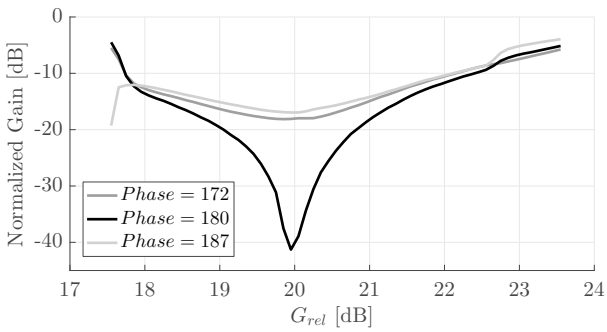

Figure 3.17. Measured normalized gain vs relative gain between gate and buried-gate signals.

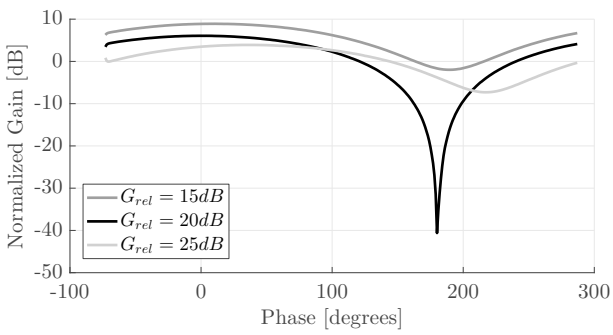

Figure 3.18. Measured normalized gain vs phase between gate and buried-gate signals.

ratio between the buried-gate and gate input powers: G_{rel} = $P_{\text{buriedgate}}$-P_{gate}. The results suggest a need for an accurate phase and amplitude tuning requirement for SI cancellation.

In Figure 3.19, normalized RX gain is plotted for an LTE-A 10MHz modulated signal. The signal is provided at the LTE-A minimum duplex distance of 30 MHz. Around 20dB of SI attenuation is achieved for the

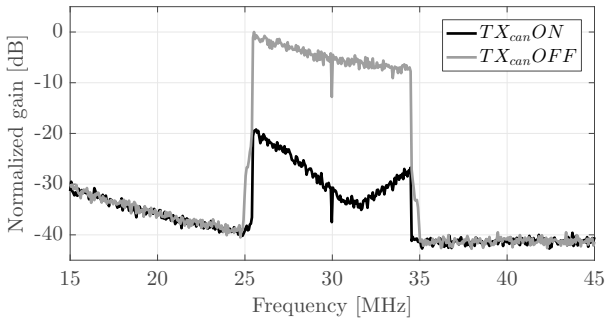

Figure 3.19. Measured normalized gain for 10MHz LTE modulated signal. Around 20dB SI cancellation is achieved when the buried-gate signaling is on and when it is off.

modulated signal. Due to the inability of the available signal generator to generate phase coherent LTE modulated signals, the above measurement was performed using off-the-shelf coarsely tuned phase-shifters and attenuators. We estimate more than 20dB of SI cancellation for more fine phase and gain tuning.

In summary, the proposed buried-gate signaling proves quite an attractive analog signal cancellation technique with no penalty on the front-end noise figure. Even though the technique was implemented on the LNA as a proof of concept, yet nothing prevents the implementation of the same technique in baseband stages as well. This will improve the SI cancellation even further. Moreover, the proposed technique can be used in conjunction with digital SI cancellation to suppress the transmitter leakage further. The only issue which needs to be addressed is the sensitivity to the phase and relative gain of a buried-gate signal. Nevertheless, measurements have demonstrated that even in the presence of a 10° mismatch, SI cancellation of above 10dB is achievable. To achieve such phase and gain tuning, algorithms can be implemented in the digital domain which measures the TX leakage at the LNA output and adjust the gain and phase of the buried-gate cancellation path for maximum attenuation. Implementation examples presented in [98–100] demonstrate how to generate the required phase and amplitude tuning.

In summary, this chapter detailed two on-chip blocker filtering techniques. One through a 3rd-order N-path filter design and the other though a capacitive feedback LNA which achieves blocker attenuation both at its input and output nodes. Circuit evaluations through measurements and simulation results demonstrate improved blocker resilience. In addition,

the chapter also presents a novel technique to attenuate transmitter signal leakage. The technique achieves this cancellation through buried-gate signaling in an FDSOI process with no penalty on the front-end noise figure.

4. Harmonic-Rejection RF front-ends

4.1 Overview

In this chapter, the research outcome of the proposed two-stage harmonic-rejection receiver will be presented. The need for a harmonic-rejection receiver arises when N-path filtering is used as an on-chip alternative for external high-quality pre-select filters [66, 67, 73, 114]. One of the major problems of N-path filtering, specifically when its number of phases is small, is its inability to sufficiently suppress blockers present at the harmonics of the LO frequency.

Various works have tried to solve the problem of N-path limited attenuation at LO harmonics. Figure 4.1 shows a conceptual diagram of a widely implemented 8-phase N-path filtering [78–81]. In this configuration, the weighting of ± 1 and $\pm\sqrt{2}$ multiplication factors ensures that the sum output signal resembles more like a sine-wave (also known as a pseudo-sine LO) [133]. Therefore, the effective waveform lacks most of the undesired harmonics. The 8-phase harmonic-rejection architecture has various limitations such as an increased number of paths leading to increased area and LO power consumption. In addition to that, harmonic-rejection is usually implemented later in the receiver chain when gain has already been applied [78–80]. This means that any blocker present at the harmonics of LO frequency may saturate the first stages of the receiver before the harmonic-rejection is even applied.

Some recent works propose a solution to the above problems. For instance, a 6-phase architecture was proposed in [82] which simplifies the LO generation as only six LO phases are required for harmonic-rejection. Another work [83] simplifies the LO generation by proposing overlapping clocks with a 25% duty-cycle which are easier to generate at high frequencies

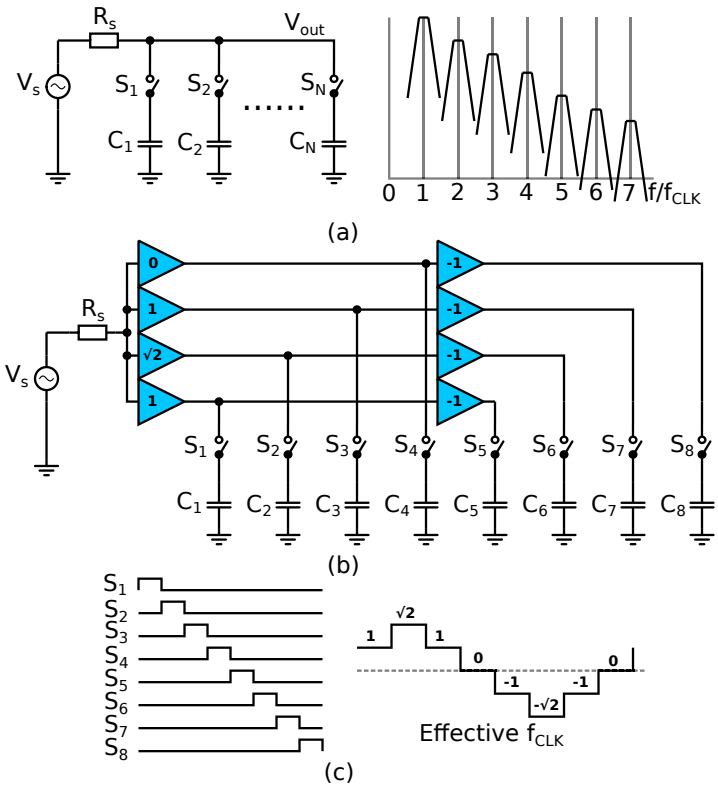

Figure 4.1. a) Basic N-path filtering technique with its frequency response. b-c) Conceptual representation of 8-phase harmonic-rejection N-path filtering. Weighted charging of N-path capacitors results in effective clock frequency with reduced harmonic content.

then a 12.5% duty-cycle in 8-phase harmonic-rejection architecture. Although, [82, 83] address the problem of LO generation complexity; they do not address the secondary problem of blockers at LO harmonics saturating the first stages of the receiver.

To address the secondary problem, [81, 105] have proposed harmonic-rejection at the output of the first gain stage to improve receiver linearity for blockers at LO harmonics. The benefit of these techniques is that they achieve promising linearity improvements for blockers at LO harmonics. However, they still implement a higher number of N-paths with the requirement of gain coefficients that are difficult to implement.

In an attempt to solve the above issues, a new two-stage harmonic-rejection receiver is proposed in this chapter. One of the key highlights of the proposed design is that the first harmonic-rejection already occurs at the output of the first gain stage. This helps to improve receiver linearity for blockers at LO harmonics. The proposed architecture is simple utilizing

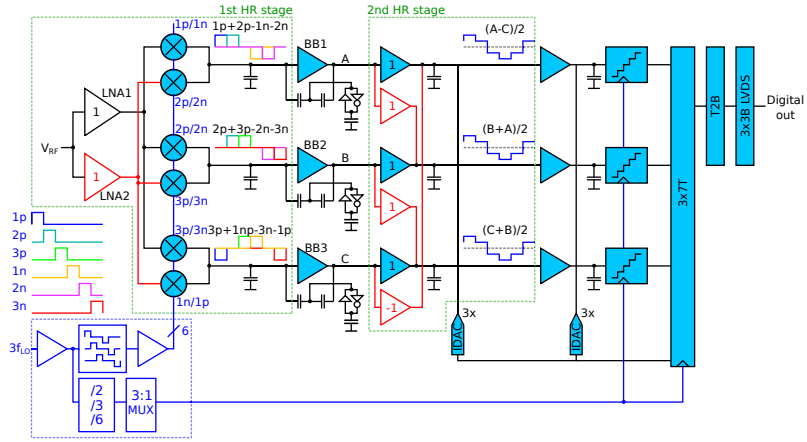

Figure 4.2. Simplified block diagram of proposed harmonic-rejection receiver.

only six clock phases, compared with other implemented works that use eight phases or more [81, 105]. In addition, the proposed architecture only requires simpler (± 1) gain coefficients while, at the same time, implementing harmonic-rejection in two stages compensates for the mismatch effects of each stage. The receiver was fabricated in the 28nm FDSOI process. In the following section, a summary of the proposed architecture together with the key measurement results from the fabricated prototype will be presented. For additional details, the reader may please refer to publications IV and VIII.

4.2 Proposed harmonic-rejection receiver

4.2.1 Architecture

Figure 4.2 presents the simplified block diagram of the proposed receiver. The required harmonic-rejection is achieved in two stages where the first implementation of harmonic-rejection already occurs at the output of the first gain stage. The architecture is simple as it only requires three baseband chain compared to an 8-phase N-path architecture. The three baseband chain outputs will have a 60° phase-shift from each other. From these three signals, conventional in-phase and quadrature signals can easily be extracted in the digital domain.

The first harmonic-rejection stage consists of two low-noise amplifiers, each connected a different baseband path at the same time through the passive mixer. The functionality of the first harmonic-rejection stage can

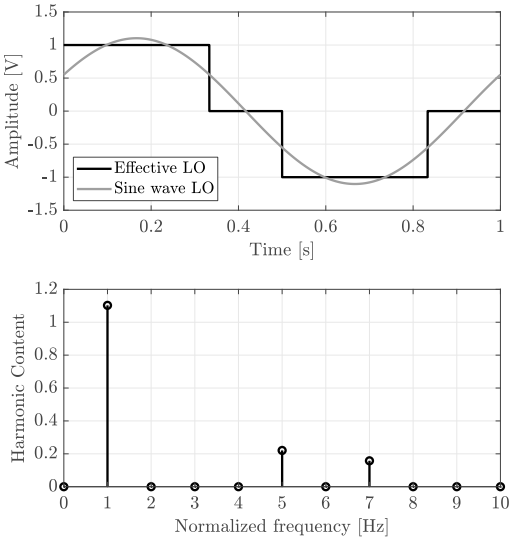

Figure 4.3. Effective LO waveform at the first stage of harmonic-rejection and gain of its frequency contents from Fourier analysis.

be explained as follows: During LO phases 1p and 2p, LNA1 and LNA2 get connected to BB1 alternatively while in phase 3p and 3n neither LNA1 nor LNA2 are connected to BB1. Finally, in phases, 1n and 2n, LNA1 and LNA2 get connected to BB1 with opposite polarity. This kind of switching results in an effective LO waveform at the input of BB1 as shown in Figure 4.3. Ideally, this waveform does not possess a third harmonic. However, device mismatches and LO non-idealities in practical implementation result in much lower harmonic-rejection from the first stage. Consequently, to compensate for the mismatch effects, an additional harmonic-rejection stage is added.

The second stage achieves harmonic-rejection by arithmetically manipulating the three generated effective waveforms (A, B and C) from the first stage. The generated signals (A-C)/2, (B+A)/2 and (C+B)/2 closely resemble a sine wave with reduced harmonic contents as shown in Figure 4.4.

4.2.2 Implementation and measurements

The proposed receiver was fabricated in 28nm CMOS technology. The detailed circuit diagram of the proposed receiver is presented in Figure 4.5 with the chip photograph of fabricated prototype in Figure 4.6. The layout was designed while keeping in mind the general layout design principles such as symmetrical layout design and maximum separation between

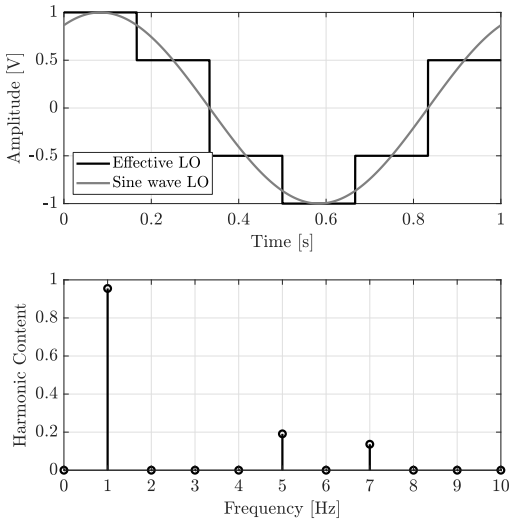

Figure 4.4. Effective LO waveform at the second stage of harmonic-rejection and the gain of its frequency contents from Fourier analysis.

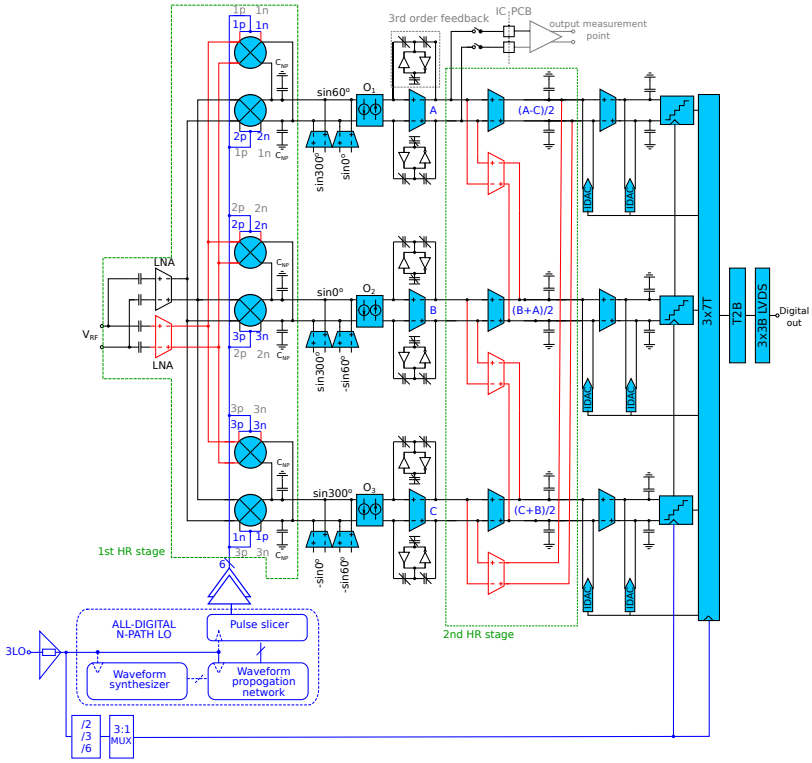

Figure 4.5. Detailed block diagram of implemented harmonic-rejection receiver.

analog/RF and digital circuits. To reduce the interference coupling through the substrate, digital, analog and RF section were made in a separate deep

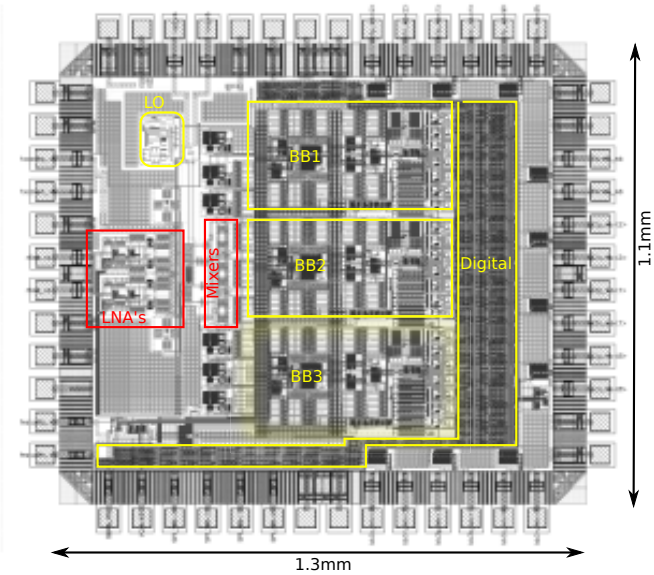

Figure 4.6. Fabricated active area of the proposed architecture highlighting different receiver secctions.

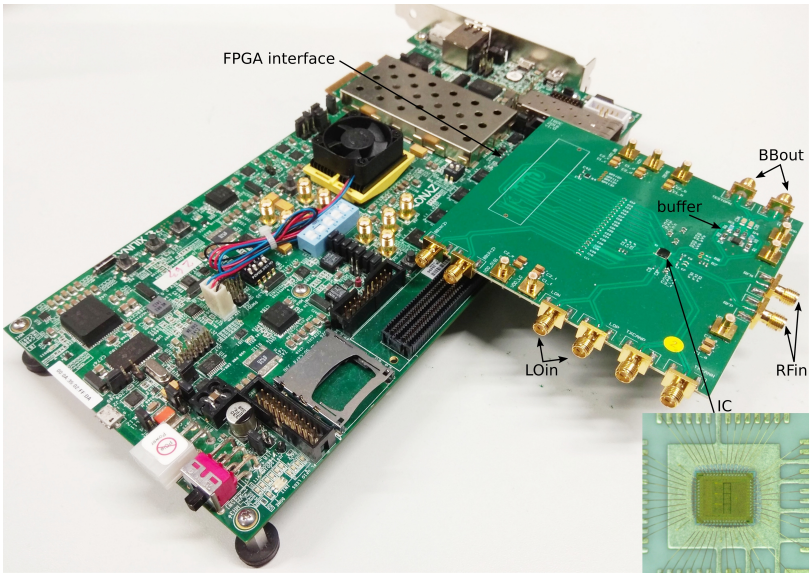

Figure 4.7. Measurement setup for the proposed receiver.

N-well. Further reduction of the interference coupling between different layout sections was done by separating the analog, RF and digital power supply pads. Separate power supply pads also helped to observe receiver behavior in different measurement conditions by enabling/disabling the

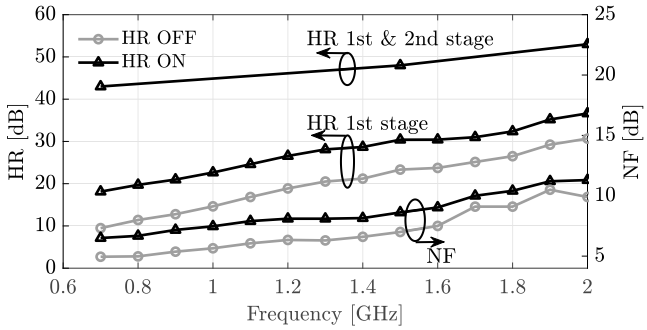

Figure 4.8. NF and the harmonic-rejection from the first and second stage of the proposed receiver, for harmonic-rejection LO clocking (black) and conventional LO clocking (grey).

power supplies of certain blocks. Finally, the empty area of the chip was filled with bypass capacitors from power supply pads to ground to suppress the supply noise.

Figure 4.7 shows the measurement setup of the proposed receiver. The first harmonic-rejection stage was measured by routing the output of the first baseband amplifier outside the IC through an external baseband buffer. An external buffer was need to allow loading the output signal with 50Ω spectrum analyzer. On the other hand, the second harmonic-rejection stage was followed by a 2nd-order $\Delta\Sigma$ quantizer. The output of the quantizer was seven-bit thermal which was then converted to binary and routed outside the IC through low-voltage differential signaling (LVDS). the fast data-rate of the quantizer output demanded a high-speed digital interface. This was implemented through an external FPGA which captured the bitstream from the IC and saved it for further processing. Matlab was then used to extract the output spectrum from the received bitstream and extract required performance parameters.

Some additional circuitry was implemented in the proposed architecture to cancel the dc-offset in the receiver chain together with the transconductance based feed-forward path. This feed-forward path was required to re-adjust the phase/frequency shift of N-path filter center frequency due to parasitics present at the LNA output [120, 134].

Figure 4.8 shows the measured noise figure and harmonic-rejection from the outputs of first stage and second harmonic-rejection stages. Without any calibration, harmonic-rejection in the range of 18 to 37 dB is observed from the first harmonic-rejection stage, while combined harmonic-rejection from both first and second stages is in the range of 46-53dB as measured

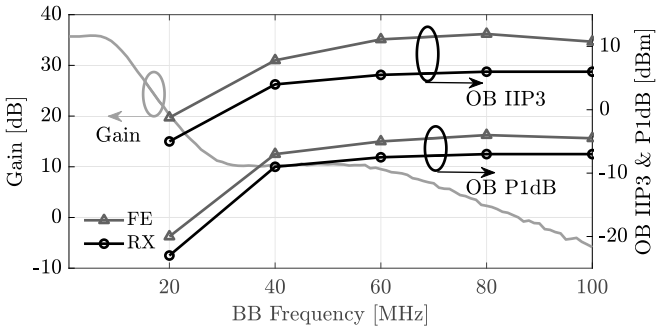

Figure 4.9. Baseband filtering response, OB IIP3 and P1dB compression point of front-end (FE) and receiver (RX) for an f_{LO} = 1.5GHz.

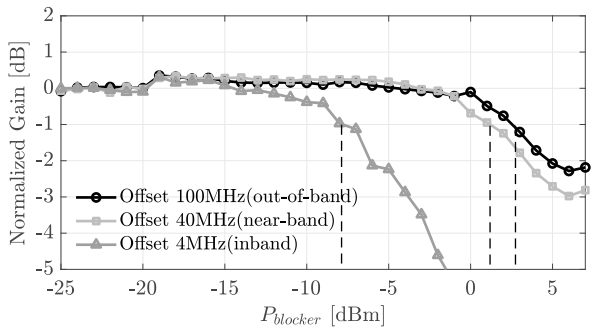

Figure 4.10. Measured signal gain under the presence of strong blocker at $3f_{LO}$. For a blocker at $3f_{LO}$+100MHz, BCP of 2.5dBm is observed.

Table 4.1. Performance summary and comparison

	This work	[81]	[105]	[83]	[63]
Frequency (GHz)	0.7-2	0.2-1	0.1-2.4	0.7-1.4	0.5-3
1st-stage HR (dB)	18-37	20	NA	NA	NA
Overall HR (dB)	46-53	51-52	52-54	40-67	35
N-path phases	6-phase	8-phase	8-phase	8-phase	8-phase
f_{BW} (MHz)	10	2	0.2-3	10	10
BCP (dBm)	-1 to -5@10f_{BW}	-2.4@10f_{BW}	-6 to 2.5@27f_{BW}	-8.5 to 10@10f_{BW}	-
BCP@3f_{LO} (dBm)	2.5@10f_{BW}	-2.8	-8	NR	NR
Near-band BCP (dBm)	-6.5@4f_{BW}	NR	NR	NR	-22 to -4@4$f_{(LO}$
NF (dB)	5-11	5.4-6	1.7	1.5-8	3.8-4.7
OB IIP3 (dBm)	8-11@10f_{BW}	9@10f_{BW}	10	1-20.5@10f_{BW}	-20 to -4.8@4f_{BW}
Process	28nm FDSOI	65nm	28nm	65nm	65nm

NR: not reported, NA: not applicable.1) signal path.

from the ADC output. The measured noise performance is increased in the high-end of the frequency range by non-optimal overlapping of the LO

waveforms in the measured prototype.

A conventional LO clocking was also implemented in the proposed design where each baseband branch is only connected to one LNA at a time (gray clocking arrangement in Figure 4.5), thus increasing LNA equivalent transconductance and reducing the time when overlapping can occur. With this arrangement, an improvement of approximately 3dB is observed in measurements. Such a LO clocking can be used in the absence of 3rd harmonic blockers.

In Figure 4.9, the third order baseband filtering response, out-of-band (OB) IIP3 and blocker 1dB gain compression points (OB P1dB) are plotted versus baseband frequency offset where out-of-band IIP3 and P1dB are measured for both the front-end and complete receiver.

For observing linearity in the presence of blockers at $3f_{LO}$, the compression point was measured with three offset frequencies, 100MHz, 40MHz, and 4MHz. These three offsets represent downconversion of the blocker to out-of-band, near-band, and in-band reception frequencies. The measurement was performed by sweeping the blocker power and determining the P1dB point of the receiver. We observe P1dB points of -7, 1 and 2.5 respectively as shown in Figure 4.10 achieving state-of-the-art results [81, 105]. Table 4.1. presents the performance summary and comparison of the proposed receiver.

In summary, the proposed architecture demonstrates an impressive blocker rejection for blockers present at the third harmonic. The architecture achieves this with simpler 6-phase LO clocking and three baseband paths compared to 8-phase architectures. In addition, two-stage implementation of harmonic-rejections helps to boost the overall harmonic-rejection even under the presence of mismatches of each stage while the chosen weighting coefficients of ± 1 offer ease of implementation.

5. Direct delta-sigma receivers

5.1 Overview

By definition, a direct delta-sigma receiver (DDSR) is defined as a $\Delta\Sigma$ ADC which contains one or more frequency translations inside the loop filter [47]. As such DDSR can be viewed as an evolution of direct-down conversion receivers towards the goal of a complete digital solution where DDSR emerges as a merger of a typical direct-conversion receiver and a $\Delta\Sigma$ based ADC. As can be seen in Figure 5.1, this merger results in signal discretization already beginning at RF nodes while each stage now participates in amplification, filtering, and noise-shaping. In this way, analog stages are maximally in use, thereby minimizing the total number of stages.

This chapter focuses on continuous-time direct delta-sigma receivers. The discussion begins with an overview of continuous-time DDSRs by highlighting some of their main benefits. This is followed by a summary of research outcomes from the author's attempt to solve a few key design challenges related to DDSRs. The results of these investigations are detailed in publications II, VII, VI, and IX.

5.2 Direct delta-sigma receivers: Benefits and challenges

A direct delta-sigma receiver is a hybrid of a direct-downconversion receiver and a $\Delta\Sigma$ ADC. The designer needs to consider the system from both receiver and ADC perspectives to ensure a successful implementation. Therefore, since the introduction of DDSR in 2010 by [58], the architecture has received increased research interest towards achieving an optimum design strategy by accurate modeling of the frequency translational loop

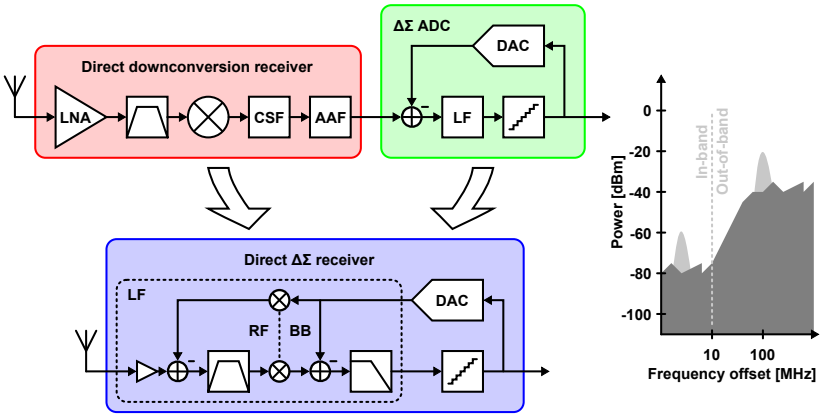

Figure 5.1. From direct-conversion receiver to direct delta-sigma receiver.

filter [60, 135–138]. However, the performance of designed DDSRs based on these works is not yet up to par with traditional $\Delta\Sigma$ ADCs [55, 139]. For example, the reported signal-to-noise and distortion ratio (SNDR) from the implemented DDSR prototypes lies within the range of 35-60dB with the noise figures ranging from 4 to 9dB [58, 59, 115, 140]. On the other hand, the reported SNDR's of lower GHz $\Delta\Sigma$ ADCs lie within the range of 30-80dB with the noise figures ranging from 20 to 55dB [52, 55, 141–144]. The comparison of performance specs clearly shows that DDSR has superior noise performance as it is designed from the perspective of a receiver. However, the dynamic ranges achieved by DDSRs is still lower than that of $\Delta\Sigma$ ADCs. In the following section, research outcomes from the author's attempt to improve the dynamic range of the DDSR will be presented.

As is well known, the dynamic range of a receiver is restricted on upper-limit by the nonlinearity arising from circuit compression and on lower-limit by the receiver noise and intermodulation products. In a typical downconversion receiver, the target dynamic range can be achieved through optimum gain partitioning and signal filtering. Though this is true for DDSRs as well, additional factors come into play while optimizing the DDSR dynamic range and therefore, these need further description.

5.3 Improving dynamic range: Upper limit

5.3.1 Reduced gain

In receivers, the upper limit of the dynamic range is restricted by the used supply voltage. Any internal signal swings reaching near the supply limits will cause the receiver circuits to compress. This compression will occur for lower input signals if there is a gain present in a receiver. Therefore, from the linearity point-of-view, high gain in receivers is not desired. This leads to a question. Why is gain even needed? The answer to this question lies in the noise behavior of receiver circuits. Gain is needed to reduce the noise contribution from later stages. Therefore, implementing gain more than the minimum required to suppress the noise contribution of later stages, does not bring any additional benefits. The selection of gain in a typical Nyquist-rate ADC receiver is based on a given SNDR specification. The typical design process starts from the V_{FS}, dictated by the maximum supply voltage, and the required SNDR is achieved by pushing the ADC's quantization noise (Qn) floor down by increasing ADC resolution. After defining this resolution, sufficient gain needs to be applied in the receiver chain so that the amplified receiver thermal noise level at the ADC input is higher than the quantization noise floor. This ensures that the quantization noise does not contribute significantly to the overall receiver noise.

An example for gain calculations can be given for an LTE standard. Most of LTE modulation schemes require peak SNR below 30dB [43]. Assuming a target SNR (SNR_{tar}) of 40dB for safety margin, an $\mathrm{SNR}_{\mathrm{min}}$ of 6dB, an LTE signal bandwidth f_{BW} of 10MHz, and an ADC full-scale power (P_{FS}) of 0dBm at its input, the required gain (G) in an ideal noiseless receiver can be found as:

$$G = P_{FS} - SNR_{tar} - SNR_{min} + 174 - 10log(f_{BW}) \tag{5.1}$$

This leads to a gain requirement of 58dB which will bring the -104dBm integrated thermal noise-floor at the input of the receiver to -46dBm at the ADC input. In addition to the thermal-noise, ADC input will also have quantization noise. From the receiver design perspective, this quantization noise should not contribute to overall noise-figure of the receiver and therefore should be kept substantially lower than the thermal-noise at ADC input. Assuming a safety margin of 10dB leads to a quatization noise level of -56dBm at the ADC input. In other words, this means the ADC will

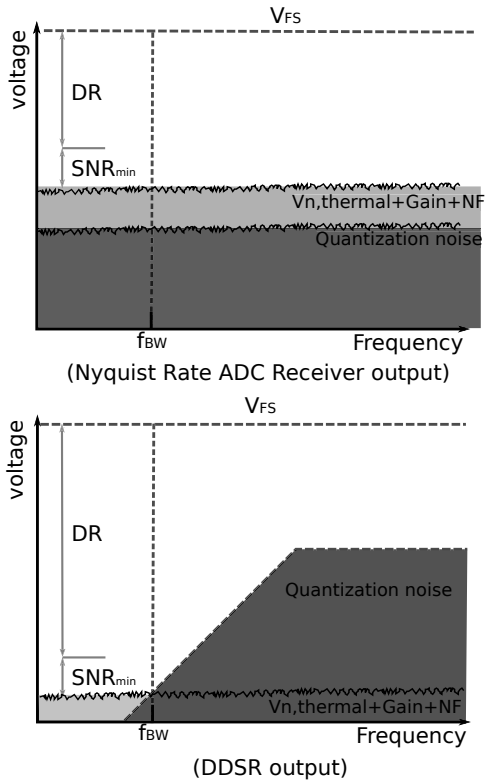

Figure 5.2. Comparison of the gain requirement for (top) a typical receiver with a Nyquist rate ADC and (bottom) a DDSR.

need an SNR of 56dB leading to atleast an 10-bit ADC implementation.

In contrast, the gain requirement in the DDSR is different and can be explained through Figure 5.2. The DDSR design begins from the inband thermal noise floor level at the input of the receiver. The amount of gain that is applied in the DDSR is selected solely based on what is needed to ensure that the LNA is the most significant noise contributor. The resolution of the quantizer and the loop-filter order are then designed so that the in-band quantization noise is sufficiently lower than the amplified thermal noise. Consequently, this means that a much lower gain value is needed in DDSRs in comparison to downconversion receivers with a Nyquist-rate based ADC. Any additional gain will inevitably lead to increased blocker power on the internal nodes of a receiver consequently decreasing the dynamic range. Therefore, in contrast to a traditional DDSR design method where the selected gain is based on conventional design principles of direct downconversion ADCs [58, 60, 135–138, 145], a DDSR based on reduced gain is proposed. The results of which are detailed in publications in II,

VII, and IX.

5.3.2 Blocker rejection at DDSR input

In addition to reduced gain design, another widely implemented technique for improving dynamic range is filtering. Ideally, the gain should always be implemented in conjunction with signal filtering. This is because we only want the desired signal to be amplified. If any out-of-channel/band interferers are amplified by the same amount, they may compress the receiver circuits due to their high power.

Ideally, these interferers should be attenuated as early as possible in the receiver chain. However, all of the recent DDSRs implement N-path filtering at the output of a low-noise amplifier [58–60, 145]. The filtering at the input of the LNA is ignored. Without input filtering and provided the low blocker gain at the LNA output due to filtering, the maximum voltage swing may be reached at the LNA transconductor input rather than at its output. This problem becomes even more severe if the external SAW band-select filter is eliminated to target a completely on-chip implementation. Therefore, an optimum design should ideally filter the out-of-band blockers already at the LNA input.

In Chapter 3, a feedback LNA based solution to provide blocker attenuation at the receiver input was presented. In the following section, another blocker filtering solution at the receiver input is presented for DDSRs. The details of which can be found in publications II and IX, The filtering is achieved through the design of a low-intrinsic input impedance LNA, which provides out-of-band voltage attenuation when driven by source impedance higher than the LNA input impedance. On the other hand, at the desired signal frequency, the input impedance is boosted to a matched condition by the implementation of positive upconverted feedback from the DDSR output. Additionally, we follow the above-mentioned approach of reduced receiver gain design which results in an improved near-band compression point.

Figure 5.3 presents the block level diagram of the proposed positive feedback receiver. The receiver was designed in 28nm technology and evaluated through transient and steady-state AC simulations. The spectrum of the DDSR output bit stream for an input signal and blocker power of -43dBm is shown in Figure 5.4. A few key points can be observed. First, the desired in-band signal is amplified with about A_{CL} = 20dB of receiver gain. Second, the blocker at the 73MHz offset from f_{LO} is filtered by the

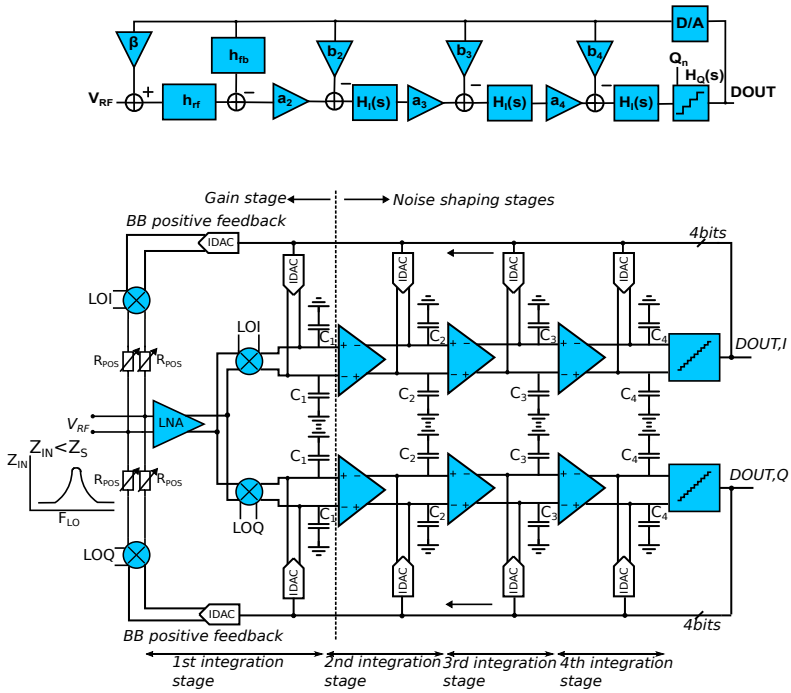

Figure 5.3. (Top) Block level representation of the proposed receiver, and (bottom) implementation of the proposed wide-band DDSR architecture.

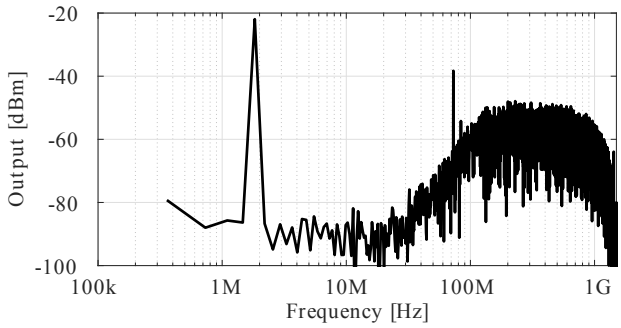

Figure 5.4. Output spectrum at f_{LO} = f_s = 1.5GHz, P_{IN} = -43dBm@f_{LO} + 1.83MHz, $P_{BLOCKER}$ = -43dBm@f_{LO} + 73MHz and f_{BW} = 10MHz.

baseband filtering response, and third, the quantization noise is shaped by the DDSR feedback loop such that the in-band quantization noise is lower than the thermal noise floor.

Figure 5.5 shows the simulated steady-state AC analysis results of the DDSR gain and S_{11}. As desired, A_{CL} = 20dB is observed within the 20MHz RF bandwidth. Further, a differential out-of-band input impedance of 30Ω can be seen needed for blocker attenuation at the LNA input. Figure 5.6 shows the simulated BCP. The receiver achieves a BCP of -11.5dBm at

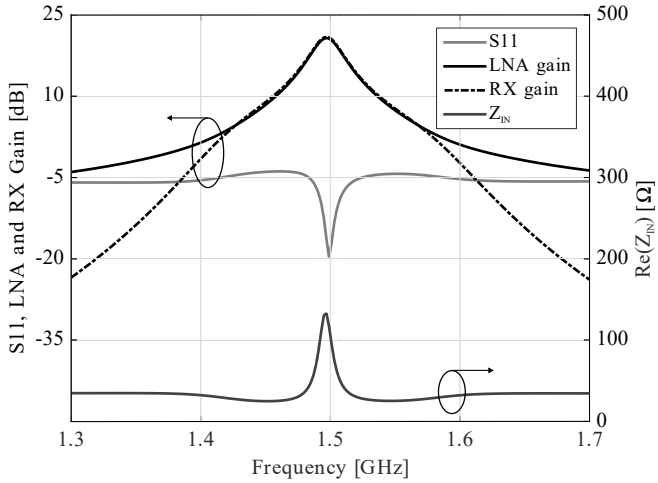

Figure 5.5. Simulated S_{11}, LNA and BB gain for f_{LO} = 1.5GHz.

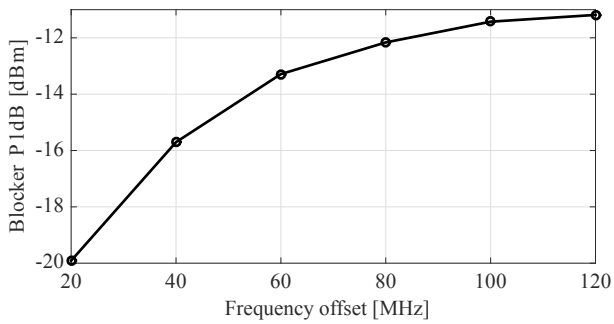

Figure 5.6. Blocker compression point (BCP) vs. frequency offset for the proposed receiver at f_{LO} = 1.5GHz.

100MHz offset from f_{LO}.

5.4 Improving dynamic range: Lower limit

In direct-downconversion receivers, the lower limit of the dynamic range is limited by the thermal noise of the receiver circuits. This is partially true for direct delta-sigma receivers. The upconversion of digital quantization noise brings three additional noise sources originating from the first feedback digital-to-analog converter (DAC). These noise sources are flicker noise, the jitter of the clock and upconversion of the spectrally repeating quantization noise. The first two noise sources are present in any sampling circuit. However, the quantization noise requires special attention in the DDSR due to the upconversion effects caused by the mixer. The upconverted quantization noise in some cases can become higher than the input

referred thermal noise of a receiver thereby reducing the sensitivity of the receiver. This problem becomes even more severe in mixer-first DDSRs as there is no RF gain to suppress the noise contribution of upconverted quantization noise.

Figure5.7(a) shows a typical DDSR output spectrum. The inherent noise shaping of the $\Delta\Sigma$ converter causes the output Qn to be low around DC and at multiples of sampling frequency (f_s). Further, the sinc function originating from the zero-order hold functionality of the quantizer helps to attenuate the Qn at higher offsets. The effect of Qn upconversion can be comprehended by selecting two different f_{LO} frequencies for upconversion as follows:

In the first case, f_{LO} is chosen as $f_s/3$. If f_{LO} is a square wave, higher order odd harmonics will also be upconverted along with the fundamental f_{LO}. Figure 5.7(b) shows the upconverted DDSR spectrum when $f_{LO} = f_s/3$ where dashed lines represent the Qn folding from negative frequencies. As can be observed, the upconverted positive and negative frequencies are not symmetric around DC. This causes a substantial increase in desired channel Qn levels where the main contributor for the desired channel Qn is from the negative frequencies. It can be shown that the worst case unsymmetry between positive and negative upconverted frequencies will occur when f_{LO}=n(f_s/4), where n is an odd integer [146].

In the second case, the degrading effects of Qn upconversion can be minimized by having f_{LO} = n(f_s/2) as illustrated in Figure 5.7(c). Now the upconverted Qn is symmetric and has minima at the desired frequency. This is straightforward to achieve by generating f_s from f_{LO} with a fixed ratio. However, maintaining a specific ratio between f_{LO} and f_s is not always desirable since the varying f_s will be limited by the stability of the $\Delta\Sigma$ loop filter in the lower edge and exceedingly high power consumption on the higher edge. Therefore, there is a need for a detailed understanding of quantization noise upconversion. In publication VI, we have presented systematic modeling and understanding of quantization noise upconversion and its effects on the receiver sensitivity. The analysis leads to simple design guidelines to reduce the degrading effects of quantization noise upconversion. A transistor level mixer-first DDSR is simulated showing a mere 1.5dB degradation from the maximum SNDR for worst-case scenarios, validating the chosen approach. In the following, a summary of the research outcomes of publication VI will be presented.

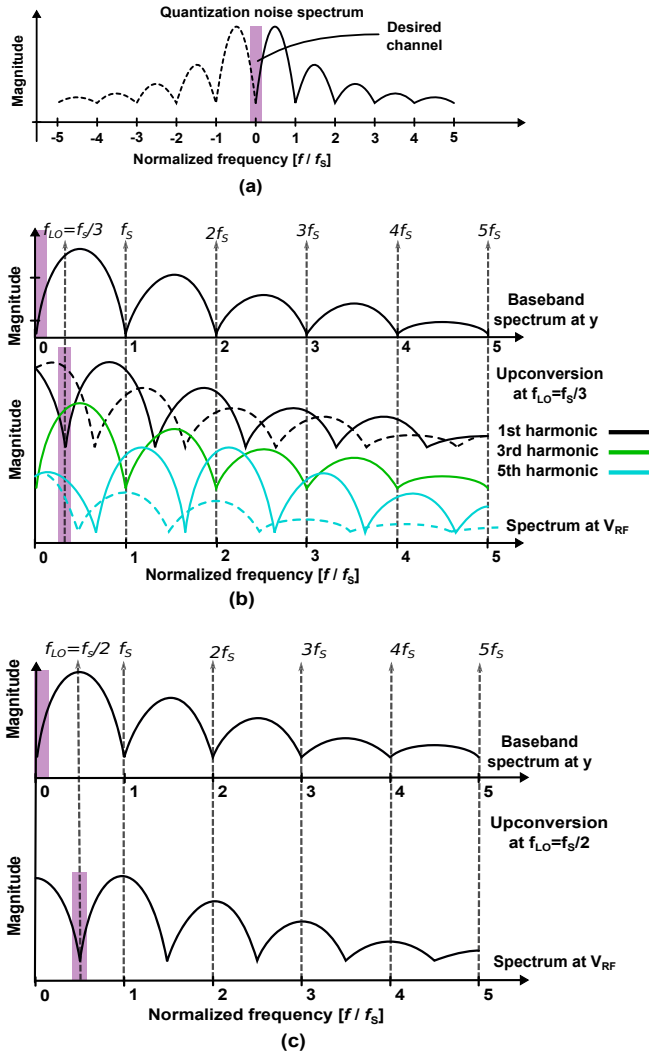

Figure 5.7. a) Typical output spectrum of DDSR at y b) Qn upconversion at $f_{LO} = f_s/3$ c) Qn upconversion at $f_{LO} = f_s/2$.

5.4.1 Modeling of quantization noise upconversion

For the modeling and analysis of upconverted Qn, a four-stage mixer first DDSR architecture is selected as an example. A simplified s-domain block diagram of the chosen architecture is presented in Figure 5.8(a). For this architecture, the upconverted Qn path is modeled with transfer function $H_{FB,upn} = V_{RF}/y$ defined from the DDSR output to RF input at n-th harmonic frequency, where n is an odd integer, and noise transfer function (NTF) = y/Qn. Further, the coefficients $a_{1\text{-}3}$ and $b_{1\text{-}3}$, described in Figure 5.8(a), represent feedforward and feedback loop filter coefficients,

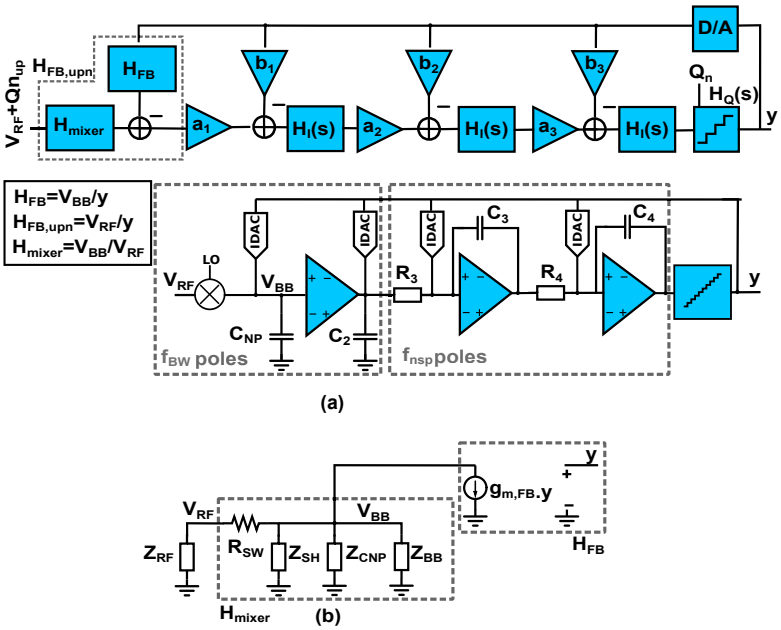

Figure 5.8. a) A four-stage mixer-first DDSR model. b) Modeling of H_{mixer} and H_{FB}.

H_I(s) represents the integrator transfer function, and H_Q(s) represents the quantizer transfer function. For such an architecture, the upconverted Qn rms voltage in $V/\sqrt{Hz}$ at the RF input nodes can be given as:

$$Q_{up} = \sum_{n=1,3,5,7..}^{\infty} H_{FB,upn}.NTF.Q_n, \tag{5.2}$$

where Qn represents the maximum value of quantizer rms noise voltage in $V/\sqrt{Hz}$ given by:

$$Q_n = \frac{\Delta}{\sqrt{6f_S}}, \tag{5.3}$$

where Δ represents the quantizer step size and f_s is the quantizer sampling frequency. Further, the NTF for the presented model can be calculated as:

$$NTF = \frac{1}{1/H_Q + a_1a_2a_3H_{FB}H_I^3 + a_2a_3b_1H_I^3 + a_3b_2H_I^2 + b_3H_I}. \tag{5.4}$$

Evaluation of NTF requires defining the transfer functions H_I, H_{FB} and H_Q. If we assume a non return to zero (NRZ) DAC implementation, H_Q(s) can be modeled with a quantizer gain G_Q and sampling frequency f_s:

$$H_Q(s) = G_Q\frac{1 - e^{-s(1/f_s)}}{s(1/f_s)}. \tag{5.5}$$

Further, H_{I} is modeled as a ideal integrator with transfer function 1/s while H_{FB} can be calculated based on the modeling of passive N-path mixer non-idealities in [135] as:

$$H_{FB} = \frac{4Z_{BB}g_{m,FB}(Z_{RF} + R_{SW})}{2Z_{RF} + 2R_{SW} + Z_{BB}}, \tag{5.6}$$

where Z_{BB} represents the input impedance of the first baseband transconductor, $g_{\mathrm{m,FB}}$ is the effective transconductance of the first current output digital-to-analog converter (IDAC), Z_{RF} is the impedance connected to the RF side of the downconversion mixer, and R_{SW} is the mixer switch resistance.

In a similar manner to H_{FB} and following the analysis performed in [135], we can derive the $\mathrm{H_{FB,upn}}$ at the n-th harmonic frequency of f_{LO} as:

$$H_{FB,upn} = \frac{4\sqrt{2}}{n\pi}\frac{g_{m,FB}Z_{BB,tot}}{(1+\gamma Z_{BB,tot}Y_{up})}\frac{Z_{RF}}{Z_{RF}+2R_{SW}}, \tag{5.7}$$

$$Y_{up} = \sum_{p=-\infty}^{\infty}\frac{2}{(4p+1)^2(Z_{RF}+2R_{SW})}. \tag{5.8}$$

Here p is an integer, γ = 2/π^2 for 25% duty cycle quadrature mixers and $\mathrm{Z_{BB,tot}}$ is the parallel combination of baseband input impedance $\mathrm{Z_{BB}}$, impedance of the N-path capacitance Z_{CNP} and the virtual shunt impedance $\mathrm{Z_{SH}}$ representing the power dissipation due to baseband signal upconversion given by [84]:

$$Z_{SH} = (\sum_{n=3,7,11..}^{\infty}\frac{1}{n^2 Z_{RF}^{*}(nf_{LO})} + \sum_{n=5,9,13..}^{\infty}\frac{1}{n^2 Z_{RF}(nf_{LO})})^{-1} \tag{5.9}$$

The upconverted quantization noise Q_{up} will add up directly with the input referred thermal noise of a receiver. This essentially means that in order to have a minimal effect on the overall receiver NF, the Q_{up} must be significantly lower than the input referred thermal noise ($\mathrm{N_{thermal}}$). Mathematically, we can write:

$$NF \approx 10log10(F_{LIN} + \frac{Q_{up}^2}{4kTZ_{RF}}) \tag{5.10}$$

where k is Boltzmann's constant, T is the temperature in Kelvin and $\mathrm{F_{LIN}}$ is the receiver noise factor without Qn contribution. For a minimal impact of Q_{up} on the receiver noise figure, $Q_{up}^2/4kTZ_{RF} << F_{LIN}$.

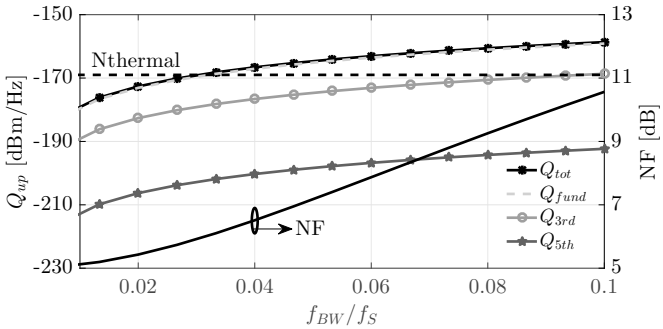

Figure 5.9. Upconverted quantization contribution from different LO harmonics at different $f_{\mathrm{BW}}/f_{\mathrm{s}}$ ratios. $f_{\mathrm{ns}}/f_{\mathrm{s}}$ = 0.1, Δ = 1, G = 20dB, and $f_{\mathrm{LO}}/f_{\mathrm{s}}$ = 3/4.

5.4.2 Model evaluation and design guidelines

The built model for Qn upconversion was analyzed through behavioral and transistor level simulations. The target was to analyze in which conditions upconverted quantization degrade the receiver NF. Below a summary of the key results is presented. Again, for detailed description, the reader may please refer to publication VI.

In Figure 5.9, the Q_{up} from different LO harmonics is plotted vs. $f_{\mathrm{BW}}/f_{\mathrm{s}}$ while keeping f_{s} constant. One can observe a higher Q_{up} for higher $f_{\mathrm{BW}}/f_{\mathrm{s}}$ ratios. This behavior can be explained as follows: The f_{BW} is controlled by the first two stage poles, created by C_{NP} and C_2, forming a second order filter. C_{NP} comes directly in the Qn upconversion path as a first order filter and is therefore the main contributor for the behavior in Figure 5.9. A smaller C_{NP} results in upconversion of the wider band of Qn consequently increasing inband Q_{up}. Generally, a designer does not have freedom to control the C_{NP} value as it is dictated by the required f_{BW} of the receiver. Nevertheless, regardless of C_{NP} value, C_{NP} helps in both channel selection and Q_{up} filtering which is beneficial from the performance point-of-view.

Figure 5.9 also elaborates a key design difference between a DDSR and a typical $\Delta\Sigma$ ADC. As is the case in a typical $\Delta\Sigma$ ADC, choosing $f_{\mathrm{BW}} = f_{\mathrm{ns}}$, where f_{ns} is the NTF pole frequency, will result in a substantial increase in Q_{up}. Therefore, for an optimum receiver sensitivity performance, f_{ns} should be chosen much larger than f_{BW}. This is also beneficial in ease of implementation as we can independently design f_{BW} and f_{ns} loop filters.

In Figure 5.10, Q_{up} from different LO harmonics is plotted vs. $f_{\mathrm{LO}}/f_{\mathrm{s}}$ while keeping f_{s} constant. As expected, the Q_{up} follows a zig-zag behavior, having much higher Q_{up} for the worst case frequencies of $f_{\mathrm{LO}} = \mathrm{n}(f_{\mathrm{s}}/4)$.

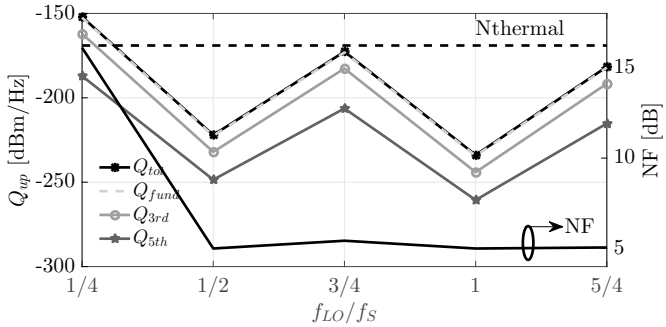

Figure 5.10. Upconverted quantization contribution from different LO harmonics at different $f_{\mathrm{LO}}/f_{\mathrm{s}}$ ratios. Δ = 1, G = 20dB, $f_{\mathrm{BW}}/f_{\mathrm{s}}$ = 0.02 and $f_{\mathrm{ns}}/f_{\mathrm{s}}$ = 0.1.

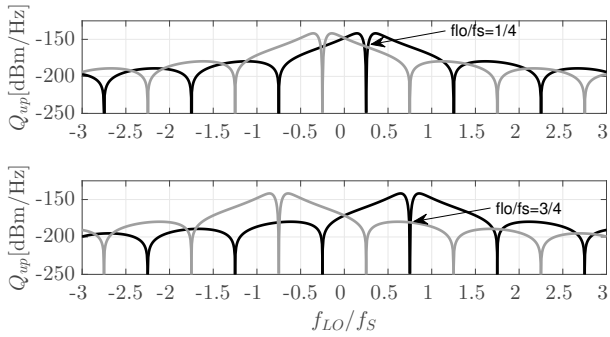

Figure 5.11. Effect of positive (black) and negative (gray) sides of upconverted spectrum at two different $f_{\mathrm{LO}}/f_{\mathrm{s}}$ ratios. $f_{\mathrm{LO}}/f_{\mathrm{s}}$ = 1/4 ratio leads to higher Q_{up}. Δ = 1, G = 20dB, $f_{\mathrm{BW}}/f_{\mathrm{s}}$ = 0.01 and $f_{\mathrm{ns}}/f_{\mathrm{s}}$ = 0.1.

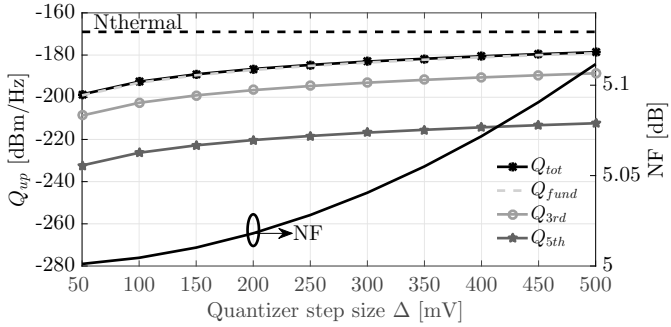

Figure 5.12. Upconverted quantization contribution for different quantizer step sizes. $f_{\mathrm{LO}}/f_{\mathrm{s}}$ =3/4, Δ = 1, G = 20dB, $f_{\mathrm{BW}}/f_{\mathrm{s}}$ = 0.02 and $f_{\mathrm{ns}}/f_{\mathrm{s}}$ = 0.1.

One can also observe that Q_{up} is very high for $f_{\mathrm{LO}}/f_{\mathrm{s}}$ = 1/4. This can be explained through Figure 5.11 where we plot the positive and negative sides of Q_{up} at two different $f_{\mathrm{LO}}/f_{\mathrm{s}}$ ratios. One can observe that even after the C_{NP} filtering effect, the sum of Q_{up} from the positive and the negative sides of spectrum is higher for $f_{\mathrm{LO}}/f_{\mathrm{s}}$ = 1/4 than $f_{\mathrm{LO}}/f_{\mathrm{s}}$ = 3/4 and therefore, will degrade the receiver NF more severely.

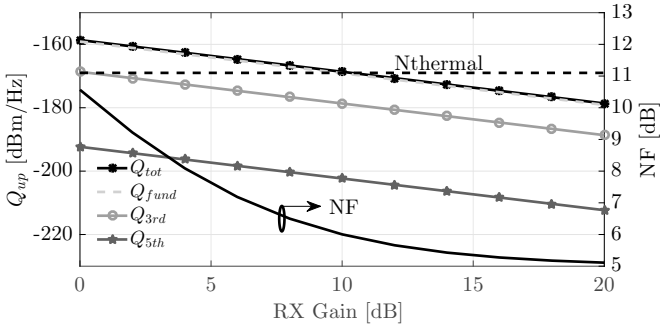

Figure 5.13. Upconverted quantization contribution for different values of receiver gain. $f_{\mathrm{LO}}/f_{\mathrm{s}}$ =3/4, Δ = 1, G = 20dB, $f_{\mathrm{BW}}/f_{\mathrm{s}}$ = 0.01 and $f_{\mathrm{ns}}/f_{\mathrm{s}}$ = 0.1.

In Figure 5.12, the Q_{up} from different LO harmonics is plotted for different values of quantizer step size Δ. One can observe that Q_{up} is a weak function of Δ. This is expected as the effect of C_{NP} already filters out a huge portion of Qn. However, in order to have a minimum effect on Q_{up}, Δ should be chosen as low as possible.

In Figure 5.13, the Q_{up} from different LO harmonics is plotted at different values of receiver gain. Results show that higher values of receiver gain are beneficial in terms of reduced Q_{up}. However, as we detailed in II and IX, only a minimum amount of gain should be applied in the DDSRs which is deemed sufficient to reduce the noise contribution from later stages. The lower gain will improve the large signal performance of a receiver. Therefore, selection of gain is a compromise between Q_{up} and receiver large signal linearity and should be chosen as minimum value that has acceptable noise performance.

From the above results we can establish the following design guidelines for the mixer-first DDSR:

- It is a good idea to limit the bandwidth of mixer nodes to f_{BW} where f_{BW} should be much less than f_{ns} and f_{s}. This is in contrast to typical $\Delta\Sigma$ ADC design where f_{BW} = f_{ns}. Selecting $f_{\mathrm{ns}} >> f_{\mathrm{BW}}$ will also allow independent design of the f_{BW} and f_{ns} loop filters.

- Among the worst case f_{LO} = n(f_{s}/4) frequencies, $f_{\mathrm{LO}}/f_{\mathrm{s}} < 1/2$ are most problematic. First order C_{NP} filtering may not be enough to filter upconverted Qn for such ratios.

- Selection of a higher number of quantizer bits is beneficial for a reduced

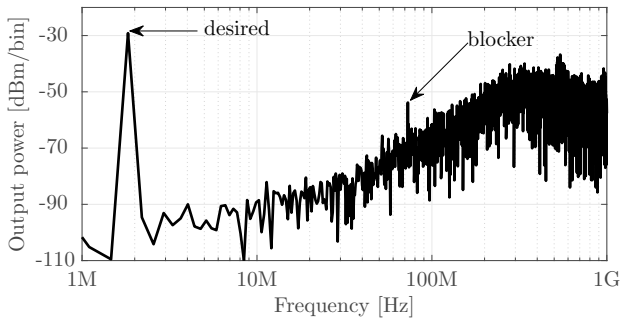

Figure 5.14. Output spectrum at f_{LO} = f_{s} = 1.5GHz, Signal power P_{in} = -42dBm@f_{LO}+1.83MHz, Blocker power P_{blk} = -42dBm@f_{LO}+70MHz and f_{BW} = 10MHz.

upconverted Qn but is not a strong function.

- In contrast to a typical $\Delta\Sigma$ ADC design, selecting a unity gain loop filter is not beneficial in the DDSR. Gain should be high for reduced Q_{up}. From our previous design experience, 15-20dB gain should suffice in most cases.

Based on the above guidelines, a mixer-first DDSR was implemented on a 28nm FDSOI technology. The DDSR is designed for a configurable band of 0.7-2.7GHz with a BB bandwidth f_{bw} of 10MHz. The first frequency translating integrator stage, which is the most important in shaping Q_{up}, consists of passive quadrature downconversion mixers with a 25% duty cycle together with a C_{NP} as N-path capacitor. C_{NP} provides dual roles of channel select and Qn filtering. The later two DDSR stages are implemented in active RC configuration for better linearity.

The spectrum of the DDSR output bit stream is shown in Figure 5.14. The DDSR functionality is observed through the following. First, the desired in-band signal is amplified with around 15dB of RX gain. Second, the blocker is attenuated by the channel select filtering response and third, the Qn is shaped by the DDSR feedback loop such that there is little in-band Qn left.

In Figure 5.15, the simulated SNDR vs. f_{LO} is presented for different standard deviations of sampling clock jitter. We keep the sampling frequency constant at 1.5GHz which means that across a 0.5-2.7GHz f_{LO} sweep, there will be worst case $f_{\mathrm{LO}}/f_{\mathrm{s}}$ ratios. As expected, a mere 1.5dB of maximum degradation in receiver SNDR is observed even for the worst

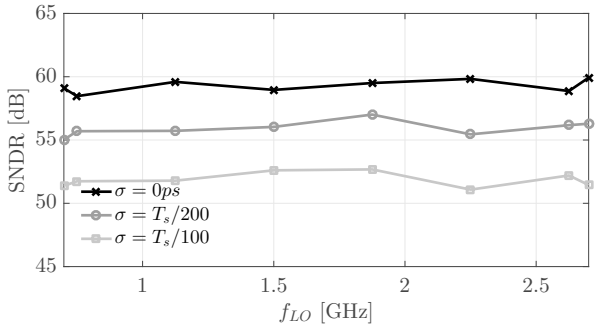

Figure 5.15. SNDR versus f_{LO} at different f_{s} clock jitter standard deviations (σ). f_{s} = 1/T_{s} = 1.5GHz and P_{in} = -35dBm. As desired, minimal impact on receiver SNDR is observed for arbitrary ratios of $f_{\mathrm{LO}}/f_{\mathrm{s}}$.

case $f_{\mathrm{LO}}/f_{\mathrm{s}}$ ratios. The impact of f_{s} jitter lowers the overall SNDR. Nevertheless, the maximum SNDR degradation remains about the same across different $f_{\mathrm{LO}}/f_{\mathrm{s}}$ ratios.

5.5 Summary

The direct delta-sigma receiver is one of the promising architectures to achieve software-defined radio goals. However, the achieved performance of the DDSR such as its dynamic range is not yet comparable to $\Delta\Sigma$ ADCs. As an original contribution to this thesis, this chapter covers a reduced gain method to improve the DDSR upper edge of the dynamic range. Further, the degrading effects of quantization noise upconversion on DDSR sensitivity have been analyzed and simple design guidelines generated. The detailed results for the presented research outcome are part of publications VI, I, II and IX.

6. Conclusions

Over the years the emergence of multiple communication standards and frequency bands has led to increased demand for fully integrated and tunable wideband receivers. This goal for further receiver development is captured by the software-defined radio (SDR) paradigm. In particular, the SDR paradigm entails the implementation of an integrated radio receiver that can be re-programmed for different communication standards and frequencies through a software code. To realize such an SDR, an intriguing approach is an RF-to-digital converter where the RF signal is ideally digitized at the antenna to IC interface. So far implementing an RF-to-digital converter in the lower GHz frequency range has not been completely successful due to various key challenges. However, to cover all design challenges of RF-to-digital converters is beyond the scope of this thesis. Instead, this dissertation is related to the author's work in an attempt to solve the following design challenges: 1) harmonic rejection in wideband front-ends, 2) blocker resilience in SAW-less front-ends, 3) self-interference cancellation in full-duplex receivers, 4) blocker resilience in direct delta sigma receivers, and finally 5) quantization noise upconversion effects in mixer-first direct delta sigma receivers.

First, a harmonic rejection wideband receiver was fabricated in 28nm technology. The receiver implemented two-stage harmonic rejection where the first implementation of harmonic rejection already occurred after the first gain stage. The proposed architecture uses simple weighting coefficients of ± 1 with 6-phase LO clocking and a reduced number of baseband paths in comparison to 8-phase harmonic rejection architectures. The measured performance of the receiver demonstrated overall third-order harmonic rejection in the range of 46-53dB with an impressive blocker compression point of 2.5dBm at a 100MHz offset from the baseband channel.

Second, a third-order baseband integrator was designed, measured and analyzed. The baseband integrator together with a quadrature passive mixer brings the third-order filtering response to RF nodes thereby improving the near-band blocker rejection. The measured results demonstrated blocker rejection for nearband blockers. For example, the blocker compression point measured at a 40MHz offset was -6.5dBm which is just 1.5dB lesser than the blocker compression point at 100MHz.

Third, a capacitive feedback low-noise amplifier was proposed which provided on-chip tunable blocker filtering at both input and output nodes of the LNA. The LNA achieved this through selective input impedance of the LNA which was lower than the source impedance at blocker frequencies and matched to the source impedance at the desired frequency. Detailed theoretical analysis was done to provide design guidelines of the presented LNA while the simulation results showed an out-of-band blocker compression point of 1.5 dBm and an out-of-band IIP3 of +14 dBm at a 100-MHz offset from LO frequency.

Fourth, a novel technique for transmitter leakage cancellation in full-duplex transceivers was proposed. The technique used the buried-gate of a FDSOI technology transistor for the RF signals compared to its usual role of just DC-biasing. An 180° phase shifted and weighted transmitter signal was fed at the buried-gate of the designed LNA to cancel the transmitter leakage. Fabricated on 28nm FDSOI technology, the measured results demonstrated 40-50dB rejection for transmitter leakage as high as -10dBm, and above 20dB for transmitter leakage of -5dBm, with no increase in the receiver noise figure.

Fifth, a direct delta-sigma receiver with selective input impedance was proposed to provide blocker attenuation already at the receiver input. This was achieved by designing the receiver input transconductor with much lower intrinsic impedance than source thereby providing the blocker voltage attenuation at the input node. On the other hand, the input impedance at the desired frequency was boosted to a matched condition through an upconverted positive feedback from the $\Delta\Sigma$ ADC output.

Sixth, an approach of reduced gain design was followed in the proposed DDSR to further improve blocker rejection. This is in contrast to previous DDSR implementations in which the selected gain value is based the general practices of receiver design. It was established that the general practices of high gain in a receiver does not provide optimum performance in DDSRs.

All of the above mentioned techniques are an attempt towards a completely integrated and tunable on-chip filtering which will either eliminate or at least alleviate the performance requirements of external non-tunable and bulky filters. Another research outcome was focused towards a different and challenging problem related to DDSRs, namely the degrading effects of quantization noise upconversion on DDSR sensitivity. A systematic modeling and understanding of quantization noise upconversion effects was presented specifically for a worst-case of a mixer-first DDSR. The resulting modeling together with behavioral simulations provided deep insights into the effects of upconverted quantization noise leading to design guidelines. A mixer-first DDSR was designed on 28nm technology demonstrating a mere 1.5dB degradation from the maximum SNDR for the worst case scenarios arising from quantization noise upconversion.

The proposed solutions in this thesis aim to overcome challenges faced by an RF-to-digital converter. However, current wireless communication trends seem to suggest a much more hostile environment for future RF-to-digital converters. Every now and then new communication standards and frequency bands crowd the wireless spectrum giving rise to additional hostile blockers. In addition, exploration of millimeter-wave frequencies for fifth generation mobile communication will give rise to additional high-frequency design challenges in practical RF-to-digital converters. It is difficult to estimate what exactly will the future solutions be. Nevertheless, it seems that the research in wideband RF-to-digital converters design will go a long way.

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An attractive approach to realize an software defined radio is an RF-to-digital converter. In best case, an RF-to-digital converter consists of an analog-to-digital converter (ADC) which is directly connected to a wideband antenna. However, such a complete RF-to-digital converter has so far proved to be an elusive goal due to impractically high power consumption requirements of ADC in the GHz range.Therefore, a practical RF-to-digital converter is followed by an RF front-end which reduces the power consumption requirements of an ADC. Software defined radio research for such a practical RF-to-digital converter implementation is focused towards reconfigurable, wideband and digital intensive RF front-ends. This thesis focuses on finding new solutions to design challenges related to RF front-ends targetted for RF-to-digital converters.

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