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Efficient Modeling of Crosstalk Noise on Power Distribution Networks for Contactless 3-D ICs

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***Abstract*— An efficient and frequency-dependent model describing the crosstalk noise on power distribution networks due to inductive links in contactless 3-D ICs is presented. A two-step approach is followed to model the crosstalk effect. During the first step, the mutual inductance between the power distribution network and the inductive link is analytically determined. Due to the weak dependence of mutual inductance to frequency, a magnetostatic model is proposed for this step. The model includes the physical and electrical characteristics of both the on-chip inductor and the wires of the power distribution network. In this way, different power network topologies can be modeled facilitating noise analysis in the vicinity of the on-chip inductor. This approach is justified by the typical use of regular power network topologies in modern integrated circuits. In the second stage, the noise is assessed with SPICE simulations, considering the mutual inductance between the two structures from the first step and the resistance variations due to high frequency effects. Thus, an efficient, scalable, and accurate method for the analysis of the crosstalk effects due to inductive links is provided, without resorting on computationally expensive and time consuming full-wave simulations. Compared with the full-wave simulations, the induced noise is evaluated four orders of magnitude faster with the proposed model. The accuracy of the proposed model is within 10% of the respective noise computed with a commercial electromagnetics simulator using the finite element method. An analysis including the effect of substrate resistivity on the crosstalk noise is also presented.**

***Index Terms*— Mutual inductance, crosstalk noise, inductive links, power distribution networks, high frequency, contactless 3-D systems.**

I. Introduction

THREE-DIMENSIONAL integration is a promising technology providing multi-functional, high performance, and low power electronics [1]. Especially heterogeneous 3-D ICs, are predicted, according to ITRS, to be a potential solution for the many challenges encountered by the Mobile and IoT markets [2]. The wider uptake and commercialisation of 3-D ICs, however, requires effective inter-tier communication. Several approaches are considered for inter-tier communication, with through silicon vias (TSV) being the most prominent. Alternatively, contactless solutions have emerged, based on either inductive or capacitive coupling [3]–[7].

Despite their inherent simplicity, TSV entail an overhead in cost due to the related manufacturing complexity and possibly low yield [8]–[10]. For example, to alleviate the impact of copper pumping due to the TSV, an additional high thermal annealing process is required, increasing the manufacturing cost [9]. Several other reliability issues need to be considered, such as copper diffusion from the TSV to the substrate, mechanical stresses, and electromigration, each requiring additional processing steps. Furthermore, considerable substrate thinning is imperative for state-of-the-art TSV integration, where the TSV has a diameter of 5 μm or smaller. Consequently, a significant processing cost is incurred due to the handling of the thin wafers.

With contactless inter-tier communication, nevertheless, significant advantages exist for both homogeneous and heterogeneous 3-D ICs. Due to the versatility of the transceiver solutions, seamless integration can be achieved without using level shifters [11] or complicated design rules imposed by TSV. In addition, standard CMOS processes and methodologies are utilised maintaining overall a low processing cost and high manufacturing yield. Furthermore, unique benefits exist including die detachability [12]. Out of the two contactless schemes, nevertheless, capacitive coupling is limited to face-to-face implementations practically supporting only two tier systems, thereby significantly narrowing the scope of multi-tier integration. Consequently, inductive links are investigated in this paper.

High performance inductive links have been developed recently [5], [13], where the performance of inductive links is comparable to TSV interfaces when signal multiplexing is employed [6]. With wireless inter-tier communication, however, new challenges arise, including interference with components in the vicinity of the on-chip inductors. In wired 3-D approaches, the crosstalk noise is localised and often dominated by the capacitive coupling between adjacent interconnects [14]. Alternatively, due to the emission of the magnetic field in inductive based communication, crosstalk noise is a long range phenomenon and an important issue in the design process of inductive links that requires attention [15]. For these reasons, in addition to design methods, the crosstalk between neighbouring inductive links [12], [16] and the interference of adjacent interconnects on inductive links have both been explored [17]. Nevertheless, the effect of the inductive links on global interconnects and the power integrity of the system has

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yet to be fully investigated. Wireless communication through magnetic flux leads to parasitic coupling with nearby conductors, such as power distribution interconnects, which operate as accidental antennas. Subsequently, undesirable voltage fluctuations develop on the power distribution network (PDN), that can hinder power integrity and degrade the robustness of the system.

In [18] and [19], the crosstalk noise effects are explored for different power distribution network topologies and arrays of multiple inductors. For example, the noise caused by an inductive link array in a 65 nm process node can reach up to 320 mV (e.g. 26% of the nominal V_{DD}); though proper PDN placement can reduce the noise up to 70% [18]. Furthermore, the sensitivity of PDN topologies to noise depend upon the geometry of each topology [19]. These results demonstrate that noise due to inductive links affects the power distribution network, thereby compromising power integrity if ignored. Nevertheless, proper allocation of the PDN wires in the vicinity of the inductor mitigates the induced noise. Therefore, placement of the PDN in close proximity to the on-chip inductor is feasible, resulting in a small increase in the IR drop noise but mitigating the overall noise.

To determine the appropriate PDN placement for minimising the aggregate noise, the crosstalk noise should accurately be evaluated. This noise depends upon the relative position of the PDN and the on-chip inductors. The mutual inductance between the coupled structures is therefore required, which can be determined with electromagnetic simulations. However, full-wave electromagnetic simulations[1] cost in time and computing resources and typically are limited to a specific inductor-PDN structure. Additionally, simulating the investigated structures for each location of the PDN conductors in the vicinity of the inductor entails excessive delay in the design process. Furthermore, commercial IC design tools do not support inductance extraction for multi-tier systems and different process nodes. Thus, there is a lack of effective means to determine the vital mutual inductance for inductive-based 3-D ICs.

Based on these observations, the contributions of this paper are:

- A methodology to describe the induced crosstalk noise on on-chip interconnects without the need for full-wave electromagnetic simulations.
- A scalable, efficient, and accurate magnetostatic model for the evaluation of the mutual inductance as part of this methodology. The spatial position and geometry of the on-chip inductor and the topology of the nearby interconnects are considered for the evaluation of the mutual inductance.
- A SPICE-based noise model to rapidly and accurately evaluate the induced noise on the PDN.

The proposed model improves power integrity, without requiring excessive computational resources.

The remainder of this paper is organised as follows. A magnetostatic model for the evaluation of the mutual inductance between an on-chip inductor and the power distribution network is described in Section II. A methodology for the evaluation of the frequency-dependent induced noise is presented in Section III, verified with SPICE simulations. The proposed methodology is applied to a case study in Section IV, utilising the mutual inductance model of Section II. Some conclusions are drawn in Section V.

[1]In this paper, full-wave electromagnetic simulations are primarily performed with Ansys HFSS and the two terms are used interchangeably.

II. Analytic Mutual Inductance Modelling

A closed-form model for the evaluation of the mutual inductance between an on-chip inductor and a loop of the power distribution network is presented in this section. In subsection II-A, a magnetostatic model for the evaluation of the mutual inductance of the investigated structures is described. The accuracy of the proposed model is verified with the Ansys Maxwell [20] simulator in subsection II-B. The computational speedup over finite element methods (FEM) is presented in subsection II-C.

Two approaches to evaluate the mutual inductance between the two structures are compared. Magnetostatic simulations of the structure are performed in Ansys Maxwell [20] to extract the mutual inductance by directly solving the Maxwell equations with the FEM solver. Alternatively, the mutual inductance is evaluated with an analytic model utilising a set of closed-form expressions of elemental structures (e.g. the mutual inductance between two thin rectangular conductors) to describe complex geometries (e.g. an inductor and a PDN). After developing the analytic model, these two approaches are compared in terms of accuracy and speed.

A. Magnetostatic Mutual Inductance Evaluation

The analytic magnetostatic model for the evaluation of the mutual inductance is presented in this subsection. The geometry of the coupled structure composed of a power distribution network loop and the on-chip inductor is depicted in Figure 1(a). A square on-chip inductor geometry is utilised, although the model can also be adapted for octagonal inductors. The wires in grey colour denote the two conductors of a PDN loop, while the wires in white colour are the windings of the inductor. The PDN wires are assumed to be placed in any position across the y-axis, parallel to the inductor windings.

Assume a current density J_{ind} and the respective current I_{ind} flow through each of the inductor windings. The current flowing through the inductor generates a magnetic field that couples with the power distribution network wires in the vicinity. The magnetic flux that couples the two structures is given by

$$\Psi_{pdn} = \int_S \mathbf{B_{ind,pdn}} \cdot d\mathbf{S} \implies M_{ind,pdn} = \Psi_{pdn}/I_{ind}, \quad (1)$$

and, therefore, the mutual inductance between the inductor and the PDN is determined. The magnetic flux, Ψ which couples with the PDN, is proportional to the area of the loop formed by the PDN wire.

To simplify the evaluation of the mutual inductance without directly solving the integral in (1), the concept of partial inductance is utilised [21]. The closed path of the PDN

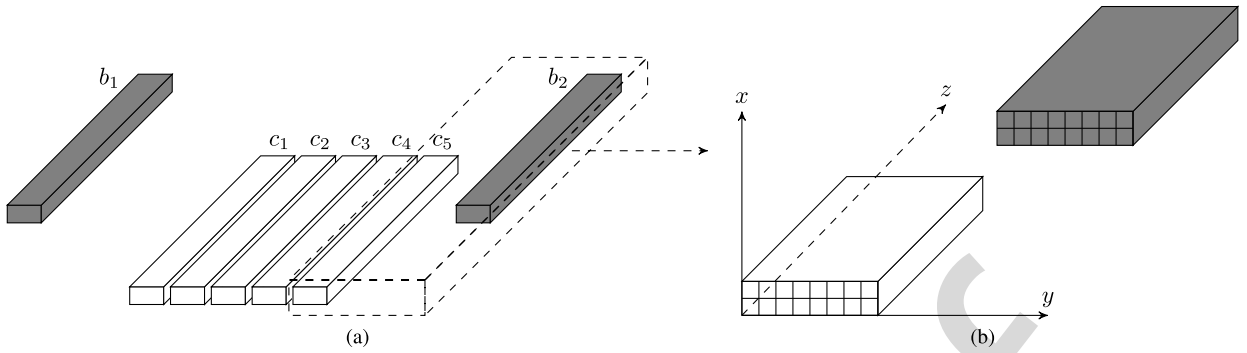


Fig. 1. (a) The segments of the windings of the inductor and the segments of a PDN loop in the vicinity of the inductor and (b) a detailed view of two segments, depicting the partition of the segments into filaments.

loop is segmented into n continuous segments b_i so that $b = b_1 \cup b_2 \cup \cdots \cup b_n$ where b is the PDN loop. Equivalently, the inductor is segmented into m partitions c_i, $c = c_1 \cup c_2 \cup \cdots \cup c_m$, where c is the inductor geometry. Each segment of the PDN or the inductor is a straight rectangular conductor of finite length, as seen in Figure 1(a). Based on this initial segmentation of the inductor-PDN structure, the problem of determining the mutual inductance is reduced to evaluating the mutual inductance for $n \times m$ segments, ignoring the perpendicular segments that evaluate to zero. The total mutual inductance between the two structures is given by the summation of the partial mutual inductances.

The mutual inductance between two filaments is extracted by Neumann's formula [22]. Solving Neumann's formula integral gives the mutual inductance closed-form expression [23]

$$M_{kl} = 10^{-5}\Big[z \ln\left(z + \sqrt{z^2+\rho^2}\right) - \sqrt{z^2+\rho^2}\Big]_{l_2+l_3-l_1,l_3}^{l_3-l_1,l_3+l_2}(z), \tag{2}$$

where z and ρ are the vertical and the cartesian distance between the two filaments, respectively, and

$$\Big[f(z)\Big]_{s_2,s_4}^{s_1,s_3}(z) = \sum_{i=1}^{4}(-1)^{k+1} f(s_i). \tag{3}$$

Expression (2) describing the mutual inductance is normalised to micrometers (μm) for the length and to nanoHenry (nH) for the inductance. The model can be parameterised by altering the s-matrix used in (3)

$$\begin{bmatrix} s_1 & s_3 \\ s_2 & s_4 \end{bmatrix} = \begin{bmatrix} l_3 - l_1 & l_3 + l_2 \\ l_2 + l_3 - l_1 & l_3 \end{bmatrix}. \tag{4}$$

In (4), l_1 is the length of the inductor segment, l_2 is the length of the PDN segment, and l_3 is the difference in length between the two filaments if projected on the z-axis as shown in Figure 1(b). Furthermore, the physical boundaries of the simulation are controlled by the variable

$$\rho = \sqrt{d^2 + t_{ild}^2}, \tag{5}$$

where d is the horizontal distance (y-axis) and t_{ild} is the vertical distance between the filaments (x-axis), respectively. The vertical distance between the filaments is equal to the inter-layer dielectric thickness and is a technology specific parameter.

The evaluation of the mutual inductance for the specific problem can also be performed with the expressions (8) or (14) from [23] that correspond to the mutual inductance between two thin tapes and the mutual inductance between mutual bars, respectively. Nevertheless, the use of filaments provides greater versatility for describing the investigated structure and, therefore, greater control of the accuracy of the simulation, as explained in the following paragraphs. Additionally, the method of rectangular bars suffers from numerical pitfalls as reported in [24].

A major advantage of utilising an arbitrary number of filaments to model rectangular conductors is the greater scalability for several physical parameters of the structure. For the method of filaments to provide sufficiently accurate results, the length l of each segment b_i (or c_i) is assumed to be much larger compared to the thickness, t, or width, w, of the particular wire, $l \gg t, w$. Since on-chip interconnect wires are utilised, this assumption is true for the thickness, t. However, the relation between the width, w, and the length, l, is not always straightforward. The number of filaments can, thus, be adjusted according to the relative size between the physical parameters of the structure to produce an accurate solution.

Another implication for the chosen evaluation method for the mutual inductance is scaling with frequency. Skin, proximity, and corner effects [25], [26] alter the current density of the conductor with increasing frequencies, leading to different results for the magnetostatic solution of the mutual inductance. However, due to the width and thickness of the integrated interconnects, the impact of high frequency effects on the mutual inductance is minimal for frequencies up to 10 GHz, well beyond the resonance frequencies of the inductors used for inductive links [4], [5]. Consequently, the magnetostatic solution of the mutual inductance is sufficient for this problem. Simulations supporting this assumption and verifying the accuracy of the model are demonstrated in the following subsection.

B. Model Verification

The accuracy of the proposed magnetostatic model is verified in this subsection. The analytic model is implemented

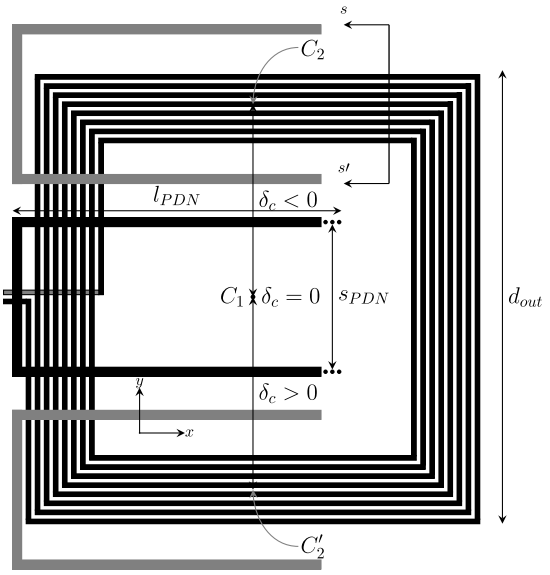


Fig. 2. Top view of the on-chip inductor with a PDN loop in its vicinity. The PDN loop is placed in three distinct positions where $\delta_c = 0\ \mu m$, $\delta_c = d_{out}/2\ \mu m$ (C_2), and $\delta_c = -d_{out}/2\ \mu m$ (C_2').

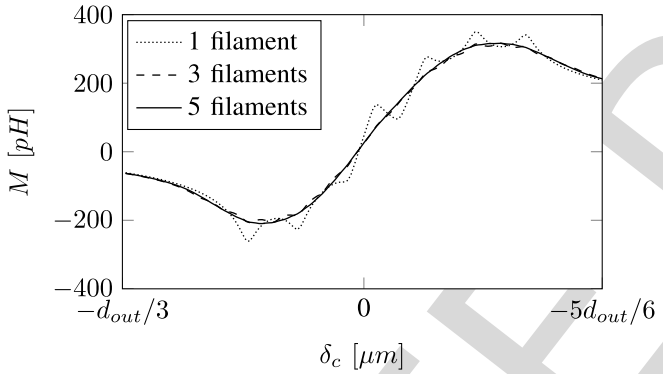


Fig. 3. Evaluated mutual inductance using the proposed model with one, three, and five filaments, respectively. Increasing the number of filaments improves the accuracy, but the improvement diminishes for more than five filaments.

in Matlab [27]. Magnetostatic FEM simulations of the same structure performed with Ansys Maxwell are used as a baseline for comparison with the analytic model.

To quantify the mutual inductance between the PDN and the inductor, the setup depicted in Figure 2 is utilised. The length of the interconnect is denoted as l_{PDN}. Distance δ_c denotes the spatial separation between the geometric centre of the inductor C_1 and the geometric centre of the interconnect loop. The topmost metal layers of a commercial 0.35 μm [28] process node are assumed for the inductor and the PDN wires. Without loss of generality, the 0.35 μm process is utilised as a common choice for sensor arrays [28], [29] and analog circuits. Moreover, fabrication of inductive links has been demonstrated in this process node [30]. Nevertheless, the proposed model is not limited to this technology, as discussed in the following paragraphs.

For the evaluation of the mutual inductance, a number of filaments is assumed that results in an accurate model.

TABLE I
VERIFICATION OF MUTUAL INDUCTANCE MODEL IN AMS 0.35 μm [28]

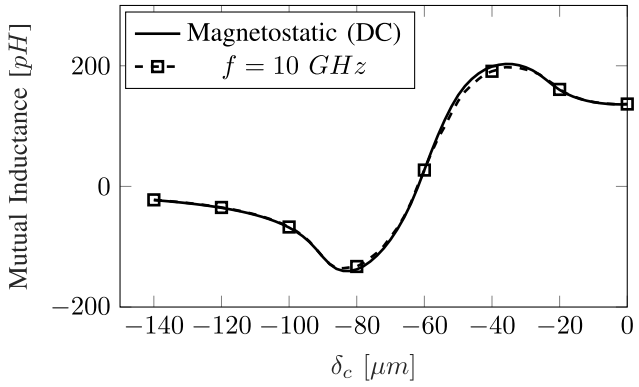
Geometry		0.35 μm				
d_{out}	[μm]	50	100	200	300	400
n	[−]	6	4	5 − 7	5 − 7	6
w_{ind}	[μm]	3 − 5	5 − 7	7 − 9	9 − 11	9 − 11
w_{PDN}	[μm]	7 − 10				8 − 12
l_{PDN}	[μm]	100 − 400				200 − 500
s_{PDN}	[μm]	20 − 50				50

The impact of the number of filaments to the evaluation of the mutual inductance is shown in Figure 3 for one, three, and five filaments denoted, respectively, with a dotted, a dashed, and a solid line. For a given length, l of each segment of the structure, increasing the width, w, of the trace requires an increased number of filaments to be modelled accurately. A length $l = 300\ \mu m$ and a width $w = 12\ \mu m$ are assumed in this example enhancing the impact of the number of filaments to the accuracy of the model. When a single filament is utilized the mutual inductance is not accurately modelled, rather it is crudely approximated due to the increased separation between the respective filaments in the y-axis in Figure 1. Increasing the density of the filaments reduces the error due to the physical dimensions of the structure. For the range of the design parameters assumed for the structure (see Table I), five filaments suffice to model the mutual inductance for this step of the methodology.

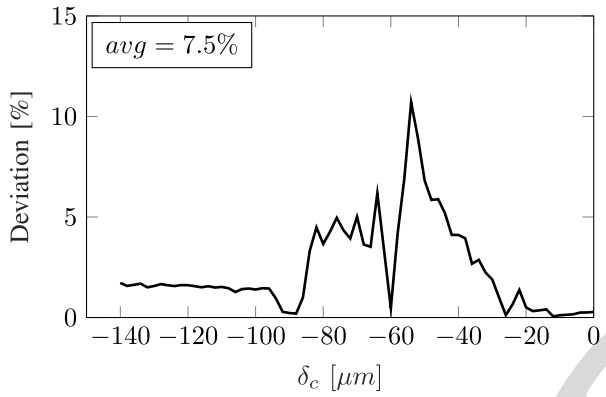
Furthermore, to demonstrate the small effect of the frequency on the mutual inductance evaluation, eddy-current simulations using Ansys Maxwell are performed at DC and at 10 GHz. An example in evaluating the mutual inductance without loss of generality is illustrated in Figure 4(a) for an on-chip inductor and a PDN loop, where $\delta_c = [-d_{out}, 0]$. The per cent difference in the mutual inductance between the magnetostatic and the high frequency simulation is shown in Figure 4(b). A maximum deviation of 10.7% is observed between the magnetostatic and frequency-dependent simulation at 10 GHz. Moreover, the deviation of the mutual inductance for the illustrated interval sweep is on average 7.5%, showing that the magnetostatic solution is reasonably accurate for the investigated frequency range.

The mutual inductance between the on-chip inductor and a PDN loop is shown in Figures 5(a) and 5(b) for two variants of the structure. A solid line is utilised for the analytic model, while a dashed line with squares is utilised for the Maxwell simulations, respectively. In Figure 5, an inductor with outer diameter $d_{out} = 200\ \mu m$ is used, with $w_{ind} = 7\ \mu m$ and $n = 5$ turns. The minimum spacing supported by the process node is chosen between the inductor turns. The PDN loop is $l_{PDN} = 300\ \mu m$ long, with spacing $s_{PDN} = 35\ \mu m$ between adjacent lines and width of $w_{PDN} = 10\ \mu m$. For the analytic model, five filaments are used since the accuracy of the model did not improve for more than five filaments.

For the second scenario, an inductor with outer diameter $d_{out} = 300\ \mu m$ is chosen with $w_{ind} = 5\ \mu m$ and four turns. The length of the PDN loop is $l_{PDN} = 400\ \mu m$, with $w_{PDN} = 5\ \mu m$ and $s_{PDN} = 40\ \mu m$. Similarly, five



(a)



(b)

Fig. 4. (a) The mutual inductance simulated at DC (magnetostatic) and at 10 GHz and (b) the deviation between the mutual inductance at magnetostatic and at 10 GHz.

filaments are used for the analytic evaluation. For each case, the per cent error compared to Maxwell simulations is, respectively, depicted in Figures 6(b) and 7(b). The deviation of the analytic model reaches 7.5% with respect to the Maxwell simulation. The error between the two methods is evaluated as

$$\text{error} = \frac{|M_{maxwell} - M_{analytic}|}{|M_{maxwell}|}. \quad (6)$$

The error graph presents a discontinuity, illustrated as a spike. This discontinuity is due to the change in sign in the value of the mutual inductance and the small value of the denominator in (6) at the relative locations where the mutual inductance is almost cancelled ($\pm d_{out}/2 + s_{PDN}/2$). Therefore, the abrupt increase in the error is a numerical pitfall of the error function and this particular discontinuity can be safely ignored. Moreover, at the spatial location of the discontinuity the mutual inductance and, therefore, the crosstalk noise are reduced to a minimum, and, consequently, the potential effect of this increase in error is further decreased.

The accuracy of the proposed model is also checked across several design parameters of the on-chip inductor and the PDN as listed in the first column of Table I. The investigated range for each of these parameters is listed in columns two to six of Table I. In Table I, the parameters chosen to verify the model are typical design parameters for inductive links. The parameters concerning the length of the interconnect structures

TABLE II
SPEEDUP GAIN THROUGH ANALYTIC EVALUATION

Design Parameters $\{d_{out}, l_{PDN}\}$	Time		Speedup
	Maxwell	Analytical	
$\{200\ \mu m, 300\ \mu m\}$	$7h22m$	$0.75\ s$	$\times 35,466$
$\{300\ \mu m, 400\ \mu m\}$	$11h9m$	$0.66\ s$	$\times 60,867$

and specifically d_{out}, l_{PDN}, and s_{PDN} significantly affect the mutual inductance between the on-chip inductor and the PDN. Alternatively, the trace widths, w_{ind} and w_{PDN} affect less the mutual inductance and, thus, can be considered as second order parameters. The number of turns, n, does not have an immediate effect on the evaluation of the mutual inductance, rather defines the total number of conductors included in the evaluation. The range of each parameter is chosen according to figures reported in literature relating to inductive links.

The AMS 0.35 μm [28] process is used throughout the simulations. Furthermore, simulations at UMC 0.18 μm and 65 nm [31] commercial processes are performed, demonstrating the applicability of the model across process nodes. A variety of geometries is covered with these scenarios, including a PDN loop shorter than the outer diameter of the inductor, a variety of PDN and inductor trace widths, and PDN loop widths. Overall, the accuracy of the model is within 10% of the simulations, constantly exhibiting a reasonable accuracy for all of the investigated technologies and geometries.

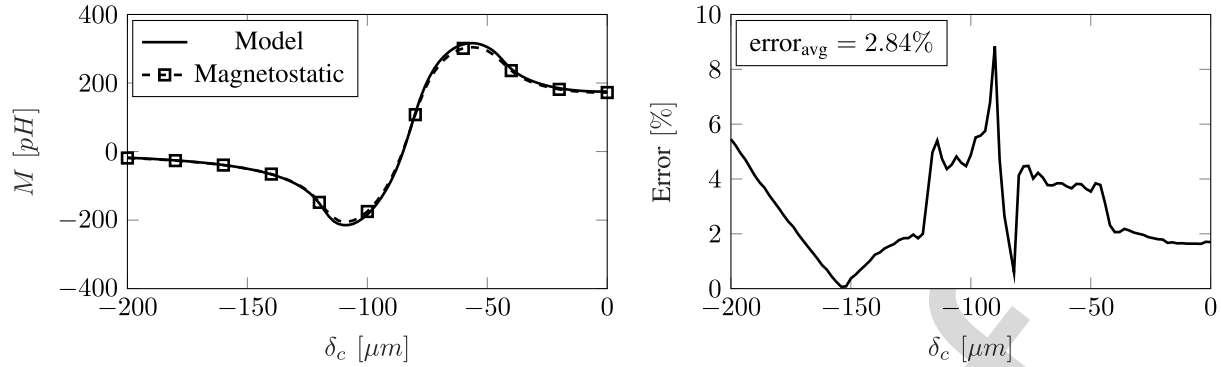
C. Performance of Analytic Modelling

The use of an analytic method to evaluate the mutual inductance exhibits specific advantages, such as faster and easily parametrised noise extraction, as discussed in this subsection. Speedup figures are reported for the evaluation of the mutual inductance between the proposed model and magnetostatic simulations. Moreover, improved insight on the behaviour of the noise is offered.

The simulation time for the evaluation of the mutual inductance with the analytic model and the electromagnetic solver (EM solver) is listed in Table II. All simulations are performed on a quad-core Intel® Core™ i7–6700HQ [32] processor with 16 GB of RAM. The two geometries considered in subsection II-B (simulation results shown in Figures 5 and 6) are used for this scenario.

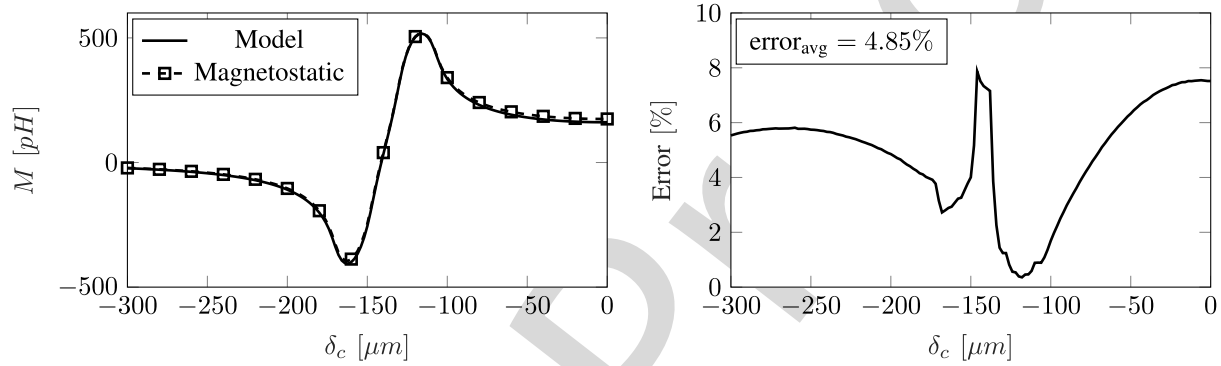
The speedup gained by the closed-form model is significant, compared to the full-wave simulation. An electromagnetic simulation is required for each position of the PDN loop in the vicinity of the on-chip inductor. Consequently, the number of simulations depends upon the step increment of δ_c, and therefore, the simulation time directly correlates to the size of the investigated structure and the granularity chosen for the sweep of δ_c between 0 and $-d_{out}$. A step of 2 μm is chosen in all simulations to model the crosstalk with adequate precision.

Alternatively, in Figure 7, the relation between the error induced by increasing the spatial step and the equivalent speedup are illustrated. The left y-axis is the departure in the maximum mutual inductance (and consequently maximum noise) as the granularity of the simulation decreases.



(a) (b)

Fig. 5. (a) The mutual inductance between an on-chip inductor with $d_{out} = 200\ \mu m$ and a PDN loop with $l_{PDN} = 300\ \mu m$ evaluated with the analytic model and magnetostatic simulations and (b) the per cent error between the analytic evaluation and the magnetostatic simulation.



(a) (b)

Fig. 6. (a) The mutual inductance between an on-chip inductor with $d_{out} = 300\ \mu m$ and a PDN loop with $l_{PDN} = 400\ \mu m$ evaluated with the analytic model and magnetostatic simulations and (b) the per cent error between the analytic evaluation and the magnetostatic simulation.

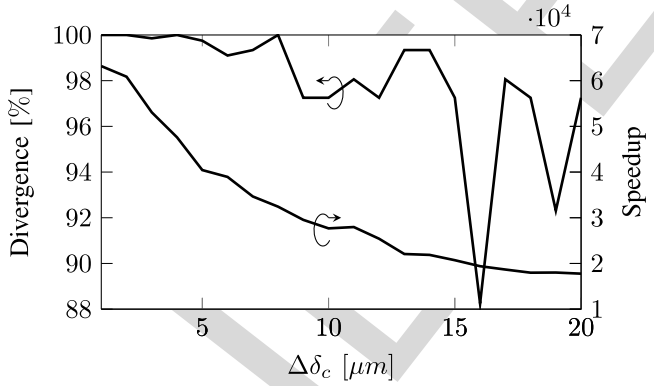


Fig. 7. On the left axis, the per cent divergence from the maximum value of the mutual inductance between the on-chip inductor and the PDN is illustrated for a coarser granularity. On the right axis, the equivalent speedup gained using the proposed methodology is shown.

Alternatively, the speedup is depicted on the right y-axis. Despite a significant reduction in the speedup as the granularity decreases, the execution time of the proposed methodology is four orders of magnitude faster, providing an effective alternative. Moreover, the value of maximum mutual inductance and the position where the mutual inductance is minimum cannot be captured for a step size of more than 10 μm, as the error increases significantly (in this case 12%). Alternatively, the analytic model offers a fast and accurate means to determine these quantities.

Additionally to gains in accuracy and computational time, the proposed methodology offers better insight on the crosstalk noise effects. Using the mutual inductance between the two structures, a methodology for the accurate evaluation of the crosstalk noise effect is proposed. A transfer function of the compact circuit model (see Figure 8) is determined, allowing an analytic or SPICE evaluation of the crosstalk noise. The frequency and other attributes of the noise are characterised, as shown in Section III.

III. Crosstalk Noise Circuit Model

In this section, the second stage of the proposed methodology to evaluate the crosstalk noise originating from the inductive link is presented. Advanced design methods and CAD tools for the power distribution network provision for the IR drop noise and the transient, high frequency voltage drop $L\frac{di}{dt}$ [33]–[35]. Nevertheless, traditional PDN design does not cope with the additional noise, originating from the on-chip inductors utilised for contactless inter-tier communication. In Figure 8, the crosstalk effect due to coupling to the

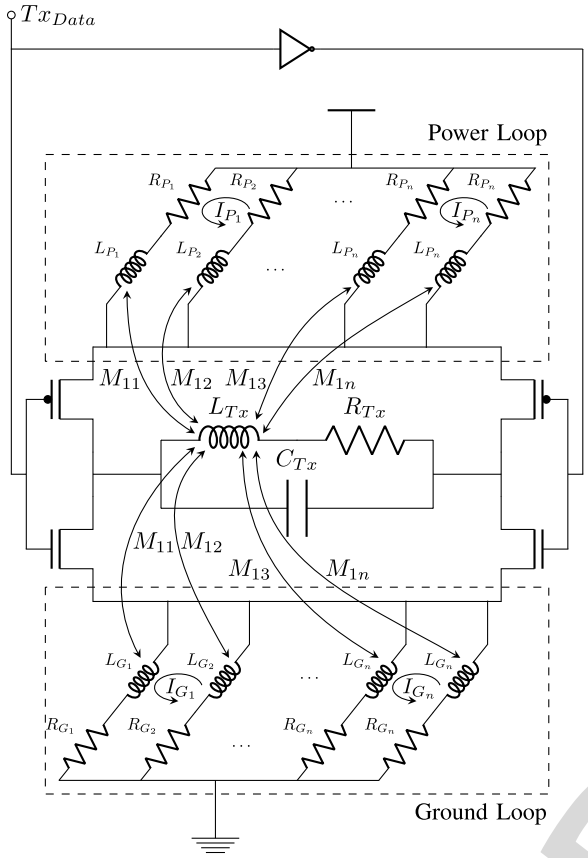


Fig. 8. A compact circuit model of an H-Bridge transmitter driving an on-chip inductor including the coupling between the on-chip inductor with the power and ground networks.

on-chip inductors is illustrated. P and G denote power and ground wires, respectively. L_{Pn} and L_{Gn} are the partial self-inductances of the power and ground interconnect wire, respectively. Equivalently, R_{Pn} and R_{Gn} are the respective wire resistances. Mij denotes the partial mutual inductance between the on-chip inductor with self-inductance L_{Tx} and each segment of the PDN. Due to the symmetry between the power and ground PDN wires, the mutual inductance is assumed to be equal. The parasitic resistance and capacitance of the on-chip inductor is illustrated as R_{Tx} and C_{Tx}, respectively. The on-chip inductor, usually placed on the topmost and thickest metal layer to reduce the wire resistance, is in the vicinity of the power network.

The amplitude of the induced current on the PDN depends upon the geometric and electrical characteristics of the closed path which alter the coupling between the inductor and the PDN loop. Depending upon the current flowing through the on-chip inductor, crosstalk noise is induced on the power distribution network (within the same tier) potentially deteriorating the power integrity of the circuit and reducing the robustness of the system. In inductive links, large currents (on the order of milliAmperes [7], [13], [30]) flow through the inductor during inter-tier communication and, consequently, the crosstalk noise effect is significant as demonstrated in this section.

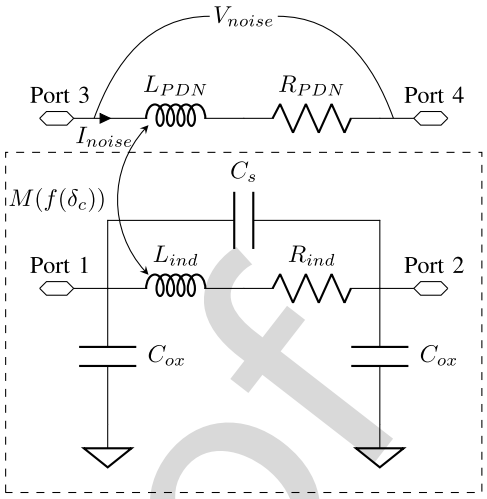


Fig. 9. Compact circuit model for the evaluation of the crosstalk noise due to the on-chip inductor.

The noise effects evaluated with Cadence® Spectre® [36] using SPICE simulations are presented in subsection III-A. The effect of frequency on the interconnect resistance is considered, yielding a frequency-dependent noise model. The speedup and accuracy of the proposed method compared to full-wave electromagnetic simulations with Ansys HFSS [37] are described in subsection III-B to demonstrate the validity of the model compared to this commercial tool. Moreover, the impact of substrate resistivity on the induced crosstalk noise is investigated in subsection III-C.

A. Frequency-Dependent Noise Evaluation

A circuit model for the high frequency crosstalk noise is depicted in Figure 9. For any given PDN loop in the vicinity of the on-chip inductor, the transimpedance of the inductor-PDN circuit is given by

$$\frac{V_{ind}}{I_{noise}} = \frac{Z_{11}Z_{22} + \omega^2 M^2}{j\omega M}, \tag{7}$$

where Z_{11} is the self impedance of the inductor and Z_{22} is the self impedance of the PDN loop. Furthermore, M is the mutual inductance between the on-chip inductor and the PDN loop.

The self impedance of the inductor is,

$$Z_{11} = \frac{R_s + j(\omega L_{ind} - \omega R_s^2 C_s - \omega^3 L_{ind}^2 C_s)}{1 - \omega^2(2L_{ind}C_s - R_s^2 C_s^2) + \omega^4 L_{ind}^2 C_s^2}, \tag{8}$$

where R_s is the frequency-dependent resistance, L_{ind} is the self-inductance, C_s is the series capacitance, and C_{ox} is the oxide capacitance of the on-chip inductor. For the PDN loop,

$$Z_{22} = R_{PDN} + j\omega L_{PDN}, \tag{9}$$

where L_{PDN} and R_{PDN} are the self inductance and the frequency-dependent resistance of the PDN loop, respectively.

To spatially model the aggregate noise on the PDN loop, the mutual inductance and, consequently, the current induced on the PDN loop is described as a function of the relative position to the inductor. Consequently, the accumulated noise

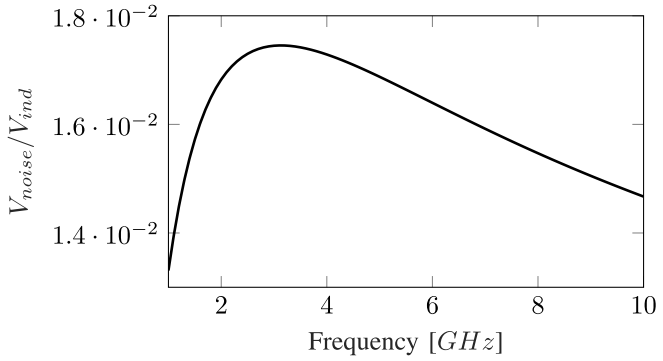


Fig. 10. Frequency response of the crosstalk noise for the circuit model in Figure 9.

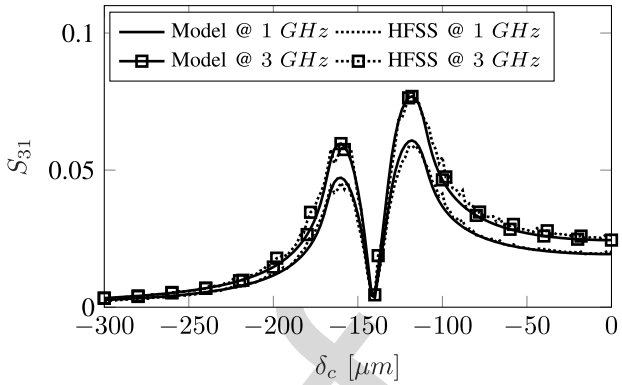


Fig. 11. Voltage gain scattering parameter S_{31} between the on-chip inductor and a PDN loop.

due to the on-chip inductor is both frequency and spatially dependent.

The frequency response of the induced noise is illustrated in Figure 10. The case where $l_{PDN} = 300\ \mu m$ and $d_{out} = 400\ \mu m$ is used for this simulation. For the evaluation of the resistance of both the inductor and the PDN, a frequency-dependent model is utilised, considering the skin effect of the wires. Furthermore, the inductance of the inductor is evaluated using the Greenhouse formula [38],

$$L_{ind} = \frac{\mu}{2} g_1 n^2 d_{avg} f(p), \tag{10}$$

where

$$f(p) = \ln(\frac{g_2}{p}) + g_3 p + g_4 p^2, \tag{11}$$

p is the fill factor $((d_{in} - d_{out})/(d_{in} + d_{out}))$, n is the number of turns, and d_{avg} is the average diameter $(0.5(d_{in} + d_{out}))$. For a rectangular inductor, the coefficients g_i are

$$[g_1\ g_2\ g_3\ g_4] = [1.27\ 2.07\ 0.18\ 0.13]. \tag{12}$$

The inductance of the PDN loop is determined by closed-form expressions for the self inductance of rectangular conductors [23]

$$L_{PDN} = \frac{0.002}{3w^2}\Big[3w^2 l \ln \frac{l + \sqrt{l^2 + w^2}}{w} - (l^2 + w^2)^{3/2} + 3wl^2 \ln \frac{w + \sqrt{l^2 + w^2}}{l} + l^3 + w^3\Big], \tag{13}$$

where l is equal to the length of each segment of the PDN, l_{PDN} and w is the trace width of the PDN, w_{PDN}. The self and oxide capacitance of the on-chip inductor are determined by [39]

$$C_s = n w_{PDN}^2 \frac{\epsilon_{ILD}}{t_{ILD}}, \tag{14}$$

and [40]

$$C_{ox} = \frac{1}{2}\big(C_A + C_P\big), \tag{15}$$

respectively. In (14), n is the number of turns, ϵ_{ILD} is the relative permittivity of the inter-layer dielectric, and t_{ILD} is the thickness of the inter-layer dielectric surrounding the metal layers of the inductor. In (15), C_A is the parasitic capacitance formed between the inductor and the substrate, while C_P is the fringe capacitance between the periphery of the inductor and the substrate.

The coupled inductor-PDN structure behaves as a band-pass filter, with a resonance frequency identical to the resonance of the on-chip inductor since the PDN capacitance is not considered, while the inductance of the PDN negligibly alters the resonance frequency. The operating frequency of the inductive link is the primary factor that determines the magnitude of the induced noise. The effect peaks near the resonance frequency, however, for frequencies farther away from the resonance frequency, the effect of the noise is gradually diminished. Note that this inductor model does not include the effect of the substrate impedance on the performance of the inductor. Nevertheless, any enhanced model can be utilised to consider this effect.

B. Validation of Noise Effects

To validate the crosstalk evaluation methodology, HFSS and SpectreRF simulations are performed on the inductor-PDN structure used in subsection III-A in Figure 9. Both the analytic method and full-wave simulations are performed on an eight-core Intel® Xeon® E5–2640 v2 [41] processor with 32 GB of RAM. Using the inductor model highlighted by a dashed rectangle, the resistive and capacitive parasitic effects of the on-chip inductor are adequately modelled without complicating the evaluation process. However, the proposed methodology can be equally effective with any on-chip inductor model, since the evaluation of the mutual inductance is independent from the circuit model of the inductor and can be integrated with more accurate on-chip inductor circuit models. Nevertheless, comparing on-chip spiral inductor models is beyond the scope of this paper. Scattering parameter simulations are performed for frequencies between 1 GHz and 10 GHz, covering a broad spectrum of frequencies usually encountered in inductive link applications [13], [30], [42].

The behaviour of the noise for $|\delta_c| = [0, d_{out}]$ is depicted in Figure 11. The voltage gain S_{31} is illustrated for a frequency of 1 GHz and for the resonance frequency of 3 GHz, notated by square markers. The solid and dotted lines denote, respectively, the SpectreRF simulations obtained using the proposed methodology and the full-wave simulations.

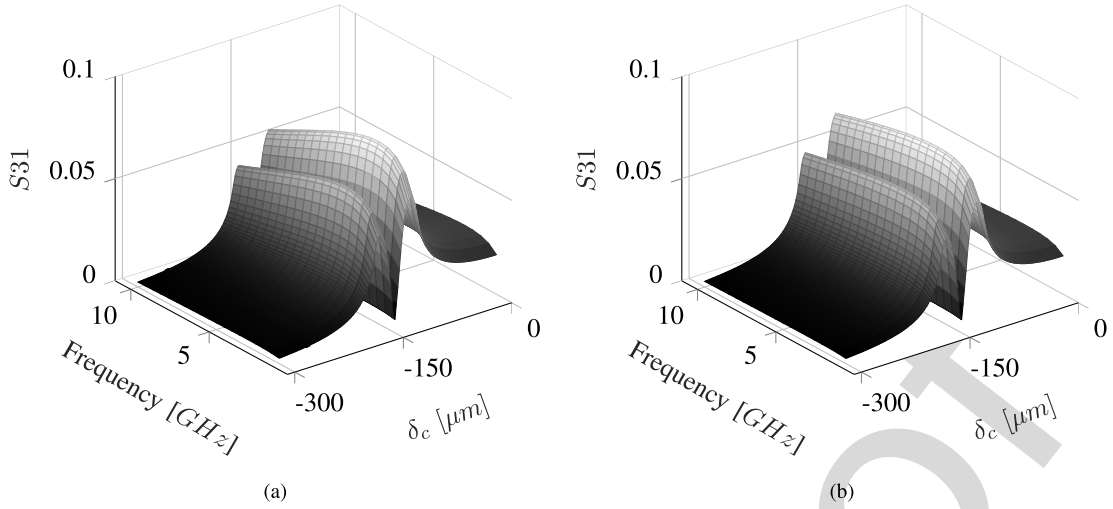


Fig. 12. Induced crosstalk noise as a function of the frequency and the spatial separation δ_c where (a) is a low resistivity (0.01 $\Omega \cdot cm$) and (b) a high resistivity (30 $\Omega \cdot cm$) substrate, respectively.

A very good fit is observed between the full-wave simulations and the proposed methodology. The average error for transmitting a signal at 1 GHz is 5.19% while at 3 GHz is 6.14%. As the frequency increases, a small decrease in accuracy is observed due to the use of the magnetostatic mutual inductance (as discussed in subsection II-A). Nevertheless, the decrease is not significant to require a re-evaluation of the mutual inductance between the investigated structures, as mentioned in subsection II-A. Note that the full-wave simulation generates artefacts in the solution due to parasitic capacitances that cannot be analytically evaluated, thus contributing to the per cent error between the two approaches.

Moreover, a notable difference is observed in the simulation time between the two approaches. Specifically, the run time of the full-wave simulation is 445 min, while the same simulation is performed within 94 min in SpectreRF, a speedup of 4.7×. No parallelisation techniques have been used for the evaluation of the presented methodology in SpectreRF. Alternatively, four full-wave simulations run in parallel to improve the simulation time and efficiently allocate the existing computing resources for solving the full-wave simulations. Consequently, the computational gains offered by the proposed method are effectively greater.

C. Impact of Silicon Substrate on Crosstalk Noise

For near field inductive communication high resistivity substrates are preferred to exploit the lower attenuation through the substrate [11]. Consequently, the coupling between the on-chip inductors in each tier is negligibly affected by substrate losses. In this subsection, the effect of the substrate resistivity on the noise induced by inductive links on the PDN is investigated.

To model the resistive losses of the substrate, the compact circuit model in Figure 9 is adapted, where a resistor R_{sub} is added in series to the oxide capacitance C_{ox} [39]. To effectively capture how the induced noise is affected, two substrate resistivities are chosen based on a broad range of available doping densities for P^+ substrates. Namely, a low resistivity 0.01 $\Omega \cdot cm$ and a high resistivity 30 $\Omega \cdot cm$ substrate [43] are, respectively, assumed. The impedance characteristics of the spiral inductor are, in this case, extracted from full-wave simulations for the investigated substrate resistivities.

The behaviour of the crosstalk noise due to the variation in the substrate resistivity is illustrated in Figure 12. The effect of the low and high resistivities for the substrate are depicted in Figures 12(a) and 12(b), equivalently. The behaviour of the noise can be subdivided into two distinct effects, the effect on the separation distance δ_c and the effect on the frequency response of the inductor. As expected, the change in the substrate resistivity did not alter the spatial behaviour of the noise across δ_c. Nevertheless, a significant divergence is observed for the on-chip inductor frequency response (and therefore the crosstalk noise) between the considered substrates due to the different losses of the inductor into the silicon substrate. Therefore, even though the monotonic behaviour of the frequency response is not altered (increases before the resonance frequency — decreases after), the slope of the frequency response differs.

Since the spatial behaviour of the noise is not affected by the substrate resistivity, the position of maximum noise is chosen for the validation of the model. A 3-D model of the investigated structure is designed and simulated with the Keysight Advanced Design System (ADS) FEM Electromagnetic Simulator [44]. The results produced with ADS are illustrated in Figure 13 in comparison to the model results simulated with Cadence Spectre. A good fit is observed between the two approaches with a maximum deviation within 7%, thus verifying the accuracy of the presented results.

Due to the reduced losses of the spiral inductor into the substrate, the high resistivity substrate leads to a significant increase in the coupling with the adjacent interconnects, thereby confirming the hypothesis of increased inter-tier coupling through high resistivity substrates. To efficiently illustrate this increase in the crosstalk noise, the per cent difference between the crosstalk noise in the considered substrates

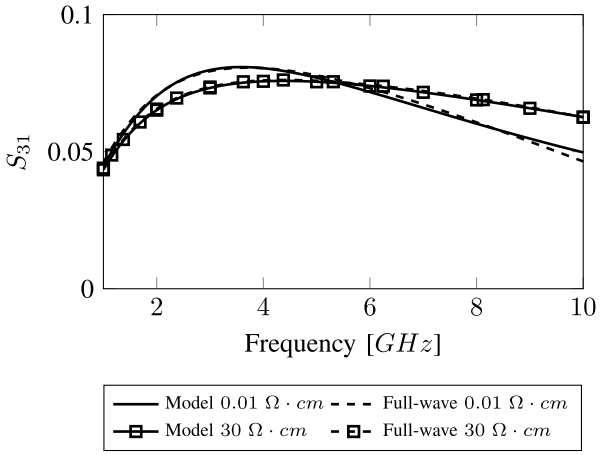


Fig. 13. Full-wave and analytical evaluation of the crosstalk noise on the PDN versus the investigated frequency spectrum for the position of maximum noise.

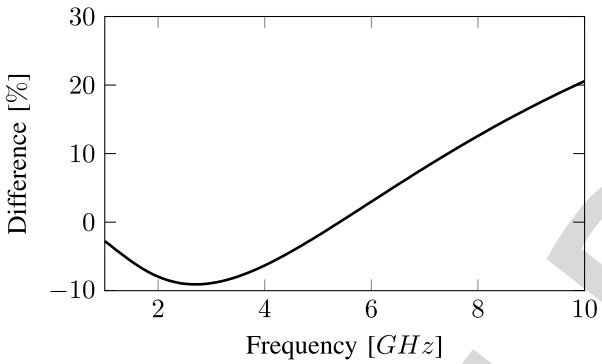


Fig. 14. The per cent difference of the induced crosstalk noise between a high and a low resistivity substrate for the position of maximum noise.

is depicted in Figure 14. In higher frequencies, where the substrate effect is more pronounced, the noise increases by 20%.

Alternatively, a dip (less than 10%) in the crosstalk noise is observed below the resonance frequency. Due to the increased resistivity of the substrate, a small decrease in the effective self-inductance of the spiral inductor is also observed [45]. Moreover, in low frequencies, the oxide capacitance C_{ox} behaves as an open circuit effectively cutting-off the path to R_{sub}. Consequently, in low frequencies where the eddy current losses are small, the efficiency of the on-chip inductor on the low resistivity substrate is superior compared to that on the high resistivity substrate. Thus, a higher coupling with the interconnects is noticed slightly increasing the crosstalk noise compared to the high resistivity substrate. As the frequency increases, however, the losses in the substrate dominate the overall effect and the noise for the low resistivity substrate is significantly lower.

IV. Case Study

The applicability of the proposed methodology is demonstrated in this section through a case study. For this case study, a single ended transmitter is assumed to drive the

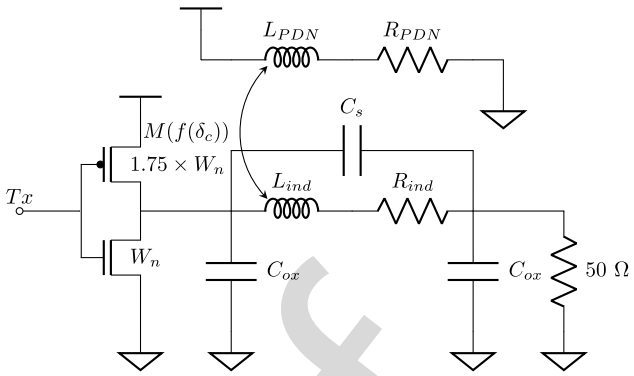


Fig. 15. Compact circuit model illustrating a single ended transmitter driving the on-chip inductor and the coupled PDN loop.

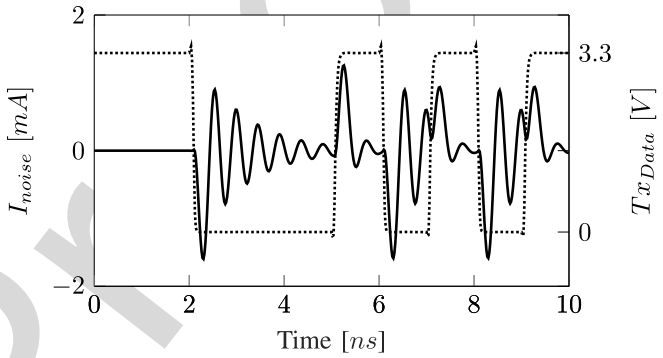


Fig. 16. Transient simulation illustrating the transmitted data through the inductive link and the corresponding induced noise on the PDN loop.

on-chip inductor. A transient analysis is performed illustrating the temporal noise characteristics given the single ended transmitter for the on-chip inductor.

Additionally to the frequency characteristics of the induced noise presented in Section III, the methodology proposed in this paper is utilised to determine the temporal behaviour of noise. To perform a transient simulation of noise, specific assumptions are made considering the driving circuit of the inductor and the utilised signal encoding.

The simulation setup for the transient analysis is illustrated in Figure 15. A single ended transmitter is chosen as the simplest circuit driving an inductive link. The second terminal of the inductor is terminated to ground with a 50 Ω resistor. Non-return to zero encoding is assumed as the communication scheme for the inductive link. The width W_n is treated as a parameter in the following analysis with a typical size of $W_n = 5\ \mu m$. Note, however, that this width exclusively serves this case study and can be accurately determined only if the full specification of the entire system, such as the outer diameter of the coupled inductors and the separation distance, are known. Therefore, this choice of W_n should not be generalised.

The transient analysis of the induced noise is depicted in Figure 16. For this analysis, a 1 $Gbps$ random bitstream is utilised as the transmitted data Tx. The induced current I_{noise} appears as a damped positive sinusoidal pulse for transitions

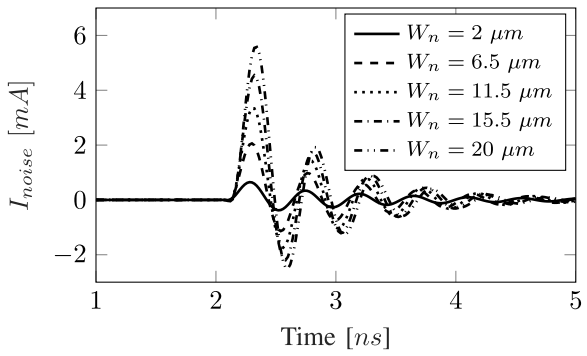


Fig. 17. Transient simulation illustrating the transmitted data for increasing device width W_n.

from logic zero to one and as a damped negative sinusoidal pulse for the opposite transition. The ringing oscillation of the noise is dampened within 3 ns, not fast enough for a data signal of 1 $Gbps$. Due to the high frequency characteristics of the induced current, the frequency-dependent LdI_{noise}/dt component of the aggregate noise of the PDN loop cannot be ommited. Therefore, the induced noise can be considered as an additional component of the high frequency on-chip Ldi/dt noise developed on the power distribution network.

The strength of the driving devices depends upon several design specifications of the inductive link. To visualise the impact of the driving strength of the transmitter circuit on the induced noise, the width of the transistors is swept from 2 μm up to 20 μm. The simulation results are depicted in Figure 17. As expected, increasing the device strength results in an increased magnitude for the induced current I_{noise}. Nevertheless, the phase and frequency of the noise are not affected by altering W_n.

V. Conclusion

A frequency-dependent model that accurately determines the effect of crosstalk noise from inductive links on the power distribution network is presented. The model is constructed in two stages. In the first stage, the mutual inductance between the power distribution network and the inductor is analytically determined. For the evaluation of the mutual inductance, a speedup on the order of magnitude 10^4 is achieved, while the accuracy is within 10% of the magnetostatic solution with Ansys Maxwell. A SPICE model is constructed in the second stage to determine the frequency-dependent noise yielding an $\sim 5\times$ speedup as compared to S-parameter noise extraction with HFSS simulations. This model can guide the design process of the PDN to avoid or limit undesirable crosstalk noise from the on-chip inductors. In this way, the robustness of the PDN does not degrade and the power integrity of contactless systems is improved.

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Efficient Modeling of Crosstalk Noise on Power Distribution Networks for Contactless 3-D ICs

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***Abstract*— An efficient and frequency-dependent model describing the crosstalk noise on power distribution networks due to inductive links in contactless 3-D ICs is presented. A two-step approach is followed to model the crosstalk effect. During the first step, the mutual inductance between the power distribution network and the inductive link is analytically determined. Due to the weak dependence of mutual inductance to frequency, a magnetostatic model is proposed for this step. The model includes the physical and electrical characteristics of both the on-chip inductor and the wires of the power distribution network. In this way, different power network topologies can be modeled facilitating noise analysis in the vicinity of the on-chip inductor. This approach is justified by the typical use of regular power network topologies in modern integrated circuits. In the second stage, the noise is assessed with SPICE simulations, considering the mutual inductance between the two structures from the first step and the resistance variations due to high frequency effects. Thus, an efficient, scalable, and accurate method for the analysis of the crosstalk effects due to inductive links is provided, without resorting on computationally expensive and time consuming full-wave simulations. Compared with the full-wave simulations, the induced noise is evaluated four orders of magnitude faster with the proposed model. The accuracy of the proposed model is within 10% of the respective noise computed with a commercial electromagnetics simulator using the finite element method. An analysis including the effect of substrate resistivity on the crosstalk noise is also presented.**

***Index Terms*— Mutual inductance, crosstalk noise, inductive links, power distribution networks, high frequency, contactless 3-D systems.**

I. Introduction

THREE-DIMENSIONAL integration is a promising technology providing multi-functional, high performance, and low power electronics [1]. Especially heterogeneous 3-D ICs, are predicted, according to ITRS, to be a potential solution for the many challenges encountered by the Mobile and IoT markets [2]. The wider uptake and commercialisation of 3-D ICs, however, requires effective inter-tier communication. Several approaches are considered for inter-tier communication, with through silicon vias (TSV) being the most prominent. Alternatively, contactless solutions have emerged, based on either inductive or capacitive coupling [3]–[7].

Despite their inherent simplicity, TSV entail an overhead in cost due to the related manufacturing complexity and possibly low yield [8]–[10]. For example, to alleviate the impact of copper pumping due to the TSV, an additional high thermal annealing process is required, increasing the manufacturing cost [9]. Several other reliability issues need to be considered, such as copper diffusion from the TSV to the substrate, mechanical stresses, and electromigration, each requiring additional processing steps. Furthermore, considerable substrate thinning is imperative for state-of-the-art TSV integration, where the TSV has a diameter of 5 μm or smaller. Consequently, a significant processing cost is incurred due to the handling of the thin wafers.

With contactless inter-tier communication, nevertheless, significant advantages exist for both homogeneous and heterogeneous 3-D ICs. Due to the versatility of the transceiver solutions, seamless integration can be achieved without using level shifters [11] or complicated design rules imposed by TSV. In addition, standard CMOS processes and methodologies are utilised maintaining overall a low processing cost and high manufacturing yield. Furthermore, unique benefits exist including die detachability [12]. Out of the two contactless schemes, nevertheless, capacitive coupling is limited to face-to-face implementations practically supporting only two tier systems, thereby significantly narrowing the scope of multi-tier integration. Consequently, inductive links are investigated in this paper.

High performance inductive links have been developed recently [5], [13], where the performance of inductive links is comparable to TSV interfaces when signal multiplexing is employed [6]. With wireless inter-tier communication, however, new challenges arise, including interference with components in the vicinity of the on-chip inductors. In wired 3-D approaches, the crosstalk noise is localised and often dominated by the capacitive coupling between adjacent interconnects [14]. Alternatively, due to the emission of the magnetic field in inductive based communication, crosstalk noise is a long range phenomenon and an important issue in the design process of inductive links that requires attention [15]. For these reasons, in addition to design methods, the crosstalk between neighbouring inductive links [12], [16] and the interference of adjacent interconnects on inductive links have both been explored [17]. Nevertheless, the effect of the inductive links on global interconnects and the power integrity of the system has

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yet to be fully investigated. Wireless communication through magnetic flux leads to parasitic coupling with nearby conductors, such as power distribution interconnects, which operate as accidental antennas. Subsequently, undesirable voltage fluctuations develop on the power distribution network (PDN), that can hinder power integrity and degrade the robustness of the system.

In [18] and [19], the crosstalk noise effects are explored for different power distribution network topologies and arrays of multiple inductors. For example, the noise caused by an inductive link array in a 65 nm process node can reach up to 320 mV (e.g. 26% of the nominal V_{DD}); though proper PDN placement can reduce the noise up to 70% [18]. Furthermore, the sensitivity of PDN topologies to noise depend upon the geometry of each topology [19]. These results demonstrate that noise due to inductive links affects the power distribution network, thereby compromising power integrity if ignored. Nevertheless, proper allocation of the PDN wires in the vicinity of the inductor mitigates the induced noise. Therefore, placement of the PDN in close proximity to the on-chip inductor is feasible, resulting in a small increase in the IR drop noise but mitigating the overall noise.

To determine the appropriate PDN placement for minimising the aggregate noise, the crosstalk noise should accurately be evaluated. This noise depends upon the relative position of the PDN and the on-chip inductors. The mutual inductance between the coupled structures is therefore required, which can be determined with electromagnetic simulations. However, full-wave electromagnetic simulations[1] cost in time and computing resources and typically are limited to a specific inductor-PDN structure. Additionally, simulating the investigated structures for each location of the PDN conductors in the vicinity of the inductor entails excessive delay in the design process. Furthermore, commercial IC design tools do not support inductance extraction for multi-tier systems and different process nodes. Thus, there is a lack of effective means to determine the vital mutual inductance for inductive-based 3-D ICs.

Based on these observations, the contributions of this paper are:

- A methodology to describe the induced crosstalk noise on on-chip interconnects without the need for full-wave electromagnetic simulations.
- A scalable, efficient, and accurate magnetostatic model for the evaluation of the mutual inductance as part of this methodology. The spatial position and geometry of the on-chip inductor and the topology of the nearby interconnects are considered for the evaluation of the mutual inductance.
- A SPICE-based noise model to rapidly and accurately evaluate the induced noise on the PDN.

The proposed model improves power integrity, without requiring excessive computational resources.

The remainder of this paper is organised as follows. A magnetostatic model for the evaluation of the mutual inductance between an on-chip inductor and the power distribution network is described in Section II. A methodology for the evaluation of the frequency-dependent induced noise is presented in Section III, verified with SPICE simulations. The proposed methodology is applied to a case study in Section IV, utilising the mutual inductance model of Section II. Some conclusions are drawn in Section V.

[1]In this paper, full-wave electromagnetic simulations are primarily performed with Ansys HFSS and the two terms are used interchangeably.

II. Analytic Mutual Inductance Modelling

A closed-form model for the evaluation of the mutual inductance between an on-chip inductor and a loop of the power distribution network is presented in this section. In subsection II-A, a magnetostatic model for the evaluation of the mutual inductance of the investigated structures is described. The accuracy of the proposed model is verified with the Ansys Maxwell [20] simulator in subsection II-B. The computational speedup over finite element methods (FEM) is presented in subsection II-C.

Two approaches to evaluate the mutual inductance between the two structures are compared. Magnetostatic simulations of the structure are performed in Ansys Maxwell [20] to extract the mutual inductance by directly solving the Maxwell equations with the FEM solver. Alternatively, the mutual inductance is evaluated with an analytic model utilising a set of closed-form expressions of elemental structures (e.g. the mutual inductance between two thin rectangular conductors) to describe complex geometries (e.g. an inductor and a PDN). After developing the analytic model, these two approaches are compared in terms of accuracy and speed.

A. Magnetostatic Mutual Inductance Evaluation

The analytic magnetostatic model for the evaluation of the mutual inductance is presented in this subsection. The geometry of the coupled structure composed of a power distribution network loop and the on-chip inductor is depicted in Figure 1(a). A square on-chip inductor geometry is utilised, although the model can also be adapted for octagonal inductors. The wires in grey colour denote the two conductors of a PDN loop, while the wires in white colour are the windings of the inductor. The PDN wires are assumed to be placed in any position across the y-axis, parallel to the inductor windings.

Assume a current density J_{ind} and the respective current I_{ind} flow through each of the inductor windings. The current flowing through the inductor generates a magnetic field that couples with the power distribution network wires in the vicinity. The magnetic flux that couples the two structures is given by

$$\Psi_{pdn} = \int_S \mathbf{B_{ind,pdn}} \cdot d\mathbf{S} \implies M_{ind,pdn} = \Psi_{pdn}/I_{ind}, \quad (1)$$

and, therefore, the mutual inductance between the inductor and the PDN is determined. The magnetic flux, Ψ which couples with the PDN, is proportional to the area of the loop formed by the PDN wire.

To simplify the evaluation of the mutual inductance without directly solving the integral in (1), the concept of partial inductance is utilised [21]. The closed path of the PDN

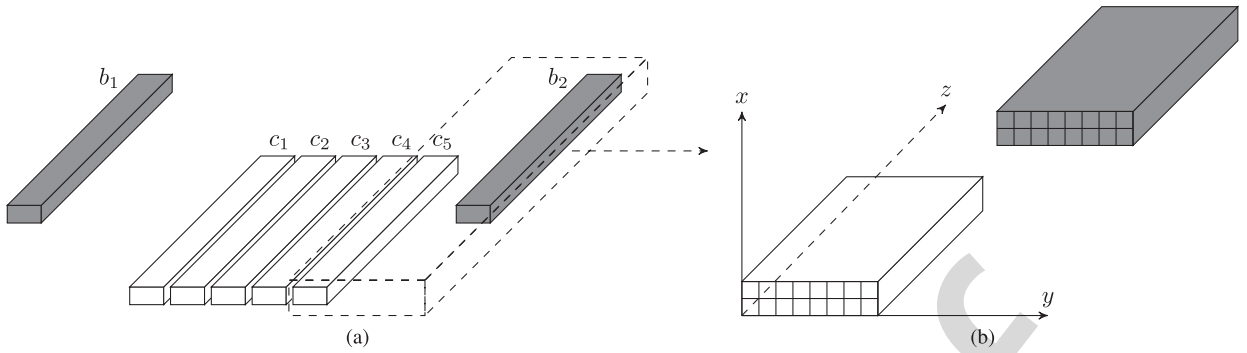


Fig. 1. (a) The segments of the windings of the inductor and the segments of a PDN loop in the vicinity of the inductor and (b) a detailed view of two segments, depicting the partition of the segments into filaments.

loop is segmented into n continuous segments b_i so that $b = b_1 \cup b_2 \cup \cdots \cup b_n$ where b is the PDN loop. Equivalently, the inductor is segmented into m partitions c_i, $c = c_1 \cup c_2 \cup \cdots \cup c_m$, where c is the inductor geometry. Each segment of the PDN or the inductor is a straight rectangular conductor of finite length, as seen in Figure 1(a). Based on this initial segmentation of the inductor-PDN structure, the problem of determining the mutual inductance is reduced to evaluating the mutual inductance for $n \times m$ segments, ignoring the perpendicular segments that evaluate to zero. The total mutual inductance between the two structures is given by the summation of the partial mutual inductances.

The mutual inductance between two filaments is extracted by Neumann's formula [22]. Solving Neumann's formula integral gives the mutual inductance closed-form expression [23]

$$M_{kl} = 10^{-5}\Big[z \ln\left(z + \sqrt{z^2+\rho^2}\right) - \sqrt{z^2+\rho^2}\Big]_{l_2+l_3-l_1,l_3}^{l_3-l_1,l_3+l_2}(z), \tag{2}$$

where z and ρ are the vertical and the cartesian distance between the two filaments, respectively, and

$$\Big[f(z)\Big]_{s_2,s_4}^{s_1,s_3}(z) = \sum_{i=1}^{4}(-1)^{k+1} f(s_i). \tag{3}$$

Expression (2) describing the mutual inductance is normalised to micrometers (μm) for the length and to nanoHenry (nH) for the inductance. The model can be parameterised by altering the s-matrix used in (3)

$$\begin{bmatrix} s_1 & s_3 \\ s_2 & s_4 \end{bmatrix} = \begin{bmatrix} l_3 - l_1 & l_3 + l_2 \\ l_2 + l_3 - l_1 & l_3 \end{bmatrix}. \tag{4}$$

In (4), l_1 is the length of the inductor segment, l_2 is the length of the PDN segment, and l_3 is the difference in length between the two filaments if projected on the z-axis as shown in Figure 1(b). Furthermore, the physical boundaries of the simulation are controlled by the variable

$$\rho = \sqrt{d^2 + t_{ild}^2}, \tag{5}$$

where d is the horizontal distance (y-axis) and t_{ild} is the vertical distance between the filaments (x-axis), respectively. The vertical distance between the filaments is equal to the inter-layer dielectric thickness and is a technology specific parameter.

The evaluation of the mutual inductance for the specific problem can also be performed with the expressions (8) or (14) from [23] that correspond to the mutual inductance between two thin tapes and the mutual inductance between mutual bars, respectively. Nevertheless, the use of filaments provides greater versatility for describing the investigated structure and, therefore, greater control of the accuracy of the simulation, as explained in the following paragraphs. Additionally, the method of rectangular bars suffers from numerical pitfalls as reported in [24].

A major advantage of utilising an arbitrary number of filaments to model rectangular conductors is the greater scalability for several physical parameters of the structure. For the method of filaments to provide sufficiently accurate results, the length l of each segment b_i (or c_i) is assumed to be much larger compared to the thickness, t, or width, w, of the particular wire, $l \gg t, w$. Since on-chip interconnect wires are utilised, this assumption is true for the thickness, t. However, the relation between the width, w, and the length, l, is not always straightforward. The number of filaments can, thus, be adjusted according to the relative size between the physical parameters of the structure to produce an accurate solution.

Another implication for the chosen evaluation method for the mutual inductance is scaling with frequency. Skin, proximity, and corner effects [25], [26] alter the current density of the conductor with increasing frequencies, leading to different results for the magnetostatic solution of the mutual inductance. However, due to the width and thickness of the integrated interconnects, the impact of high frequency effects on the mutual inductance is minimal for frequencies up to 10 GHz, well beyond the resonance frequencies of the inductors used for inductive links [4], [5]. Consequently, the magnetostatic solution of the mutual inductance is sufficient for this problem. Simulations supporting this assumption and verifying the accuracy of the model are demonstrated in the following subsection.

B. Model Verification

The accuracy of the proposed magnetostatic model is verified in this subsection. The analytic model is implemented

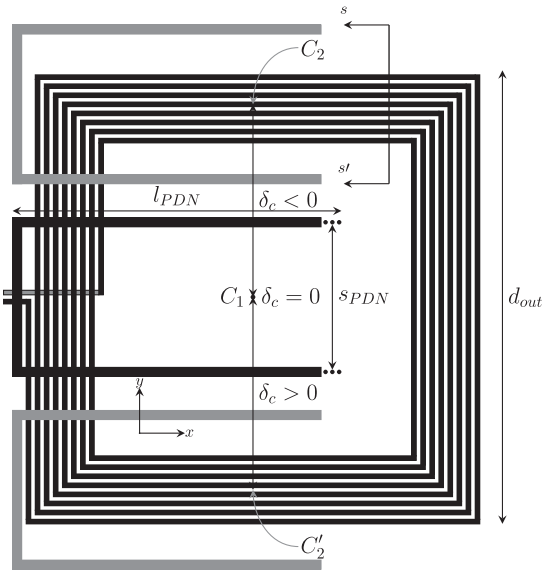


Fig. 2. Top view of the on-chip inductor with a PDN loop in its vicinity. The PDN loop is placed in three distinct positions where $\delta_c = 0\ \mu m$, $\delta_c = d_{out}/2\ \mu m$ (C_2), and $\delta_c = -d_{out}/2\ \mu m$ (C_2').

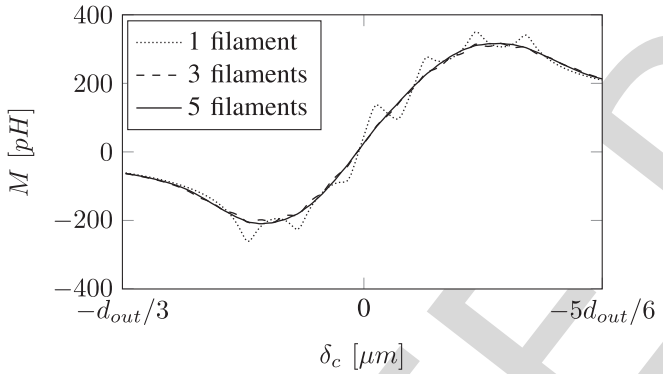


Fig. 3. Evaluated mutual inductance using the proposed model with one, three, and five filaments, respectively. Increasing the number of filaments improves the accuracy, but the improvement diminishes for more than five filaments.

in Matlab [27]. Magnetostatic FEM simulations of the same structure performed with Ansys Maxwell are used as a baseline for comparison with the analytic model.

To quantify the mutual inductance between the PDN and the inductor, the setup depicted in Figure 2 is utilised. The length of the interconnect is denoted as l_{PDN}. Distance δ_c denotes the spatial separation between the geometric centre of the inductor C_1 and the geometric centre of the interconnect loop. The topmost metal layers of a commercial 0.35 μm [28] process node are assumed for the inductor and the PDN wires. Without loss of generality, the 0.35 μm process is utilised as a common choice for sensor arrays [28], [29] and analog circuits. Moreover, fabrication of inductive links has been demonstrated in this process node [30]. Nevertheless, the proposed model is not limited to this technology, as discussed in the following paragraphs.

For the evaluation of the mutual inductance, a number of filaments is assumed that results in an accurate model.

TABLE I
VERIFICATION OF MUTUAL INDUCTANCE MODEL IN AMS 0.35 μm [28]

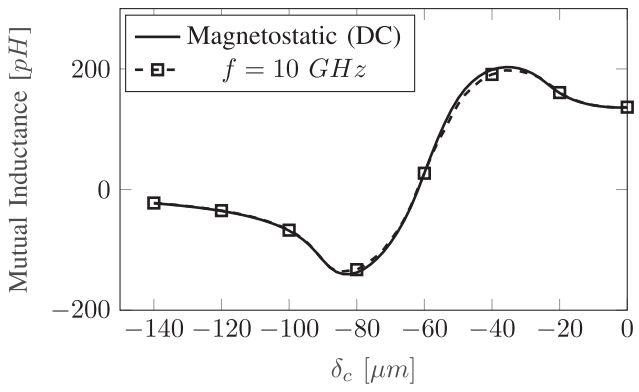
Geometry		0.35 μm				
d_{out}	[μm]	50	100	200	300	400
n	[−]	6	4	5 − 7	5 − 7	6
w_{ind}	[μm]	3 − 5	5 − 7	7 − 9	9 − 11	9 − 11
w_{PDN}	[μm]	7 − 10				8 − 12
l_{PDN}	[μm]	100 − 400				200 − 500
s_{PDN}	[μm]	20 − 50				50

The impact of the number of filaments to the evaluation of the mutual inductance is shown in Figure 3 for one, three, and five filaments denoted, respectively, with a dotted, a dashed, and a solid line. For a given length, l of each segment of the structure, increasing the width, w, of the trace requires an increased number of filaments to be modelled accurately. A length $l = 300\ \mu m$ and a width $w = 12\ \mu m$ are assumed in this example enhancing the impact of the number of filaments to the accuracy of the model. When a single filament is utilized the mutual inductance is not accurately modelled, rather it is crudely approximated due to the increased separation between the respective filaments in the y-axis in Figure 1. Increasing the density of the filaments reduces the error due to the physical dimensions of the structure. For the range of the design parameters assumed for the structure (see Table I), five filaments suffice to model the mutual inductance for this step of the methodology.

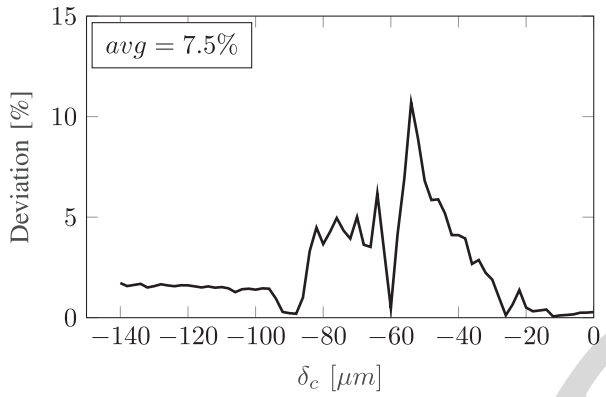
Furthermore, to demonstrate the small effect of the frequency on the mutual inductance evaluation, eddy-current simulations using Ansys Maxwell are performed at DC and at 10 GHz. An example in evaluating the mutual inductance without loss of generality is illustrated in Figure 4(a) for an on-chip inductor and a PDN loop, where $\delta_c = [-d_{out}, 0]$. The per cent difference in the mutual inductance between the magnetostatic and the high frequency simulation is shown in Figure 4(b). A maximum deviation of 10.7% is observed between the magnetostatic and frequency-dependent simulation at 10 GHz. Moreover, the deviation of the mutual inductance for the illustrated interval sweep is on average 7.5%, showing that the magnetostatic solution is reasonably accurate for the investigated frequency range.

The mutual inductance between the on-chip inductor and a PDN loop is shown in Figures 5(a) and 5(b) for two variants of the structure. A solid line is utilised for the analytic model, while a dashed line with squares is utilised for the Maxwell simulations, respectively. In Figure 5, an inductor with outer diameter $d_{out} = 200\ \mu m$ is used, with $w_{ind} = 7\ \mu m$ and $n = 5$ turns. The minimum spacing supported by the process node is chosen between the inductor turns. The PDN loop is $l_{PDN} = 300\ \mu m$ long, with spacing $s_{PDN} = 35\ \mu m$ between adjacent lines and width of $w_{PDN} = 10\ \mu m$. For the analytic model, five filaments are used since the accuracy of the model did not improve for more than five filaments.

For the second scenario, an inductor with outer diameter $d_{out} = 300\ \mu m$ is chosen with $w_{ind} = 5\ \mu m$ and four turns. The length of the PDN loop is $l_{PDN} = 400\ \mu m$, with $w_{PDN} = 5\ \mu m$ and $s_{PDN} = 40\ \mu m$. Similarly, five



(a)



(b)

Fig. 4. (a) The mutual inductance simulated at DC (magnetostatic) and at 10 GHz and (b) the deviation between the mutual inductance at magnetostatic and at 10 GHz.

filaments are used for the analytic evaluation. For each case, the per cent error compared to Maxwell simulations is, respectively, depicted in Figures 6(b) and 7(b). The deviation of the analytic model reaches 7.5% with respect to the Maxwell simulation. The error between the two methods is evaluated as

$$\text{error} = \frac{|M_{maxwell} - M_{analytic}|}{|M_{maxwell}|}. \quad (6)$$

The error graph presents a discontinuity, illustrated as a spike. This discontinuity is due to the change in sign in the value of the mutual inductance and the small value of the denominator in (6) at the relative locations where the mutual inductance is almost cancelled ($\pm d_{out}/2 + s_{PDN}/2$). Therefore, the abrupt increase in the error is a numerical pitfall of the error function and this particular discontinuity can be safely ignored. Moreover, at the spatial location of the discontinuity the mutual inductance and, therefore, the crosstalk noise are reduced to a minimum, and, consequently, the potential effect of this increase in error is further decreased.

The accuracy of the proposed model is also checked across several design parameters of the on-chip inductor and the PDN as listed in the first column of Table I. The investigated range for each of these parameters is listed in columns two to six of Table I. In Table I, the parameters chosen to verify the model are typical design parameters for inductive links. The parameters concerning the length of the interconnect structures

TABLE II
SPEEDUP GAIN THROUGH ANALYTIC EVALUATION

Design Parameters $\{d_{out}, l_{PDN}\}$	Time		Speedup
	Maxwell	Analytical	
$\{200\ \mu m, 300\ \mu m\}$	$7h22m$	$0.75\ s$	$\times 35,466$
$\{300\ \mu m, 400\ \mu m\}$	$11h9m$	$0.66\ s$	$\times 60,867$

and specifically d_{out}, l_{PDN}, and s_{PDN} significantly affect the mutual inductance between the on-chip inductor and the PDN. Alternatively, the trace widths, w_{ind} and w_{PDN} affect less the mutual inductance and, thus, can be considered as second order parameters. The number of turns, n, does not have an immediate effect on the evaluation of the mutual inductance, rather defines the total number of conductors included in the evaluation. The range of each parameter is chosen according to figures reported in literature relating to inductive links.

The AMS 0.35 μm [28] process is used throughout the simulations. Furthermore, simulations at UMC 0.18 μm and 65 nm [31] commercial processes are performed, demonstrating the applicability of the model across process nodes. A variety of geometries is covered with these scenarios, including a PDN loop shorter than the outer diameter of the inductor, a variety of PDN and inductor trace widths, and PDN loop widths. Overall, the accuracy of the model is within 10% of the simulations, constantly exhibiting a reasonable accuracy for all of the investigated technologies and geometries.

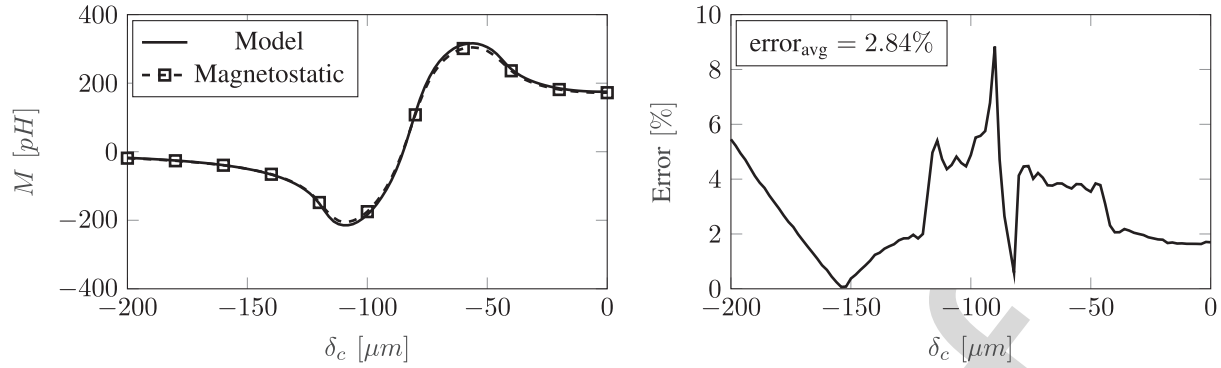
C. Performance of Analytic Modelling

The use of an analytic method to evaluate the mutual inductance exhibits specific advantages, such as faster and easily parametrised noise extraction, as discussed in this subsection. Speedup figures are reported for the evaluation of the mutual inductance between the proposed model and magnetostatic simulations. Moreover, improved insight on the behaviour of the noise is offered.

The simulation time for the evaluation of the mutual inductance with the analytic model and the electromagnetic solver (EM solver) is listed in Table II. All simulations are performed on a quad-core Intel® Core™ i7–6700HQ [32] processor with 16 GB of RAM. The two geometries considered in subsection II-B (simulation results shown in Figures 5 and 6) are used for this scenario.

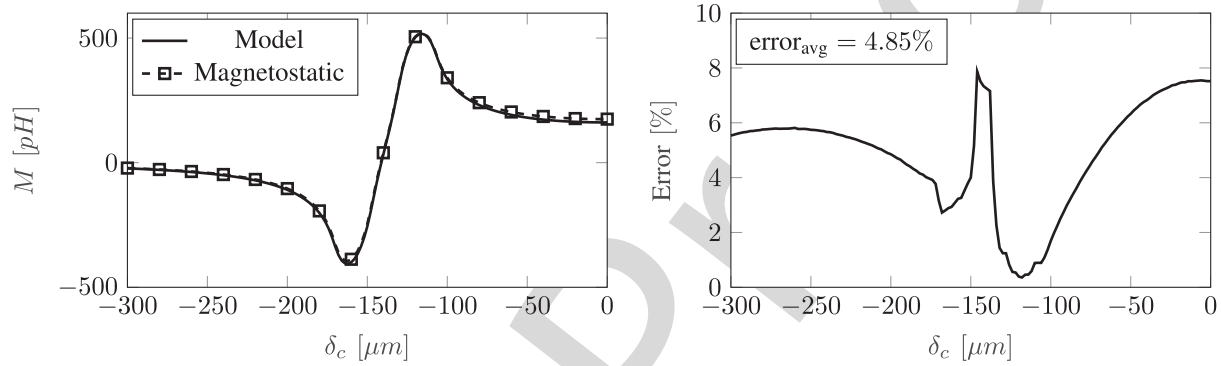
The speedup gained by the closed-form model is significant, compared to the full-wave simulation. An electromagnetic simulation is required for each position of the PDN loop in the vicinity of the on-chip inductor. Consequently, the number of simulations depends upon the step increment of δ_c, and therefore, the simulation time directly correlates to the size of the investigated structure and the granularity chosen for the sweep of δ_c between 0 and $-d_{out}$. A step of 2 μm is chosen in all simulations to model the crosstalk with adequate precision.

Alternatively, in Figure 7, the relation between the error induced by increasing the spatial step and the equivalent speedup are illustrated. The left y-axis is the departure in the maximum mutual inductance (and consequently maximum noise) as the granularity of the simulation decreases.



(a) (b)

Fig. 5. (a) The mutual inductance between an on-chip inductor with $d_{out} = 200\ \mu m$ and a PDN loop with $l_{PDN} = 300\ \mu m$ evaluated with the analytic model and magnetostatic simulations and (b) the per cent error between the analytic evaluation and the magnetostatic simulation.



(a) (b)

Fig. 6. (a) The mutual inductance between an on-chip inductor with $d_{out} = 300\ \mu m$ and a PDN loop with $l_{PDN} = 400\ \mu m$ evaluated with the analytic model and magnetostatic simulations and (b) the per cent error between the analytic evaluation and the magnetostatic simulation.

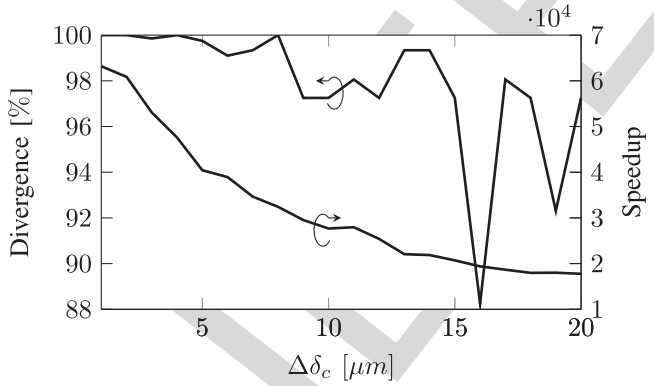


Fig. 7. On the left axis, the per cent divergence from the maximum value of the mutual inductance between the on-chip inductor and the PDN is illustrated for a coarser granularity. On the right axis, the equivalent speedup gained using the proposed methodology is shown.

Alternatively, the speedup is depicted on the right y-axis. Despite a significant reduction in the speedup as the granularity decreases, the execution time of the proposed methodology is four orders of magnitude faster, providing an effective alternative. Moreover, the value of maximum mutual inductance and the position where the mutual inductance is minimum cannot be captured for a step size of more than 10 μm, as the error increases significantly (in this case 12%). Alternatively, the analytic model offers a fast and accurate means to determine these quantities.

Additionally to gains in accuracy and computational time, the proposed methodology offers better insight on the crosstalk noise effects. Using the mutual inductance between the two structures, a methodology for the accurate evaluation of the crosstalk noise effect is proposed. A transfer function of the compact circuit model (see Figure 8) is determined, allowing an analytic or SPICE evaluation of the crosstalk noise. The frequency and other attributes of the noise are characterised, as shown in Section III.

III. Crosstalk Noise Circuit Model

In this section, the second stage of the proposed methodology to evaluate the crosstalk noise originating from the inductive link is presented. Advanced design methods and CAD tools for the power distribution network provision for the IR drop noise and the transient, high frequency voltage drop $L\frac{di}{dt}$ [33]–[35]. Nevertheless, traditional PDN design does not cope with the additional noise, originating from the on-chip inductors utilised for contactless inter-tier communication. In Figure 8, the crosstalk effect due to coupling to the

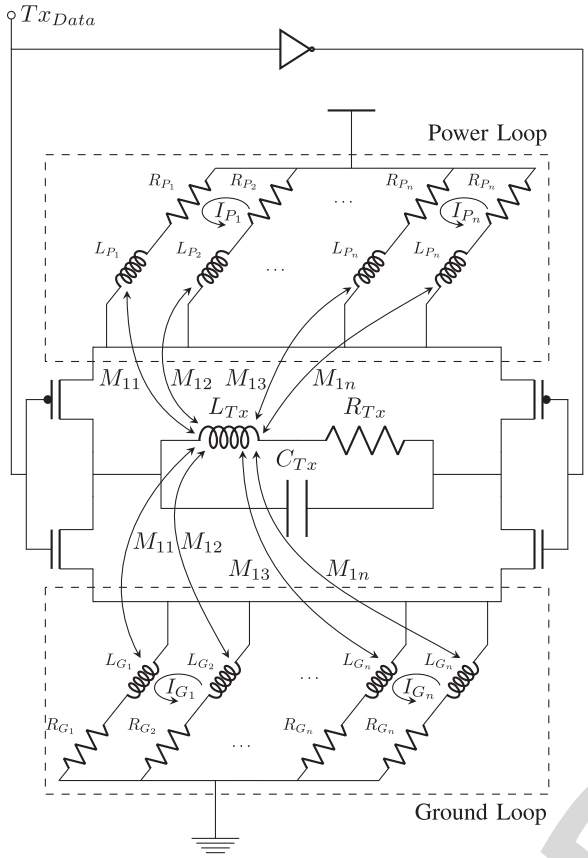


Fig. 8. A compact circuit model of an H-Bridge transmitter driving an on-chip inductor including the coupling between the on-chip inductor with the power and ground networks.

on-chip inductors is illustrated. P and G denote power and ground wires, respectively. L_{Pn} and L_{Gn} are the partial self-inductances of the power and ground interconnect wire, respectively. Equivalently, R_{Pn} and R_{Gn} are the respective wire resistances. Mij denotes the partial mutual inductance between the on-chip inductor with self-inductance L_{Tx} and each segment of the PDN. Due to the symmetry between the power and ground PDN wires, the mutual inductance is assumed to be equal. The parasitic resistance and capacitance of the on-chip inductor is illustrated as R_{Tx} and C_{Tx}, respectively. The on-chip inductor, usually placed on the topmost and thickest metal layer to reduce the wire resistance, is in the vicinity of the power network.

The amplitude of the induced current on the PDN depends upon the geometric and electrical characteristics of the closed path which alter the coupling between the inductor and the PDN loop. Depending upon the current flowing through the on-chip inductor, crosstalk noise is induced on the power distribution network (within the same tier) potentially deteriorating the power integrity of the circuit and reducing the robustness of the system. In inductive links, large currents (on the order of milliAmperes [7], [13], [30]) flow through the inductor during inter-tier communication and, consequently, the crosstalk noise effect is significant as demonstrated in this section.

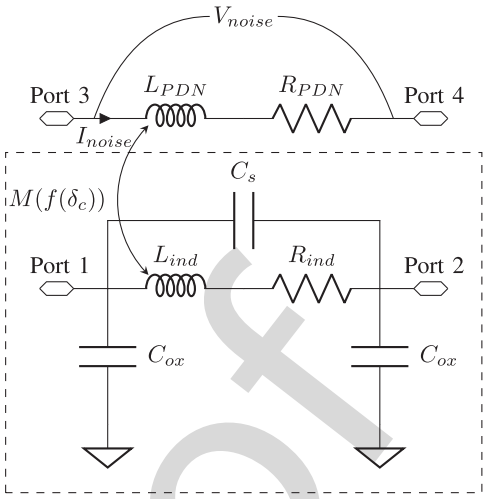


Fig. 9. Compact circuit model for the evaluation of the crosstalk noise due to the on-chip inductor.

The noise effects evaluated with Cadence® Spectre® [36] using SPICE simulations are presented in subsection III-A. The effect of frequency on the interconnect resistance is considered, yielding a frequency-dependent noise model. The speedup and accuracy of the proposed method compared to full-wave electromagnetic simulations with Ansys HFSS [37] are described in subsection III-B to demonstrate the validity of the model compared to this commercial tool. Moreover, the impact of substrate resistivity on the induced crosstalk noise is investigated in subsection III-C.

A. Frequency-Dependent Noise Evaluation

A circuit model for the high frequency crosstalk noise is depicted in Figure 9. For any given PDN loop in the vicinity of the on-chip inductor, the transimpedance of the inductor-PDN circuit is given by

$$\frac{V_{ind}}{I_{noise}} = \frac{Z_{11}Z_{22} + \omega^2 M^2}{j\omega M}, \tag{7}$$

where Z_{11} is the self impedance of the inductor and Z_{22} is the self impedance of the PDN loop. Furthermore, M is the mutual inductance between the on-chip inductor and the PDN loop.

The self impedance of the inductor is,

$$Z_{11} = \frac{R_s + j(\omega L_{ind} - \omega R_s^2 C_s - \omega^3 L_{ind}^2 C_s)}{1 - \omega^2(2L_{ind}C_s - R_s^2 C_s^2) + \omega^4 L_{ind}^2 C_s^2}, \tag{8}$$

where R_s is the frequency-dependent resistance, L_{ind} is the self-inductance, C_s is the series capacitance, and C_{ox} is the oxide capacitance of the on-chip inductor. For the PDN loop,

$$Z_{22} = R_{PDN} + j\omega L_{PDN}, \tag{9}$$

where L_{PDN} and R_{PDN} are the self inductance and the frequency-dependent resistance of the PDN loop, respectively.

To spatially model the aggregate noise on the PDN loop, the mutual inductance and, consequently, the current induced on the PDN loop is described as a function of the relative position to the inductor. Consequently, the accumulated noise

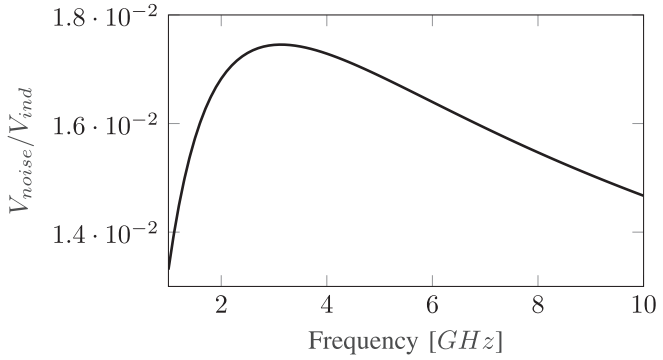


Fig. 10. Frequency response of the crosstalk noise for the circuit model in Figure 9.

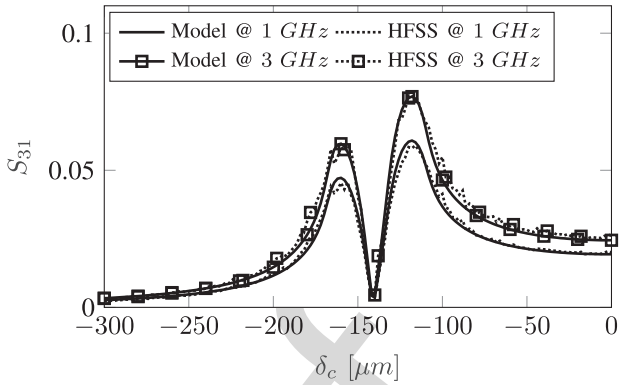


Fig. 11. Voltage gain scattering parameter S_{31} between the on-chip inductor and a PDN loop.

due to the on-chip inductor is both frequency and spatially dependent.

The frequency response of the induced noise is illustrated in Figure 10. The case where $l_{PDN} = 300\ \mu m$ and $d_{out} = 400\ \mu m$ is used for this simulation. For the evaluation of the resistance of both the inductor and the PDN, a frequency-dependent model is utilised, considering the skin effect of the wires. Furthermore, the inductance of the inductor is evaluated using the Greenhouse formula [38],

$$L_{ind} = \frac{\mu}{2} g_1 n^2 d_{avg} f(p), \tag{10}$$

where

$$f(p) = \ln(\frac{g_2}{p}) + g_3 p + g_4 p^2, \tag{11}$$

p is the fill factor $((d_{in} - d_{out})/(d_{in} + d_{out}))$, n is the number of turns, and d_{avg} is the average diameter $(0.5(d_{in} + d_{out}))$. For a rectangular inductor, the coefficients g_i are

$$[g_1\ g_2\ g_3\ g_4] = [1.27\ 2.07\ 0.18\ 0.13]. \tag{12}$$

The inductance of the PDN loop is determined by closed-form expressions for the self inductance of rectangular conductors [23]

$$L_{PDN} = \frac{0.002}{3w^2}\Big[3w^2 l \ln\frac{l + \sqrt{l^2 + w^2}}{w} - (l^2 + w^2)^{3/2} + 3wl^2 \ln\frac{w + \sqrt{l^2 + w^2}}{l} + l^3 + w^3\Big], \tag{13}$$

where l is equal to the length of each segment of the PDN, l_{PDN} and w is the trace width of the PDN, w_{PDN}. The self and oxide capacitance of the on-chip inductor are determined by [39]

$$C_s = n w_{PDN}^2 \frac{\epsilon_{ILD}}{t_{ILD}}, \tag{14}$$

and [40]

$$C_{ox} = \frac{1}{2}\big(C_A + C_P\big), \tag{15}$$

respectively. In (14), n is the number of turns, ϵ_{ILD} is the relative permittivity of the inter-layer dielectric, and t_{ILD} is the thickness of the inter-layer dielectric surrounding the metal layers of the inductor. In (15), C_A is the parasitic capacitance formed between the inductor and the substrate, while C_P is the fringe capacitance between the periphery of the inductor and the substrate.

The coupled inductor-PDN structure behaves as a band-pass filter, with a resonance frequency identical to the resonance of the on-chip inductor since the PDN capacitance is not considered, while the inductance of the PDN negligibly alters the resonance frequency. The operating frequency of the inductive link is the primary factor that determines the magnitude of the induced noise. The effect peaks near the resonance frequency, however, for frequencies farther away from the resonance frequency, the effect of the noise is gradually diminished. Note that this inductor model does not include the effect of the substrate impedance on the performance of the inductor. Nevertheless, any enhanced model can be utilised to consider this effect.

B. Validation of Noise Effects

To validate the crosstalk evaluation methodology, HFSS and SpectreRF simulations are performed on the inductor-PDN structure used in subsection III-A in Figure 9. Both the analytic method and full-wave simulations are performed on an eight-core Intel® Xeon® E5–2640 v2 [41] processor with 32 GB of RAM. Using the inductor model highlighted by a dashed rectangle, the resistive and capacitive parasitic effects of the on-chip inductor are adequately modelled without complicating the evaluation process. However, the proposed methodology can be equally effective with any on-chip inductor model, since the evaluation of the mutual inductance is independent from the circuit model of the inductor and can be integrated with more accurate on-chip inductor circuit models. Nevertheless, comparing on-chip spiral inductor models is beyond the scope of this paper. Scattering parameter simulations are performed for frequencies between 1 GHz and 10 GHz, covering a broad spectrum of frequencies usually encountered in inductive link applications [13], [30], [42].

The behaviour of the noise for $|\delta_c| = [0, d_{out}]$ is depicted in Figure 11. The voltage gain S_{31} is illustrated for a frequency of 1 GHz and for the resonance frequency of 3 GHz, notated by square markers. The solid and dotted lines denote, respectively, the SpectreRF simulations obtained using the proposed methodology and the full-wave simulations.

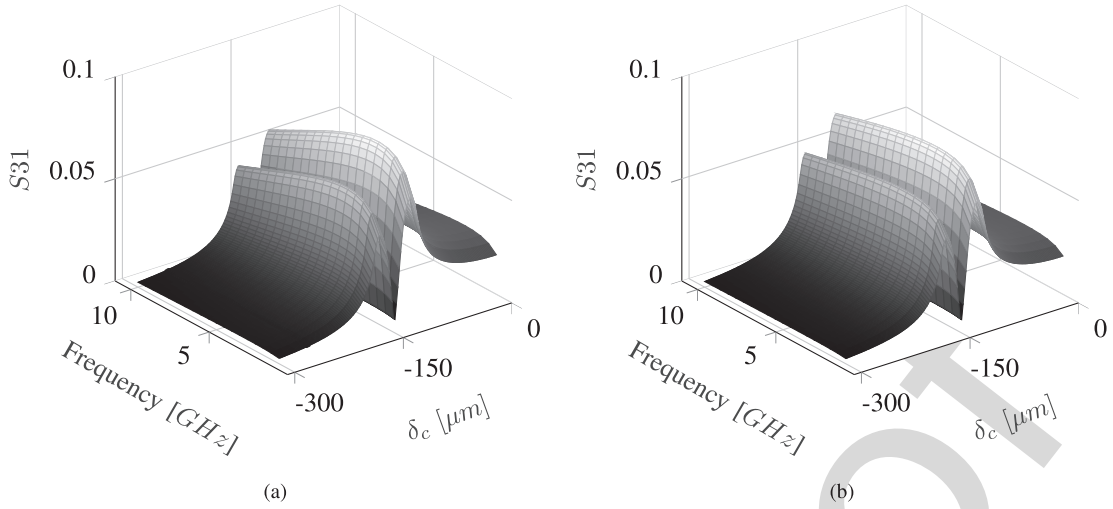


Fig. 12. Induced crosstalk noise as a function of the frequency and the spatial separation δ_c where (a) is a low resistivity (0.01 $\Omega \cdot cm$) and (b) a high resistivity (30 $\Omega \cdot cm$) substrate, respectively.

A very good fit is observed between the full-wave simulations and the proposed methodology. The average error for transmitting a signal at 1 GHz is 5.19% while at 3 GHz is 6.14%. As the frequency increases, a small decrease in accuracy is observed due to the use of the magnetostatic mutual inductance (as discussed in subsection II-A). Nevertheless, the decrease is not significant to require a re-evaluation of the mutual inductance between the investigated structures, as mentioned in subsection II-A. Note that the full-wave simulation generates artefacts in the solution due to parasitic capacitances that cannot be analytically evaluated, thus contributing to the per cent error between the two approaches.

Moreover, a notable difference is observed in the simulation time between the two approaches. Specifically, the run time of the full-wave simulation is 445 min, while the same simulation is performed within 94 min in SpectreRF, a speedup of 4.7×. No parallelisation techniques have been used for the evaluation of the presented methodology in SpectreRF. Alternatively, four full-wave simulations run in parallel to improve the simulation time and efficiently allocate the existing computing resources for solving the full-wave simulations. Consequently, the computational gains offered by the proposed method are effectively greater.

C. Impact of Silicon Substrate on Crosstalk Noise

For near field inductive communication high resistivity substrates are preferred to exploit the lower attenuation through the substrate [11]. Consequently, the coupling between the on-chip inductors in each tier is negligibly affected by substrate losses. In this subsection, the effect of the substrate resistivity on the noise induced by inductive links on the PDN is investigated.

To model the resistive losses of the substrate, the compact circuit model in Figure 9 is adapted, where a resistor R_{sub} is added in series to the oxide capacitance C_{ox} [39]. To effectively capture how the induced noise is affected, two substrate resistivities are chosen based on a broad range of available doping densities for P^+ substrates. Namely, a low resistivity 0.01 $\Omega \cdot cm$ and a high resistivity 30 $\Omega \cdot cm$ substrate [43] are, respectively, assumed. The impedance characteristics of the spiral inductor are, in this case, extracted from full-wave simulations for the investigated substrate resistivities.

The behaviour of the crosstalk noise due to the variation in the substrate resistivity is illustrated in Figure 12. The effect of the low and high resistivities for the substrate are depicted in Figures 12(a) and 12(b), equivalently. The behaviour of the noise can be subdivided into two distinct effects, the effect on the separation distance δ_c and the effect on the frequency response of the inductor. As expected, the change in the substrate resistivity did not alter the spatial behaviour of the noise across δ_c. Nevertheless, a significant divergence is observed for the on-chip inductor frequency response (and therefore the crosstalk noise) between the considered substrates due to the different losses of the inductor into the silicon substrate. Therefore, even though the monotonic behaviour of the frequency response is not altered (increases before the resonance frequency — decreases after), the slope of the frequency response differs.

Since the spatial behaviour of the noise is not affected by the substrate resistivity, the position of maximum noise is chosen for the validation of the model. A 3-D model of the investigated structure is designed and simulated with the Keysight Advanced Design System (ADS) FEM Electromagnetic Simulator [44]. The results produced with ADS are illustrated in Figure 13 in comparison to the model results simulated with Cadence Spectre. A good fit is observed between the two approaches with a maximum deviation within 7%, thus verifying the accuracy of the presented results.

Due to the reduced losses of the spiral inductor into the substrate, the high resistivity substrate leads to a significant increase in the coupling with the adjacent interconnects, thereby confirming the hypothesis of increased inter-tier coupling through high resistivity substrates. To efficiently illustrate this increase in the crosstalk noise, the per cent difference between the crosstalk noise in the considered substrates

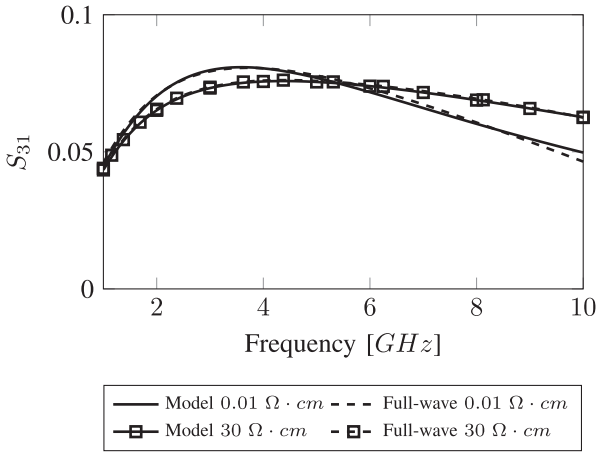


Fig. 13. Full-wave and analytical evaluation of the crosstalk noise on the PDN versus the investigated frequency spectrum for the position of maximum noise.

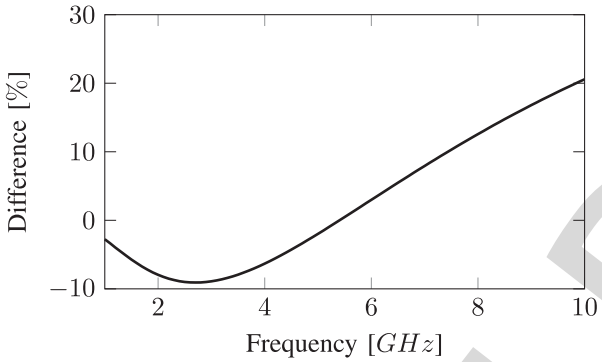


Fig. 14. The per cent difference of the induced crosstalk noise between a high and a low resistivity substrate for the position of maximum noise.

is depicted in Figure 14. In higher frequencies, where the substrate effect is more pronounced, the noise increases by 20%.

Alternatively, a dip (less than 10%) in the crosstalk noise is observed below the resonance frequency. Due to the increased resistivity of the substrate, a small decrease in the effective self-inductance of the spiral inductor is also observed [45]. Moreover, in low frequencies, the oxide capacitance C_{ox} behaves as an open circuit effectively cutting-off the path to R_{sub}. Consequently, in low frequencies where the eddy current losses are small, the efficiency of the on-chip inductor on the low resistivity substrate is superior compared to that on the high resistivity substrate. Thus, a higher coupling with the interconnects is noticed slightly increasing the crosstalk noise compared to the high resistivity substrate. As the frequency increases, however, the losses in the substrate dominate the overall effect and the noise for the low resistivity substrate is significantly lower.

IV. Case Study

The applicability of the proposed methodology is demonstrated in this section through a case study. For this case study, a single ended transmitter is assumed to drive the

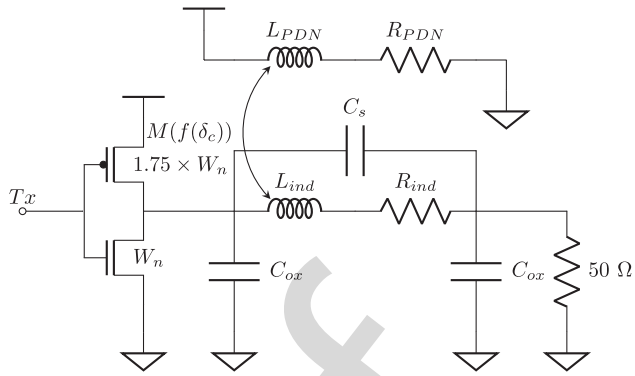


Fig. 15. Compact circuit model illustrating a single ended transmitter driving the on-chip inductor and the coupled PDN loop.

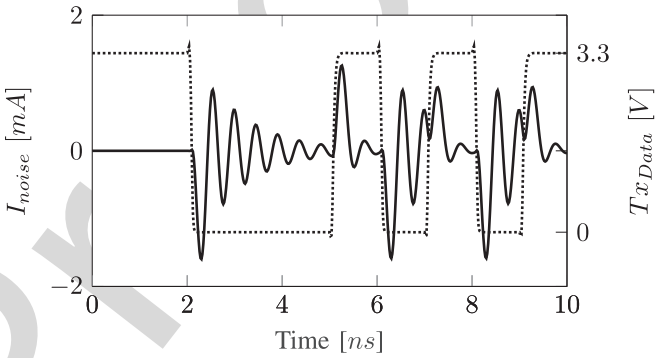


Fig. 16. Transient simulation illustrating the transmitted data through the inductive link and the corresponding induced noise on the PDN loop.

on-chip inductor. A transient analysis is performed illustrating the temporal noise characteristics given the single ended transmitter for the on-chip inductor.

Additionally to the frequency characteristics of the induced noise presented in Section III, the methodology proposed in this paper is utilised to determine the temporal behaviour of noise. To perform a transient simulation of noise, specific assumptions are made considering the driving circuit of the inductor and the utilised signal encoding.

The simulation setup for the transient analysis is illustrated in Figure 15. A single ended transmitter is chosen as the simplest circuit driving an inductive link. The second terminal of the inductor is terminated to ground with a 50 Ω resistor. Non-return to zero encoding is assumed as the communication scheme for the inductive link. The width W_n is treated as a parameter in the following analysis with a typical size of $W_n = 5\ \mu m$. Note, however, that this width exclusively serves this case study and can be accurately determined only if the full specification of the entire system, such as the outer diameter of the coupled inductors and the separation distance, are known. Therefore, this choice of W_n should not be generalised.

The transient analysis of the induced noise is depicted in Figure 16. For this analysis, a 1 $Gbps$ random bitstream is utilised as the transmitted data Tx. The induced current I_{noise} appears as a damped positive sinusoidal pulse for transitions

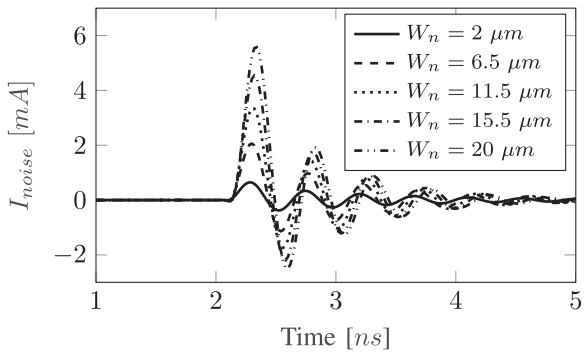


Fig. 17. Transient simulation illustrating the transmitted data for increasing device width W_n.

from logic zero to one and as a damped negative sinusoidal pulse for the opposite transition. The ringing oscillation of the noise is dampened within 3 ns, not fast enough for a data signal of 1 $Gbps$. Due to the high frequency characteristics of the induced current, the frequency-dependent LdI_{noise}/dt component of the aggregate noise of the PDN loop cannot be ommited. Therefore, the induced noise can be considered as an additional component of the high frequency on-chip Ldi/dt noise developed on the power distribution network.

The strength of the driving devices depends upon several design specifications of the inductive link. To visualise the impact of the driving strength of the transmitter circuit on the induced noise, the width of the transistors is swept from 2 μm up to 20 μm. The simulation results are depicted in Figure 17. As expected, increasing the device strength results in an increased magnitude for the induced current I_{noise}. Nevertheless, the phase and frequency of the noise are not affected by altering W_n.

V. Conclusion

A frequency-dependent model that accurately determines the effect of crosstalk noise from inductive links on the power distribution network is presented. The model is constructed in two stages. In the first stage, the mutual inductance between the power distribution network and the inductor is analytically determined. For the evaluation of the mutual inductance, a speedup on the order of magnitude 10^4 is achieved, while the accuracy is within 10% of the magnetostatic solution with Ansys Maxwell. A SPICE model is constructed in the second stage to determine the frequency-dependent noise yielding an $\sim 5\times$ speedup as compared to S-parameter noise extraction with HFSS simulations. This model can guide the design process of the PDN to avoid or limit undesirable crosstalk noise from the on-chip inductors. In this way, the robustness of the PDN does not degrade and the power integrity of contactless systems is improved.

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