Passive SC ΔΣ Modulator Based on Pipelined Charge-Sharing Rotation in 28-nm CMOS

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***Abstract*— In this paper, we introduce a new switched-capacitor (SC) passive delta-sigma (ΔΣ) modulator architecture. It is based on a charge-sharing rotation technique, which eliminates any inter-stage loading effects that plague the conventional SC passive ΔΣ modulators. To improve the proposed modulator's noise suppression and stability, an independent extra feedback path and a zeroing stage are added to the 2nd-stage integrator. Moreover, a pipelining (i.e. interleaving) technique is employed in the passive low-pass filter to relax settling requirements and improve power efficiency. Compared to the ΔΣ modulators with active integrators, the proposed modulator contains only switches, capacitors and one comparator, thus being greatly amenable to nanoscale CMOS process nodes. Implemented in 28-nm CMOS, the proposed ADC occupies a core area of 0.059 mm^2. It achieves measured SNDR of 81.1 dB and a measured dynamic range (DR) of 83.6 dB with a signal bandwidth of 80 kHz at 40.96 MS/s, while consuming 101.5 μW. SNDR is maintained above 70 dB across a ±20% supply variation.**

***Index Terms*— Analog-to-digital converter (ADC), delta-sigma, inter-stage loading effect, passive, pipelining, switched capacitor.**

I. Introduction

THE ever increasing demands for Internet-of-Things (IoT) networks and portable devices promote the trend of power-efficient system design. This is further motivated by the relatively slow development in the power storage technology and the consumer expectations of long operational and stand-by time. To achieve inexpensive large-scale integration while exploiting good digital power efficiency, the IoT networks and portable devices normally integrate in the deep nanoscale CMOS technology. For applications demanding high resolution and good linearity, ΔΣ ADCs can be a suitable option since they can relax front-end anti-aliasing filtering and suppress in-band quantization noise by oversampling and noise-shaping techniques.

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Low-pass ΔΣ ADCs universally adopt active integrators built on operational amplifiers (op-amps) to filter out the quantization noise. Typically, the ADC power consumption is dominated by such op-amps, especially the one in the first integrating stage which demands lower noise and wider bandwidth to achieve good settling performance. It is however rather challenging to implement *high-performance* op-amps in the deep nanoscale technology because of the low intrinsic gain of the bulk transistors. This typically requires the adoption of multi-stage amplifier topologies, often power-hungry and requiring extremely careful design to mitigate stability concerns.

Considering that the integrator op-amps only work during the corresponding integration phase, while merely consuming static power otherwise, an op-amp sharing technique among constituent integrators and even adders during different phases can be employed to increase the system power-efficiency [1], [2]. However, the single op-amp in [1] is over-constrained by the noise and settling specifications of the 1st-stage, which are rather unnecessary for the following two stages. Complex timing control logic must also be employed to properly share the op-amps among different stages. Alternative techniques attempt to replace the op-amps with other blocks, such as zero-crossing detectors [3], [4], dynamic-comparators [5], and inverters [6]. ΔΣ modulators with zero-crossing detectors can hardly achieve high resolution due to the voltage overshoots caused by delays from the zero-crossing event to the stable detection result generated, while the accuracy of ΔΣ modulators employing comparator-based and inverter-based integrators is mainly impaired by their limited dc gain and input-referred offset.

An attractive alternative to the active integrators invariably employing power-hungry op-amps are "passive integrators."[1] References [7], [8], and [9] partially apply this technique and utilize hybrid typologies made of both passive and active integrators, in which *high-performance* op-amps are still required. The continuous-time (CT) implementation in [10] adopts a loop filter with low-gain open-loop inter-stage amplifiers, and passive integrators made of only resistors and capacitors. Another CT implementation, presented in [11], employs a MASH topology to obtain higher-order noise-shaping by also exploiting passive integrators and inter-stage low-gain amplifiers. However, due to excessive

[1]They are called "passive integrators" in the literature but, actually, they are pseudo integrators.

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area occupancy, this architecture is not suitable for signal bandwidths lower than 1 MHz. The SC implementation in [12] also employs the inter-stage open-loop low-gain amplifiers. It further adds a positive feedback into the passive integrators to move the pole of the integrator closer to dc, in which the dc gain and bandwidth of the low-gain amplifiers will affect the system performance and stability. The SC ΔΣ modulators in [13], [14], [16] embed a fully passive low-pass filter (LPF). The topologies proposed in [13] and [14] exhibit sensitivity to the parasitic capacitance at the comparator input in terms of the noise performance and loop stability.

In *all* of the SC ΔΣ modulators with passive LPFs published to date, the sampling capacitor of the subsequent integrator stage is charged by the integrating capacitor of the preceding stage. This is referred to as *inter-stage loading* [15], with a detrimental impact of shifting the loop filter's pole to a higher frequency and leading to an inner feedback between stages, thus degrading the noise-shaping performance. Due to the significant attenuation in the passive ΔΣ modulator, the order of the fully passive loop filters is typically limited to two, and a satisfactory signal-to-quantization-noise ratio (SQNR) can only be realistically achieved by means of a sufficiently high oversampling ratio (OSR), which imposes however more strict requirements on the filter settling time. To relax the signal attenuation, an SC gain-boosting technique, proposed in [13] and also adopted in [16], is used to obtain a low-frequency voltage gain by means of properly changing how the sampling capacitors are connected (i.e. in parallel or in series) during the various phases of operation. However, that will worsen the inter-stage loading effect.

In this paper, we propose a passive SC ΔΣ modulator based on a principle of charge-sharing rotation. This allows charging the integrating capacitors of subsequent stages with the same sampling capacitor but without affecting the previous integrator stage. This avoids the inter-stage loading effects, thus ultimately improving the quantization-noise shaping performance. A zeroing stage and an extra independent feedback path are added in order to improve the modulator's stability and the equivalent gain of the comparator (i.e. the ratio between the comparator output and input rms values), thus improving the in-band quantization noise attenuation. In order to allow operating at high OSR, relaxing the settling requirement and maximizing the power efficiency, a pipelining technique is exploited.

This paper is organized as follows. Section II provides a comparison between the modulators with active and passive low-pass loop filters, analyzes the impact of the inter-stage loading effect, and describes the proposed topology and its noise characteristics. The ΔΣ modulator implementation and relevant circuit details are presented in Section III. The measured results are shown in Section IV, while Section V concludes the paper.

II. System Analysis

A. Second-Order Passive SC ΔΣ Modulators

The linear model of a conventional cascade-of-integrators feedback-form (CIFB) second-order low-pass ΔΣ modulator,

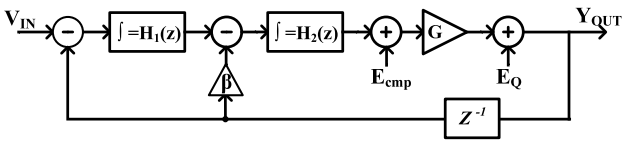

Fig. 1. Linear model of a CIFB second-order ΔΣ modulator.

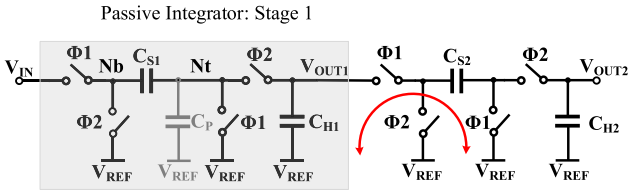

Fig. 2. Passive SC integrator adapted from [13].

which includes a low-pass filter implemented using two integrators and a comparator with an equivalent gain of G and behaving as a 1-bit quantizer, is shown in Fig. 1. As this closed-loop feedback system has two poles, it is conditionally stable depending on the gain of $H_{1,2}(z)$, the feedback path parameter β and the input signal amplitude. The transfer function of each integrator present in the loop can be expressed as:

$$H_{1,2}(z) = \frac{K \cdot z^{-1}}{1 - \alpha \cdot z^{-1}} \tag{1}$$

where K represents the gain factor, while α is the integrator's pole.

The passive integrator presented in [13] (Fig. 2) allows removing the *high-performance* op-amps from the system, thus helping to reduce the modulator's power consumption. Passive integrators embed only capacitors and CMOS switches, and are therefore suitable for deep nanoscale CMOS process nodes. As the passive integrator is based on the charge-sharing technique, the parasitic capacitance at the nodes between the sampling capacitor C_{S1} and the hold capacitor C_{H1} (Nt and V_{OUT1}) could somewhat affect the transfer function. Considering that the effect of these parasitics at node V_{OUT1} can be treated as a variation of C_{H1}, the only meaningful parasitic is capacitor C_P at node Nt. Consequently, with $C_P > 0$, the transfer function of the passive integrator is as follows [17]:

$$H_1(z) = \frac{\frac{1}{\gamma+\rho+1} \cdot z^{-1}}{1 - \frac{\gamma}{\gamma+\rho+1} \cdot z^{-1}} \tag{2}$$

where the integrator's capacitor ratio $\gamma = C_{H1}/C_{S1}$, $\rho = C_P/C_{S1}$ and the integrator's gain K is represented by the term $\frac{1}{\gamma+\rho+1}$, while the real pole ($z = e^{2\pi f_{-3\ \mathrm{dB}}/f_S}$) is located at $\frac{\gamma}{\gamma+\rho+1}$ in the z-plane. This indicates that a non-zero factor ρ leads both to a slight gain loss, and to a shift of the pole slightly away from dc. The pole in the linear frequency domain can be obtained:

$$f_{-3\mathrm{dB}} \approx \frac{f_S}{2\pi} \cdot \left(\frac{1}{\gamma + \rho + 1}\right) \tag{3}$$

where, f_S is the sampling frequency. To achieve sufficient attenuation of the in-band quantization noise and a better trade-off with the OSR in the high-resolution regime,

$f_{-3\ \mathrm{dB}}$ should be located in-band, and therefore $f_{-3\ \mathrm{dB}} \leq \frac{f_S}{2\ \mathrm{OSR}}$ and $\frac{1}{\gamma+1} \leq \frac{\pi}{\mathrm{OSR}}$. For example, for an OSR of 256, γ should be > 80.

For active $\Delta\Sigma$ modulators, an important trade-off is between performance and loop dynamics. While large loop parameters of K and feedback path coefficient β allow the system to boost its SNR, they result in a greater risk of instability and degrade the overload level (OL), i.e. the normalized input amplitude when the SNR decreases by 3 dB from its peak. For the passive $\Delta\Sigma$ modulators, on the other hand, K must be $\ll 1$ so as to move the integrator pole in-band, thus ensuring the attenuation of in-band quantization noise. Indeed, in passive $\Delta\Sigma$ modulators, the loop gain is "lumped" within the comparator (i.e. the entire dc gain of the loop is provided by the comparator), resulting in a small voltage signal swing within the loop filter, thus enabling the system to achieve a higher OL that can be actually larger than 1, as well as better linearity. However, the lack of gain within the loop filter causes the system more vulnerable to noise coupling and to the off-state drain current of CMOS switches.

B. Inter-Stage Loading Effect

The operation of two cascaded passive integrators employed in the passive $\Delta\Sigma$ modulator of Fig. 2 implies that capacitor C_{H1} is used to charge capacitor C_{S2} during phase $\Phi1$. However, because of charge sharing, the charge information stored on C_{H1} ($C_{H1}V_{C_{H1}}$) will also be affected by the charge information stored on C_{S2} ($-C_{S2}V_{C_{H2}}$) during the previous phase, which leads to an inner feedback from the 2nd-stage to the 1st-stage. Based on the charge sharing, during $\Phi1$, the top-plate voltage of C_{H1} ($V_{C_{H1}}$) can be expressed as:

$$V_{C_{H1}}(z) = \frac{-C_{S2} \cdot V_{C_{H2}}(z-1) + C_{H1} \cdot V_{C_{H1}}(z-1)}{C_{S2} + C_{H1}} \quad (4)$$

where, $\frac{C_{S2}}{C_{S2}+C_{H1}}$ is the feedback coefficient from the 2nd-stage to the 1st-stage, while $\frac{C_{H1}}{C_{S2}+C_{H1}}$ can be used to quantify the inter-stage loading effect on the 1st-stage pole position. In the frequency domain, this effect moves up the pole of the first passive integrator stage, which ultimately degrades the noise-shaping performance of the modulator. In [13], the two poles of the second-order passive $\Delta\Sigma$ modulator could not be made identical due to such inter-stage loading effect, which deteriorates the in-band noise performance by 2 dB. This is despite the attempts of maximizing the ratio between the integrating and sampling capacitors in the 2nd-stage (C_{H2}/C_{S2}).

The topology presented in [16] is redrawn in Fig. 3 in three configurations: without SC gain-boosting, with the SC gain-boosting technique, and with a unity-gain buffer but without the SC gain-boosting technique. It serves the purpose of representing a reference structure for carrying out an analytical study on the inter-stage loading effect. Based on Fig. 3a, signal and quantization noise transfer functions (STF anf NTF, respectively) can be expressed as:

$$\mathrm{STF(z)} = \frac{\alpha^*(1-\alpha_1)H_2G}{1+[(G(1-\alpha^*\alpha_1)-1+\alpha^*)H_2-\alpha^*\alpha_1]z^{-1}} \quad (5)$$

$$\mathrm{NTF(z)} = \frac{1-\alpha^*\alpha_1 z^{-1}-(1-\alpha^*)H_2z^{-1}}{1+[(G(1-\alpha^*\alpha_1)-1+\alpha^*)H_2-\alpha^*\alpha_1]z^{-1}} \quad (6)$$

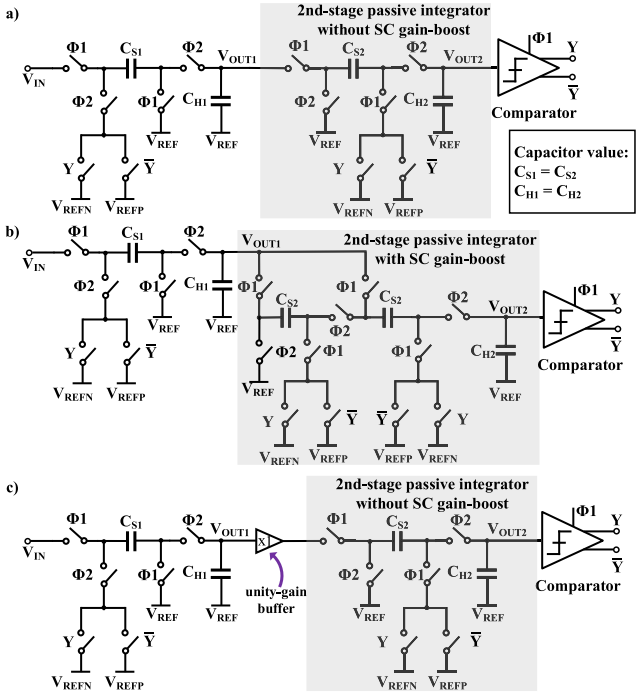

Fig. 3. Passive $\Delta\Sigma$ modulator in [16]: without SC gain-boosting circuit (a), with the 2nd-stage integrator exploiting SC gain-boosting ($N = 2$) (b), and with unity-gain buffer but without the SC gain-boosting circuit (c).

where H_2 is the transfer function of the 2nd-stage passive integrator, G is the equivalent gain of the comparator, α_1 is $\frac{\gamma}{\gamma+1}$ ($\gamma = \frac{C_{H1}}{C_{S1}}$) and α^* is $\frac{C_{H1}}{C_{S2}+C_{H1}}$. The zero of NTF generated by the 1st-stage integrator is pushed towards higher frequencies to around $\alpha_1\alpha^*$, resulting in a worse suppression of the in-band quantization noise.

To analyze the effects of the gain-boosting technique on the inter-stage loading, a SC gain-boosting sampling stage with a gain factor $N = 2$ is implemented as the 2nd-stage, shown in Fig. 3b. It promotes a reduction of α^* down to $\frac{C_{H1}}{2\ C_{S2}+C_{H1}}$, whose effect is to potentially shift the zero of the NTF generated by the 1st-stage out of the system's signal bandwidth, and to increase the zero generated by the 2nd-stage up to $\frac{C_{H2}}{0.5\ C_{S2}+C_{H2}}$, which is close to dc. For a gain factor of 2 and assuming that $C_{H1} = C_{H2}$ and $C_{S1} = C_{S2}$, the capacitor ratio γ needs to be larger than 241 so as to keep the first zero of the modulator in-band, which will in turn increase the area occupied by the capacitors. In the second-order passive modulator presented in [16], the measured output spectrum exhibits a 20 dB/decade slope between 1 kHz and 100 kHz, which is due to the gain factor of the gain-boosting technique of $N = 5$, causing the first zero of the NTF to be pushed outside the signal bandwidth. It could therefore be argued that while the SC gain-boosting technique raises the gain of the 2nd-stage and pulls the pole of the 2nd-stage closer to dc, it worsens the inter-stage loading effects and results in a shift of the NTF zero (which is generated by the 1st-stage integrator) further away from dc.

Alternatively, the use of a unity-gain buffer interposed between these two integrator stages, shown in Fig. 3c, so as to completely eliminate the inter-stage loading, will modify the

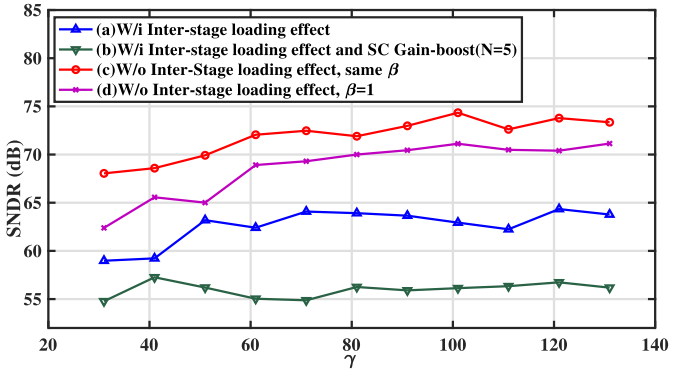

Fig. 4. Behavioral modeling of the Fig. 3 modulator: SNDR vs. γ at OSR = 256 for the following cases: with inter-stage loading effect (a), with inter-stage loading effect and the SC gain-boosting ($N = 5$) (b), without inter-stage loading effect ($\beta = \frac{C_{S2}}{C_{S2}+C_{H1}}$) (c), and without inter-stage loading effect ($\beta = 1$) (d).

STF and NTF, which can now be written in the form:

$$\mathrm{STF}_{\mathrm{w/buf}}(z) = \frac{H_1 H_2 G}{1 + H_1 H_2 G z^{-1} + \beta H_2 G z^{-1}} \tag{7}$$

$$\mathrm{NTF}_{\mathrm{w/buf}}(z) = \frac{1}{1 + H_1 H_2 G z^{-1} + \beta H_2 G z^{-1}} \tag{8}$$

where, β is the feedback coefficient from the modulator's output to the 2nd-stage (see Fig. 1), which is equal to 1 when employing the unity-gain buffer (Fig. 3c). For fair comparison, β is set to $\frac{C_{S2}}{C_{S2}+C_{H1}}$, which is equal to the case shown in Fig. 3a and can be achieved by adjusting the reference voltages of the feedback path to the 2nd-stage.

System investigation of the inter-stage loading effects with respect to the capacitance ratio γ ($C_{H1,2}/C_{S1,2}$) is carried out by means of behavioral modeling for all the configurations mentioned above, and is revealed in Fig. 4 with OSR of 256 and assuming $C_{H1} = C_{H2}$ and $C_{S1} = C_{S2}$. The worst-case SNDR degradation can be as large as 10 dB. Engaging the SC gain boost causes a further drop in SNDR as a result of the equivalent pole of the 1st-stage integrator moving up and outside of the signal bandwidth, although the pole of the 2nd-stage is pulled in towards dc.

C. Proposed Second-Order Passive ΔΣ Modulator

The simplified schematic of the proposed passive second-order ΔΣ modulator based on the charge-sharing rotation is presented in Fig. 5b. It contains a second-order low-pass IIR filter (IIR2), 1-bit feedback DACs and a comparator.

The IIR2 filter itself was inspired by the charge-sharing rotation scheme introduced in [18] and redrawn in Fig. 5a. It is a fully-passive topology which avoids operational or any active amplifiers and employs only capacitors and CMOS switches. It purposefully prevents any inter-stage loading effects. During Φ1, V_{IN} is sampled on capacitor C_S, and then during Φ2 the top-plate of C_S is connected to the top-plate of C_{H1}, causing the charge sharing between C_S and C_{H1}. Therefore, at the end of Φ2, C_S and C_{H1} store the same voltage information. Consequently, instead of using C_{H1} to charge C_{S2}

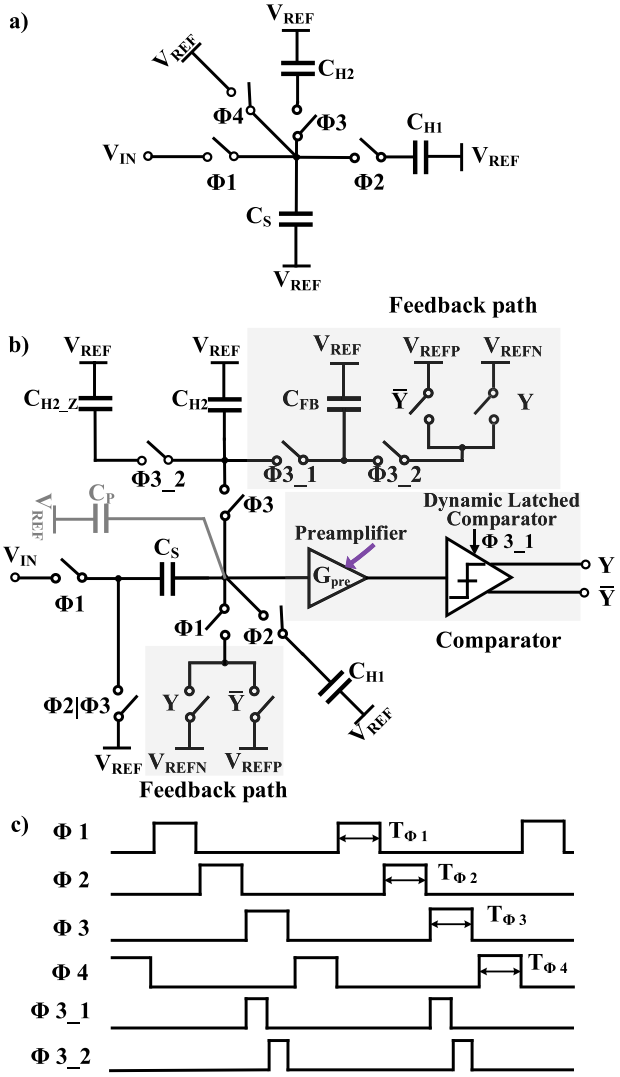

Fig. 5. IIR2 filter based on charge-sharing rotation (a). Proposed passive second-order ΔΣ modulator (b), and its timing diagram (c).

and then taking C_{S2} to charge C_{H2}, as done earlier in Fig. 2, the IIR2 uses C_S to directly charge C_{H2}. When Φ3 is asserted, C_S is connected to the top-plate of C_{H2}, by which the voltage information stored in C_S, which is identical to the voltage information stored in C_{H1} at the end of Φ2, passes to C_{H2} without any charge loss in C_{H1}. In contrast to the cascaded passive SC integrators exemplified by Fig. 2, the cascaded passive integrators in IIR2 share the single sampling capacitor C_S between the stages. For this reason, the IIR2 does not exhibit any inter-stage loading effects despite the fact that two cascaded passive integrators are employed.

At the proposed modulator level, during Φ1, the voltage difference between the input signal V_{IN} and the 1-bit feedback DAC output controlled by the 1-bit quantizer output, $\overline{Y}$ and Y, is sampled on capacitor C_S. Considering that the voltage signal swing at the input of the preamplifier is reasonably small (tens to few hundreds of μV), the memory charge inside C_S at the end of Φ3_1 is small enough not to affect the settling of the new sample. During Φ2, the charge information stored on C_S and C_{H1} is shared and updated, which represents the action

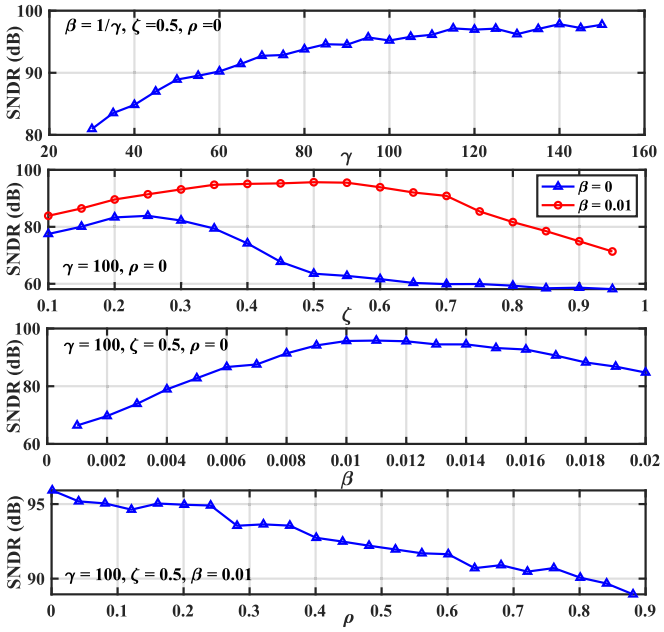

Fig. 6. SNDR of the proposed ADC, obtained through behavioral modeling simulations, versus γ, ζ, β and ρ at an OSR of 256.

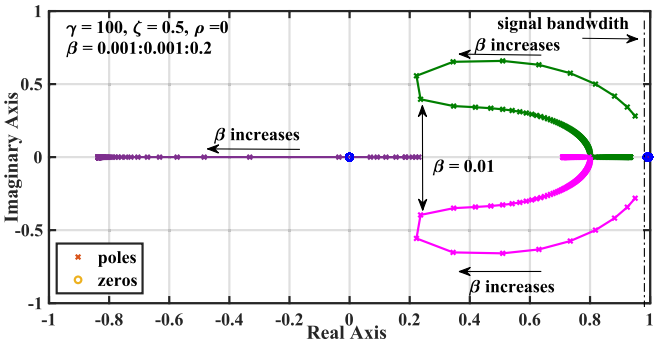

Fig. 7. Pole-zero constellation of the NTF of the proposed ADC at different values of β.

of the 1st-stage passive integrator. Φ3_1 and Φ3_2 are the two non-overlapping phases of Φ3. During Φ3_1, the top-plates of C_S, C_{H2} and feedback capacitor C_{FB} are connected together to share their charges. This represents in turn the action of the 2nd-stage integrator with an extra independent feedback path. The comparator compares the voltage swing at the input of the preamplifier and generates the system output Y/$\overline{\text{Y}}$ at the falling edge of Φ3_1. During Φ3_2, the top-plates of C_{H2} and C_{H2_Z} are connected together. This adds a zero to the transfer function of the 2nd-stage integrator, which helps with the stability. In order to minimize the input-referred noise and maximize the gain of the comparator, a preamplifier stage is employed before the conventional dynamic latched comparator. Considering the parasitic capacitor C_P at the connection node between the sampling capacitor C_S and the hold capacitors, the transfer function of the 1st-stage integrator $H_1(z)$ is identical to (2), while the transfer function of the 2nd-stage integrator $H_2(z)$ can be expressed as:

$$H_2(z) = \frac{[1-(1-\zeta)z^{-1}]\cdot\frac{1}{\gamma+\rho+1+\beta}z^{-1}}{1-(1-\zeta\frac{1+\rho+\beta}{\gamma+\rho+1+\beta})z^{-1}} \tag{9}$$

where γ is C_{H2}/C_S, β is C_{FB}/C_S, $\rho = C_P/C_S$ and ζ is $C_{H2}/(C_{H2}+C_{H2\_Z})$ which affects the position of the zero of the transfer function. The term $\zeta\frac{1+\rho+\beta}{\gamma+\rho+1+\beta}$ in the denominator of (9) can be treated as an indicator of how far away the pole is from the unit circle ($z = 1$). The location of the pole is thus determined by γ, β, ρ and ζ. By reducing ζ, the pole can be moved closer to the unit circle. The STF and quantization NTF of the proposed $\Delta\Sigma$ modulator exhibit the same forms as (7) and (8), with $H_2(z)$ expressed by (9). As the $\Delta\Sigma$ modulator is a non-linear system, the comparator gain G can only be obtained via simulations. However, the method proposed in [13] estimates that the loop gain of the modulator is 1 at $f_S/2$, meaning that an approximation of the comparator gain of the proposed modulator is $G_{\text{est}} = \frac{1}{H_1(-1)H_2(-1)}$. A high G_{est} value can be achieved by increasing γ.

To reach the targeted accuracy of 13 bits over a bandwidth of 80 kHz and assuming a second-order $\Delta\Sigma$ modulator, a minimum OSR of 128 would be needed. In order to maintain sufficient margin against potential nonidealities, such as noise and leakage currents, an OSR of 256 has therefore been adopted. For stronger attenuation of the in-band quantization noise, the zeros of the NTF should be within the signal bandwidth. With the assumption that $C_{H1} = C_{H2}$, based on (3), γ ($C_{H1,2}/C_S$) needs to be larger than 80 at an OSR of 256. Capacitor C_{H2_Z} shifts the pole of the 2nd-stage integrator towards dc and further adds a zero to the system, improving the stability. If ζ is set to 1/2 and ρ is set to 0, the pole error ($\zeta\frac{1+\rho+\beta}{\gamma+\rho+1+\beta}$) will be reduced by half, thus increasing the ADC's SNR. It is worth noting the trade-off between ζ and the modulator's area, i.e. lowering $\zeta = C_{H2}/(C_{H2}+C_{H2\_Z})$ is practically done by substantially increasing C_{H2_Z}.

Thanks to the introduced capacitor C_{FB}, one additional feedback path with the feedback coefficient β (C_{FB}/C_S) can be realized. If β is very small, the ability of the system to attenuate noise is diminished, since the poles of the NTF are close to the signal bandwidth. On the other hand, for sufficiently large β, the ADC behavior would resemble the operation of a second-order $\Delta\Sigma$ modulator when β is still smaller than or comparable to the value of $H_1(z)$ at low frequencies. Likewise, it would resemble a first-order $\Delta\Sigma$ modulator at high frequencies, when β is much larger than the value of $H_1(z)$. To set β to an appropriate value such that the proposed system acts as second-order and the poles of the NTF are allocated around $f_S/4$ for the consideration of stability, β should be comparable to $H_1(0) = \frac{1}{\gamma}$. At such a value, the output swing of the first integrator stage would be comparable to that of the 1-bit feedback DAC output, which would in turn reduce the output swing of the 2nd-stage integrator, and therefore the equivalent G would increase, resulting in a higher ADC linearity even at full-scale. Moreover, a higher G allows for the in-band quantization noise to be further attenuated. The inner feedback path implemented with C_{FB}, employed to achieve higher G without adopting a higher γ and shifting the modulator poles towards lower frequencies, allows relaxing the trade-off between in-band quantization noise power and area.

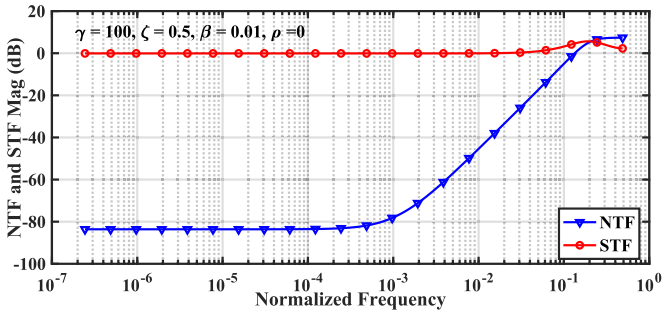

Fig. 8. STF and NTF plots of the proposed modulator ($f_s = 40.96$ MHz).

The sensitivity of the proposed modulator to the γ, ζ, β and ρ parameters can be studied through behavioral-modeling simulations, as indicated by the trends in ADC SNDR plots in Fig. 6. By assuming $C_{H1} = C_{H2}$, $\beta = \frac{1}{\gamma}$, $\rho = 0$ and $\zeta = 0.5$, as γ increases, SNDR increases gradually. This happens until γ reaches 100. Afterwards, the SNDR remains almost constant around 95 dB, thus justifying the choice of $\gamma = 100$ in this design, and implying $\beta = 0.01$. Now, by sweeping ζ, SNDR reaches its maximum at $\zeta = 0.5$. Compared to a system that does not embed the additional feedback stage ($\beta = 0$), SNDR of the proposed modulator is considerably higher (as much as 35 dB for ζ between 0.5 and 0.6). Due to the area and physical layout matching constraints, the chosen value for ζ is 0.5, meaning that C_{H2_Z} must be equal to C_{H2}. Behavioral modeling simulations show that the maximum SNDR occurs at $\beta = 0.01$, and it drops quickly when $\beta < 0.009$, whereas it decreases more gradually for $\beta > 0.015$. Considering the effect of the parasitic capacitor C_P, the SNDR only degrades by 3 dB for $\rho = 0.4$.

The equivalent internal comparator gain G can be obtained by getting the rms value of comparator input voltage, from which the signal and noise transfer functions can be derived. Fig. 7 shows the root locus of the poles and zeros of the NTF as β varies. When β increases, the poles are shifted away from the signal bandwidth until $\beta = 0.01$, while when $\beta = 0.2$ one pole is around the signal bandwidth, making the system behaving like a first-order modulator. This confirms the previous discussion that β needs to be set to a value comparable to $\frac{1}{\gamma}$ in order to guarantee the system acting as a second-order one and achieving better noise shaping. Through behavioral modeling, the optimized design parameters which have been outlined are $\gamma = 100$, $\beta = 0.01$ and $\zeta = 0.5$, since they would result in an SNDR of 95 dB, therefore ensuring enough margin for the noise and leakage current.

Compared to the second-order ΔΣ modulator shown in Fig. 3a and Fig. 3b, the proposed single-bit ΔΣ modulator avoids the detrimental inter-stage loading effect by exploiting the charge-sharing rotation. Furthermore, it is optimized by optimally outlining the system parameters γ, β and ζ through behavioral modeling. As a consequence, it can achieve SNDR comparable to that of active and hybrid topologies, in a completely digitally friendly implementation, thus amenable to nanoscale technology. For the obtained value of G, the magnitudes of the signal and noise transfer functions are plotted in Fig. 8. The NTF contains two zeros within the 80 kHz signal bandwidth, around 32 kHz and 64 kHz for a sampling frequency of 40.96 MHz. Attenuation of 84 dB for the in-band quantization noise is achieved.

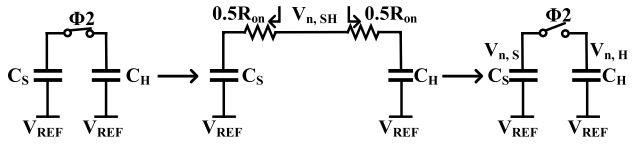

Fig. 9. Charge-sharing circuit model utilized to carry out the proposed noise analysis.

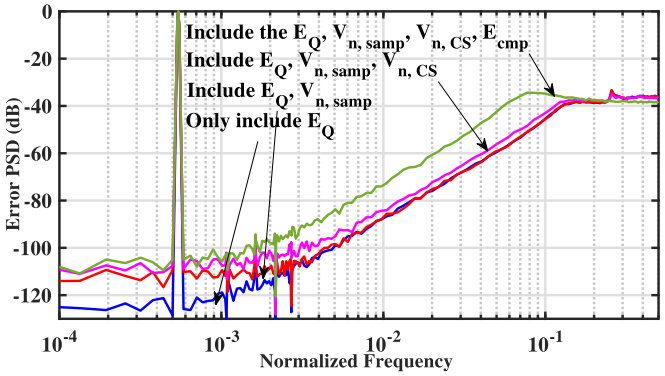

Fig. 10. Comparison of spectra obtained with modeling using different noise source contributions.

D. Noise Analysis

There are three main sources of noise within the proposed modulator, each of which experiences a different transfer function towards the converter's output. They are the kT/C thermal noise generated during the sampling and integrating operational phases, the comparator noise E_{cmp} (from both the preamplifier and the dynamic stages), and the quantization noise of the 1-bit quantizer, E_Q. Concerning the kT/C thermal noise, the portion of it generated during Φ1 ($V_{\text{n,samp}}$) exhibits the same transfer characteristic as the STF, while the one generated during Φ2 ($V_{\text{n,H1}}$) transfers to the output shaped by the function $G \cdot H_2 \cdot$ NTF. The kT/C noise generated during Φ3_1 ($V_{\text{n,H2}}$) transfers instead according to $G \cdot$ NTF, whereas the transfer function of that generated during Φ3_2 ($V_{\text{n,H2\_Z}}$) is $G \cdot \gamma \cdot H_2 \cdot$ NTF. The input-referred comparator noise (E_{cmp}) experiences a transfer to the ADC output as $G \cdot$ NTF. Due to the passive implementation of the low-pass filter, E_{cmp} is not attenuated in-band but is high-pass filtered by the $G \cdot$ NTF out-band characteristic. It is worth observing that lowering the integrator's pole frequency results in increasing G, thus leading to a higher attenuation of the in-band quantization noise. However, this would also result in higher input-referred noise of the modulator contributed by E_{cmp}.

For the aforementioned kT/C noise, $V_{\text{n,samp}}$ is the voltage noise generated and stored on capacitor C_S, which is equal to $\sqrt{\frac{2kT}{C_S}}$. The residual kT/C thermal noise ($V_{\text{n,CS}}$) is generated during the charge-sharing operation between capacitors C_S and C_H (note that C_H represents here generically either C_{H1} or C_{H2}), as shown in Fig. 9. When the switch is

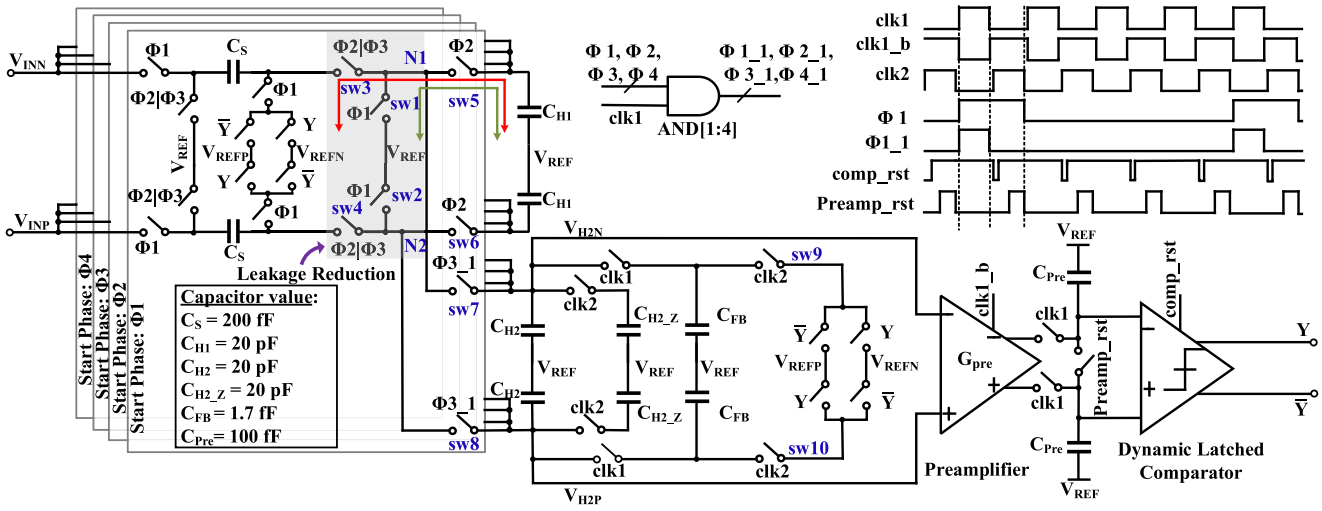

Fig. 11. Block diagram of the proposed passive $\Delta\Sigma$ modulator.

closed (i.e. during phase $\Phi2$), the thermal noise voltage is $V_{\mathrm{n,SH}} = \sqrt{\frac{kT}{C_S+C_H}}$ and the total noise charge q_{tot} is equal to $(C_S+C_H)V_{\mathrm{n,SH}} = \sqrt{kT(C_S+C_H)}$, and so the noise energy is $E_{\mathrm{tot}} = \frac{q_{\mathrm{tot}}^2}{C_S+C_H} = kT$. Because of energy conservation, when the switch opens ($\Phi2$ is de-asserted), the total noise energy distributed between C_S and C_H is fixed, implying that the total energy can be expressed as $E_{\mathrm{tot}} = \frac{q_S^2}{C_S} + \frac{q_H^2}{C_H} = kT$. Based on the charge conservation principle, the sum of the charge stored by C_S and C_H is constant, and equal to the total charge on the capacitors during phase $\Phi2$. By only considering thermal noise and by assuming, for the sake of example, that the total charge on C_S and C_H before the switch is closed is equal to zero, then when the switch opens, $q_S + q_H = 0$ ($q_S = -q_H$). Therefore, $V_{\mathrm{n,S}} = \sqrt{\frac{kT}{C_S+C_H}}\sqrt{\frac{C_H}{C_S}}$. If $C_H \gg C_S$, $V_{\mathrm{n,S}} \approx \sqrt{\frac{kT}{C_S}}$ and $V_{\mathrm{n,H}} \approx \frac{1}{\gamma}\sqrt{\frac{kT}{C_S}}$.

Considering that C_S must be traded-off between the kT/C noise and chip area, to reach an accuracy of 13 bits, a value of 0.2 pF has been chosen based on behavioral modeling simulations, which allows achieving an SNDR of 83 dB. This results in in-band $V_{\mathrm{n,samp}}$ noise of 12.7 μV_{rms}. According to the developed behavioral model, the input swing of the comparator is $\sim 100\,\mu V_{\mathrm{rms}}$. Compared to the case of $E_{\mathrm{cmp}} = 0$, the system's SNR only degrades by 3 dB to 80 dB with $E_{\mathrm{cmp}} = 90\,\mu V_{\mathrm{rms}}$ over the full-band, only part of which will be distributed in-band. This 3-dB degradation means that E_{cmp} contributes to the in-band noise equally with the kT/C noise. Spectra with different noise sources are compared in Fig. 10.

III. Circuit Implementation

As revealed in Fig. 5b, three phases are needed for the proposed passive LPF. The modulator output is updated at the rising edge of $\Phi3\_1$. Therefore, achieving higher OSR and better attenuation of the in-band quantization noise demands the choice of higher f_S, which in turn shortens the duration of the modulator operational phases, thus posing more stringent requirements on the settling time of the negative-exponential voltage transients. In order to relax the settling-time requirements for the targeted OSR and resolution, the proposed modulator exploits a pipelining technique by interleaving four parallel input sampling stages. Fig. 11 shows the proposed fully differential passive SC $\Delta\Sigma$ modulator and the timing diagram of the control signals. The passive LPF output terminals, V_{H2N} and V_{H2P}, are connected to the comparator, implemented as a cascade of the clocked preamplifier and dynamic latched comparator.

A. Pipelined Low-Pass Filter

Given the targeted OSR and signal bandwidth (80 kHz in this design), the sampling frequency f_S can be derived. The control signals $\Phi1$, $\Phi2$, $\Phi3$ and $\Phi4$ are non-overlapping clocks with a frequency of $f_S/4$, while clk1 and clk2 are also non-overlapping clocks running at f_S. The rising edges of Φk ($k = 1, 2, 3, 4$) are synchronous with the rising edges of clk1. During $\Phi1$, capacitor C_S belonging to the sampling stage, whose starting phase is $\Phi1$, samples the voltage difference between the input signal and the 1-bit output of the feedback DAC, and then it shares its charge with capacitor C_{H1} during phase $\Phi2$, and with C_{H2} and C_{FB} during phase $\Phi3\_1$. Similarly, capacitor C_S within the neighboring sampling stage whose starting phase is $\Phi2$, also samples the voltage difference between the input signal and the 1-bit output of the feedback DAC during phase $\Phi2$, then it shares its charge with C_{H1} during $\Phi3$, and finally with C_{H2} and C_{FB} during $\Phi4\_1$. In the end, C_S capacitors within the sampling stages, whose starting phases are $\Phi3$ and $\Phi4$, undertake the same sequence of operations. As C_{H2} and C_{H2_Z} are shared among the different phases, the charge-sharing operation between them is controlled by clk2. Therefore, the modulator output is updated at each new phase rather than at each $\Phi3\_1$.

Considering the settling behavior which occurs during the charge sharing between capacitors C_S and C_H (see Fig. 9) when $\Phi2$ is asserted, the voltages across C_S and C_H at the end of $\Phi2$ (V_{C_S} and V_{C_H}, respectively) can be expressed as:

$$V_{C_H}[n] = V_{SH} \cdot (1 - e^{\frac{-T_{\Phi2}}{\tau}}) + V_{C_H}[n-1] \cdot e^{\frac{-T_{\Phi2}}{\tau}} \quad (10)$$

$$V_{C_S}[n] = V_{SH} \cdot (1 - e^{\frac{-T_{\Phi2}}{\tau}}) + V_{C_S}[n-1] \cdot e^{\frac{-T_{\Phi2}}{\tau}} \quad (11)$$

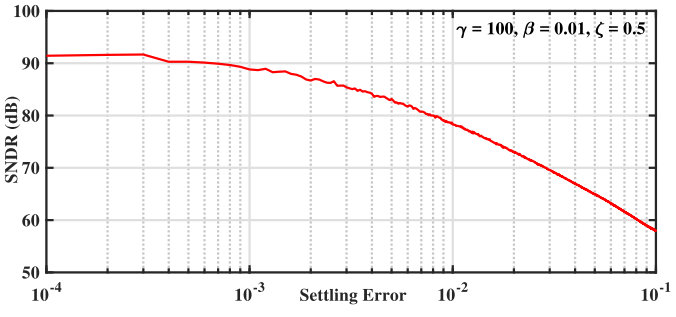

Fig. 12. Behavioral simulation of SNDR versus normalized settling error.

where $V_{SH} = \{C_S \cdot V_{C_S}[n-1] + C_H \cdot V_{C_H}[n-1]\}/(C_S + C_H)$ is their theoretical asymptotic value ($V_{C_S}[n-1]$ and $V_{C_H}[n-1]$ are the voltage values at the end of the previous phase Φ_2), $\tau = R_{on}(C_S + C_H)$ is the time constant (R_{on} is the switch on-resistance) and $T_{\Phi 2}$ is the time duration of phase $\Phi 2$. In other words, $T_{\Phi 2}$ is the available time for the internal nodes to settle to their asymptotic value, while $e^{\frac{-T_{\Phi 2}}{\tau}}$ in (10) and (11) is the residual (normalized) settling error due to charge sharing, under the modeling assumption of the charge sharing network as a 1st-order RC network. Based on behavioral modeling simulations, SNDR of the proposed modulator drops gradually when the settling error is larger than 0.001, as shown in Fig. 12 for the chosen OSR of 256.

Assuming for the moment that the proposed pipelining technique was not exploited, the modulator would be characterized by a single sampling phase and two integration phases, each with the same duration T_{phase} equal to $1/(3f_S)$ (i.e. the period $1/f_S$ is equally distributed for the sampling, 1st-stage and 2nd-stage integration). Low kT/C noise demands an higher capacitance ($C_S = 200\,fF$), which in turns requires large enough CMOS switches to minimize R_{on} so as to guarantee a sufficiently fast settling of the filter's internal nodes. This, however, would increase the off drain current of the turned-off CMOS switches and increase the load capacitance on the digital control signal lines. Exploitation of the above-mentioned pipelining technique, characterized by a time interleaving factor n ($n = 4$ in this implementation), allows T_{phase} to be beneficially extended n times, with a maximum duration of $1/f_S$. This relaxes the requirement on the switches' channel on-resistance by $n\times$, which is beneficial in limiting the detrimental impact of the their leakage current in off-state (causing the discharge of capacitors in hold-state) and in reducing the load capacitance of the digital control signal generator. At the same time, each of the control signals $\Phi 1$, $\Phi 2$ and $\Phi 3$ operates at a rate $n\times$ slower than the sampling clock (f_S/n), thus helping to further reduce the power consumption of the digital control signal generator.

Another advantage brought by the pipelining of the modulator loop filter is that the longer duration of the phases allows relaxing the slew rate and bandwidth of the comparator's preamplifier, which also promotes a lower power consumption. As the preamplifier is the only component in the modulator which dissipates static power, its power efficiency can be increased by sampling its input voltage and generating a new corresponding output during each of the three phases of the IIR2 filter operation, rather than performing preamplification during only one of the phases and remaining idle during the others (thus dissipating static power). Therefore, the time interleaving factor should be $n \geq 3$ to allow the preamplifier to perform preamplification for all the phases. However, as the maximum phase length is upper bounded by $1/f_S$, choosing $n > 3$ does not help with further extending T_{phase}. Due to the higher complexity in generating an odd number of phases, $n = 4$ is chosen so as to simplify the design of waveform generator. Considering that the relatively large integrating capacitors (C_{H1} and C_{H2}) and the comparator will be shared among the four interleaved filter stages, the overall area of the modulator is only slightly larger (i.e. $< 1.1\times$ of a modulator with a single-stage filter implementation).

The sampling capacitors C_S are implemented using a 200 fF metal-oxide-metal (MOM) capacitor, while the integrating capacitor $C_{H1,2}$ consists of 100 units of C_S, thus improving matching. Based on a 1000-run Monte Carlo simulation, the local mismatch between C_S sampling capacitors is equal to 0.05%. To account for extra margin, an accuracy of 0.1% has been considered for the behavioral modeling simulations, showing an SNDR standard deviation of 1.3 dB for the proposed modulator. Any deviation in C_{FB} from its nominal value can be seen as a variation in parameter β (nominally equal to 0.01), which can be tolerated if in between 0.009 and 0.015 as per Fig. 6 (i.e. the range of β for which the modulator SNDR is reasonably invariant) and, therefore, the parasitic capacitor added to C_{FB} needs to be carefully sized during the schematic and layout design phases. Capacitor C_{FB} is implemented as the series of 10 units of 17 fF, so as to keep the local mismatch to about 0.05%. The parasitic capacitance at the top-plate of C_{FB} is in the range between 1.02 fF and 1.25 fF, as observed from PVT simulations. Therefore, β can approximately be controlled between 0.0136 and 0.0148, thus ensuring a reasonably invariant SNDR, as visible from Fig. 6.

Because of the passive implementation adopted for the pipelined loop filter, the signal voltage swings inside it are relatively low (e.g. as low as $100\,\mu V_{rms}$ at the input of the comparator's preamplifier). This renders the topology more sensitive to the off-current of CMOS switches, which degrades in the nanoscale CMOS technology. However, such small voltage swings allow simplifying the design of switches within the proposed LPF, which are all transmission gates, except those within the feedback path. For what concerns the impact of the off leakage current of CMOS switches, given the fact that the small signal voltage swings imply nearly zero voltage drops across capacitors C_{H1} and C_{H2}, the impact of the leakage current is larger when one terminal of the transmission gates is connected to V_{REFP} or V_{REFN} (e.g. almost half the supply away from V_{REF}), while it is smaller when it is connected to V_{REF}. Therefore, without the part in the grey-shaded rectangle in Fig. 11, the harmful contribution in terms of leakage current arises from the CMOS switches around the 1-bit feedback path. For the feedback path to the 1st-stage integrator, in the example of the sampling stage whose starting phase is $\Phi 1$, but without the leakage reduction circuitry in the grey-shaded rectangle, the off currents from its switches (i.e. sw5, sw6,

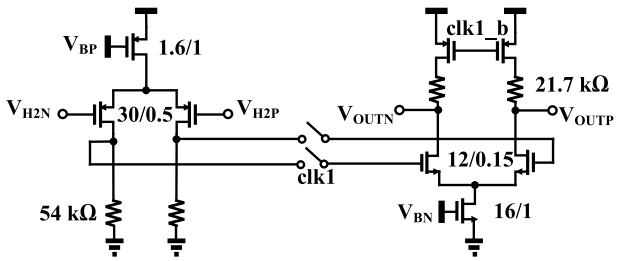

Fig. 13. Clocked preamplifier.

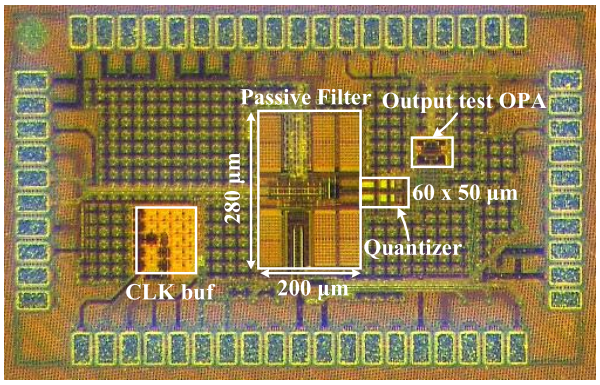

Fig. 14. Chip micrograph.

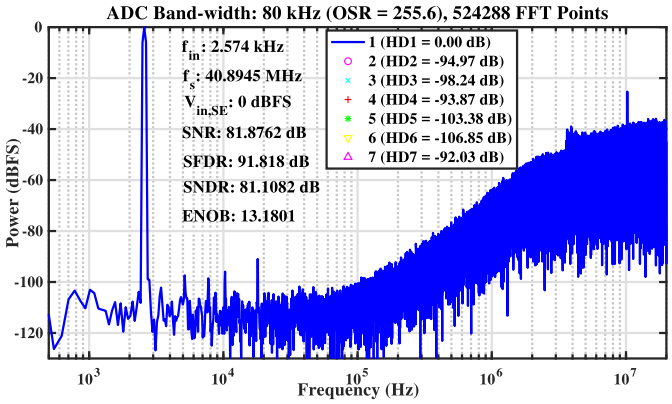

Fig. 15. Measured spectrum with a 2.574 kHz full-scale sinusoidal input.

sw7 and sw8) behave as a feedback path for both C_{H1} and C_{H2} during phase Φ1, and its feedback parameter cannot be precisely controlled during the design. Therefore, a leakage reduction mechanism is necessary to minimize the detrimental impact on the modulator performance. A way of exploiting it is represented by the switches marked as sw1, sw2, sw3 and sw4 in the grey-shaded rectangle in Fig. 11, which serve the purpose of setting the voltage of nodes N1 and N2 to the reference voltage V_{REF} during phase Φ1. This helps reducing the off-state current of the transmission gates, such as sw5, sw6, sw7 and sw8, connected to capacitors C_{H1} and C_{H2}. For the feedback path to the 2nd-stage, given the small value of C_{FB}, which is around 1.7 fF, the size of the switch connected to it (i.e. sw9 and sw10) can be smaller without introducing any time-constant limitations, and thus the impact of the switch off leakage current is negligible.

B. Clocked Preamplifier

The comparator consists of a preamplifier stage followed by a dynamic latched comparator. The former serves the purpose of mitigating the offset and noise (including the kick-back) of the latter. It could therefore be assumed that the input-referred noise E_{cmp} and offset are mainly contributed by the preamplifier. Similarly to the SC loop filter and custom digital logic, the dynamic latched comparator only consumes dynamic power consumption, while the preamplifier is the sole component in the system which dissipates static power. As stated earlier, a way of improving its power efficiency is represented by the exploited pipelining technique, which allows the operation of comparator during each phase. However, the preamplifier is still in idle state (e.g. no comparison performed) during half of each phase duration. To reduce the dissipated power during this idle period, the topology chosen for the preamplifier, as shown in Fig.13, consists of a continuous-time front-end stage followed by a clocked amplifier, which is indeed switched off during such idle half phase. To achieve a better isolation between the passive loop filter and the switching activity of the downstream comparator, the clocked topology is used for the 2nd-stage of the preamplifier.

The input differential pair of the continuous-time 1st-stage of the preamplifier is implemented using large-size PMOS devices to reduce the input-referred offset and 1/f noise. The total dc gain of the preamplifier (G_{pre}) when clk1 is logic high is 38 dB, which is large enough to amplify the filter output and to neglect the impact of metastability of the dynamic latched comparator. The implemented comparator is designed with input-referred noise (full-band integrated) below $90\,\mu V_{rms}$, which is the value outlined through behavioral modeling in order to allow the modulator to achieve ENOB >13 bits. As the $\Delta\Sigma$ modulator is a negative feedback loop, the time-averaged single-bit output tracks the input voltage signal even though there is a dc offset at the comparator input. As long as the offset is small enough so as not to cause the saturation of the comparator, the system's performance is not affected. This has been verified via behavioral modeling and circuit simulations.

IV. Measurement Results

The proposed ADC is implemented in a low-power flavor of TSMC 28-nm CMOS technology. The chip micrograph in Fig. 14 shows the core ADC which occupies an area of 0.059 mm^2 and is made of the switched-cap passive loop filter and the 1-bit quantizer, as well as the clock buffer and an output test operational amplifier (OPA).

Fig. 15 shows the measured output spectrum for a 2.574 kHz full-scale sinusoidal input signal, demonstrating SNDR and SFDR of 81.1 dB and 91.82 dB, respectively, over a signal bandwidth of 80 kHz and at OSR of 255.6. This proves that the proposed modulator achieves good linearity even at full-scale. The two-tone output spectrum shown in Fig. 16 uses two input sinewaves at 20.046 kHz and 25.0138 kHz and with -6 dBFS amplitude. All of the second and third intermodulation

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART PASSIVE AND HYBRID ΔΣ MODULATORS

	[8]	[10]	[9]	[12]	[14]	[16]	**This Work**
Type	hybrid CT	hybrid CT	hybrid DT	hybrid DT	passive DT	passive DT	**passive DT**
Tech (nm)	250	65	130	65	130	65	**28**
Frequency (MHz)	150	320	640	13	102.4	0.5	**40**
Bandwidth (kHz)	2000	2000	10000	25	100	0.5	**80**
OSR	37	80	32	260	512	500	**256**
Order	5th	3rd	3rd	3rd	2nd	2nd	**2nd**
Power (μW)	2700	256	5500	73.6	1275	0.43	**101.5**
peak SNDR (dB)	63.4	69.1	56	88.2	74.1	65	**81.11**
DR (dB)	68	76.2	54	91	80.5	65	**83.6**
FoM$_{W,peak}$(fJ/c-s)	558	27.5	533	70	1538	290	**68.4**
FoM$_S$(dB)	156.7	175.1	146.5	176.3	159.4	155.6	**172.5**
Area (mm^2)	0.42	0.013	N/A	0.1	0.1	0.125	**0.059**

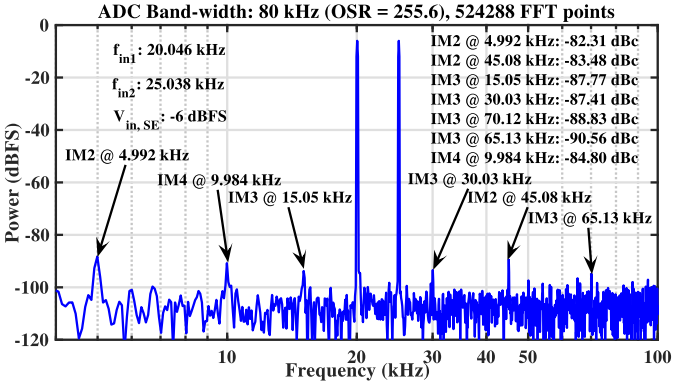

Fig. 16. Output spectrum of the modulator for a 20 kHz and 25 kHz two-tone input signal.

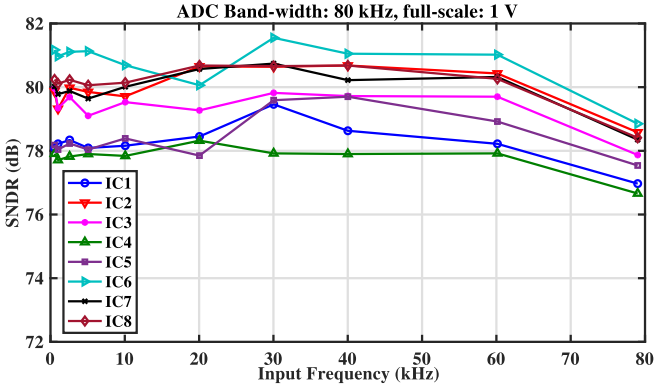

Fig. 18. Measured SNDR versus frequency for a full-scale sinusoidal input.

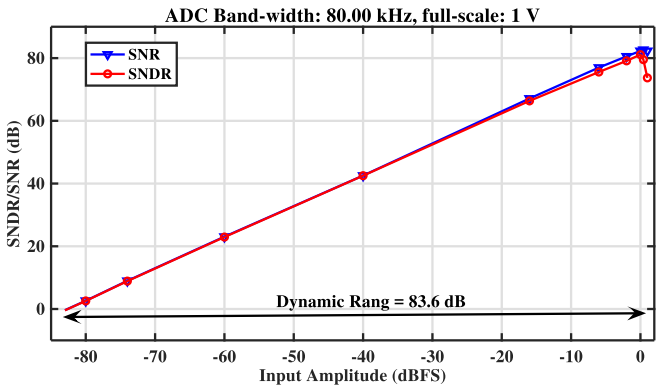

Fig. 17. Measured SNDR versus amplitude at 2.574 kHz frequency for a sinusoidal input.

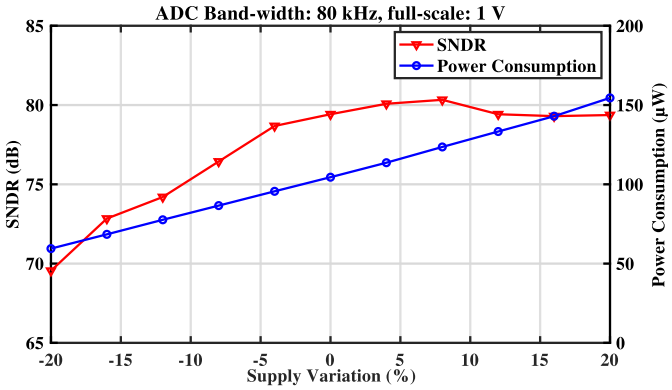

Fig. 19. SNDR and power consumption versus ±20% supply variation.

products fall below -80 dBc. The SNDR and SNR versus the amplitude of an input sinewave at 2.574 kHz is plotted in Fig. 17, indicating the the proposed ADC can achieve a DR of 83.6 dB.

Performance of the proposed ADC has been measured across multiple dies. Fig. 18 shows the SNDR versus frequency when applying a full-scale sinewave at the input. The minimum measured SNDR is 76.5 dB at 79 kHz input frequency, while the measured SNDR's variation across different dies is within 3 dB, mainly caused by the spread in the preamplifier's gain G_{Pre} and the comparator's noise E_{cmp}.

The ADC performance is also measured versus a supply variation of up to ±20% from nominal (while scaling the input sinusoidal signal amplitude proportionally). The SNDR and power consumption with a 20.046 kHz full-scale input sinewave versus supply variation are shown in Fig. 19. The SNDR drops gradually at lower supplies due to the fact that the preamplifier's input-referred noise increases while its gain decreases, which in turn also means less attenuation of the noise from the following dynamic latched comparator. At the nominal supply voltage, the digital control signal generator, including the waveform generator, the non-overlapping clock generator and the digital buffers, altogether

consumes 41.2 μW. The passive LPF consumes 19.6 μW, while the preamplifier and the dynamic latched comparator consume 36.6 μW and 4.1 μW, respectively. Finally, Table I summarizes the performance of the proposed passive $\Delta\Sigma$ modulator and compares it to state-of-the-art in discrete-time passive and hybrid $\Delta\Sigma$ modulators. Compared to the passive DT designs, our design achieves the best FoM_W and the smallest area, demonstrating the SNDR of 81.1 dB using a second-order CIFB loop filter topology, and at a much lower OSR.

V. Conclusion

A second-order passive $\Delta\Sigma$ modulator leveraging on a charge-sharing rotation technique to suppress the inter-stage loading effect within the switched-capacitor loop filter is presented. An independent additional feedback path and an additional stage introducing a zero in the transfer function are added to the 2nd-stage of the passive LPF and optimized through behavioral modeling simulations so as to increase the attenuation of the in-band quantization noise and to improve stability. A pipelining technique is proposed, in which four parallel switched-cap sampling stages are time-interleaved so as to concurrently relax the voltage settling time constraints of internal nodes and improve the modulator power efficiency. With an OSR of 256, the proposed modulator achieves SNDR of 81.1 dB over a signal bandwidth of 80 kHz, while dissipating 101.5 μW and occupying 0.059 mm^2.

Acknowledgment

The authors would like to thank TSMC for chip fabrication. They also thank Viet Anh Nguyen and Jianglin Du for technical discussions, Paulo Vieira for lab assistance, and MCCI for technical support.

Appendix

The STF and NTF, expressed by (5) and (6), of the topology shown in Fig. 3a, can be obtained from the charge-redistribution scenarios which take place during different phases. The input information is sampled by C_{S1} during $\Phi1$. During $\Phi2$, voltage V_{OUT1} (at the node connecting C_{S1} and C_{H1}) can be expressed as:

$$V_{OUT1}(z) = (1-\alpha_1)(V_{IN} - Yz^{-1}) + \alpha_1 V^*_{OUT1} z^{-1} \quad \text{(a1)}$$

in which $\alpha_1 = \frac{\gamma}{\gamma+1}$ ($\gamma = \frac{C_{H1}}{C_{S1}}$), V^*_{OUT1} is the voltage on the top-plate of C_{H1} at the end of $\Phi1$, and Y is the output of the modulator.

During the next phase $\Phi1$, the voltage V^*_{OUT1}, now at the connection node between C_{S2} and C_{H1}, can be expressed as:

$$V^*_{OUT1}(z) = (1-\alpha^*)(V_{OUT2} - Y)z^{-1} + \alpha^* V_{OUT1} \quad \text{(a2)}$$

in which α^* is $\frac{C_{H1}}{C_{S2}+C_{H1}}$, V_{OUT1} is the voltage on the top-plate of C_{H1} at the end of $\Phi2$. This equation shows that during $\Phi1$, the voltage at the top-plate of C_{H1} is attenuated by a factor of α^*, and it is *also* affected by the feedback factor $1-\alpha^*$ from the 2nd-stage, which is caused by C_{S2} being directly charged with C_{H1}.

During the next phase $\Phi2$, the voltage V_{OUT2} at the top-plate of C_{H2} can be expressed as:

$$V_{OUT2}(z) = H_2 V^*_{OUT1} \quad \text{(a3)}$$

where H_2 is the transfer function of the 2nd-stage integrator. Then, $Y = G \cdot V_{OUT2} + E_Q$, in which E_Q is the quantization noise and G is the gain of the comparator. From these equations, the STF and NTF in (5) and (6) can be derived.

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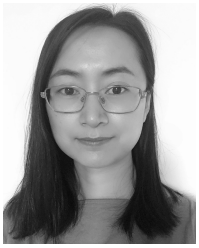

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