Bootstrapped Driver and the Single-Event-Upset Effect

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***Abstract*—As VLSI circuits are progressing in very Deep Submicron (DSM) regime without decreasing chip area, the importance of global interconnects increases but at the cost of performance and power consumption. This work proposes a low power circuit for driving a global interconnect at voltages close to the noise level. In order to address ultra-low power (ULP) design limitations, a novel driver scheme has been configured. This scheme uses a bootstrap circuitry which boosts the driver's ability to drive a long interconnect with an important feedback feature in it. Hence, this approach achieves two objectives: improving performance and mitigating power consumed. Those achievements are essential in designing ULP circuits along with occupying a smaller footprint and being immune to noise, observed in this design as well. These have been verified by comparing the proposed design to the previous and traditional circuits using a simulation tool. Additionally, the boosting based approach has been shown beneficial in mitigating the effects of single-event upsets (SEU), which are known to affect DSM circuits working under low voltages. As a result, the proposed circuit demonstrates a promising solution to address the energy and performance issues related to scaling effects on interconnects along with soft errors that can be caused by neutron particles.**

***Index Terms*—ultra-low power (ULP), interconnect, charge pump, driver, boosting, single event upset (SEU).**

I. Introduction

THE rapid development of energy-constrained applications has made low power design, a primary concern. This is a paradigm shift from traditional performance-led design to emerging energy-constrained system development. Novel applications such as Internet of Things (IoT) devices, wearable computing and smart grids mainly require longer energy source life and small silicon costs; on the other hand, their performance is typically considered a secondary concern [1], [2]. Operating of such applications is based on a supply voltage of battery sources or scavenging energy from the environment. Therefore, devices involved in applications of IoT requiring to consume a certain amount of power for the sake of securing extended operability [2], as in Fig. 1. This requires driving research towards engineering new solutions which are expected to run at low voltages of 300mV or much less [3].

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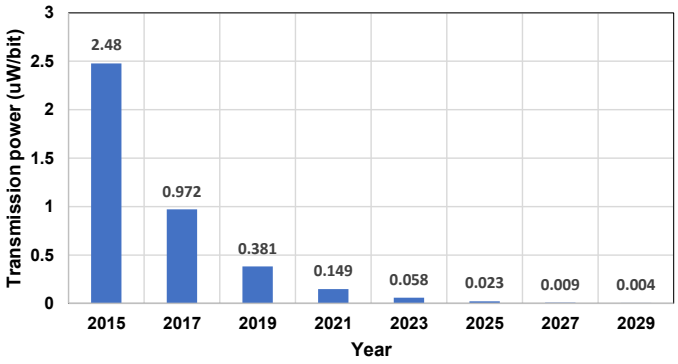


Fig. 1: Trend of limitations for power consumption in the IoT environment [2].

Recently, scaling the power supply has become an effective way to reduce energy consumption in digital systems. Supply voltages less than the threshold voltage of the Complementary Metal Oxide Semiconductor (CMOS) circuits have emerged showing the ability to meet the requirements of ultra-low power regime (ULP). This approach is called the sub-threshold logic circuit. However, since CMOS scaling reaching its limits, the issue of global and long interconnects has become an important consideration due to the problem of capacitance [4].

At sub-threshold, this effect is even worse when the conventional CMOS driver needs to be as large as possible to deal with the leak of driving efficiency associated with a scaled power supply [5]; in addition, it requires to bear with the static current I_{off} issue which is increasing at this region, particularly, in the nanometre regime [6]. Another issue comes with this advancing in semiconductor technology is that the reliability of electronic system has become more susceptible to transient faults caused by the effects of neutron and alpha-particle strikes [7]. A number of investigations have shown that the transient faults are the predominant cause of failures experienced by the state-of-the-art computer systems [8], [9]. Thus, from a system reliability perspective, it is important to consider this type of errors in the analysis of the circuit robustness.

In this work, in order to address these limitations, the bootstrap method is proposed because of its capability to improve the driving ability with adding feedback feature to control power consumption, as will be shown later in the results section.

By producing a voltage swing nearly of $2V_{DD}$ to -V_{DD} for the gate to source transistor voltage (V_{gs}) of the NMOS and PMOS independently, the proposed CMOS inverter provides better

performance and reduces leakage current. Hence, according to the formula for I-V in a sub-threshold region [10], [11], I_{off} will be reduced exponentially. Furthermore, in order to ensure the reliability of the design against the radiation-induced faults such as SEU, an investigation for its impact has been performed. Therefore, the main **contributions** of our proposed approach to the ULP applications are as follows:

1) This work presents an improvement in power dissipation, a smaller footprint occupying, control leakage circuits and a robustness to alpha-particle strikes.
2) The approach here adds an important feature of robustness to the circuit design by connecting the pumped output of driver to (feed) pumping components in the circuit.
3) Simulations based on MATLAB software illustrated the obtained advantages of the suggested approach.
4) A number of experiments have been carried out using a 90nm UMC toolkit as an emulated environment to investigate the proposed design.

To the best of our knowledge, this is the first approach that investigates a bootstrapped driver which incorporates feedback configuration at the output and evaluates it in term of SEU tolerance.

The rest of the work is organized as follows. A brief introduction to the sub-threshold mode circuit, the charge boosting and the SEU, which can happen in Very Large Scale Integration (VLSI) circuits, has been presented in Section II. Section III introduces the operation of the circuit and its structure. Section IV describes the implementation considerations and presents the circuit design and initial simulation results for this circuit comparing it with existing designs, as well as with a conventional driver from the point of view of energy consumption and delay. Finally, the conclusions are presented in Section V.

II. Background

In this section, a background is introduced in the context of the work regarding the basic concepts of sub-threshold mode circuits, the boosting charge circuits and errors caused by the Single Event Upset.

A. Sub-threshold mode circuits

The operation region of any circuit depends on the supply voltage at which the circuit operates. This region of operation can be shifted from super-threshold to sub-threshold if the supply voltage is reduced to less than the threshold voltage (V_{th}). The supply voltage considerably above V_{th} and large current drives are what characterize the regime of the super-threshold, also known as the strong inversion region. Contrary, the regime of the sub-threshold, or the weak inversion region, is well-known by less current drives and an operating voltage below V_{th}. Between these two regions, there is a region called the moderate inversion which has a supply voltage near V_{th} and higher current drives as compared to the sub-threshold regime [12].

In the region when the voltage level of circuits is lower than the threshold voltage ($V_{DD} < V_{th}$), the channel between the drain and source region ceases. Nevertheless, the circuits have the ability to operate correctly owing to a steady leakage current flow through the transistor [13]. This happens due to some electrons in the source can overcome barriers and diffuse to the drain. As the gate voltage V_{gs} approaches V_{th}, the flux can become effective particularly in ultra-low power integrated circuits [13]. The sources of this current are mainly four: gate leakage (I_{GATE}), gate induced drain leakage (I_{GIDL}), diode reverse bias junction leakage (drain to the substrate) (I_{REV}) and sub-threshold leakage (I_{sub-th}), as shown in Fig. 2. Given this type of current is quite small compared to the transition current of the super-threshold, the dissipation of power in sub-threshold circuits is considerably reduced besides a certain delay [14].

The sub-threshold leakage I_{sub-th} is the dominant component amongst all leakage current components, which flows through the transistor from the drain to the source. This occurs in the weak inversion mode when the operating applied voltage V_{gs} to the transistor is less than its threshold voltage V_{th} [15]. The sub-threshold current can be considered as the total drain current in the sub-threshold regime [13], where its value can be given by the following equation [16].

$$I_{sub-th} = \mu_{eff} C_{ox} \frac{W_t}{L_{eff}} (m-1) V_t^2 e^{\left(\frac{V_{gs}-V_{th}}{m V_t}\right)} \left(1 - e^{\left(\frac{-V_{ds}}{V_t}\right)}\right) \quad (1)$$

where μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, W_t is the device width, L_{eff} is the effective length of the device, V_t is the thermal voltage, m is the sub-threshold slope factor and V_{ds} is a voltage of the drain-source. In this model, the first term is basically the current flows by diffusion, while the parenthetical term represents the roll-off in current which happens when V_{ds} equals a few times V_t. Thus, the sub-threshold current depends on different factors and varies exponentially with the gate voltage V_{gs}.

This expression (1) has been discussed further [10], [17] to lead to identify sub-regions in the sub-threshold region. Accordingly, the drain current expression has been modified to interpret the transition zone between sub-threshold and saturation, namely the triode region:

$$I_d = \mu C_{ox} \frac{W}{L} \left((V_{gs} - V_{th}) V_{ds} - 0.5 V_{ds}^2 \right) \quad (2)$$

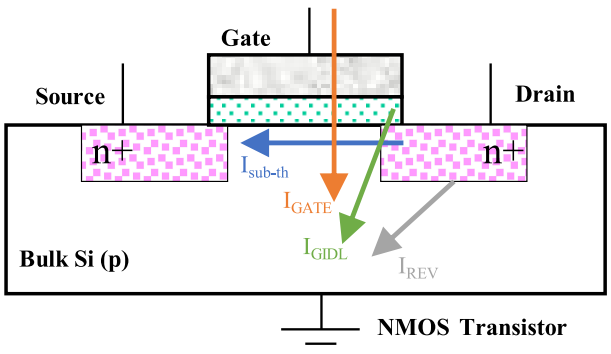


Fig. 2: MOS device's leakage current sources.

where I_d is the current flowing from drain to source. This empirical model provides decent matching with the empirical data if its parameters are chosen carefully [10].

This relationship between I_{sub-th} and the applied voltage in this regime will exhibit almost linear behaviour in a logarithmic plot. The slope S_t of this linear behaviour is another important characteristic of the sub-threshold region since it represents the effectiveness of the transistor to turn off when V_{gs} is below the threshold voltage. It is defined as [15]:

$$\frac{1}{S_t} = \frac{\partial(\log I_d)}{\partial V_{gs}} \tag{3}$$

S_t at the end will equal $mV_t \ln(10)$, which is given in millivolts per decade. Its ideal value at room temperature is $60\text{mV}/\text{decade}$. In other words, in order to decrease or increase the current magnitude a one decade in the sub-threshold region, it needs reducing or raising in V_{gs} by no less than 60mV.

B. The charge pumping principle

In our approach, the bootstrap has been used based on a charge pump that is a type of DC-to-DC converters, which utilities a capacitor as a charge holder to generate a voltage higher than the power source voltage [18]. Although the design of this technique is electrically a simple circuit, it is able to achieve a level of efficiency reaching 90-95% [19]. To see how this is possible, consider a simple 4-stages Dickson charge pump as shown in Fig. 3. When the signal $\phi 1$ is low, D1 will charge C1 to V_{in}. When $\phi 1$ goes high, the top plate of C1 is pushed up to $2V_{in}$. D1 is then turned off and D2 turned on and C2 begins to charge to $2V_{in}$. On the next clock cycle, $\phi 1$ again goes low and now $\phi 2$ goes high, the top plate of C2 is pushed to $3V_{in}$. D2 switches off and D3 switches on, charging C3 to $3V_{in}$ and so on with charge passing up the chain hence, the name 'charge pump'. The final diode-capacitor cell represents a peak detector and not a multiplier in the cascade [19].

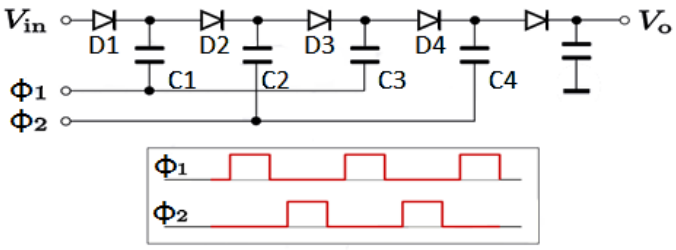


Fig. 3: Four-stages Dickson charge pump [19].

This technique increases the supply voltage efficiently, however, it only includes the positive part of the voltage; that is, V_o will swing just from 0 to 2 or 3 V_{in}. Therefore, we have modified the cross-coupled MOSFET voltage doubler to give a full swing from -V_{DD} to $2V_{DD}$.

C. Single event upsets (SEU)

Soft errors generated by the radiation impact become increasingly a major concern with improving the scale of microelectronic design to nanometer era. What induces a fault in integrated circuits is the energy transfer from high energy particles (i.e. electrons, protons, energetic heavy ions and alpha particles) to the impinged material. This happens through indirect or direct ionization mechanisms. Amongst these energetic particles, high-speed neutron and alpha particles which emit from cosmic rays and packaging materials, respectively, are the main sources of SEU in semiconductor devices. However, by using packaging materials which have fewer alpha particles emission, neutrons surpasses alpha particles as the cause of soft errors since 1990 [20].

This event affects the functioning of the digital parts of a circuit in a certain aspect, which eventually causes incorrect results. When one of these high-energy particles penetrates a sensitive region such as the area near the reverse biased drain junction of a transistor, electron-hole pairs are formed, as demonstrated in Fig. 4. The amount of energy to create

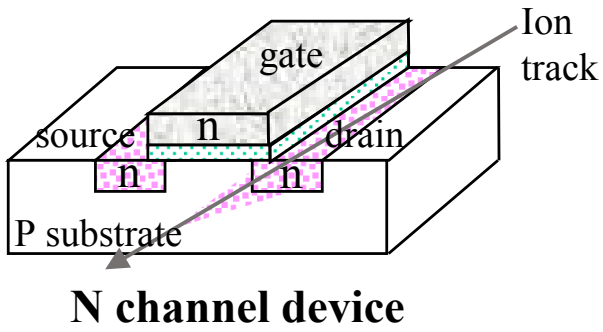


Fig. 4: Particle strikes an NMOS device.

the electron-hole pairs has been recorded by many studies to investigate this phenomenon. Since 1990, the lowest observed energy causing a glitch, termed Linear Energy Transfer (LET), was $15\text{MeV}\cdot\text{cm}^2/\text{mg}$. While, at a high level of this value, the duration of the measured Single Event Transient (SET) was 40ns which was adequate to introduce an error at the system level. In 2004, however, LET by value at $2\text{MeV}\cdot\text{cm}^2/\text{mg}$, was enough to cause a transient pulse with a duration of a few nanoseconds [9], [21] because of the technological scaling [22]. This confirms that with every new technology node, the susceptibility of circuits to the effects of particle strikes rises.

The particle minimum energy which creates a voltage transition of sufficient strength to switch a logic value on a node is given by [23]:

$$E_{LET_{min}} = 3.6\text{eV}\frac{Q_{crit}}{q} \tag{4}$$

where 3.6eV is the electron-hole pair energy required to generate in silicon and Q_{crit} is the critical charge which is the necessary amount of charge to set off a change in the logical level. The Q_{crit} value of any struck node can be determined as follows:

$$Q_{crit} = C_N V_{DD} + I_{MDP} T_{pulse} \tag{5}$$

where I_{MDP} is the maximum drain conduction current of the PMOS transistor, C_N is the capacitance of the affected node and T_{pulse} is the the transient pulse width [9], [22], [24].

From (5), it can be seen that the applied V_{DD} to the node and its capacitance have a direct impact on the Q_{crit} value. Accordingly, decreasing the supply voltage and the node capacitance as a consequence of the technology scaling down will reduce the Q_{crit} value of the node. This leads to an increase in the susceptibility to radiation-induced soft errors in new design technologies.

III. Proposed CMOS inverter

The bootstrap driver fundamentally consists of two combinations. The first one is a pre-driver comprising of:
a) an inverter (PM1 and NM1) for the bootstrap control,
b) pre-charging and pre-discharge transistors (PM2 and NM2) for the bootstrap capacitors C_{bootP} and C_{bootN} and, finally,
c) a driver (PM3 and NM3) for the boosted output.
The second part and how it is fed back by the boosted voltage represents the main difference with reported bootstrap circuits along with the low hardware overhead. In other words, this part has been implemented with minimal components and without the need for additional circuitry such as level shifter and extra V_{DD} supplies. This combination has the ability to theoretically provide a voltage swing between -V_{DD} and $2V_{DD}$ in order to address the fundamental limitations of the leakage current and poor driving capability in sub-threshold regime. This is through shifting the circuit operation region to above the applied supply voltage.
The second combination is a normal buffer (inverter) with PMOS and NMOS transistors that are driven by the boosting voltage circuit (the first combination). Fig. 5 shows the circuit scheme of the proposed driver and its main components, where the pre-driver is the circuit on the left which uses the capacitors to boost the voltage. Then the buffer, the circuit on the right, is used to drive the interconnect with a sub-threshold voltage swing from GND to V_{DD}.
Given the exponential behaviour of the current toward the applied voltage in the sub-threshold region, 10 times higher driving current can be expected with at least 60mV boost in the driver voltage [12]. At the same time, this extra voltage suppresses the leakage current, while the PMOS or NMOS is turned off. Additionally, regarding the hardware overhead, the proposed design has low effect.
We have used this approach to improve the driving capability of the CMOS circuits due to the increase in the sub-threshold swing which increases the driving current exponentially. In this design, using the charge pump as a booster (bootstrap) for the final stage (the second combination) means that its effect will be implicit; in other words, the boosted swing voltage will not be used to charge and discharge the capacitor load (CL), hence this will not have a considerable effect on the circuit power consumption.

A. Circuit operation

The schematic of our approach is highlighted in Fig. 5. There are significant nodes in the design which were highlighted and named VV_{DD}, VGND and B-out. VV_{DD} and VGND are the boosted nodes and act as virtual supply voltage and ground for the PM3 and NM3 driver, respectively. B-out

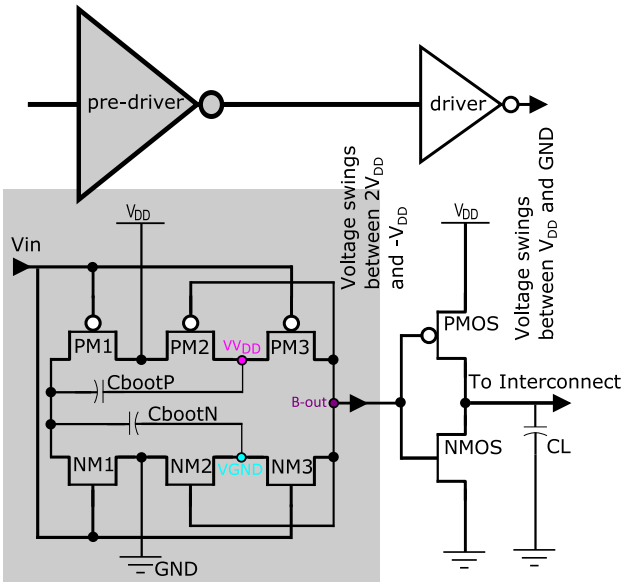
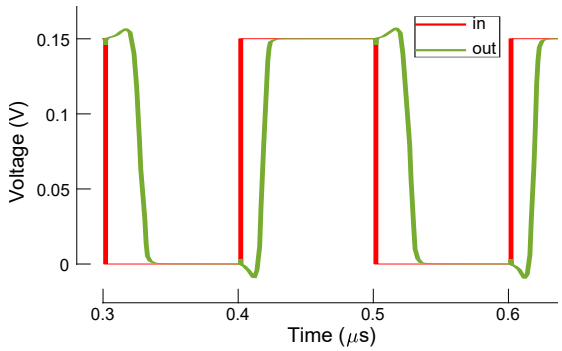


Fig. 5: Circuit of the proposed driver.

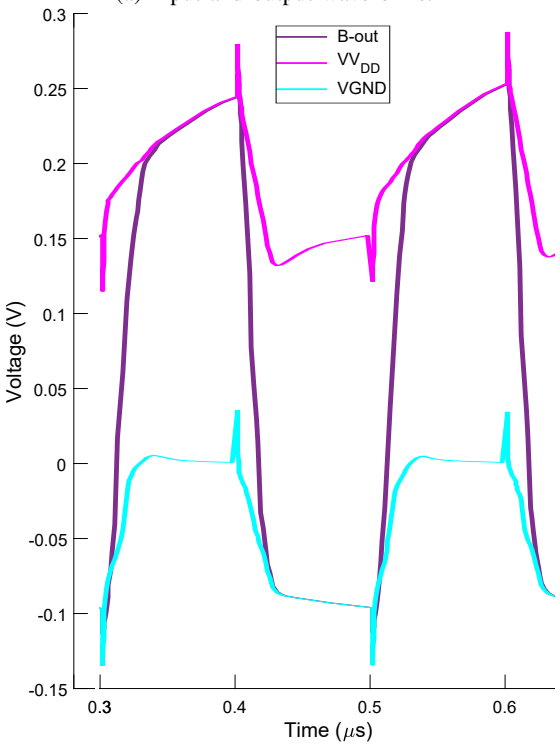
node is boosted above VV_{DD} and below ground depending on voltages of the former boosted nodes.
Fig. 6 displays transient waveforms of the significant nodes besides the input and output signals with a power supply of 150mV. Based on this figure, when V_{in} goes low, the output of PM1 and NM1 inverter will be pushed up. It bootstraps VV_{DD} above V_{DD} through boost capacitor C_{bootP} that assumes to be pre-charged a voltage near the V_{DD} from the previous cycle. Meanwhile, PM3 is turned on to pass the bootstrapped voltage (above V_{DD}) to B-out. The voltage of B-out does not merely drive NMOS of the second stage better but also turn off PMOS better to reduce the leakage current beside switch on NM2 to the pre-discharge of VGND (C_{bootN}).
A similar but opposite operation takes place in the second state when V_{in} goes high, that is VGND boosted below ground which initially has a voltage of 0 V. At the same time, NM3 is turned on, so the boosted signal at VGND passes to B-out to drive PMOS of the next stage in order to pull up the capacitive load CL. Not only that but also it turns on PM2 better to pre-charge C_{bootP} along with closes NMOS and NM2 better to reduce the leakage current.
The size (W/L) of transistors (PM1, PM3, NM1 and NM3) is 200nm/160nm and (PM2 and NM2) is 120nm/ 80nm, while MOM (metal-oxide-metal) capacitors were used as the bootstrap capacitors.

B. Boosting efficiency

Theoretically, the boosted voltage should present a voltage swing from -V_{DD} to $2V_{DD}$. However, the boosting efficiency (η_B) is influenced by the boosting capacitance and the boosted node capacitance, which has been defined as the ratio between the former capacitance and the sum of both [6]. For example, the capacity of the boost capacitance (C_{bootP}) together with the total parasitic capacitance (C_{B-out}) of the boosted node B-out, which produces due to associated transistors PM2, PM3, NM2, NM3, PMOS and NMOS, determine the efficiency of



(a) Input and output waveforms.



(b) Significant nodes waveforms.

Fig. 6: Signal waveforms of the circuit.

the boosting during the pulling down case. Accordingly, the voltage of the relevant node can be estimated as follows:

$$V(pulldown) = \frac{C_{bootP}}{C_{bootP} + C_{B-out}} \cdot 2V_{DD} \tag{6}$$

Likewise, for the pulling up voltage as:

$$V(pullup) = \frac{C_{bootN}}{C_{bootN} + C_{B-out}} \cdot -V_{DD} \tag{7}$$

Therefore, the efficiency of the boosting depends on the parasitic capacitance of the relevant transistors as well as the boosting capacitance which should be designed to be as large as possible for better efficiency. Consequently, the last stage of the driver circuit is pushed to a higher operation region, i.e. moderate or strong inversion rather than weak inversion based on the amount of boosted voltage.

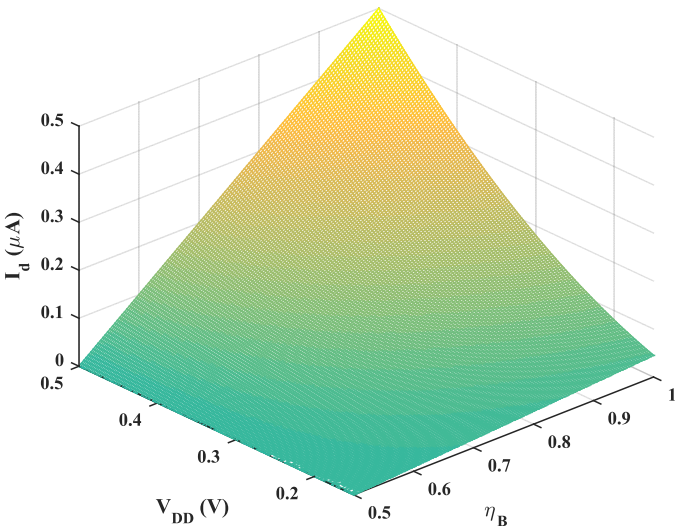


Fig. 7: Interaction between discharge current and V_{DD} with boosting effect.

Owing to the boosted voltage, the discharge current I_d in the components exposed to this voltage will be:

$$I_d = \mu C_{ox} \frac{W}{L} \left((\eta_B \cdot 2V_{DD} - V_{th}) V_{DD} - 0.5V_{DD}^2 \right) \tag{8}$$

As a result, the boosted voltage increases the current driving capability. Fig. 7 demonstrates this effect, which is a significant potential to fulfil the ULP design requirements regarding the effectiveness and error tolerance.

Similarly, not only will the discharge current be affected by the boosted voltage but also the leakage current and the equivalent resistance (R_{eq}) of the MOS transistor, where the latter will improve according to the following:

$$R_{eq} = \frac{V_{ds}}{I_{sub-th}} = \frac{V_t}{k_t e^{\frac{\eta_B \cdot 2V_{DD}}{mV_t}}} \tag{9}$$

where $k_t = \mu_{eff} C_{ox} \frac{W_t}{L_{eff}} (m-1) V_t^2 e^{(\frac{-V_{th}}{mV_t})}$, which represents strength of the transistor. This expression (9) has been driven based on (1), which can be rearranged to have:

$$I_{sub-th} = \mu_{eff} C_{ox} \frac{W_t}{L_{eff}} (m-1) V_t e^{(\frac{\eta_B \cdot 2V_{DD} - V_{th}}{mV_t})} V_{ds} \tag{10}$$

where the booted voltage was taken into account and the last term $(1 - exp(-V_{ds}/V_t))$ of (1) has been expanded in Taylor series and truncated to first order. This assumption can be applied for values of V_{ds} lower than V_{th} [26]. Furthermore, the leakage current will be suppressed exponentially depending on this applied voltage.

IV. Implementation and Results

In this section, the 90nm technology has been utilised to implement the studied circuits and present their simulation results. The device sizes of the circuits are listed in Table I.

TABLE I: Devices' sizes.

The work	[5] (nm/nm)	[6] (nm/nm)	[25] (nm/nm)
Inverter No. (NMOS W/L)(PMOS W/L)	2 (200/90)(400/90)	2 (200/90)(400/90)	1 (200/90)(400/90)
Switch No. (NMOS W/L)(PMOS W/L)	1 (200/160)(200/160)	3 (200/90)(200/90)	3 (200/90)(200/90)
Driver No. (NMOS W/L)(PMOS W/L)	1 (285/90)(340/90)	1 (260/90)(300/90)	1 (250/90)(340/90)

TABLE II: Comparison summary.

Driver	This work		[5]	[25]	[6]
Supply voltage (V)	0.15	0.2	0.2	0.2	0.2
Voltage swing	$-V_{DD}-2V_{DD}$		$-V_{DD}-2V_{DD}$	$GND-2V_{DD}$	$-V_{DD}-2V_{DD}$
Boosted components of total (%)	50		25	25	27
Frequency max (MHz)	5	13.37	10	4	5
Leakage power/Total power (%)	3.57	2.06	10.59	37.29	48.71
Average delay (ns)	10.5	7.1	6.9	15.1	13.9
FoM (pJ)	0.05	0.094	0.1	0.19	0.34
EDP ($\times 10^{-22}$ J×s)	5.24	6.67	6.97	28.7	47.3

A. Circuit implementation and results

The reported bootstrapped circuits of [25], [5] and [6] along with the proposed design have been implemented using Cadence software to demonstrate the proposed scheme effectiveness. The circuits employ a standard performance regular threshold voltage (SPRVT) transistor, 25fF boost capacitors (C_{bootP} and C_{bootN}) of a metal-oxide-metal (MOM) type, and 200fF capacitance connected to the driver output (CL) to emulate the 10mm interconnect.

At this point, it is important to mention that the consumed average total power and the leakage power have been measured separately. The latest was observed as the average value from the possible combinations, i.e. high and low logic, of the input signals in a stable state. On the other side, the average power was counted when a train of pulses is applied to the input. While the delay was measured at 1MHz using a relevant function that is already built-in in the simulation environment.

The simulation was executed under a 150mV supply voltage and 5MHz frequency as the input frequency of the driver to imitate the worst case transition activity. Under these conditions, the proposed driver achieves an average power consumption of 24nW and 85.5pW as a leakage power dissipation with 10.5ns average input to output delay. Then, the simulation has been carried out for the same circuit at a different supply voltage, where the results also stated in Table II.

Whilst, under a 200mV supply voltage, the reported driver circuit in [25] reached 0.74µW and 276nW as an average and leakage power, respectively, with 15.1ns as an average circuit delay. In another study [5], the estimated results of the designed driver were 1µW average power with leakage power 107nW and 6.9ns driver time delay. Furthermore, the results of [6] were 1.7µW for total average power and 833nW leakage power where, from the point of view of the power leakage, this was the worst results so far among tested drivers.

Table II summaries the comparison results of the proposed driver circuit with these works. In terms of the figure of merit (FoM), the power-delay-product (PDP) is an important measurement for evaluating the energy efficiency of a circuit in general. Meanwhile, the metric of the energy-delay product (EDP) was used, because it is preferable for low-frequency circuits [27]. While I_{off}/I_{on} is a critical factor in the design evaluation, particularly regarding ULP circuits [11]. The proposed work demonstrates very good merit for these measurements, comparing to the others. The advantage of the proposed design scheme regarding these measurements is owing to the number of components operating in the boosted voltage as shown in Table II. The boosted components in the table refer to the transistors that are driven and improved by the produced bootstrapped voltage. Accordingly, promoting these components amount in the circuit improves the performance of the circuit as a whole.

Even though the proposed driver achieves the best results for power saving and energy efficiency, it has not provided the best recorded delay time, particularly at $V_{DD} = 0.15$V, which is normal as going deeper in sub-threshold voltage area. It should be noted that the results of other works are for a higher supply voltage than this work. Therefore, the EDP metric has been applied as another measure to demonstrate that the proposed design is the best in the context of energy saving compared with the reported works.

Moreover, an investigation has been conducted to find the trade-off between the conventional buffer, i.e. regular one with two inverters, and the proposed design from the point of view of energy consumption and circuit delay. Thus, to run this comparison, we repeated the same experiments under the same circumstances except that the boosting technique was not used, in order to design the normal buffer in such a way as to be close to a bootstrap driver design. The results were as predicted, where the conventional buffer, with the same proposed circuit's transistors size where PMOS (NMOS) W/L is 800nm/100nm (650nm/100nm), does not have the capability to drive the same load (200fF) with 150mV as the supply voltage to obtain the same transient response as the design with boosting. The transient response results at the CL for the two drivers are demonstrated in Fig. 8.

Therefore, the solutions are either splitting the load into 8 parts and using repeaters for each part with 25fF, or increasing the size of the normal buffer transistors so as to have the ability to drive this load. Preliminary results show that both situations lead to a power consumption increase, regardless of the chosen solution. A large transistors buffer, its transistors approximately 12 times are larger than these in the proposed design where PMOS (NMOS) W/L is 12.5µm/100nm, has

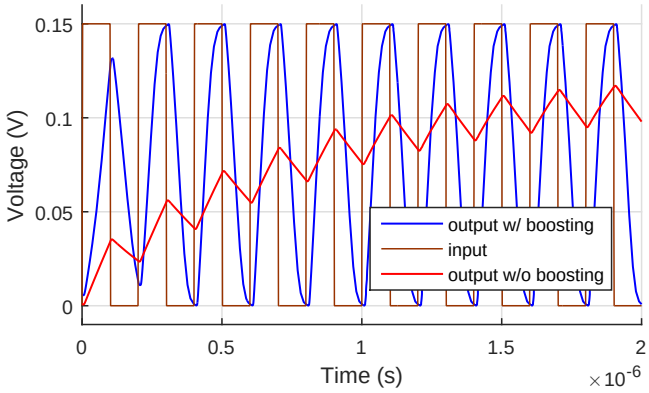


Fig. 8: Transient response waveforms of drivers at the CL with the same transistors size and conditions.

been implemented so as to give a fair comparison with the bootstrapped design, where the two drivers are designed to have the same rise and fall output waveform response.

The results of the experiments have been obtained by implementing the UMC 90nm technology using the Cadence Spectre simulation toolkit. The simulation was carried out for a long enough time to ensure that the output of the circuits being examined has reached a steady-state condition.
The bootstrapped driver has shown an improvement of 20.5% in the energy efficiency compared to the conventional driver. While, w.r.t the average power, the driver without boosting has consumed 23.96% more power than the proposed driver. This saving is due to the reduced leakage current which has a main role in the power dissipation of sub-threshold circuits. Table III lists the results of this comparison when the supply voltage is 150mV, the load is 200fF and the frequency is 5MHz. The table also shows that the estimated chip area of the proposed driver is 112.9μm^2 versus 142.8μm^2 for the normal driver ,where these were measured based on post-layout simulations.

However, the improvements in chip area, power and energy consumption of the proposed driver are accompanied by a greater circuit delay, as shown in Fig. 9. These results are normal from the delay point of view if it has realized that the bootstrapped driver practically has more stage since it involves using capacitors as shown in Fig. 5. Meanwhile the conventional driver is designed to have two stages, i.e. two regular inverters, which require fewer but larger transistors. Despite that, the main consideration in this report is not the delay but the energy saving which have been achieved by using

TABLE III: Summary of comparison results.

Item	Buffer without boosting	Buffer with boosting
Average power (nW)	31.45	25.37
Total energy per 10cycle (fJ)	62.9	49.97
Average delay (ns)	9.9	10.5
EDP ($\times 10^{-23}$ J×s)	62.27	52.39
Chip area estimated (μm^2)	142.8	112.9
Load (CL) (fF)	200	
Supply voltage(mV)	150	

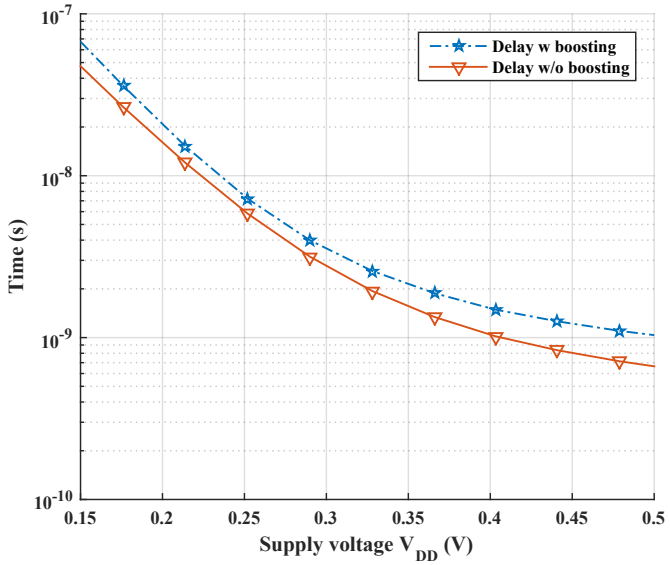


Fig. 9: Drivers with/without boosting delay with 200fF load and 5MHz frequency.

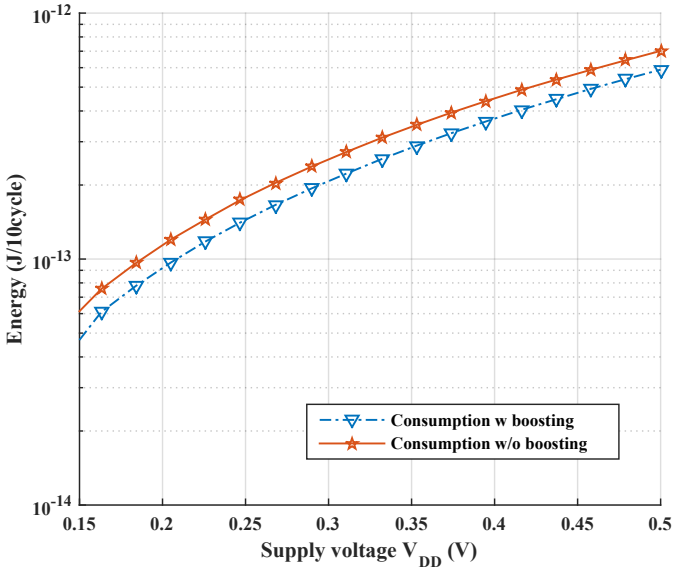


Fig. 10: Energy power consumption of buffers under scaling of supply voltage.

a boosting technique.
Another perspective is that the buffer's consumption of energy, which is shown in Fig. 10. Accordingly, the figure provides the outcome of these experiments where the supply voltage has been changed from deep sub-threshold to near super-threshold voltage, which obviously shows the advantage of the buffer with boosting compared to the one without boosting.

On the other hand, Fig. 11 shows the improvement of the bootstrapped driver compared to the normal driver from the point of view of leakage power. Furthermore, Fig. 12 demonstrates the proposed scheme advantage in the context of the energy efficiency. This efficiency or Power-Down efficiency is

calculated in this work based on the following equation:

$$E_{efficiency} = \frac{Useful_{energy}}{Total_{energy}} \times 100\% \quad (11)$$

where the leakage energy is considered wasted energy. This occurs when the circuit is considered in idling state, i.e. it does not perform any activity. Accordingly, the dynamic power of the circuit for a certain period of time was deemed as the useful energy. This metric is not accounting energy consumed during computing only, i.e. when the circuit performs an activity due to changes applied to its circuit input, but also energy consumed while idling. A higher this metric implies a more energy-efficient solution.

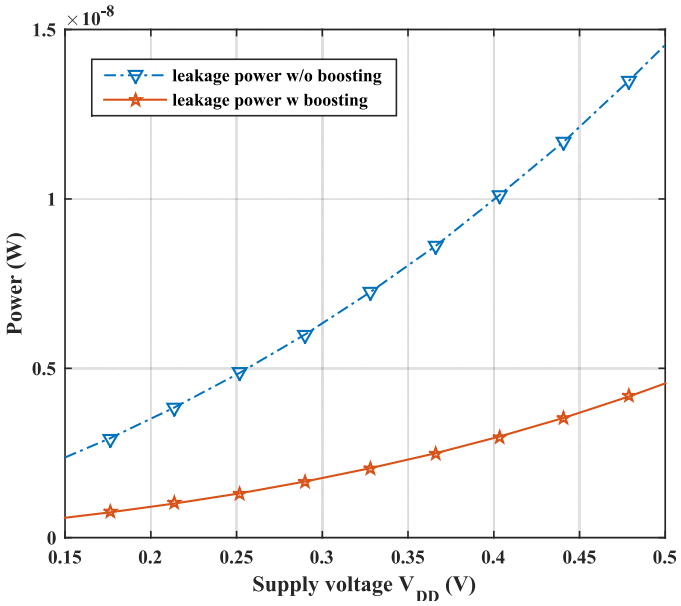


Fig. 11: Power leakage of the drivers.

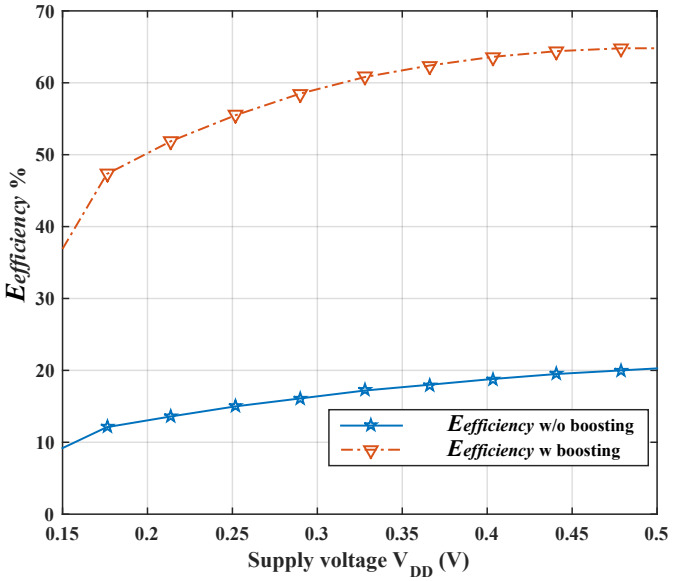


Fig. 12: Energy efficiency of the drivers.

From this comparison, the power consumption of the proposed scheme is lower than that of regular or other bootstrap-based schemes, by at least 25%. Thus, if the proposed design can make this amount of improvement, then its sustainable battery life can be extended at the same rate for the fixed throughput compared to others. In addition, it demonstrates the ability to operate at extremely low voltage, yet, with effectiveness regarding energy dissipation, which is our main focus. Therefore, the solution presented in this work can be utilised to meet the requirements of IoT applications, such as these are regarding lower supply voltage and provided by sources of batteries and energy collected from the environment.

B. Measurement and modelling of an SEU

The neutron particle strike is chosen to be the cause of the fault in a digital circuit. Therefore, in order to estimate the reliability of the designed circuit, we need to model the transient current pulse that is generated because of the particle strike. This model needs to be chosen carefully, since it has a significant impact on the accuracy of the estimated reliability. A model reported in [28] is used, which has been introduced as follows:

$$I_{SRC}(t) + C_S \frac{\mathrm{d}V(C_S)}{\mathrm{d}t} = G_{REC}(t) + G_{RAD}(t) \quad (12)$$

where C_S is a value used to conserve the deposited charge, its value is assigned arbitrarily and neither critical nor related to any internal capacitor in the circuit. G_{REC} is a dependent current source represents the recombination current in the device. G_{RAD} is a dependent current source and represents the transient current pulse induced from the particle strike. Finally, I_{SRC} represents the current that deposits the required amount of charge into the device, the independent double-exponential current source is used to generate this component of the model.

$$I_{SRC}(t) = \frac{Q_{crit}}{(\tau_F - \tau_R)}[e^{\frac{-t}{\tau_F}} - e^{\frac{-t}{\tau_R}}] \quad (13)$$

where τ_F and τ_R are time parameters representing the falling and rising time constants of the exponentials. Based on results collected for a 90nm technology, the $-\tau_R$ and τ_F range from a few to tens of picoseconds, respectively [29].

The model in (12) is used here because of its ease of implementation in SPICE simulations and for its accuracy [7]. In this model, the effect of a neutron strike is represented as a dependent current source added into a BSIM4 SPICE model of a MOSFET transistor. This model is attached with Cadence simulation tool in circuit-level simulation to inject different SETs in the circuit.

Fig. 13 illustrates using this current source model to generate transient current pulses at a fixed value of supply voltage and different LET values. It is obvious that the current pulse splits into two regions. The first one is a spike pulse simulating the drift charge collection and representing the instant response of the device and depends on the LET value. Whereas the second region represents the charge diffusion phase and depicted by the plateau region of the pulse. The magnitude of this part also depends on the value of LET but has a longer response in time

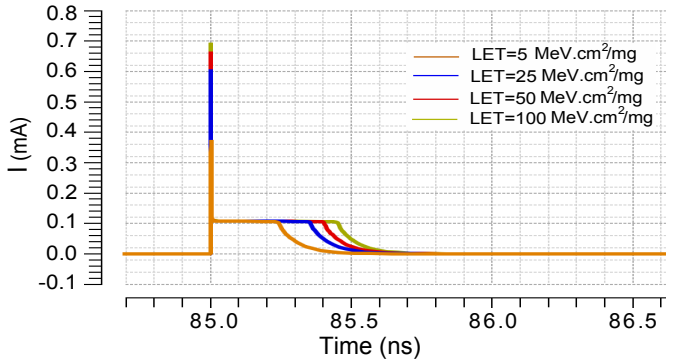


Fig. 13: Transient current pulses generated at $V_{DD} = 1$V and different LET values.

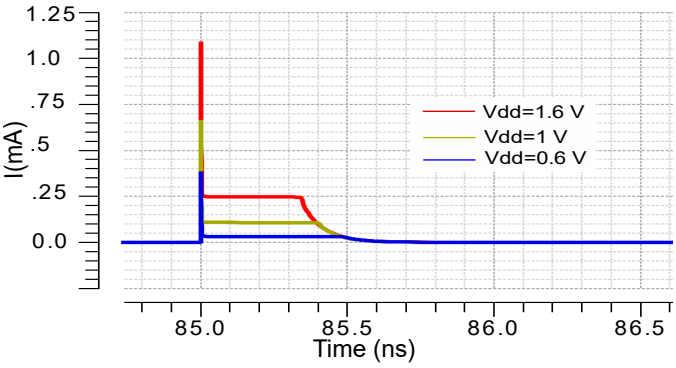


Fig. 14: Transient current pulses generated at LET=50 and different V_{DD} values.

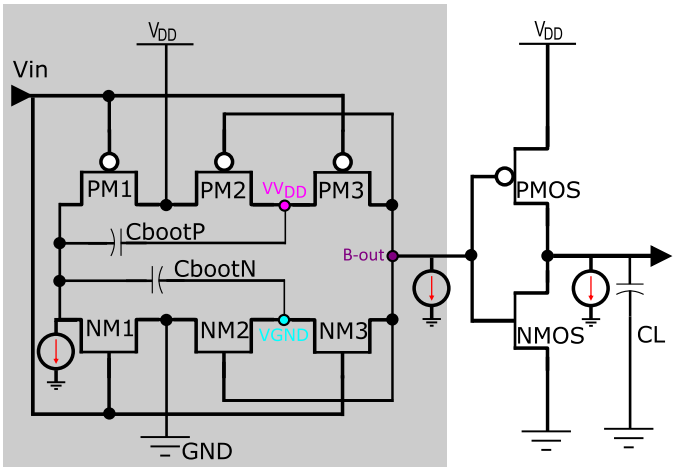


Fig. 15: Circuit implementation of SEU analysis.

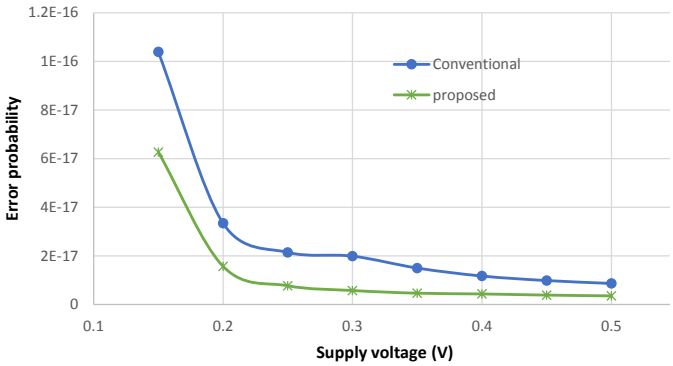


Fig. 16: Comparison of error probability at different voltages.

than the first one. Besides, Fig. 14 shows the transient current pulses at different supply voltages and LET=50MeV $\cdot$ cm^2/mg produced by using the bias-dependent current source. As can be noted, the amplitude and duration of the transient pulses differs in accordance with the supply voltage values. Hence, this demonstrates the advantage of this model to correlate with the applied voltage of the struck node.

The conventional and the proposed designs have brought to study one more time, in order to test the circuit drivers against the SEU. We attached the current source to all design's nodes one after the other, as shown in Fig. 15, and in each case observed every change in the output voltage swing. For the conventional driver, there are only two nodes to inject the current source. These circuits are implemented in 90nm UMC technology with the same V_{DD}, operating frequency and temperature.

This process enabled us to obtain the Parameter Vector (PV) (SET characterised with two parameters, namely, the LET and arrival time) and simulating the circuit in order to determine the critical values of this vector [7]. We repeat this for different V_{DD} values in order to see how the reliability changes under voltage-frequency scaling (the clock period is adjusted to the propagation delay under each V_{DD} value). This approach has been adopted rather than the complex, traditional methods that use multi-iteration statistical procedures. The experiments were carried out for different V_{DD} values from 0.15V to 0.5V.

This minimum supply voltage is chosen to ensure that the signal integrity of the drivers is still intact. Fig. 16 indicates that the proposed driver is better among the two circuits under the test for regarding this kind of soft errors. This improvement is mainly owing to two reasons.

Firstly, based on the results in previous Section IV-A, the proposed scheme has enhanced the current and the voltage of the driver internally. Subsequently, the critical charge for the proposed driver has increased as well based on (5). Secondly, regardless of the fact that the proposed circuit has been tested more than conventional one because of having more nodes, the boosting stage acts as a mask for glitches generated by SET. This is because the boosted voltage at the nodes where the pulses are produced minimizes the effect of these pulses, preventing them from propagating to the next stage. Roughly, our circuit achieved 60% improvement relative to the conventional driver.

V. Conclusion

Interconnect drivers used in ultra-low power regime for clock distribution networks and on-chip buses suffer from considerable performance degradation due to the fact that wire capacitance has not been scaled as the supply voltage is scaled down. Added to that, there is an issue of performance variability at sub-threshold region. Hence, our approach has

proposed using buffers with a charge pump booster, and this has met the expectations of improvements in performance by reducing power consumption and increasing energy efficiency. The reason for this is that the current driving is improved due to the exponential relationship between the transistor drain-to-source current and the gate-to-source voltage. The proposed driver has shown an improvement in the energy efficiency of 20.5% compared to that of a conventional driver and other previously reported boosted drivers. Meanwhile, the driver without boosting consumes 23.96% more power than our driver. The proposed driver circuit achieves a better tolerance to the SEU effect reached 60% compared to the traditional circuit.

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