# Ultra-Low-Power FDSOI Neural Circuits for Extreme-Edge Neuromorphic Intelligence

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Abstract-Recent years have seen an increasing interest in the development of artificial intelligence circuits and systems for edge computing applications. In-memory computing mixed-signal neuromorphic architectures provide promising ultra-low-power solutions for edge-computing sensory-processing applications, thanks to their ability to emulate spiking neural networks in realtime. The fine-grain parallelism offered by this approach allows such neural circuits to process the sensory data efficiently by adapting their dynamics to the ones of the sensed signals, without having to resort to the time-multiplexed computing paradigm of von Neumann architectures. To reduce power consumption even further, we present a set of mixed-signal analog/digital circuits that exploit the features of advanced Fully-Depleted Silicon on Insulator (FDSOI) integration processes. Specifically, we explore the options of advanced FDSOI technologies to address analog design issues and optimize the design of the synapse integrator and of the adaptive neuron circuits accordingly. We present circuit simulation results and demonstrate the circuit's ability to produce biologically plausible neural dynamics with compact designs, optimized for the realization of large-scale spiking neural networks in neuromorphic processors.

Index Terms—Edge computing, silicon neurons, FDSOI, ultralow-power, slow synaptic dynamics, IoT, real-time, analog circuit

# I. Introduction

A technological revolution is in the making where more and more Internet of Things (IoT) and edge-computing devices are being produced to sense and process signals, for example in environmental or health monitoring applications, and extract relevant information locally, without resorting to cloud computing or transferring large amounts of data to remote data centers. This poses a serious challenge in terms of memory and power consumption requirements for IoT systems, especially when they are expected to operate autonomously in a compact package directly on the sensed signals (i.e., in "extreme-edge" computing application scenarios). Due to the limitations of Dennard scaling law [1] and the von Neumann memory

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bottleneck problems [2], [3], a disruptive change is needed in the development of new memory and computing technologies to be able to sustain these processing requirements under tight power and size constraints.

A promising computational paradigm that can support the ultra-low-power implementation of "extreme-edge" computing processing tasks is that of Spiking Neural Networks (SNNs) and attractor dynamics [4]–[6]. In particular, it has been shown that recurrent SNNs provide a valuable algorithmic basis for efficient processing of temporal signals: the rich dynamics of these networks are instrumental in minimizing the amount of memory resources required to process, recognize, and classify long temporal sequences of data [7]. In addition, recent studies suggest that longer time constants in the SNN synapse and neuron models are very beneficial in lengthening the socalled "fading memory" of the recurrent network [8]. The best-suited approach to implement such networks in hardware which minimizes power consumption and area is that of using mixed-signal neuromorphic circuits [9], [10]. By exploiting the temporal properties of such circuits to adapt them to the temporal dynamics of the signals being processed, it is possible to implement an optimal "matched filter" approach that minimizes power consumption and maximizes the Signal to Noise Ratio (SNR) [11]. This approach forgoes the need for storing the data and the state of the processing elements, since they operate in real-time directly on the signals being acquired by the sensor. By combining the adaptive analog signal processing strategies of these neuromorphic circuits with digital eventbased asynchronous communication schemes, it is possible to build large-scale multi-core neuromorphic processors that combine the best of both (analog and digital) world for lowpower signal processing, computation, and communication. These processors typically operate with sub-mWatt powerconsumption figures and support the emulation of a wide range of SNN models, for solving artificial intelligence tasks directly on the sensory signals, as they are acquired (e.g., see [12], [13]). We refer to the combination of this technology with this approach as "extreme-edge neuromorphic intelligence".

The key enabling features of neuromorphic intelligence circuits are twofold: (i) They operate in continuous real-time on sensory signals, dissipating power only when the data becomes available and (ii) their operation speed is adapted (typically slowed down) to the time-scale of the signals being processed. For natural signals such as speech, human gestures, bio-signals, and a wide range of environmental signals, these time constants are the biologically plausible ones that range from fractions of milli-seconds to seconds. To optimize edge-

computing applications that operate on these types of input signals, a crucial precondition is to be able to support the processing of data on these different biological time scales. It is challenging to realize a similar range of timescales using conventional technologies, as they require very large capacitors and/or big digital memory storage blocks which limits the scalability of these circuits. As the technology nodes move toward deep sub-micron processes, the increased leakage current limits the time constants and also poses a challenge in terms of the static power consumption. Moreover, as the technology node scales down and the transistor's channel length decreases, its parameter variations (e.g. the threshold voltage) increase, and device mismatch increases even further.

In this paper, we present sub-threshold neuron and synapse circuits that have been designed to implement large-scale multi-neuron multi-core neuromorphic computing architectures using a 22 nm Fully-Depleted Silicon on Insulator (FDSOI) process. In Section II we show how it is possible to implement bio-physically complex neural and synaptic dynamics using ultra-low-power analog circuits in advanced scaled processes, by analyzing the features of the 22 nm FDSOI technology and addressing the analog design issues that arise from the advanced scaling. In particular, we exploit the properties of the FDSOI technology to design a synapse circuit that can reach 6 sec-long time constant, operating reliably with femto-Ampere currents. We also optimize the design of the FDSOI silicon neuron circuit recently proposed in [14] to further reduce the device mismatch effects.

In Section III we present circuit simulation results highlighting how the synapse and neuron dynamics change as a function of their bias parameters. We also characterize the power consumption figures as a function of the neuron average firing rate, and quantify the effect of device mismatch with Monte Carlo analysis simulations.

## II. METHODS

# A. FDSOI process advantages

Neuromorphic analog circuits typically use transistors operated in the sub-threshold or weak-inversion regime [15]-[17], using currents that range from fractions of pico-Amperes to hundreds of nano-Amperes. Indeed, to emulate biologically plausible dynamics, with time constants of the order of tens of milli-seconds, while using small capacitors (e.g., of the order of pico-Farads), it is necessary to limit the currents to pico-Ampere amplitudes. Furthermore, to implement circuits with even longer time-scales, for example to emulate homeostatic plasticity phenomena that last multiple seconds or tens of seconds, it would be necessary to reduce the currents even below femto-Ampere amplitudes. However, the non-ideal transistor effects of advanced Complementary Metal-Oxide-Semiconductor (CMOS) technology nodes (e.g., drain-induced-barrier-lowering (DIBL), band-to-band tunnelling (BTB), gate-induced-drain-leakage (GIDL), or random dopant fluctuation (RDF)) produce leakage currents that are well above the single pico-Ampere digits and severely limit the functionality of subthreshold neuromorphic circuits.

To design neuromorphic circuits in advanced technology nodes, one option is to resort to above-threshold circuits, either accelerating time constants by a factor of  $\times 1000$  [18] giving up the ability to optimally process slowly changing sensory signals, or by using switched-capacitor techniques [19]-[21] increasing the complexity of the circuit design techniques and power-consumption figures; the other option is to use FDSOI technology and exploit its features. The FDSOI technology introduces a variety of enhancements over the bulk CMOS technology. For instance, this more advanced technology utilizes a thin insulating layer of buried oxide, together with shallow trench isolation, which improves the electrical isolation between the channel and the substrate. As a result, bulk effects such as source/drain leakage, latch-up, parasitic source/drain junction capacitances and substrate noise coupling are reduced to a significant extent. The lower doping features lead to less threshold voltage variation and device mismatch across the chip. Moreover, the control over the channel and lower junction capacitances are enhanced by the addition of the second gate terminal, referred to as "body" or "back-gate", which can be reverse or forward biased to set the transistor in low leakage or high performance modes respectively. Here we will focus on a 22 nm FDSOI process which offers two main transistor types with thin and thick gate oxides. This provides the designer with a variety of transistor models that can have different threshold voltages and hence leakage currents. In analog circuit designs it is often necessary to use non-minimum size devices (large transistors). For these cases, it will be necessary to resort to the use of thick gate oxide devices, to avoid gate-leakage due to tunneling effects. These thick gate oxide devices can come in two flavors: Low-Threshold-Voltage LVT and Super-Low-Threshold-Voltage SLVT devices. SLVT are typically flip-well devices featuring the same doping type for their well and channel, and the  $V_{th}$  can be further reduced with forward backgate biasing. LVT are conventional-well devices which have opposite doping types between channel and well and the  $V_{th}$ can be further increased with reverse back-gate biasing.

# B. Key sub-circuits in 22 nm FD-SOI processes

In the neuron and synapse designs presented in this section, we use the 1.2 V I/O Low Threshold Transistors (LVT) at a  $V_{dd}$  of 0.8 V. These transistors are thick gate oxide, conventional well devices with high enough  $V_{th}$  which offer ultra-low leakage baseline, essential for achieving ultra-low leakage current levels. Moreover, due to their large utilizable range of channel lengths and minimal channel doping, these transistors offer less device mismatch.

In both designs the capacitances are implemented using Alternate Polarity Metal On Metal (APMOM) structures. The density of these devices depends on the value and on the number of used metal layers: larger capacitances can be implemented with more metal layers to attain a higher capacitance density. However, as these devices exhibit parasitic resistance effects that scale with their area, there are severe limitations to the maximum capacitance that can be attained.

1) The neuromorphic synapse circuit: Here we present an FDSOI synapse circuit based on the DPI [22], [23] which

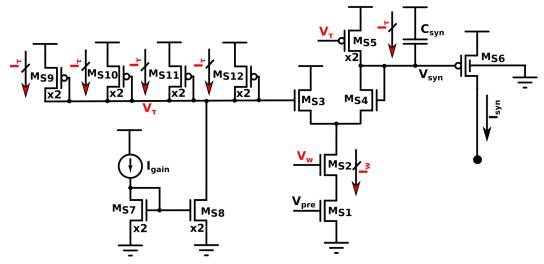


Fig. 1: Schematic of the DPI synapse circuit. Input spikes are applied to the  $V_{pre}$  node. The output EPSC  $I_{syn}$  has an amplitude proportional to  $V_w$  and decays exponentially with a time constant  $\tau_{syn}$  directly proportional to  $C_{syn}$  and inversely proportional to  $I_{\tau}$ .

models the synaptic response behavior as a first order linear system. The schematic diagram of the circuit is shown in Fig. 1. Input spikes applied to the  $V_{pre}$  node get integrated into an EPSC which obeys the following dynamics:

$$\tau_{syn} \frac{dI_{syn}}{dt} + I_{syn} = \frac{I_{gain}}{I_{\tau}} I_w \tag{1}$$

where  $I_{syn}$  is the synapse output current,  $I_{gain}$  is a reference current,  $I_{\tau}$  is a current equivalent to  $I_{gain}/4$ , and  $I_w$  is a subthreshold current set by  $V_w$ . The synapse time constant  $\tau_{syn}$  is defined as:

$$\tau_{syn} \coloneqq \frac{C_{syn} \ U_T}{\kappa \ I_{\tau}}$$

where  $C_{syn}$  is the DPI capacitor,  $U_T$  is the thermal voltage KT/q, and  $\kappa$  is the subthreshold slope factor [17]. To increase the circuit time constant it is therefore necessary to either increase capacitor sizes or to reduce  $I_{\tau}$  currents. Increasing capacitor sizes however is problematic, because of large area requirements and area-dependent leakage drawbacks (e.g., with APMOM structures). So the most viable solution is to minimize the  $I_{\tau}$  current. By exploiting the features of FDSOI technology and analog circuit design techniques, the synapse circuit presented on Fig. 1 can reliably produce  $I_{\tau}$  currents of the order of femto-Amperes. This allows the circuit to reach  $\tau_{syn}$  values of up to 6 s with compact synaptic  $C_{syn}$  capacitors that have capacitance values below 1 pF (specifically, 821 fF with an APMOM structure of  $12 \times 12 \,\mu\text{m}^2$  in our design). Furthermore, by setting the DPI gain term to a constant ratio  $(I_{qain}/I_{\tau}=4)$  we ensure that changes in the synapse time constant do not affect the maximum synapse current amplitude.

The transistors in the synapse circuit are operated with a power-supply voltage  $V_{dd}=0.8\,\mathrm{V}$ , which is set below the nominal supply voltage of 1.2 V, to reduce channel leakage and

power consumption. To achieve the aimed long time constants, we configured the conventional well devices with full reverse back-gate biases ( $\pm$  2 V). In the schematic of Fig. 1, all transistors are fully reverse body biased for minimum leakage operation, except for the current injecting PFET ( $M_{S6}$ ) whose body contact was set to gnd for achieving higher synaptic efficacy. To improve the synaptic efficacy further, the NFETs of the differential pair ( $M_{S3}$  and  $M_{S4}$ ) are designed with high  $\frac{W}{L}$  ratio so that they accommodate a lower  $V_{gs}$  drop and provide enough  $V_{ds}$  headroom for  $M_{S1}$  and  $M_{S2}$  to remain in saturation while  $V_{syn}$  discharges to lower voltages.

To achieve even lower leakage currents and higher output impedance for the  $I_{\tau}$  and  $I_{gain}$  current mirrors, and allow them to operate correctly with sub-pico-Ampere currents, we adopted the self-cascoding technique proposed in [24]. The transistor self-cascoded configuration is denoted in the figure by "x2" symbol.

The operation of the DPI synapse circuit is controlled by the input  $V_{pre}$ , which is a pulse signal representing the incoming spikes from the previous synaptic neurons. When  $V_{pre}$  is at gnd there is no current flowing in the bottom branch  $(M_{S1}, M_{S2} \text{ and } M_{S4})$  and  $I_{\tau}$  keeps  $V_{syn}$  charged at  $V_{dd}$ , switching OFF  $M_{S6}$ . When  $V_{pre}$  is at  $V_{dd}$ ,  $V_{syn}$  discharges with a speed set by  $I_w$  -  $I_{\tau}$  and as  $M_{S6}$  starts switching ON, the DPI synapse circuit injects  $I_{syn}$ . When  $V_{pre}$  returns to gnd,  $V_{syn}$  charges back to  $V_{dd}$  with a rate set by  $I_{\tau}$ , switching  $M_{S6}$  back to the OFF state.

2) The silicon neuron circuit: It has been recently argued that SNNs can accomplish remarkable learning and inference performance figures, if they are endowed with complex dynamics which comprise multiple and diverse time-scales [8]. To support such networks, we propose the use of the Adaptive-Exponential Integrate and Fire (AdExp-I&F) silicon neuron circuit [10], [14], [25]–[27]. The AdExp-I&F neuron model has been shown to be able to reproduce a wide range of

spiking behaviors and explain a wide set of experimental measurements from pyramidal neurons [28], [29]. Similar to the Izhikevich neuron model [30], it is a two-variable model with a "fast" variable that describes the dynamics of the membrane potential and includes an activation term with an exponential voltage dependence, and a "slow" variable that describes the spike-frequency adaptation mechanism. This is a negative-feedback mechanism which decreases the effect of the input current to the neuron with every output spike, therefore acting as a high-pass filter which reduces the neuron firing rate in response to instantaneous increases in the input.

The equations that describe the original computational model [28] are the following:

$$C\frac{dV}{dt} = -g_L \left(V - E_L\right) + g_L \Delta_T \cdot e^{\frac{V - V_T}{\Delta_T}} - w + I \qquad (2)$$

$$\tau_w \frac{dw}{dt} = a \left( V - E_L \right) - w \tag{3}$$

where V represents the neuron membrane potential, C its membrane capacitance,  $g_L$  the leak conductance,  $E_L$  the resting potential, I the neuron's input current, and w is the slow variable that represents the after-hyperpolarizing current of biological neurons responsible for their spike-frequency adaptation behavior [31]. The term  $\Delta_T$  represents the exponential slope factor,  $V_T$  the neuron's spiking threshold potential, a the adaptation weight, and  $\tau_w$  the adaptation time constant. At every spike, the neuron is reset to the resting potential and the adaptation variable is increased by a.

The AdExp-I&F FDSOI neuron we propose is depicted in Fig. 2. It is a current-mode circuit, in which the currents represent the state variables. Therefore the V and w variables of the computational model described by Eqs.(2) and (3) are represented in the circuit by the currents  $I_{mem}$  and  $I_{ahp}$  respectively. By adopting the same translinear-circuit analysis techniques used for the DPI synapse circuit, and described in [10], and using very low leakage currents such that  $I_{leak} \ll I_{in}$ , it is possible to express the circuit dynamics as:

$$C_{mem} \frac{d}{dt} I_{mem} = -g_L I_{mem} + g_L f(I_{mem})$$
$$-g_L I_{ahp} + g_L I_{in}$$
(4)

$$\tau_{ahp} \frac{d}{dt} I_{ahp} = I_a - I_{ahp} \tag{5}$$

where  $g_L$  and  $\tau_{ahp}$  are defined as:

$$\begin{split} g_L \coloneqq & \frac{\kappa \, I_{leak}}{U_T} \\ \tau_{ahp} \coloneqq & \frac{C_{ahp} \, U_T}{\kappa \, I_{\tau_{ahp}}}, \end{split}$$

and where  $I_a$  represents the adaptation weight for the slow variable, and  $f(I_{mem})$  is a current produced by the positive-feedback block transistors  $(M_{N1}-M_{N6})$  which has been shown to well fit a positive-exponent exponential function [32].

The AdExp-I&F FDSOI circuit schematic can be subdivided into different functional blocks: An input DPI  $(M_{L1}-M_{L5})$  models the neuron's leak conductance (LEAK). A current-based positive feedback module  $(M_{N1}-M_{N6})$  models the

TABLE I: Capacitance values and sizes used in the neuron design

	$C_{mem}$	$C_{ahp}$	$C_{ref}$	$C_{pex}$	$C_{cc}$
Value	821 fF	1 pF	102 fF	136 fF	116 fF
Width	12 μm	14 μm	5.8 μm	6 μm	6 μm
Length	12 μm	14 μm	5.5 μm	7 μm	6 μm

neuron's Sodium (Na+) activation and inactivation channels, and is coupled to a low-power current comparator (CC) block  $(M_{C1}-M_{C9})$  which triggers a spike as soon as the membrane current  $I_{mem}$  exceeds the spiking threshold parameter  $I_{thr}$ . A spike reset circuit with refractory period functionality ( $M_{K1}$ - $M_{K11}$ ) models the neuron's Potassium (K+) channels. A negative feedback LPF circuit implemented with an additional instance of a DPI  $(M_{A1}-M_{A9})$  (AHP) emulates Calciumdependent after-hyperpolarization Potassium currents observed in real neurons to produce the spike-frequency adaptation mechanism. This circuit is driven each time the neuron produces an output spike event, which is conveyed to a pulse extender circuit (Fig. 3) to lengthen the duration of the spike-event and ensure proper sub-threshold operation of the DPI. Finally, an asynchronous digital handshaking (HS) block  $(M_{HS1}-M_{HS4})$  implements the interface to Address-Event Representation (AER) circuits for transmitting the spikes as address-events to AER routers and destinations. This block generates the Req and Ack signals used to implement a fourphase handshaking cycle with the destination AER circuits: at rest, when the neuron current is below the spiking threshold, Req and Ack are both set to gnd. As the  $I_{mem}$  crosses the spiking threshold, provided Ack is still at gnd, Req is set to  $V_{dd}$ . Once the AER receiver consumes the event request and sets Ack to  $V_{dd}$  the neuron resets and Req is pulled back to gnd. As the AER receiver senses this change, it should lower the Ack signal, and the cycle can repeat.

To minimize leakage currents we reduced the Early effect of critical transistors by using a pseudo-cascode split-transistor sub-threshold technique [33] (see transistors  $M_{L4}$  and  $M_{A5}$  of Fig. 2). As for the DPI synapse schematic of Fig. 1, the "×2" symbol in the figure denotes the presence of two transistors in series connected to form a diode-connected transistor. All transistors are configured with the default back-gate bias (0 V). All capacitors in this circuit are implemented using APMOM devices. The value of the capacitances and their size is shown in Table I.

The neuron behavior can be set by 6 tunable parameters (see bold labels in Fig. 2) that control the neuron's time constant  $(V_{leak})$ , its spike-frequency adaptation properties  $(V_a \text{ and } V_{\tau\_ahp})$ , its refractory period  $(V_{ref})$ , and its spiking threshold  $(V_{thr})$ . As the DPI circuits of the LEAK and AHP blocks have been configured to have a gain term  $I_{gain}/I_{\tau}=1$  (similar to how the gain term was set to 4 in the synapse circuit), the  $V_{leak}$  and  $V_{\tau\_ahp}$  signals can be tuned by modifying the  $I_{gain}$  and  $I_{gain\_ahp}$  currents respectively.

The spiking threshold parameter  $V_{thr}$  controls the current comparator block  $(M_{C1}-M_{C9})$ . This is a novel circuit, modified from the one originally proposed in [34] to reduce

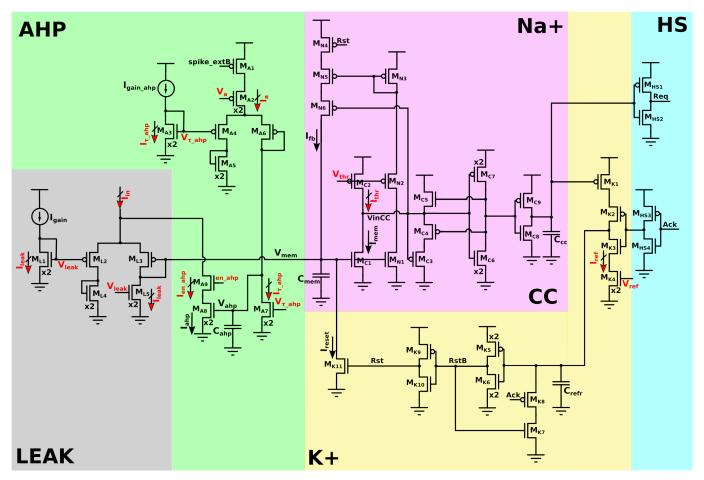


Fig. 2: AdExp-I&F neuron circuit schematic: In grey the input DPI LPF, in pink the positive-feedback and the current comparator, in yellow the reset block, in light blue the handshake block and in green the spike-frequency adaptation block. Adapted from [14].

the neuron's static and dynamic power consumption. It has been introduced to decouple the slow and gradual changes of the neuron's membrane potential dynamics (represented by the  $I_{mem}$  current) from the digital switching mechanism required to generate a spike. This is necessary to minimize the switching time of the digital circuits, during which they can dissipate large amounts of power. The  $V_{inCC}$  voltage of the comparator circuit is set by the competition between the currents representing the spiking threshold,  $I_{thr}$  , and  $I_{mem}$ . If  $I_{mem}$  is smaller than  $I_{thr}$ , this node is actively clamped to  $V_{dd}$ . However as  $I_{mem}$  approaches  $I_{thr}$ ,  $V_{inCC}$  drops sharply to produce a spike event with very low dynamic power consumption figures. The transistor  $M_{C3}$  was introduced in the CC block to reduce the neuron's power consumption in its resting (OFF) state: when  $I_{in}$ =0, the node  $V_{inCC}$  is driven to  $V_{dd}$  by  $M_{C2}$  which turns on a discharging path to gnd via  $M_{C4}$ . As both  $M_{C2}$  and  $M_{C4}$  are conducting, there exists a direct path between  $V_{dd}$  and gnd which undesirably adds to the static power consumption figure. The addition of  $M_{C3}$  to this circuit breaks the discharging path to gnd, further reducing the neuron static power consumption. The  $C_{CC}$  capacitance ensures that at each input current threshold crossing corresponds only one spike.

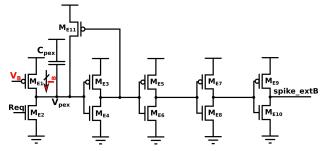


Fig. 3: Pulse extender circuit schematic. Adapted from [14].

The pulse extender circuit depicted in Fig. 3 is used to extend the spike-event pulse created by the neuron and to drive the spike-frequency adaptation circuit  $(M_{A1}-M_{A9})$ . When a spike is produced and Req goes to  $V_{dd}$ , the transistor  $M_{E2}$  discharges the node  $V_{pex}$  to gnd. As a consequence, the node  $spike\_extB$  is discharged to gnd switching ON  $M_{A1}$  of Fig. 2. The length of the  $spike\_extB$  pulse is set by the  $V_B$  bias voltage and the capacitance  $C_{pex}$ . The higher the value of  $V_B$ , the slower  $V_{pex}$  is charged back to  $V_{dd}$  and hence the larger the extension.

#### III. RESULTS

#### A. Synaptic circuit simulation

The simulations presented in this section demonstrate how the DPI synapse presented in Section II-B1 can achieve very large time constants and high synaptic efficacy. The results demonstrating the integration and steady-state profiles of the synapse EPSC ( $I_{syn}$ ) are shown in Fig. 4a and 4c respectively. To assess the corresponding synaptic time constants ( $\tau_{syn}$ ), we plot the linear fits to the natural logarithm of the normalized EPSC in Fig. 4b and 4d.

To measure the circuit's dynamic range we stimulate it with a pulse train of 50 Hz rate, with each pulse lasting 100 nsec; and we sweep  $I_{\tau}$  to cover a wide spectrum of time constants extending from 50 msec to 6 sec. To demonstrate the integration property of the synapse at lower  $I_{\tau}$  values (i.e., larger time constants), we apply the pulse train for 1 sec, adjust the weight  $I_w$  accordingly to obtain a peak integrated response of 1 nA, and measure the decay time of  $I_{syn}$ . Moreover, to observe the different steady-state response behavior, we extend the pulse train stimulation duration to 5 sec, fix  $I_w$  to 500 nA and use smaller time constant values which are comparable with the input pulse train inter-spike interval.

Figure 4a shows the synapse response in integration mode with the time constants in the range 250 msec-6 sec. Here, the inter-spike interval of 20 msec is much smaller than the synaptic time constants, and thus the EPSC charges up to 1 nA for all  $I_{\tau}$  values. However, to obtain equal peak EPSC magnitudes we had to make small adjustments of  $I_w$  for the values of  $I_{\tau}$  between 5 and 50 fA, and larger adjustments for  $I_{\tau}=1$  fA and  $I_{\tau}=100$  fA. As the value of  $I_{\tau}$  decreases to fA values, the APMOM capacitor parasitic effects become non-negligible: specifically, the capacitor's leak increases the effective value of  $I_{\tau}$ . For ideal values of  $I_{\tau}=1$  fA, the effective synaptic efficacy term  $\frac{I_{gain}}{I_{\tau}}$  is in practice much less than the nominal value of 4. To compensate for this effect it is therefore necessary to increase the value of  $I_w$  (e.g., see solid line in Fig. 4a).

Figure 4c shows how the synapse reaches a steady-state with shorter time constants and a longer stimulus duration. In this mode of operation, the discharge of the synapse during the inter-spike interval balances out with the charge induced by the spikes. Hence, the steady-state value scales with the time constant. In addition, the EPSC at steady-state features fluctuations around its peak value due to the ongoing rapid synaptic charging-discharging process.

The fits to the synaptic current data illustrated in Fig. 4b and 4d verify that the synapse behaves as a first order system as Eq. (1) suggests. Table II compares the theoretical time constants to the values obtained by linear fitting. The table shows that the fitting results are in very good agreement with the theory for fast synaptic dynamics while the difference increases as the synapse becomes slower. This is due to the APMOM capacitor leakage building on  $I_{\tau}$  which limits the maximum time constant of the circuit. This limitation is particularly significant for  $I_{\tau}$ =1 fA, where the capacitor leakage dominates the synaptic discharging process. As a consequence, the time constant saturates at  $\tau_{sun}$ =5.81 sec above which the circuit

TABLE II: Comparison between the measured and theoretical time constants  $\tau_{syn}$  of the DPI synapse for  $C_{syn}$ =821 fF,  $\kappa$ =0.75, and  $U_T$ =25 mV

$I_{ au}$	Theoretical	Linear Fit	$ I_{\tau} $	Theoretical	Linear Fit
1 fA	27.37 sec	5.81 sec	100 fA	274 msec	270 msec
5 fA	5.47 sec	3.42 sec	200 fA	137 msec	138 msec
10 fA	2.74 sec	2.21 sec	300 fA	91 msec	93 msec
20 fA	1.37 sec	1.26 sec	400 fA	68 msec	70 msec
50 fA	547 msec	535 msec	500 fA	55 msec	56 msec

cannot extend. Based on the results, the capacitor leakage is found to constitute a 3–4 fA of peak baseline current which is much higher than the cumulative leakage of all transistors. Although the reduction in the transistor leakage has increased the available time constant range, the capacitive leakage would need to be reduced to sub-femto-Ampere regime as well, in order to increase the time constants further up to 30 sec as the theory suggests. Increasing the capacitance size is not a viable option, since the capacitor leakage scales up with its area as well. Moreover, this capacitive leakage is voltage dependent hence utilizing different synaptic weights or pulse configurations can result in slight deviations in the available time constant range.

In general, the designed DPI synapse circuit with ultra-low leakage capability can offer a wide dynamic range of time constants with sub-pico-Ampere  $I_{\tau}$  values and can generate EPSC on the order of nano-Amperes for 100 nsec of pulse duration. The ultra-low current operation of the circuit makes time constants up to several seconds achievable with capacitors below 1 pF which reduces the layout area and enables denser integration in addition to the benefit of reducing the power consumption of the overall circuit.

#### B. Neuron circuit simulation

In this section we present the FDSOI neuron simulation results, demonstrating examples of biologically plausible behaviors, characterizing its power consumption properties, and quantifying the effects of device mismatch on its response properties. Figure 5 shows the response of the neuron to a step input current for different parameter settings: Fig. 5a shows the membrane current  $I_{mem}$  for two different values of  $I_{ref}$ . As the  $I_{ref}$  increases, the refractory period is shorter and hence the neuron's maximum spiking frequency increases. Figure 5b and 5c show the  $I_{mem}$  for different values of  $I_{thr}$ when keeping the same  $I_{in}$  (Fig. 5b) and when changing  $I_{in}$  (Fig. 5c) to obtain the same spiking frequency as  $I_{thr}$ changes. As  $I_{thr}$  increases the neuron is less facilitated to spike as it has to integrate more current to reach the threshold. Higher  $I_{thr}$  leads to more time needed in the integrating phase and therefore less frequent spikes, which gives lower spiking frequency.

Figure 6a and 6b show the neurons F-I curve for different  $I_{ref}$  bias settings. The neurons average firing rate increases linearly with the input current, until it reaches a saturation level that depends on the refractory period setting (see Fig. 6a). The saturation frequency depends on the duration of the refractory period, as the  $I_{ref}$  increases the refractory period is shorter

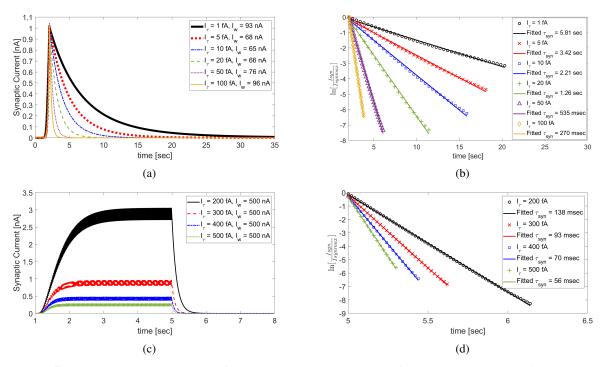


Fig. 4: Synapse  $I_{syn}$  EPSC measurements and fits with the natural logarithm of the normalized EPSC for estimating its time constants  $\tau_{syn}$ : (a) & (b) for a 50 Hz stimulus applied for 1 sec with synaptic time constants in the range 250 msec-6 sec. (c) & (d) for a 50 Hz stimulus applied for 5 sec, with synaptic time constants in the range 50 msec-150 msec, causing the synapse to reach different steady state levels.

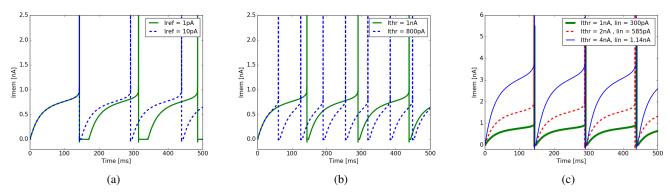


Fig. 5: FDSOI neuron biologically plausible behaviour: (a) Membrane current  $I_{mem}$  for two different values of  $I_{ref}$ , (b)  $I_{mem}$  for two different values of  $I_{thr}$  keeping the same  $I_{in}$ , (c)  $I_{mem}$  for three different values of  $I_{thr}$  changing  $I_{in}$  to obtain the same spiking frequency.

and hence the neuron's maximum spiking frequency increases. For shorter refractory periods (Fig. 6b) the maximum spiking frequency is linear with the input current for a larger range of  $I_{in}$  and it reaches saturation only for very high values of  $I_{in}$ . When  $I_{ref}$  is  $1\,\mu\mathrm{A}$ , hence when the refractory period is very short (few hundreds of ns), the maximum spiking frequency does not saturate for the chosen  $I_{in}$  range.

Figure 6c shows the neuron spiking frequency versus input current (F-I curve), for different settings of the  $I_{gain}/I_{leak}$  bias ratio. We modify the default ratio  $(I_{gain}/I_{leak}=1)$  to higher values. As expected, increase in the ratio results in the increase of the neuron's firing rate.

Figure 7 demonstrates the spike-frequency adaptation behavior, obtained by appropriately tuning the relevant parameters in the AHP block of Fig. 2 and measuring the neuron's step response to a constant injection current. At each spike the  $I_{ahp}$  current increases, decreasing the total current charging  $C_{mem}$ . When  $I_{ahp}$  reaches the steady state, the neuron spiking frequency remains constant to a lower value compared to the initial one.

## C. Energy per spike

Once proven that the design is able to reproduce a biologically plausible behavior, we evaluated whether it can imple-

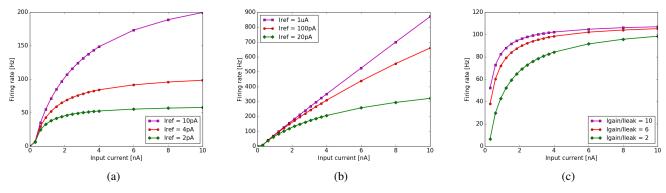


Fig. 6: Firing rate vs Input current (F-I) curve: (a) for lower values of  $I_{ref}$  hence longer refractory period, (b) for higher value of  $I_{ref}$  hence shorter refractory period and (c) for different values of  $I_{gain}/I_{leak}$  ratio. Adapted from [14].

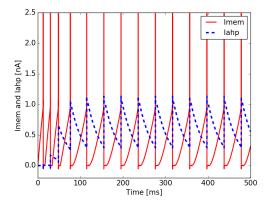


Fig. 7: Spike-frequency adaptation: Membrane current and after-hyperpolarization current trace over time. Adapted from [14].

ment massively parallel large-scale neuromorphic processors. The energy per spike is equal to:

$$\frac{Energy}{Freq \cdot Time} = \frac{Power \cdot Time}{Freq \cdot Time} = \frac{Power}{Freq}$$
 (6)

where Energy, the total energy consumed, is the product of total power consumed (Power) and simulation time (Time) and Freq is the maximum spiking frequency. As is shown in Fig. 8, the energy per spike for lower frequencies is in the order of tens of pJ, while it decreases to 1 pJ for higher frequencies. This is due to the fact that in lower frequencies the inverters spend more time in their high gain region with both transistors conducting, since the  $V_{mem}$  at their input is charging much slower compared to the case with higher frequencies.

We compare the energy per spike of our proposed neuron with previously published state-of-the-art neuromorphic processors in Table III.

The neuron designed in this work consumes less energy per spike compared to a similar circuit [34] in a similar technology (28 nm FDSOI) at a biological plausible spiking frequency (30 Hz). Moreover, the circuits used in [34] and our work have similar  $V_{dd}$  and  $C_{mem}$ , which we can consider as the

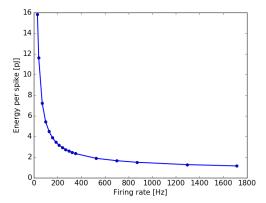


Fig. 8: Energy per spike estimation: Energy per spike vs Firing

TABLE III: Energy per spike comparison with previous works

Work	[12]	[19]	[34]	This work
Techn.	180 nm	28 nm	28 nm	22 nm
	CMOS	CMOS	FDSOI	FDSOI
Type	Mixed	Mixed	Mixed	Mixed
$V_{dd}$	1.8 V	0.7-1 V	1 V	$0.8\mathrm{V}$
Freq	30 Hz	-	30 Hz	30 Hz
En./spike	883 pJ	2.3 nJ-30 nJ	50 pJ	16 pJ

predominant capacitance for power consumption. Therefore, according to the scaling factor, the energy per spike of the circuit proposed in [34] will be similar when scaled to the 22 nm process. Hence the differences reported here can be explained by the optimizations made at the circuit design level.

The neuron circuit energy consumption at higher frequencies is compared with the Sigma-Delta neuron proposed in [35], which is one of the most recent mixed-signal silicon neuron circuit designs presented in the literature. Since the Sigma-Delta neuron presented in [35] was optimized for operation at higher frequencies in a range of 1 kHz to 10 MHz, we compare the energy per spike between these circuits in these ranges: the neuron proposed in this work consumes 1 pJ@2.1 kHz, approximately one order of magnitude less than the Sigma-Delta neuron (10 pJ).

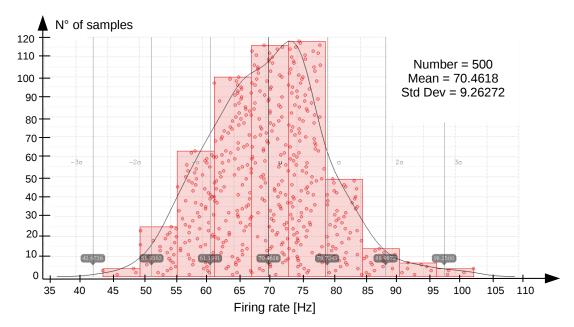


Fig. 9: Monte Carlo analysis result distribution of the neuron circuit. Adapted from [14].

#### D. Monte Carlo Analysis

To evaluate the sensitivity of the circuit to device mismatch we ran a series of Monte Carlo simulations. We performed this analysis with 500 runs for this neuron circuit, with DC current injected in the LEAK block in Fig. 2, and with bias currents set to obtain a firing rate of approximately 70 Hz while switching off the spike-frequency adaptation circuit.

The mean of the distribution obtained is centered around the expected value ( $\approx$ 70 Hz) and the standard deviation is equal to 9.26 (see Fig. 9). The variability of the neuron circuit is thus 13 %. Our analysis found that this variability is governed by the LEAK block and the first part of the CC, where the comparison between  $I_{mem}$  and  $I_{thr}$  is made ( $M_{C1}$  and  $M_{C2}$ ). In particular, in the LEAK block the transistors more affected by process variation are  $M_{L2}$  and  $M_{L3}$ . The K+ block, in particular  $M_{K4}$ , also shows sensitivity to device mismatch, but it is negligible compared to the other two blocks.

#### IV. CONCLUSION

We determined process and circuit parameters in order to implement efficient (low power and slow dynamics) analog neuron circuits using an advanced scaled 22 nm FDSOI process. We optimized the design of the synapse and neuron circuits for producing biologically plausible neural dynamics, with time constants matched to those of natural signals, such as speech or bio-signals.

The presented silicon synapse circuit can achieve time constants of up to 6 sec without having to increase the synaptic capacitance  $C_{syn}$  over 1 pF. The neuron circuit presented has an energy per spike of tens of pJ for lower frequencies and pJ for higher frequencies, which is considerably lower compared to an analogous neuron design implemented in a 180 nm CMOS process [12]. Furthermore, it consumes less compared to a more recent design [34] at biologically plausible frequencies and it consumes one order of magnitude less

compared to the state-of-the-art neuron circuit [35] at higher frequencies. We studied the mismatch sensitivity of the neuron circuit by performing Monte Carlo simulations and identified the parts of the circuit that are most critical to be optimized for variations, showing how the more sensitive sub-parts of the silicon neuron circuit are the LEAK block and the first part of the CC block. In summary in this paper we demonstrate how it is possible to exploit the features of advanced 22 nm FDSOI processes to design complex analog circuits that can be used to implement low-power neuromorphic processors for edge computing sensory-processing tasks and, more generally, "neuromorphic intelligence" applications.

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