

Gain-Boosted Super Class AB OTAs Based on Nested Local Feedback

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Abstract—A new approach to design super class AB operational transconductance amplifiers (OTAs) with enhanced large-signal and small-signal performance is presented. It is based on employing two nested positive and negative feedback loops at the active load of an adaptively biased differential pair in weak inversion region. As a result, DC gain, gain-bandwidth product, settling time and noise are improved compared to conventional super class AB OTAs without extra circuit nodes or power consumption. Measurement results of a 180 nm CMOS test chip prototype show a current boosting factor higher than 5000 and a nearly ideal current efficiency. Due to the ultra-low quiescent currents and high driving capability, the circuit exhibits an excellent large-signal figure-of-merit (FOM_L) of 236 V⁻¹. To illustrate the applicability of the proposed approach, a differential sample-and-hold (S/H) circuit was designed and fabricated on the same test chip. Measurement results of the S/H validate the advantages of the proposal.

Index Terms—Super class AB OTA, Local Common-Mode Feedback, Partial Positive Feedback, Amplifier, Sample and Hold.

I. INTRODUCTION

LOW-POWER design constitutes one of the main current challenges in analog design. As a result, low-power OTAs that preserve high performance are a research priority, motivated by the proliferation of portable devices and energy-autonomous systems. To achieve a good trade-off between power, area and performance, single-stage OTAs often constitute the best option. In terms of power, they are very efficient because the number of branches where current flows is reduced in comparison with multi-stage topologies. This can be quantified by the current efficiency factor, defined as the ratio between the load and supply currents $CE = I_{out}/I_{supply}$. A highly efficient topology delivers most of the supply current to the output. Regarding stability, single-stage OTAs are unconditionally stable since they are load-compensated. This avoids the use of complex compensation schemes that may increase the area and power. Conversely, their main drawback is their limited gain. For this reason, various techniques have been developed in order to improve not only the gain, but also the gain-bandwidth product (GBW), slew rate (SR) and settling time while keeping a low power consumption.

A limitation of class A amplifiers is that the maximum load current is limited by the bias current, leading to a power-performance tradeoff. To overcome this drawback, class AB topologies are employed [1]-[8]. These topologies can improve large signal performance without increasing quiescent currents. This improvement can be quantified by the current boosting factor, $CB = I_{out}^{MAX}/I_b$, defined as the ratio between the maximum output current and the bias current. Usually, in class A amplifiers, $CB = K$, where K is a current mirror ratio. However, in class AB amplifiers CB may reach higher values, yielding larger SR with the same static power. Moreover, if the dynamic current boosting occurs at the output branches so that no internal dynamic current replication exists, near optimal current efficiency ($CE \approx 1$) can be achieved.

Several class AB techniques have been proposed, which can be applied to either the differential input pair or active load. A particularly suitable approach is the so-called super class AB OTAs [1]. They are single-stage topologies that provide dynamic current boosting both at the differential pair and at the active load, yielding very large CB and CE values. Typically, Local Common-Mode Feedback (LCMFB) [9] with passive resistors is used in the active load of these OTAs to increase both SR and GBW.

Unfortunately, the DC gain of these super class AB OTAs is modest [1] due to the use of single-stage architectures without cascode transistors at the output branch. This drawback limits the settling performance of super class AB OTAs, which is determined by both the speed and the accuracy that can be achieved. Fast settling demands single-pole settling performance with a large GBW, and high accuracy implies high DC gain.

Numerous techniques exist for gain enhancement, including operation in weak inversion, cascading, cascoding and positive feedback. However, cascading various gain stages requires compensation, penalizing speed. Cascading also employs multiple circuit branches, degrading power efficiency. The use of cascode transistors at the output branch reduces the output swing, bandwidth and slew rate. By contrast, positive feedback can increase gain and GBW without requiring extra nodes or

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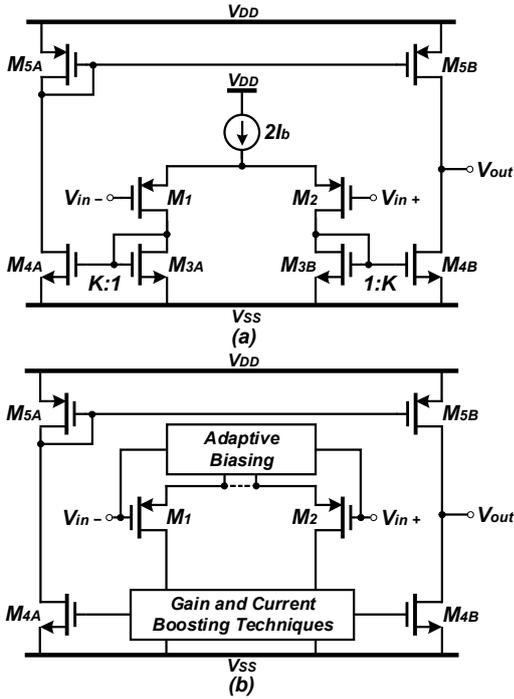


Fig. 1. (a) Class A OTA. (b) Super class AB OTA. power consumption.

In this paper, we propose an alternative approach to design power-efficient super class AB OTAs with DC gain and GBW enhancement, based on combining operation in weak inversion and positive feedback. As a result, both settling time and settling accuracy are improved. The use of weak inversion optimizes the g_m/I_d ratio [10] that is a good approach to improve power efficiency, signal swing and linearity if the application does not require very large bandwidth. Partial Positive Feedback (PPFB) [11] is added to LCMFB leading to two nested (positive and negative) local feedback loops at the active load.

The proposed approach yields very high output driving currents with ultra-low quiescent values, improving the slew rate and exhibiting the highest large-signal figure of merit (FOM_L) reported as far as we know. To show its usability, a Sample and Hold (S/H) circuit is designed based on this technique. The rest of the paper is organized as follows. In Section II, the proposed amplifier is introduced. Section III presents a detailed analysis of the circuit. Section IV describes the S/H. Measurement results for a 180 nm CMOS implementation are given in Section V. Concluding remarks are drawn in Section VI.

II. WEAK INVERSION SUPER CLASS AB OTA

The current mirror OTA is one of the best choices in single-stage amplifiers. Shown in Fig. 1(a), it offers almost rail-to-rail output, and the choice of the current-mirror factor K provides flexibility to the design [12]. The open-loop gain is $A_{OL} = Kg_{m1,2}R_{out}$ and $GBW = Kg_{m1,2}/(2\pi C_L)$, where $g_{m1,2}$ is the transconductance of M_1 and M_2 , R_{out} is the equivalent output resistance, and C_L is the load capacitance. Moreover, the maximum driving current is KI_b , and the slew rate is $SR = KI_b/C_L$. The current efficiency is $CE = K/(K + 1)$ [1]. Notice how the OTA performance can be improved by increasing K . However,

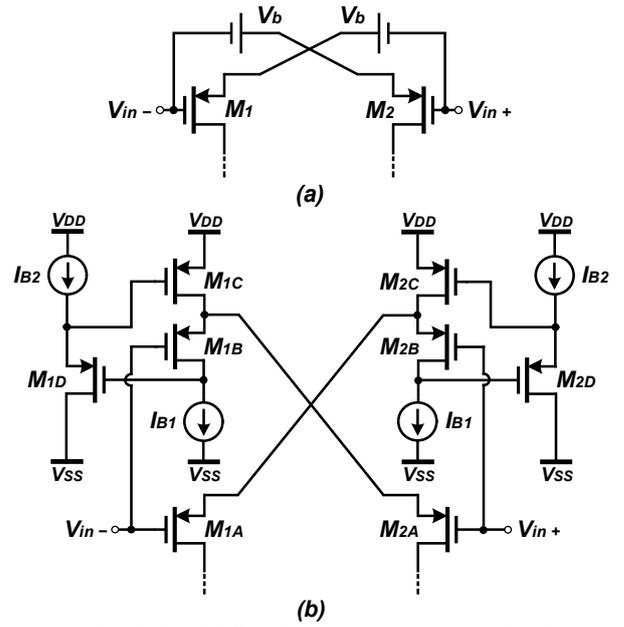


Fig. 2. Adaptive biasing of differential pair. (a) Diagram. (b) Circuit.

various drawbacks appear. First, the power consumption is increased. Secondly, the parasitic capacitance of the current mirror increases, reducing the frequency of the non-dominant pole and the phase margin of the OTA. Finally, area and noise are increased too. Hence, a trade-off between power, speed, area and noise exists.

A modified super class AB version of the current mirror amplifier proposed here is depicted in Fig. 1(b). It is based on replacing the constant tail bias current of the differential pair by an adaptive bias current, and changing the diode-connected active load by an alternative load that provides DC gain and GBW enhancement as well as additional boosting of dynamic currents. Both modifications are described in the following paragraphs.

A. Adaptive Tail Current Biasing

Two cross-coupled floating batteries provide the adaptive biasing of the differential pair as shown in Fig. 2(a). These batteries are implemented by Flipped Voltage Follower (FVF) circuits as can be seen in Fig. 2(b) [1]. Under quiescent conditions, by setting equal $M_{1A,B}$ - $M_{2A,B}$ aspect ratios and assuming perfect matching, current through M_{1A} and M_{2A} is I_{B1} . This current can be properly chosen to operate transistors in weak inversion region, in order to save power consumption and maximize transconductance for such bias current. By contrast, if a large input step is applied, a large dynamic current is delivered by the FVF, which is not bounded by I_{B1} . Due to the cross-coupling of the floating batteries, the full differential input signal is applied to the input transistors, doubling the transconductance of the differential input pair ($g_m \approx 2g_{m1A,2A}$). Hence this technique not only improves large-signal performance, but also the small-signal one [1], [13].

A practical drawback of the conventional FVF is its limited input range. To keep all transistors in saturation $(V_{DD} - V_{SG1B} - V_{SG1C} + V_{SD1B,sat}) \leq V_{in} \leq (V_{DD} - V_{SG1B} - V_{SD1C,sat})$ where $V_{SDi,sat}$ is the saturation voltage of transistor M_i . Hence

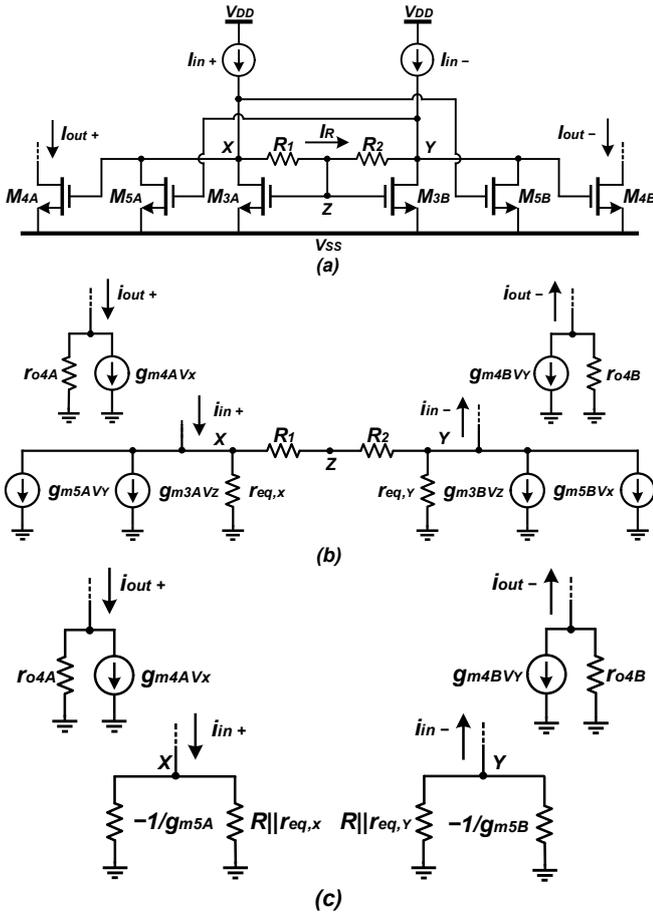


Fig. 3. Non-linear current mirror: (a) Circuit. (b) Small-signal model. (c) Simplified small-signal model.

the peak-to-peak input range is $V_{inpp} = V_{SG1C} - V_{SD1B,sat} - V_{SD1C,sat}$. In weak inversion $V_{SD,sat} \approx 100$ mV [14] so that $V_{inpp} \approx V_{SG1C} - 200$ mV. As V_{SG1} is increased, the input range is improved. However, the transistor then enters strong inversion and the input range becomes $V_{inpp} = |V_{TH}| - V_{SD1B,sat}$, where V_{TH} is the transistor threshold voltage. Note that this range does not increase with higher V_{DD} . In modern nanometer technologies, the reduced V_{TH} degrades significantly the input range, avoiding wide swing operation. In order to increase it, DC level shifters are included in the FVF loop, implemented by M_{1D} , M_{2D} and I_{B2} in common-drain configuration. The new input peak-to-peak range is $V_{inpp} = V_{SG1C} + V_{SG1D} - V_{SD1B,sat} - V_{SD1C,sat}$. Again, assuming weak inversion operation, $V_{inpp} \approx V_{SG1C} + V_{SG1D} - 200$ mV. Notice how the signal swing is incremented by an additional gate-to-source voltage, achieving the desired wide swing operation. A drawback of the DC level shift introduced is an increase in quiescent power. However, very low I_{B2} and W/L of M_{1D} , M_{2D} can be used, obtaining a large input range extension with very little extra power. Moreover, an additional pole is created, but it does not influence the OTA since it is at high frequency.

B. Active Load Based on Nested Feedback Loops

The active load employed is the input stage of the non-linear differential current mirror shown in Fig. 3(a). It combines local

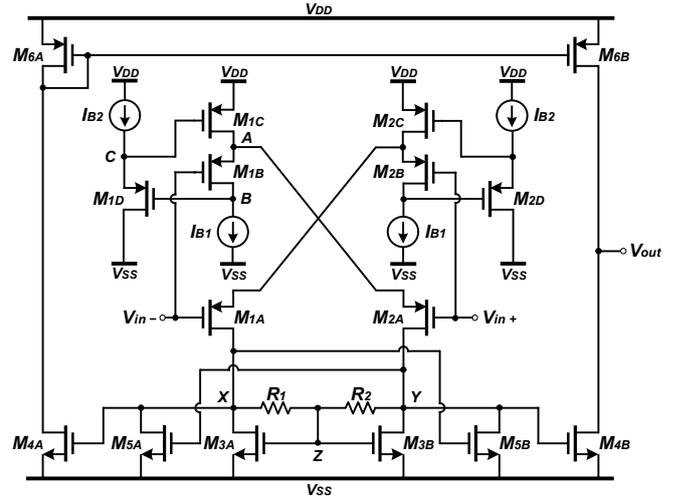


Fig. 4. Proposed super class-AB OTA.

negative feedback to the common Z node via resistors R_1 and R_2 as well as partial positive feedback by transistors M_{5A} and M_{5B} . To analyze the operation of the circuit three different conditions are studied: quiescent behavior, small-signal operation and large-signal operation.

In static conditions, there is no current through resistors $R_{1,2}$, so $V_X = V_Y = V_Z$ and M_{3A} and M_{3B} can be regarded as diode-connected devices. Hence the quiescent behavior is like a conventional differential current mirror. Transistors M_{5A} and M_{5B} act as current starving devices that reduce the quiescent output current by a factor α , with $\alpha = (W/L)_{5A,B}/(W/L)_{3A,B}$. Therefore they contribute to increasing output resistance and DC gain of the OTA.

Considering small-signal performance, the effect of the nested feedback loops is evidenced by the equivalent small-signal model of Fig. 3(b), with g_{mi} and r_{oi} the transconductance and output resistance of transistor M_i , $r_{eq,X} = r_{o3A} || r_{in}$, $r_{eq,Y} = r_{o3B} || r_{in}$ and r_{in} the resistance of the input current sources. Let's assume that the circuit of Fig. 3(a) is perfectly symmetrical with $R_1 = R_2 = R$ and matched M_{iA} and M_{iB} devices ($i = 3, 4, 5$) and that the input current is fully differential ($i_{in+} = -i_{in-} = i_d/2$). Then a nonzero i_d leads to complementary voltages at nodes X and Y ($v_X = -v_Y$), node Z becomes a virtual ground ($v_Z = 0$) and the small-signal model can be simplified as shown in Fig. 3(c). Positive feedback by M_{5A} and M_{5B} leads to a negative resistance that raises the resistance at the X and Y nodes:

$$R_X = R_Y = R_{X,Y} = R || r_{eq,X,Y} || \frac{-1}{g_{m5A,B}} = \frac{R || r_{eq,X,Y}}{1 - g_{m5A,B}(R || r_{eq,X,Y})} \quad (1)$$

The small-signal current gain is therefore

$$A_I = \frac{i_{od}}{i_{id}} = g_{m4A,B} R_{X,Y} = \frac{g_{m4A,B}(R || r_{eq,X,Y})}{1 - g_{m5A,B}(R || r_{eq,X,Y})} \quad (2)$$

Note that due to the virtual ground at node Z , A_I does not depend on $g_{m3A,B}$, and that any parasitic capacitance at node Z has no effect. Note also that A_I (and therefore the OTA transconductance) increases due to the increased resistance at nodes X and Y . Both local feedback loops contribute to this increase.

Regarding large-signal operation, when a large positive differential current $I_{id} = I_{in+} - I_{in-}$ is applied, voltages at nodes X and Y start to unbalance due to the voltage drop at the feedback resistors. This unbalance is reinforced due to the positive feedback of transistors M_{5A} and M_{5B} acting as inverting amplifiers, improving settling time. Soon V_X becomes large and V_Y is near 0. Then transistor M_{5A} enters cut-off and M_{5B} is in deep-triode region, so they no longer influence during slewing. Transistor M_{4A} enters strong inversion and since it is in saturation, it delivers a large current while current in M_{4B} becomes approximately 0. Using the simple square law model for strong inversion and saturation, the differential output current becomes:

$$I_{od} \approx I_{o+} \approx \frac{\beta_{4A}}{2} \left(\sqrt{\frac{2I_{cm}}{\beta_{3A,B}}} + \frac{R_1 I_{id}}{2} \right)^2 \quad (3)$$

where $\beta_i = \mu_n C_{ox}(W/L)_{Mi}$ and $I_{cm} = (I_{in+} + I_{in-})/2$ is the common-mode input current. Analogously, a large negative I_{id} leads to a large positive swing at node Y and a differential output current

$$I_{od} \approx -I_{o-} \approx -\frac{\beta_{4B}}{2} \left(\sqrt{\frac{2I_{cm}}{\beta_{3A,B}}} - \frac{R_2 I_{id}}{2} \right)^2. \quad (4)$$

Hence, a quadratic boosting of the dynamic input current is produced, improving SR. This boosting takes place directly in the output transistors, avoiding internal replicas. Consequently, a near optimal CE is achieved [1].

III. CIRCUIT ANALYSIS

The detailed schematics of the proposed OTA using the techniques presented in Section II is shown in Fig. 4. The main performance parameters are analyzed below.

A. Small-Signal Performance

When a small-signal differential voltage v_{id} is applied to the OTA input, the adaptively biased input pair provides two complementary currents $i_{1A} = -i_{2A} = g_{m1A,2A}v_{id}$ that enter into the non-linear current mirror of Fig. 3. Hence the OTA transconductance is:

$$G_m = \frac{i_{od}}{v_{id}} = A_I \frac{i_{id}}{v_{id}} = 2g_{m1A,2A}g_{m4A,B}R_{X,Y} = \frac{2g_{m1A,2A}g_{m4A,B}(R||r_{eqX,Y})}{1 - g_{m5A,B}(R||r_{eqX,Y})} \quad (5)$$

and $GBW = G_m/(2\pi C_L)$. Note from (1) that the negative resistance generated by the PPFB increases $R_{X,Y}$, enhancing G_m .

If $(R||r_{eqX,Y}) = 1/g_{m5A,B}$, then G_m ideally tends to infinity. However, the system becomes unstable. Using the expression $GBW = f_{nd}tg(90^\circ - \varphi)$ with $GBW = G_m/(2\pi C_L)$ and $f_{nd} = 1/(2\pi R_{X,Y}C_{X,Y})$ the non-dominant pole, the phase margin φ is

$$\varphi \approx 90^\circ - tg^{-1} \left(\frac{2g_{m1A,2A}g_{m4A,B}R_{X,Y}^2 C_{X,Y}}{C_L} \right) \quad (6)$$

where $C_{X,Y} \approx C_{GS4} + C_{GB4} + C_{GS5} + C_{GB5}$ is the parasitic capacitance at nodes X and Y . A maximum value to preserve stability considering PVT variations in PPFB is $\alpha = 0.8$ [11], which avoids in the proposed OTA too large values for $R_{X,Y}$. In our case, an even more conservative value of $\alpha = 0.5$ was chosen to enforce stability even with very large PVT variations.

Notice from (6) the negligible effect of C_{GS3} and C_{GB3} due to the AC virtual ground at node Z . As a design remark, the gate-to-bulk parasitic capacitance is considered in weak inversion, where $C_{GB} > (C_{GS} \approx C_{GD})$. This differs from strong inversion, in which $C_{GS} \gg C_{GB} > C_{GD}$ is usually adopted.

Note that the phase margin of (6) is an approximate expression that considers only the output dominant pole and the non-dominant ones at nodes X and Y . However, the FVF introduces additional poles, located at A , B and C nodes. For relatively large C_L these poles have a minor effect due to their high frequency behavior.

B. Linear Small-Signal Settling

To compute the nested loop influence on the linear settling response, the time constant τ is calculated. For simplicity, a single-pole system is considered with $H(s) = A_{OL}/(1 + s/\omega_o)$, where ω_o is the dominant pole. The OTA is configured in unity gain closed-loop configuration, where the feedback factor is $\beta = 1$. Defining $A_{CL}(s) = H(s)/(1 + \beta H(s))$ the closed-loop transfer function, once substituted $H(s)$ becomes:

$$A_{CL}(s) = \frac{A_{OL}/(1 + A_{OL})}{1 + \frac{s}{(1 + A_{OL})\omega_o}} \approx \frac{A_{OL}}{1 + A_{OL}} \cdot \frac{1}{1 + \frac{s}{A_{OL}\omega_o}} \quad (7)$$

where $\tau = 1/(A_{OL}\omega_o) = 1/(2\pi GBW)$. Defining $GBW = G_m/(2\pi C_L)$, the time constant is given by

$$\tau = \frac{1 - g_{m5A,B}(R||r_{eqX,Y})}{2g_{m1A,2A}g_{m4A,B}(R||r_{eqX,Y})} C_L \quad (8)$$

where the output response for a unity input step $V_{in} = u(t)$ can be expressed as

$$V_{out}(t) \approx \frac{A_{OL}}{1 + A_{OL}} (1 - e^{-t/\tau}). \quad (9)$$

Notice the effect of both PPFB and LCMFB nested techniques. As $g_{m5A,B}(R||r_{eqX,Y})$ approaches 1, τ is proportionally reduced and A_{OL} is increased, improving the settling response. However, for values higher than 1, the time constant becomes negative, producing an unstable exponential output (equivalently, the pole is shifted to the RHP). In the same manner, as

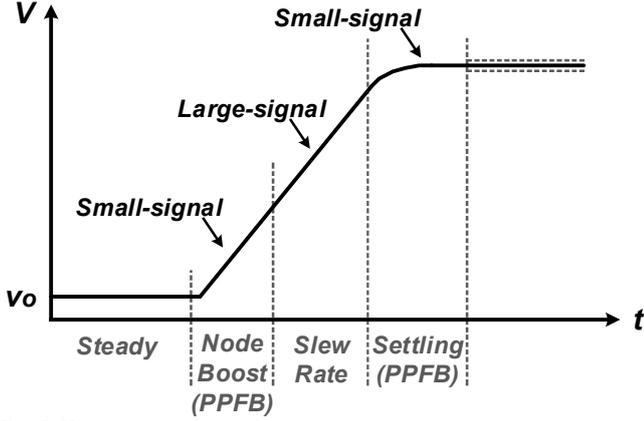


Fig. 5. Unity gain transient response.

LCMFB resistors $R_{1,2}$ are increased, the response becomes faster. The analysis becomes more complex since as $R_{X,Y}$ increases, the pole at nodes X and Y shifts to lower frequencies, and the single-pole approximation used for linear settling analysis is no longer valid.

C. Non-Linear Large-Signal Settling

To evaluate the non-linear settling performance, the slew rate of the circuit is analyzed. During static conditions, no differential input is present in the OTA. Currents I_{1A} and I_{2A} in M_{1A} and M_{2A} are equal to I_{B1} , and no current flows through R_1 and R_2 . This gives rise to define X , Y and Z node voltages in weak inversion as

$$V_X = V_Y = V_Z = V_{TH} + nV_t \ln \left(\frac{I_{B1}(1-\alpha)}{I_o(W/L)_{3A,B}} \right) \quad (10)$$

where I_o is a process-dependent current, V_t is the thermal voltage and n is the slope factor. However, upon application of a large input step $V_{id} = V_{in+} - V_{in-}$, a differential input current $I_{id} = I_{1A} - I_{2A}$ is delivered by the FVFs. Due to the presence of the LCMFB, a large voltage swing is generated at nodes X and Y , leading to a current $I_R = I_{id}/2 = (I_{1A} - I_{2A})/2$ flowing through both resistors. Besides, PPFB speeds up the voltage unbalance at nodes X and Y . The current through M_{3A} and M_{3B} is the common-mode component, $I_{cm} = (I_{1A} + I_{2A})/2 - (I_{5A} + I_{5B})/2 = I_{B1}(1-\alpha)$.

As described in Section II, PPFB by M_{5A} and M_{5B} reinforces the initial voltage unbalance at nodes X and Y , enhancing settling time. However, once a large differential voltage appears between nodes X and Y , these transistors have not effect. When the transient response is ending so that the circuit enters again the linear mode, PPFB again helps to get a faster and more accurate response due to its effect on increasing gain and GBW. These concepts are illustrated in Fig. 5.

Note that due to the high dynamic currents, some transistors leave weak inversion; they go through moderate inversion and finally enter strong inversion region. However, once reached the steady state, the circuit returns to the initial inversion mode. This is an intrinsic characteristic of class AB circuits, in which, in spite of designing them in a low power weak inversion quiescent mode, they operate in strong inversion during transients.

Considering operation in strong inversion for transistors carrying large dynamic currents, and noting that PPFB has not effect in the value of these large currents, the slew rate $SR = I_{out}/C_L$, is the same as in [1] and given by:

$$SR \approx \frac{\beta_{4A,B}}{2C_L} \left(\sqrt{\frac{\beta_{1A,2A}}{2\beta_{3A,B}}} |V_{id}| + \frac{\beta_{1A,2A}R}{4} V_{id}^2 \right)^2 \quad (11)$$

where it has been assumed that $R \ll r_{eq,X,Y}$. Note that SR ideally increases with V_{id}^4 .

Current efficiency is approximately given by $|I_{out}|/(|I_{out}| + I_{cm})$. Noting that $|I_{out}| \gg I_{cm}$ under dynamic conditions, current efficiency approaches the ideal value of 1.

D. Noise

Both thermal and flicker noise are considered, whose spectral densities are defined in a CMOS device as

$$\overline{V_n^2}(f) = \frac{4kT\gamma}{g_m} + \frac{K_{P/N}}{C_{ox}WLf} \quad (12)$$

where k is the Boltzmann's constant, T is the temperature, γ is equal to 1/3 in weak inversion and 2/3 in strong inversion [15], $K_{P/N}$ is the flicker noise coefficient (different for a PMOS or NMOS transistor), and f is the frequency. The first and second terms corresponds to the thermal and flicker noise densities, respectively. Note also that this expression is valid for the three regions of inversion [15]. In the same way, the thermal noise density for a resistor of resistance R is

$$\overline{V_{nR}^2} = 4kTR. \quad (13)$$

Assuming all noise sources are uncorrelated and $g_m r_o \gg 1$, the input referred thermal and flicker noise density expressions are given by

$$\overline{V_{T,in}^2} = \frac{2kT\gamma}{g_{m1A}} \left[2 + (1+\alpha) \frac{g_{m3A}}{g_{m1A}} + \frac{g_{m1B1}}{g_{m1A}} + \frac{1}{\gamma g_{m1A} R} + \frac{1}{A_f^2} \left(\frac{g_{m4A}}{g_{m1A}} + \frac{g_{m6A}}{g_{m1A}} \right) \right] \quad (14)$$

$$\overline{V_{F,in}^2}(f) = \frac{K_P}{2C_{ox}f} \cdot \left[\frac{2}{W_{1A}L_{1A}} + (1+\alpha) \frac{K_N}{K_P} \left(\frac{g_{m3A}}{g_{m1A}} \right)^2 \frac{1}{W_{3A}L_{3A}} + \frac{1}{A_f^2} \frac{K_N}{K_P} \left(\frac{g_{m4A}}{g_{m1A}} \right)^2 \frac{1}{W_{4A}L_{4A}} + \frac{1}{A_f^2} \left(\frac{g_{m6A}}{g_{m1A}} \right)^2 \frac{1}{W_{6A}L_{6A}} + \frac{K_N}{K_P} \left(\frac{g_{m1B1}}{g_{m1A}} \right)^2 \frac{1}{W_{1B1}L_{1B1}} \right] \quad (15)$$

where g_{m1B1} is the transconductance of the transistors implementing the I_{B1} current sources, and the following assumptions $g_{m1A} = g_{m2A} = g_{m1B} = g_{m2B}$, $g_{m3A} = g_{m3B} = \alpha g_{m5A} = \alpha g_{m5B}$, $g_{m4A} = g_{m4B}$, $g_{m6A} = g_{m6B}$ and $R_1 = R_2 = R$ has been used. As expected,

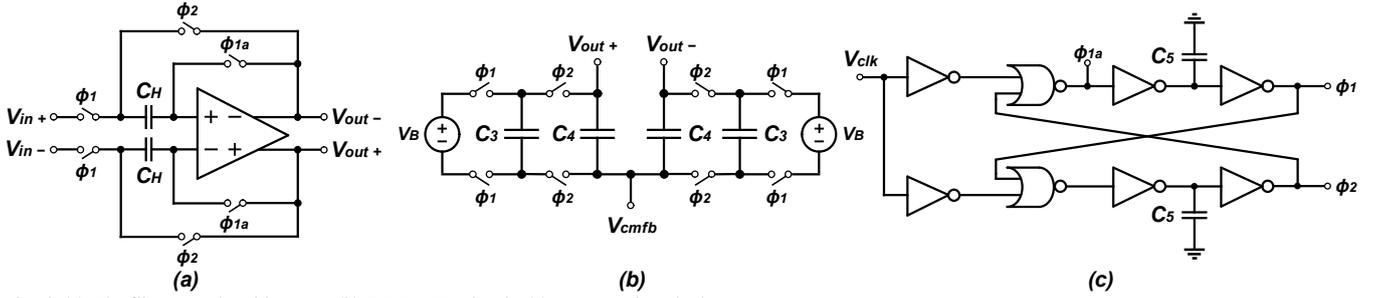


Fig. 6. (a) S/H flip-around architecture. (b) SC-CMFB circuit. (c) Non-overlap clock generator.

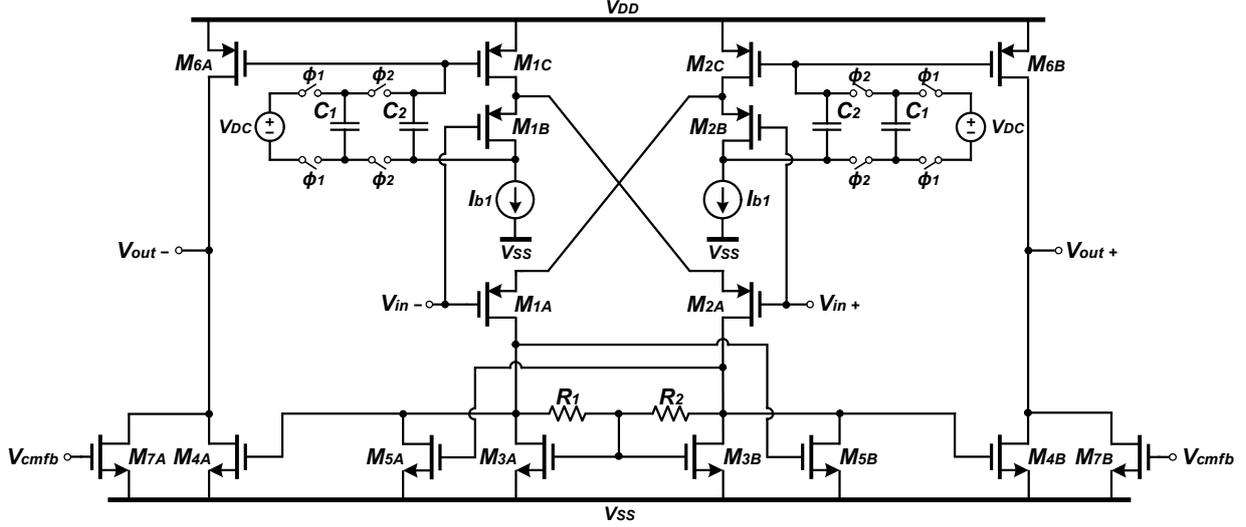


Fig. 7. Proposed fully-differential switched-capacitor super class-AB OTA.

input-referred noise is minimized by maximizing transconductance and channel area of the input transistors. Note that due to the small-signal gain A_I in (2) of the nested-feedback nonlinear current mirror, the output branch transistors have less influence on the input-referred noise. A larger α increases noise contribution of $M_{5A,B}$, but it also increases A_I and hence the gain, leading to an overall input-referred noise reduction.

IV. SAMPLE-AND-HOLD APPLICATION EXAMPLE

In order to apply the high driving capability of the OTA, a low-power S/H is designed. It is based on the well-known *flip-around* architecture [16], [17], shown in Fig. 6(a). One intrinsic characteristic is its reset nature during the sample mode (ϕ_1 - ϕ_{1a} phases), generating a virtual ground at the input and output. In the hold mode (ϕ_2 phase), the capacitor is switched to process the sample. As a result, the output experiences a large step from the previous virtual ground to the actual sampled value. Consequently, a high slew rate is required. Another characteristic is the reduced offset, being stored during ϕ_1 - ϕ_{1a} and subtracted during ϕ_2 [18].

The architecture is very simple, requiring only an OTA, the sampling capacitors and various switches. Due to the non-idealities of the switches, clock feedthrough and charge injection effects should be considered [16], [20], which lead to a voltage error of

$$\Delta V = V_{CLK} \frac{WC_{ov}}{WC_{ov} + C_H} + \frac{q_{inj}}{C_H} \quad (16)$$

where V_{CLK} is the clock amplitude, W and C_{ov} are the switch transistor width and overlap capacitance, respectively, and q_{inj} is the charge injection produced by the switches. Notice how this error can be minimized by increasing C_H , at the cost of degrading the area. Hence, a trade-off between non-ideal effects mitigation and increased area exists. The relatively large supply voltage employed allows simple small-size transmission gate switches with relatively low on resistance without having to resort to clock boosting circuits. Remark also how phase ϕ_{1a} is turned off slightly before than ϕ_1 , avoiding the charge injection introduced by the switches controlled by ϕ_1 . Therefore, the critical element is the OTA, which must exhibit a good set of characteristics in terms of power, slew rate, bandwidth, settling time and linearity. Due to its high performance, the proposed OTA is highly suitable in those low-power switched-capacitor (SC) applications requiring large slew rates to rapidly charge and discharge the capacitors.

A. Switched-Capacitor Super Class-AB OTA

In order to implement the S/H, some modifications are carried out in the OTA. Shown in Fig. 7, the topology is converted into fully-differential. The FVF nodes are re-used to drive the output transistors [19], the output being a true class AB stage. This arrangement does not affect the current efficiency because the driving current is generated directly at the output, which is given by $|2I_{out}|/(|2I_{out}| + I_{cm}) \approx 1$. The conventional FVF with a continuous time DC level-shifter is replaced by a novel SC-FVF with a dynamic DC level-shifter, implemented by C_1 and C_2 . During ϕ_1 , C_1 is pre-charged to V_{DC} , being this voltage the desired DC level shift. During ϕ_2 , C_1 transfers to C_2 such

TABLE I
CLASS-AB OTA PERFORMANCE PARAMETERS AND COMPARISON

Parameter	This work	[2] [TCAS-2'12]	[3] [TCAS-1'15]	[4] [TCAS-1'16]	[5] [TCAS-1'16]	[6] [JSSC'18]	[7] [TCAS-1'18]	[8] [TCAS-1'20]
CMOS process	0.18- μm	0.18- μm	65-nm	0.18- μm	0.18- μm	0.5- μm	40-nm	0.18- μm
Supply voltage [V]	± 0.75	0.8	0.5	1.8	1.1	± 1	1.1	0.8
Capacitive load [pF]	100	8	3	200	100	70	0.5	130
Stage Type	Single	Single	Pseudo-Three	Single	Pseudo-Single	Single	Two	Single
Pos. Slew Rate [V/ μs]	4	0.14	43	74.1	8.7	13.2	1250	1.24
Neg. Slew Rate [V/ μs]	-4.5	--	--	--	--	-25.3	--	-0.826
Pos. settling (1%) [μs]	9.5	--	--	--	1.2	0.12	0.0018	0.55
Neg. settling (1%) [μs]	1.6	--	--	--	--	0.10	--	0.56
GBW [MHz]	0.038	0.049	38	86.5	1.7	3.4	3600	1.12
Phase Margin [$^\circ$]	90	60	57	50	69	75.1	65	67.8
	-56	-52				-55.5	-55.7	-56.3
THD [dB]	@1 kHz 0.75 V _{pp}	@1 kHz 0.5 V _{pp}	-48	--	--	@25 kHz 0.5 V _{pp}	@500 MHz 1 V _{pp}	@10 kHz 0.1 V _{pp}
Eq. Input Noise [nV/ $\sqrt{\text{Hz}}$]*	71.4 @38 kHz	--	926	0.8 @100 kHz	--	35 @1 MHz	2.6 @250 MHz	68.8 @100 kHz
DC gain [dB]**	46	51	46	72	100	76.8	49	102.7
CMRR (DC) [dB]**	106	--	35	--	--	112	--	137.7
PSRR+ (DC) [dB]**	47	--	37	--	--	92	--	114.8
PSRR- (DC) [dB]**	69	--	--	--	--	113	--	136.9
Input offset [mV]†	-0.3	0.5	7.3	--	--	--	--	1.24
Power [μW]	1.8	1.2	182	11900	7.4	100	3300	36
Area [mm^2]	0.012	0.057	0.005	0.070	0.0021	0.030	0.050	0.021
FOM _L [(V/ μs)(pF/ μW)]	236.1	0.93	0.71	1.25	117.5	13.5	0.19	3.73
FOM _S [(MHz)(pF/ μW)]	2.1	0.33	0.63	1.45	23.0	2.38	0.55	4.04

* Simulation.

** Post-layout simulation.

† Averaged with 10 chips.

voltage, generating the desired level.

An advantage of the proposed SC-FVF is the reduced power in comparison with the continuous time counterpart because of the bias current elimination. Another advantage is that the DC level shift can be accurately programmed in a wider range in comparison with the continuous-time version, providing flexibility to the design. Denoting such DC shifting value as V_{DC} , the input swing is given by the following equation

$$V_{inpp} = V_{DC} + \Delta V + V_{SG1C} - V_{SD1B,sat} - V_{SD1C,sat} \quad (17)$$

with ΔV the voltage error due to the switch non-idealities, as mentioned in (16). Substituting $V_{SD,sat} \approx 100$ mV, last expression can be approximated by $V_{inpp} \approx V_{DC} + \Delta V + V_{SG1C} - 200$ mV. One drawback of this implementation is the increased area. However, in those SC applications in which area is not a critical constraint, it is a good choice because of its widely programmable input range and reduced power consumption.

The output is controlled by a switched-capacitor common-mode feedback (SC-CMFB) [21], [22], shown in Fig. 6(b). This scheme has the advantage of being a passive circuit, not affecting the power consumption and not limiting the output swing. The output DC voltage is pre-charged across C_3 and then the charge is transferred into C_4 to regenerate the common-mode component. Capacitors C_4 sense the common-mode output voltage, generating the required control signal. This signal is applied to M_{7A} and M_{7B} . A detailed analysis of this CMFB circuit can be found in [22]. As described in [22], the main effect of the switches is an output common-mode voltage error mainly due to charge injection of the switches controlled by ϕ_1 and leakage currents of the switches controlled by ϕ_2 , which can be

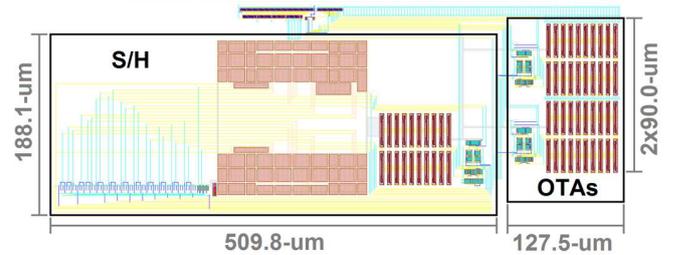
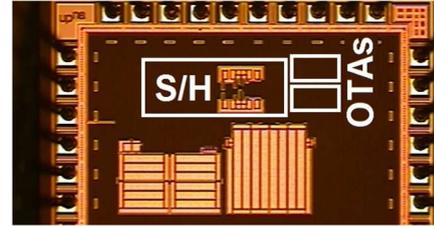


Fig. 8. Test chip microphotograph and layout. Due to the opaque passivation layer, only MiM capacitors are shown.

minimized by properly sizing such switches and choosing large enough C_3 and C_4 .

The non-overlap clock phases are generated by the topology of Fig. 6(c). The delay between ϕ_1 and ϕ_{1a} phases is controlled by C_5 .

V. SIMULATION AND MEASUREMENT RESULTS

A test prototype was fabricated in UMC 0.18- μm 1P6M MiM 1.8 V CMOS technology. The chip contains both OTA (Fig. 4) and S/H (Figs. 6 and 7) circuits, to validate experimentally each design. The OTA was loaded off-chip with 100 pF and the S/H with 15 pF. The die photograph and layout for both OTA as well as S/H are shown in Fig. 8.

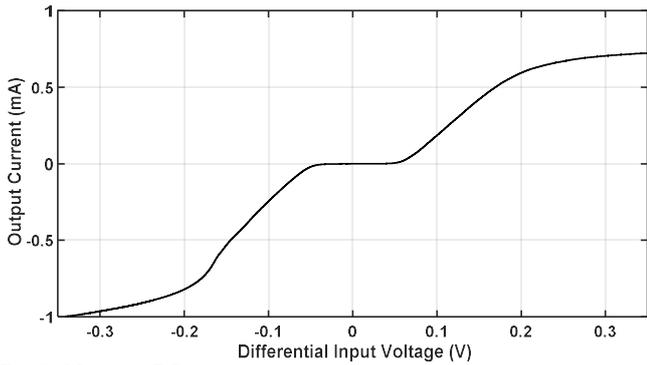


Fig. 9. Measured DC output characteristics.

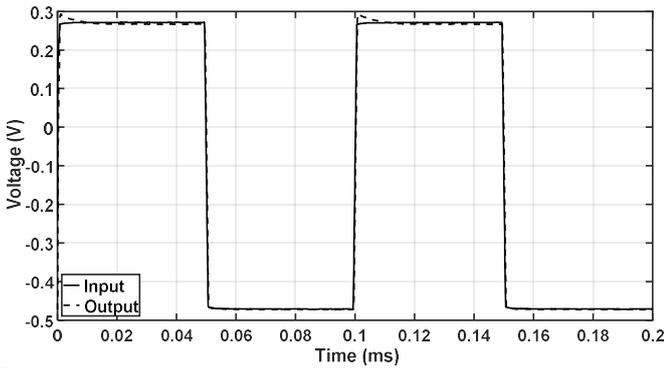


Fig. 10. Measured large-signal response.

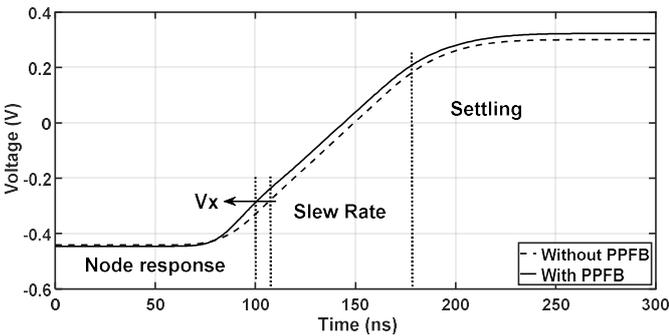


Fig. 11. Simulated settling performance.

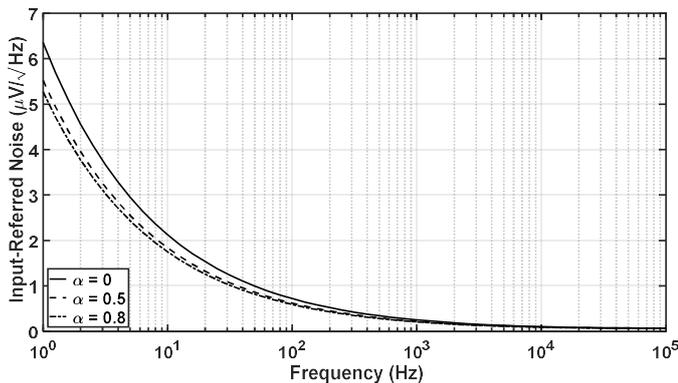


Fig. 12. Simulated input-referred noise for different α values.

The proposed OTA of Fig. 4 was fabricated in both open-loop and unity gain closed-loop configurations. The aspect ratios (in $\mu\text{m}/\mu\text{m}$) of transistors $M_{1A,B,C}$, $M_{2A,B,C}$, $M_{3A,B}$, $M_{4A,B}$ and $M_{6A,B}$ were 18/0.36 and those of M_{1D} and M_{2D} were 1/0.25. The PPFB $M_{5A,B}$ were 9/0.36, hence $\alpha = 0.5$. As mentioned above,

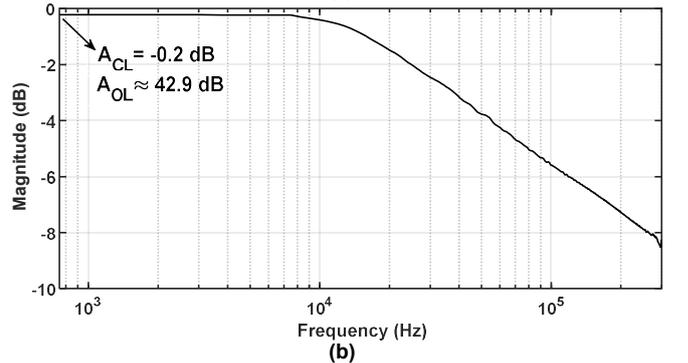
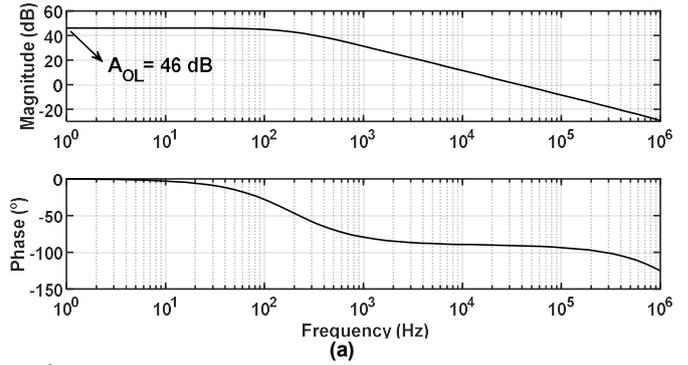


Fig. 13. (a) Simulated open-loop and (b) measured closed-loop frequency responses when $C_L = 100$ pF.

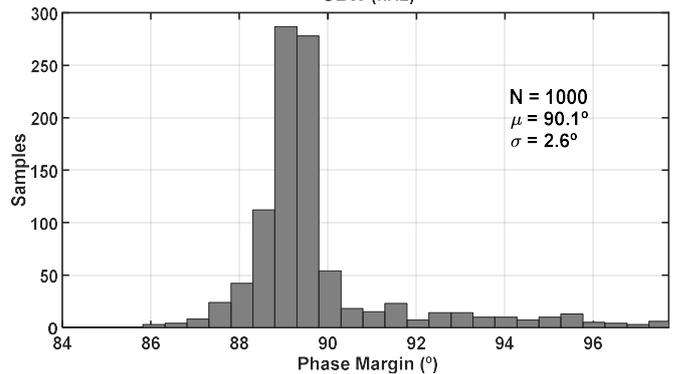
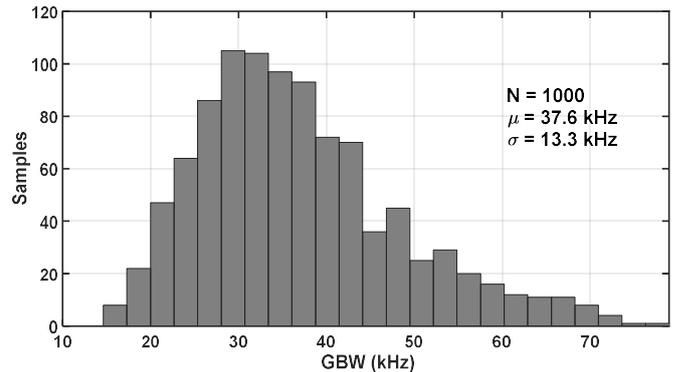


Fig. 14. GBW and Phase Margin Monte-Carlo analysis when $C_L = 100$ pF.

this ratio keeps a very conservative safety margin to enforce stability even with very large PVT variations or mismatch. Finally, resistors $R_{1,2}$ were 300 k Ω . Both resistors were implemented by a high-resistivity polysilicon layer. They were interdigitized and surrounded by dummy strips. Similar layout techniques were also adopted for the transistors. The supply voltage was set to ± 750 mV, and the bias currents I_{B1} and I_{B2} to 130 nA

and 65 nA, respectively. In this way, all transistors are biased in weak inversion.

Regarding the input range, simulations show that $V_{SG1,2C} \approx 400$ mV and $V_{SG1,2D} \approx 550$ mV, leading to an input range of 750 mV. Without the level shifter, the input range would be 200 mV. Fig. 9 shows the measured DC open-loop output current versus differential input voltage, driven by an Agilent 33522A arbitrary waveform generator. To measure it, a transimpedance amplifier was connected to the OTA output for current-to-voltage conversion [6]. The resulting response was measured in a Tektronix TDS5104 oscilloscope. Note the class AB operation, with output currents not limited by the bias current. The measured CB is larger than 5000.

To characterize the slew rate, the unity-gain configuration was used with a 750 mV_{pp} 10 kHz square input signal. Fig. 10 shows the measured response. The positive and negative slew rates were 4 V/ μ s and -4.5 V/ μ s, respectively. Fig. 11 compares the simulated settling performance with and without PPFB. Note that as predicted in Section III, PPFB reduces the time it takes for the output to start rising (hence reducing settling time) and leads to a final value closer to the input voltage (increasing settling accuracy).

The simulated input noise for different α values is depicted in Fig. 12. The curves correspond to the cases without PPFB ($\alpha = 0$), the conservative configuration ($\alpha = 0.5$) and the maximum recommended value regarding PVT variations ($\alpha = 0.8$). Notice the good agreement with the theoretical prediction in equations (14) and (15). Remark again how PPFB reduces the input noise as α is increased.

The simulated open-loop and measured unity gain closed-loop frequency responses are shown in Fig. 13 for a 100 pF load. The measured closed-loop unity gain was $A_{CL} = -0.2$ dB. Defining this as $A_{CL} \approx A_{OL}/(1 + A_{OL})$, the extrapolated open-loop gain is 42.9 dB, which is consistent with the simulated $A_{OL} = 46$ dB value. The simulated open-loop GBW was 37.7 kHz and the measured -3 dB bandwidth for the closed-loop configuration was 38 kHz with a phase of -45°. Hence, the extrapolated phase margin is 90°. These are good approximations to the GBW and phase margin due to the strongly dominant pole at the output. Notice that the measured values are in good agreement with simulations.

In Fig. 14, a Monte-Carlo analysis shows the effects of process and mismatch variations in terms of GBW and phase margin, obtained for a run of 1000 simulations. Due to the short transistor lengths employed, the GBW variability is evident, as it is usual in micrometer technologies. By contrast, the phase margin exhibits lower variations, mainly due to the high capacitive load, approximating the OTA to a single-pole amplifier.

Table I summarizes the main measured parameters and compares them with other existing OTAs. To quantitatively compare the OTA performance with other reported designs, the following well-known figures-of-merit are used:

$$FOM_L = SR \frac{C_L}{P} \quad (18)$$

$$FOM_S = GBW \frac{C_L}{P} \quad (19)$$

where P is the quiescent power consumption. Equations (18) and (19) reflect the performance in terms of large and small-signal for a given capacitive load and power, respectively. It is worth noting that the designed OTA exhibits the highest FOM_L , demonstrating the possibility of achieving high slew rates for high capacitive loads while preserving at the same time a very low power consumption.

The measured noise efficiency factor [23] for $\alpha = 0.5$ is

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{\pi \cdot V_t \cdot 4kT \cdot BW}} = 5.18 \quad (20)$$

with $V_{ni,rms}$ the input referred noise voltage and I_{tot} the total quiescent current. The NEF is especially useful when low frequency signals are considered and the flicker noise degrades considerably the signal-to-noise ratio. Due to the low frequency S/H proposed, this metric might result useful in its characterization. So as to calculate $V_{ni,rms}$, the total input referred noise density was integrated from 1 Hz to 38 kHz, leading a value of 24.0 μ V_{rms}. Although the fabricated OTA was not optimized for low noise, the overall OTA exhibits a NEF performance similar to other designs reported in [23], or the neural amplifier proposed in [24]. To further reduce NEF, various design guidelines can be considered. As mentioned, the noise performance is improved by increasing the α ratio. Another strategy consists in keeping the input differential pair in weak inversion and operating the current mirrors in strong inversion in order to maximize and minimize their g_m/I_D ratio, respectively. Other option consist of increasing the transistor widths and lengths while keeping a constant aspect ratio (especially for input transistors), which in general terms reduces the flicker noise. Finally, high performance noise-reduction techniques such as chopping stabilization can be implemented [20].

The fabricated S/H employs the switched OTA of Fig. 7 as well as MiM capacitors. The bias current and the transistor aspect ratios were the same as the single-ended OTA. The aspect ratio of M_{7A} and M_{7B} was 18/0.36. The capacitor values were 750 fF for C_1 and C_3 , 250 fF for C_2 and C_4 and 500 fF for C_H and C_5 . These values have been selected as a trade-off between area and non-idealities mitigation. The output common-mode voltage V_B was applied externally with the negative terminal grounded. The switched DC level shifter V_{DC} was set externally to 500 mV.

The response of the S/H is given in Fig. 15(a). To measure it, an input sinusoid of 1 kHz, with a full-range of 750 mV_{pp} was used. The sampling frequency was 10 kHz. Notice how, in those samples with high values, the transient response is very fast because of the class AB behavior. The maximum overshoot is 14%, mainly due to the highly non-linear operation during large transients.

The maximum sampling frequency is 25 kHz at full-scale. This value is measured by the acquisition and hold mode settling times t_{acq} and t_{hs} . Considering both parameters, the maximum sample rate is given by $f_{s,max} = 1/(t_{acq} + t_{hs})$. This

TABLE II
S/H PERFORMANCE PARAMETERS AND COMPARISON

Parameter	This work	[25] [JSSC'07]	[26] [TCAS-2'09]	[27] [ISCAS'10]	[28] [TCAS-2'10]	[29] [TCAS-1'11]	[30] [TCAS-2'18]	[18] [Acc.'20]
CMOS process	0.18- μm	0.25- μm	0.13- μm	90-nm	90-nm	0.13- μm	0.18- μm	0.13- μm
Supply voltage [V]	± 0.75	0.5	0.8	1	1.2	0.6	± 0.9	± 0.6
Capacitive load [pF]	15	--	0.2	--	2.5	--	23	25
Architecture Type	S/H	T/H	S/H	T/H	T/H	S/H	T/H	S/H
Fabricated	Yes	Yes	No	No	Yes	No	Yes	Yes
Sampling Frequency [MHz]	0.025	1	40	500	100	0.02	1	1.5
Pedestal Error [mV]	10	0.8	--	≤ 4.9	--	--	--	--
Droop rate [$\mu\text{V}/\text{ms}$]	≤ 5	7600	--	--	--	--	--	--
Acquisition time [μs]	25.5	--	--	--	--	--	--	--
Hold mode settling [μs]	14	--	--	--	--	--	--	--
THD [dB]*	-45 @2.5 kHz 0.75 V _{pp}	--	-56 @40 MHz 1.4 V _{pp}	-60.5	-68 @100 MHz 0.8 V _{pp}	-40 @1 kHz	--	-72
SFDR [dB]*	48	--	57	69	70	60	68	--
SNDR [dB]*	45	60	67	60.5	61	59.3	--	--
ENOB†	7.2	9.7	10.8	9.8	9.8	9.6	11.0	11.7
Power [μW]	2	300	500	6000	2970	0.028	360	300
Area [mm^2]	0.096	0.16	--	--	0.023	--	0.11	--
FOM [kHz/ μW]	90	32.3	864	817	330	6857	30.6	58.5

* Post-layout simulation.

† ENOB = (SNDR - 1.76) / 6.02 (In those cases in which SNDR is not reported, the SFDR or THD are used instead).

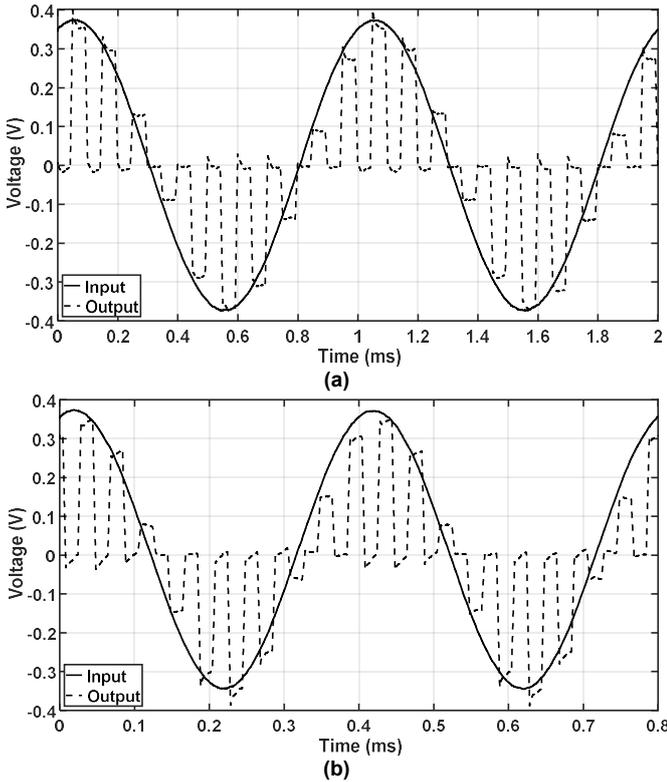


Fig. 15. Measured S/H response with 750 mV sinusoidal input. (a) $f_{in}=1$ kHz, $f_s=10$ kHz. (b) $f_{in}=2.5$ kHz, $f_s=25$ kHz.

characterization is depicted in Fig. 16. In Fig. 15(b) the S/H response for a sinusoidal input of 2.5 kHz, sampled at 25 kHz is shown. Finally, Table II summarizes the main measured parameters of the S/H. To allow comparison with other S/H circuits the following figure of merit has been used, which relates the sampling frequency f_s , the equivalent number of bits ENOB and the total power dissipation P

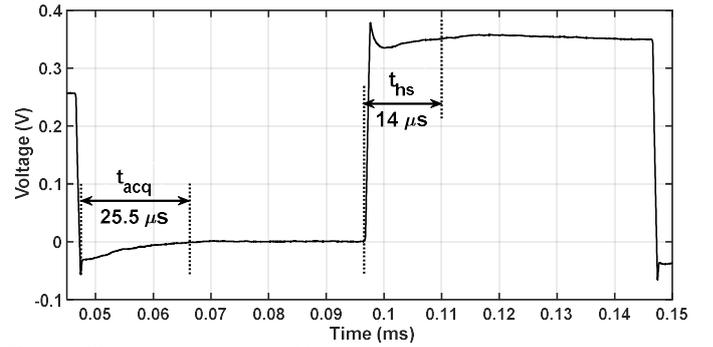


Fig. 16. Measured acquisition and hold mode settling times.

$$FOM = f_s \frac{ENOB}{P} \quad (21)$$

Notice from Table II how the performance of the S/H is competitive with other designs, confirming the usability of the OTA in low power SC applications. Note the trade-off between P , f_s and ENOB, as reflected in (21). The super class AB operation of the proposed OTA mitigates the degradation of the f_s and ENOB due to the ultra-low power consumption, avoiding the limitation of t_{acq} and t_{hs} , which improves the FoM. Although references [26]-[29] exhibit a higher FOM, it is worth mentioning that the power consumptions in [26]-[28] are in the order of mW, so they are not amenable for e.g. portable applications with small-size batteries and ultra-low power constraints. An outstanding FoM for very low power is reported in [29], but for a current-mode S/H, which requires including highly-linear input V-I and output I-V conversion blocks in voltage-mode systems. These blocks may complicate the design and increase power consumption. Hence, a direct comparison between the proposed solution and [29] is difficult. Note that despite its simplicity, the proposed S/H exhibits the second largest FoM for the fabricated circuits in Table II, and the largest one for the fabricated micropower S/H circuits.

VI. CONCLUSIONS

A power-efficient high drive super class AB OTA and its application to a fully-differential S/H have been presented. A novel non-linear differential current mirror based on two nested feedback loops (negative feedback for common-mode signals and positive feedback for differential signals) is employed at the active load of the adaptively biased differential pair. Operation in weak inversion allows optimal g_m/I_D operation, further improving gain and reducing power consumption. The OTA employed in the S/H includes a novel dynamically biased FVF suitable for SC applications, which allows a widely and accurately programmable FVF input range. Due to the low quiescent currents and high driving capability achieved, the OTA exhibits the highest FOM_L reported to date, demonstrating its usability in SC applications requiring high slew rate, low settling time and improved settling accuracy under low power constraints.

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