Editorial
Special Issue for 50th Birthday of Memristor Theory and Application of Neuromorphic Computing Based on Memristor—Part I

IN 1971, Dr. Leon Chua, known as the father of nonlinear circuits and cellular neural networks, postulated the existence of memristor, a portmanteau of memory resistor, in his seminal paper: Memristor-the missing circuit element published in IEEE TRANSACTIONS ON CIRCUIT THEORY, the predecessor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. Thirty-seven years after he predicted its existence, in the May 1 (2008) issue of the journal *Nature*, a team at HP Labs led by the scientist R. S. Williams proved that the memristor was real by formulating a physics-based model of a memristor and build nanoscale devices in their lab that demonstrate all of the necessary operating characteristics. Since then, the extensive interest of academic and industrial circles on neuromorphic computing based on memristor has been skyrocketed. Moreover, the unusual electrical properties of circuits and systems based on memristor can mimic the functionalities of the human brain, and can provide an in-depth understanding of key design implications of memristor-based memories, such as learning and anticipating. As a result, neuromorphic computing based on memristor is expected to bring significant breakthrough in dynamic neuromorphic memories, memristor-based resistive RAM, nonvolatile memory technology, and so on.

This Special Issue provides a platform to disseminate original research in the fields of resistive random access memory, neural computing, hybrid CMOS/memristor circuits, and memristor dynamics. This was an excellent opportunity for researchers to share their findings with the scientific community. All manuscripts submitted to this Special Issue have been reviewed through the peer-reviewing process. Some original research articles have been accepted for publication. A brief summary of each published article in this Special Issue by providing a short editorial note has also been presented as follows.

In [A1], Jin *et al.* analyzed some unknown neuromorphic dynamics of the Chua corsage memristor (CCM). By applying the theories of local activity and edge of chaos, this pioneering paper exploits the unique highly-nonlinear dynamics (for instance, chaos and Hopf bifurcation) in CCM-based second-order and third-order circuits. This seminal work provides a theoretical foundation for further studying memristor dynamics in brain-like learning and AI applications.

In [A2], Puglisi *et al.* proposed a new synthesis method for implication logic circuits based on memristors. They developed a generalized rule to derive the sequence of operations needed to realize any logic function written in the classical AND–OR form. The proposed method can allow a fair comparison between the performance of CMOS and implication logic implementations of the same logic function under the same degree of optimization, and be shown to outperform existing approaches.

In [A3], Liu *et al.* analyze the different effects of bridge defects and aggregate their faulty behavior into new fault models, undefined coupling fault, and dynamic undefined coupling fault. In addition, an enhanced March algorithm is designed to detect all the modeled faults.

In [A4], Aljafar and Acken proposed a novel 3-D memristive crossbar architecture with a specific focus on the way of connecting the crossbar arrays to the CMOS layer. The proposed architecture enabled parallel and pipeline computations where data can move or be processed in planes perpendicular to the stacked crossbar arrays.

In [A5], James and Chua presented a technique to improve the resolution by building a super-resolution memristor crossbar with nodes having multiple memristors to generate r-simplicial sequence of unique conductance values. The proposed super-resolution approach will, in particular, be useful in building analog neural network layers.

In [A6], Moitra and Panda showed that adversarial inputs can have a higher sum of column currents compared to clean inputs. They implemented the DetectX module using 32-nm CMOS circuits and integrate it with a Neurosim-like analog crossbar architecture. Moreover, they performed hardware evaluation of the Neurosim+DetectX system on the Neurosim platform using datasets-CIFAR10 (VGG8), CIFAR100 (VGG16), and Tiny-Imagenet (ResNet18).

In [A7], Fu *et al.* proposed a general method of using a memristor-capacitor circuit to solve inhomogeneous linear ordinary differential equations (ODEs) and systems of ODEs of any order in initial value problems. In addition, the proposed method can be used to quickly solve the object motion state in the spring mass damping system in actual engineering.

In [A8], Wu *et al.* considered the positivity and stability of a class of Cohen-Grossberg memristive neural networks (CG-MNNs). The existence and uniqueness of the solution of CG-MNNs with unbounded time-varying delays are proved at the beginning, which provides vital guidance for relevant

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system analysis. Not neglecting the memristor nonlinearity, they derived some sufficient and necessary conditions for the positivity and stability of CG-MNNs with unbounded time-varying delays with the aid of Lyapunov method. These criteria are not so conservative, and, meanwhile, help scholars understand the convergence performance of memristive systems.

In [A9], Wang *et al.* investigate the event-based extended dissipative state estimation problem for memristor-based Markovian neural networks in the presence of hybrid time-varying delays and sensor nonlinearity. To tackle the effect caused by information latching, sudden interference and environmental variation, the Markov jump model is employed to describe the memristor-based neural network. In addition, an event-triggered scheme is introduced to economize the cost of communication.

In [A10], Bao *et al.* focused on a class of discrete memristor (DM) model, a type of memristor that has not been paid too much attention. They established a general DM model, gave its four representations, and exhibited, respectively, their pinched hysteresis loops. On top of that, they generated four 2-D DM maps and explored their parameter- and initial-relied behaviors using multiple numerical measures. These 2-D DM models can generate hyperchaos with coexisting bi-stable or memristor initial-boosted behavior. To implement these maps, a hardware device is constructed and the analog voltage signals are experimentally acquired. At last, high randomness pseudo-random number generators are successfully designed based on these DM maps.

Finally, we would like to pay a great homage to all the authors for their valuable contributions rendered in this respect and also to the reviewers for their valuable suggestions made in the evaluation of the articles during the reviewing process.

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APPENDIX: RELATED ARTICLES

[A1] P. Jin, G. Wang, Y. Liang, H. H.-C. Iu, and L. O. Chua, "Neuromorphic dynamics of Chua corsage memristor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Oct. 29, 2021, doi: 10.1109/TCSI.2021.3121676.

[A2] F. M. Puglisi, T. Zanotti, and P. Pavan, "Optimized synthesis method for ultra-low power multi-input material implication logic with emerging non-volatile memories," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, May 21, 2021, doi: 10.1109/TCSI.2021.3079986.

[A3] P. Liu, Z. You, J. Wu, B. Liu, Y. Han, and K. Chakrabarty, "Fault modeling and efficient testing of memristor-based memory," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Jun. 27, 2021, doi: 10.1109/TCSI.2021.3098639.

[A4] M. J. Aljafar and J. M. Acken, "A 3-D crossbar architecture for both pipeline and parallel computations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Sep. 3, 2021, doi: 10.1109/TCSI.2021.3108564.

[A5] A. P. James and L. O. Chua, "Analog neural computing with super-resolution memristor crossbars," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, May 21, 2021, doi: 10.1109/TCSI.2021.3079980.

[A6] A. Moitra and P. Panda, "DetectX-adversarial input detection using current signatures in memristive XBar arrays," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Sep. 16, 2021, doi: 10.1109/TCSI.2021.3110487.

[A7] H. Fu, Q. Hong, C. Wang, J. Sun, and Y. Li, "Solving non-homogeneous linear ordinary differential equations using memristor-capacitor circuit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Sep. 20, 2021, doi: 10.1109/TCSI.2021.3111620.

[A8] A. Wu, Y. Chen, S. Zhu, and S. Wen, "Positivity and stability of Cohen–Grossberg-type memristor neural networks with unbounded delays," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Sep. 23, 2021, doi: 10.1109/TCSI.2021.3113050.

[A9] T. Wang, B. Zhang, D. Yuan, and Y. Zhang, "Event-based extended dissipative state estimation for memristor-based Markovian neural networks with hybrid time-varying delays," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, May 14, 2021, doi: 10.1109/TCSI.2021.3077485.

[A10] H. Bao, Z. Hua, H. Li, M. Chen, and B. Bao, "Discrete memristor hyperchaotic maps," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Jun. 4, 2021, doi: 10.1109/TCSI.2021.3082895.