Editorial
Special Issue for 50th Birthday of Memristor Theory and Application of Neuromorphic Computing Based on Memristor - Part II

IN 1971, Dr. Leon Chua, known as the father of nonlinear circuits and cellular neural networks, postulated the existence of memristor, a portmanteau of memory resistor, in his seminal paper: "Memristor—The missing circuit element" published in IEEE TRANSACTIONS ON CIRCUIT THEORY, the predecessor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS. In 2008, Hewlett-Packard researchers made nanomemristor devices for the first time, setting off an upsurge of memristor research. The emergence of nanomemristor devices is expected to realize nonvolatile RAM. Moreover, the integration, power consumption, and read–write speed of the RAM based on memristor are superior to those of traditional RAMs. The hardware network based on memristor synaptic devices is an important development direction of neuromorphic computing. It is a powerful technical candidate to break through the traditional von Neumann computing architecture in the post-Moore era, which will provide a feasible scheme about a technological breakthrough for surpassing Moore's law.

This Special Issue provides a platform to disseminate original research in the fields of compact memristive models, in-memory computation, memristor synaptic circuits, and memristor dynamics. This was an excellent opportunity for researchers to share their findings with the scientific community. All manuscripts submitted to this Special Issue have been reviewed through the peer-reviewing process. Some original research articles have been accepted for publication. A brief summary of each published article in this Special Issue by providing a short editorial note has also been presented as follows.

In [A1], Kang *et al.* present and experimentally validate two minimal compact memristive models for spiking neuronal signal generation using commercially available low-cost components. This work will help to promote more experimental demonstrations of memristive circuits that do not rely on prohibitively expensive fabrication processes.

In [A2], for hardware implementation, the performance of the memristive neural network is always affected by quantization error, writing error, and conductance drift, which seriously hinders its applications in practice. Zhou *et al.* propose a novel weight optimization scheme combining quantization and Bayesian inference to alleviate this problem. The experiments on a Multilayer Perceptron and LeNet demonstrate that the proposed weight optimization scheme can significantly enhance the robustness of memristive neural networks.

In [A3], Maheshwari *et al.* demonstrate the behavior of a fabricated custom memristor model and its integration into the Cadence Electronic Design Automation (EDA) tools for verification. Also, the designers can integrate this memristor model with CMOS technology to build hybrid CMOS/memristor systems.

In [A4], Maheshwari *et al.* demonstrate with examples the design flow for memristor-based electronics, after the custom memristor model already being integrated and validated into the chosen computer-aided design tool to perform layout-versus-schematic and post-layout checks including the memristive device.

In [A5], Mannocci *et al.* present a fully analog, universal primitive capable of executing linear algebra operations such as regression, generalized least-square minimization, and linear system solution with and without preconditioning. Moreover, Mannocci *et al.* also discuss the impact of additional nonidealities such as interconnect parasitic resistance and capacitance, operational amplifier offset voltage, and output resistance.

In [A6], Wang *et al.* investigate the transfer function of an in-memory analog circuit based on crosspoint memristor arrays. By optimizing these parameters synergistically, the dominant pole shifts to higher frequencies and the computing speed is consequently optimized. The obtained results provide a guideline for design and optimization of in-memory machine learning accelerators with analog memristor arrays.

In [A7], Zoppo *et al.* present circuit models for open-loop and feedback configurations, and perform detailed analyses that include memristor programming errors, thermal noise sources, and element nonidealities in realistic circuit simulations to determine both the precision and accuracy of the analog solutions. In addition, Zoppo *et al.* compare the derived analog results to those from digital computations and find a significant power efficiency advantage for the crossbar approach for similar precision results.

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In [A8], Cheng *et al.* analyze the state estimation for switched memristive neural networks with nonhomogeneous sojourn probabilities. By applying the dynamic event-triggered state estimation, some sufficient conditions to ensure the stochastic stability of the augmented switched memristive neural networks are exploited. The superiority and effectiveness of the proposed method are also demonstrated.

In [A9], Jiang *et al.* analyze two memristors with abundant dynamics including attractor merging and quasi-periodic oscillation. The proposed oscillator can realize direct offset boosting, which is rare in other memristive hyperchaotic systems.

In [A10], Zhang *et al.* develop a memristor coupling method to establish a new memristive Sprott A system (MSAS) by coupling a flux-controlled memristor with multi-piecewise linear memductance into the Sprott A system. The proposed MSAS can generate different numbers of multi-one-scroll hidden attractors and multi-double-scroll/wing hidden attractors according to the coupling position of the memristor.

In [A11], Wang *et al.* propose a unified framework to address the synchronization problem of memristor chaotic systems via the sliding-mode control method. Based on the Lyapunov stability and sliding-mode control theories, the finite-/fixed-time synchronization results are obtained.

In [A12], Yi *et al.* present a computationally light, memristor-based, highly accurate static compact model for the silicon-oxide-nitride-oxidesilicon (SONOS) synapses. Also, Yi *et al.* show how to exploit analog errors in programming resistances and current leakage, and the continuous tunability of the SONOS synapses to enable transient chaotic group dynamics.

In [A13], Messaris *et al.* propose an accurate, particularly simplified version of a recently introduced physical model suitable for large scale circuit simulations, and then conduct a small-signal circuit-theoretic derivation of the impedance and associated small-signal equivalent circuit elements to analyze device stability and frequency response. Moreover, Messaris *et al.* have also shown how the connection of a capacitor in parallel to the investigated memristor affects the stability properties of certain stationary states.

Finally, we would like to pay a great homage to all the authors for their valuable contributions rendered in this respect and also to the reviewers for their valuable suggestions made in the evaluation of the articles during the review process.

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APPENDIX: RELATED ARTICLES

[A1] S. M. Kang *et al.*, "How to build a memristive integrate-and-fire model for spiking neuronal signal generation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[A2] Y. Zhou, X. F. Hu, L. D. Wang, G. D. Zhou, and S. K. Duan, "QuantBayes: Weight optimization for memristive neural networks via quantization-aware Bayesian inference," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Oct. 29, 2021, doi: 10.1109/TCSI.2021.3115787.

[A3] S. Maheshwari *et al.*, "Design flow for hybrid CMOS/memristor systems—Part I: Modelling and verification steps," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[A4] S. Maheshwari *et al.*, "Design flow for hybrid CMOS/memristor systems—Part II: Circuit schematics and layout," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[A5] P. Mannocci, G. Pedretti, E. Giannone, E. Melacarne, Z. Sun, and D. Ielmini, "A universal, analogue, in-memory computing primitive for linear algebra using memristors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[A6] S. Q. Wang *et al.*, "Optimization schemes for in-memory linear regression circuit with memristor arrays," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[A7] G. Zoppo, A. Korkmaz, F. Marrone, S. Palermo, F. Corinto, and R. S. Williams, "Analog solutions of discrete Markov chains via memristor crossbars," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[A8] J. Cheng, L. Liang, J. H. Park, H. Yan, and K. Li, "A dynamic event-triggered approach to state estimation for switched memristive neural networks with nonhomogeneous sojourn probabilities," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Oct. 11, 2021, doi: 10.1109/TCSI.2021.3117694.

[A9] Y. C. Jiang, C. B. Li, C. Zhang, Y. B. Zhao, and H. Y. Zang, "A double-memristor hyperchaotic oscillator with complete amplitude control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[A10] S. Zhang, C. Li, J. Zheng, X. Wang, Z. Zeng, and G. Chen, "Generating any number of diversified hidden attractors via memristor coupling," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Oct. 5, 2021, doi: 10.1109/TCSI.2021.3115662.

[A11] L. M. Wang, S. Jiang, M.-F. Ge, C. Hu, and J. H. Hu, "Finite-/fixed-time synchronization of memristor chaotic systems and image encryption application," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[A12] S.-I. Yi, S. Kumar, and R. S. Williams, "Improved Hopfield network optimization using manufacturable three-terminal electronic synapses," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Oct. 27, 2021, doi: 10.1109/TCSI.2021.3119648.

[A13] I. Messaris *et al.*, "NbO_2-Mott memristor: A circuit-theoretic investigation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, 2021.