Flicker Phase-Noise Reduction Using Gate–Drain Phase Shift in Transformer-Based Oscillators

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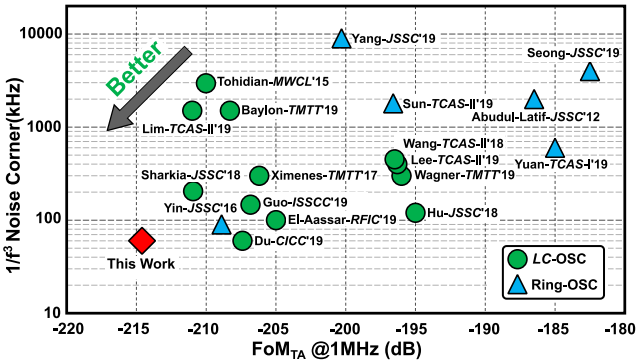
***Abstract*— This article presents a wide-band suppression technique of flicker phase noise (PN) by means of a gate–drain phase shift in a transformer-based complementary oscillator. We identify that after naturally canceling its second-harmonic voltage by the complementary operation itself, third-harmonic current entering the capacitive path is now the main cause of asymmetry in the rising and falling edges, leading to the $1/f$ noise upconversion. A complete $1/f^3$ PN analysis for the transformer-based complementary oscillator is discussed. By tuning gate–drain capacitance ratio, a specific phase-shift *range* is introduced at the gate and drain nodes of the cross-coupled pair to mitigate the detrimental effects of ill-behaved third-harmonic voltage, thus lowering the flicker PN. To further reduce the area and improve the PN in the thermal region, we introduce a new triple-8-shaped transformer. Fabricated in 22-nm FDSOI, the prototype occupies a compact area of 0.01 mm^2 and achieves $1/f^3$ PN corner of 70 kHz, PN of −110 dBc/Hz at 1 MHz offset, figure-of-merit (FoM) of −182 dB at 9 GHz, and 39% tuning range (TR). It results in the best FoM with normalized TR and area (FoM$_{TA}$) of −214 dB at 1 MHz offset.**

***Index Terms*— Transformer-based oscillator, gate–drain phase shift, passive gain, complementary oscillator, flicker noise upconversion, electromagnetic interference, compact area, FDSOI.**

I. Introduction

With the CMOS devices scaling down, their worsening $1/f$ noise [1], [2] leads to the increase of flicker phase noise (PN) in oscillators. This has become a serious problem, attracting extensive research [3]–[14]. Hajimiri and Lee [3] first explained the $1/f$ noise upconversion mechanisms using an impulse sensitivity function (ISF), which suggests that a symmetric oscillation waveform could suppress any $1/f$ noise from upconversion. The original ISF theory works well in explaining flicker PN in ring oscillators [4], [15], [16], but does not clearly explain the origins of the asymmetric waveform in LC-tank oscillators and their flicker PN mechanisms.



*FoM$_{TA}$ = PN - 20log$_{10}$(f_0/Δf) + 10log$_{10}$(P_{DC}/1mW) - 20log$_{10}$(TR/10) + 10log$_{10}$(Area/1mm^2)

Fig. 1. Survey of $1/f^3$ PN corner versus FoM$_{TA}$ (emphasizing tuning range and area) in LC-tank and ring oscillators.

Bonfanti *et al.* [7] and Pepe *et al.* [8] claimed that the $1/f^3$ PN in LC-tank oscillators is caused by the third-harmonic current (i.e., I_{H3}) entering the capacitive path of LC-tank, while Shahmohammadi *et al.* [9] demonstrated that it is the second-harmonic current (i.e., I_{H2}), rather than I_{H3}, entering the non-resistive path, causing waveform asymmetries, which ultimately leads to the flicker PN. Recently, these two pioneering but obviously conflicting explanations were unified in [12] concluding that both ill-behaved second- and third-harmonic voltages (i.e., V_{H2} and V_{H3}) result in the flicker noise upconversion, but V_{H2} dominates over V_{H3} in nMOS-only oscillators, while in complementary oscillators, V_{H3} is an order-of-magnitude larger than V_{H2}. Compared with its nMOS-only counterpart, the complementary oscillator is more favorable for applications requiring low-power consumption, limited swing (avoiding thick-oxide devices), elimination of additional biasing, and supporting standard supply voltages [14]. However, a detailed quantitative analysis of a common-mode (CM) return path and flicker noise upconversion in a conventional complementary oscillator is still missing.

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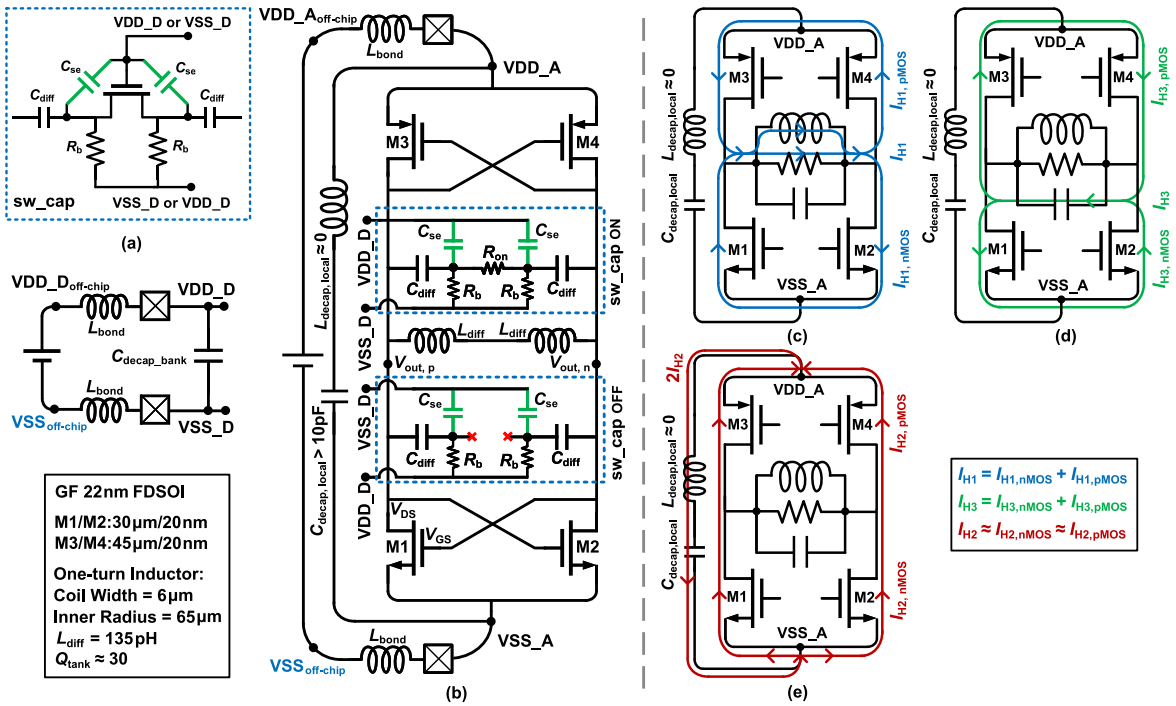


Fig. 2. (a) Conventional sw-cap tuning unit. (b) Model of a conventional 11 GHz LC-tank complementary oscillator. (c) DM current I_{H1} return path. (d) DM current I_{H3} return path. (e) CM current I_{H2} return path.

Several flicker PN reduction mechanisms have been identified [12]: 1) second-harmonic resonance [9], [10], [17]–[20]; 2) narrowing of the conduction angle (i.e., class-C) [11], [21]–[25]; 3) gate–drain phase shift based on an RC delay [8], [26]. However, the second-harmonic resonance is a narrow-band suppression technique, the narrowing of a conduction angle needs a careful consideration of start-up, and the gate–drain phase shift based on an RC delay suffers from process, voltage, and temperature (PVT) variations. Thus, a new flicker PN suppression technique that is wide-band and PVT-robust would be highly sought, especially for supporting 5G/6G communications or other emerging applications [27]–[37].

Concurrently, saving the silicon area has always been desired by IC designers. This is especially true for LC-tank oscillators since the passive devices cannot scale down with the technology advancements [31], [38]–[42]. Although some researchers put active devices underneath the inductive structures at the cost of quality (Q)-factor degradation [31], [41], [42], customarily, a sufficient separation between the inductive devices and other sensitive blocks should be kept to mitigate the electromagnetic interference (EMI). An 8-shaped inductor is a favorable solution to relieve the EMI, but at the cost of a larger area and the Q-factor degradation [43]. In [38] and [40], an ultra-compact 8-shaped transformer-based oscillator was proposed with the switched-capacitor (sw-cap) banks placed in the EMI-free regions to save the area, but the long and ill-defined differential-mode (DM) return path of the transformer significantly worsens its Q-factor. On the other hand, ring oscillators benefit from the CMOS technology scaling, occupying a compact area with a wide TR, and are not susceptible to magnetic pulling. However, both their thermal and flicker PN are much worse than in the LC oscillators, and they are highly susceptible to the supply noise (i.e., high supply pushing).

In this article, we propose a complementary oscillator using a triple-8-shaped transformer, simultaneously featuring a compact area of 0.01 mm^2, wide tuning range (TR) of 39%, $1/f^3$ PN corner of 70 kHz, and electromagnetic compatibility, combining both benefits of LC-tank-based and inverter-ring-based oscillators (see the survey in Fig. 1) [14]. The rest of the paper is organized as follows. Section II discusses in detail the CM return path in a conventional complementary LC oscillator and analyzes quantitatively its flicker noise upconversion mechanism.

Section III presents a complete theory of the transformer's gain and phase shift. Section IV discloses the proposed transformer-based complementary oscillator design, fully clarifying the flicker noise upconversion mechanism in a complementary class-F operation, and reveals how the gate–drain phase shift can suppress it. Experimental results are shown in Section V.

II. Flicker Noise Upconversion and CM Return Path in Complementary Oscillators

For the purpose of fully clarifying the mechanism of flicker noise upconversion in complementary oscillators, a conventional 11 GHz complementary class-B oscillator was designed in 22-nm FDSOI CMOS, as shown in Fig. 2(b). It comprises the complementary cross-coupled switching pairs (M1-M2 & M3-M4) providing transconductance G_m, main inductor L_{diff},

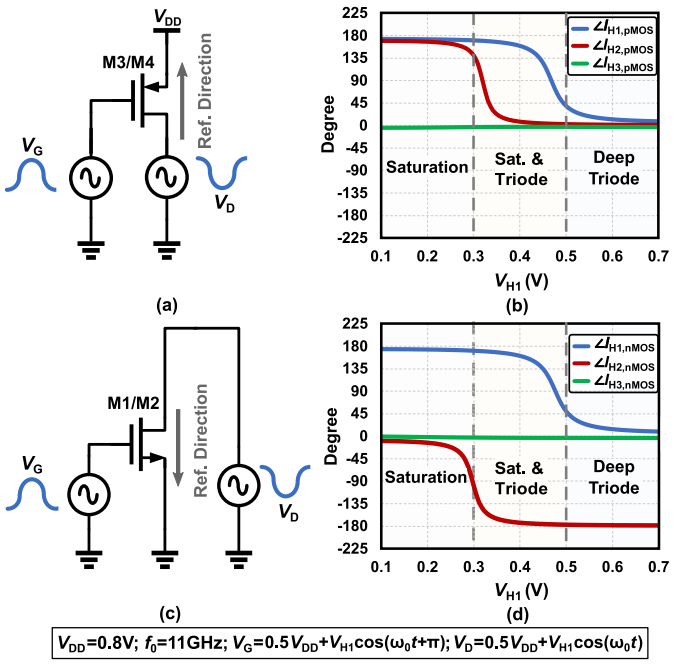


Fig. 3. Effect of oscillating amplitude on phase shift of various harmonic currents in nMOS and pMOS transistors mimicking M1 (or M2) and M3 (or M4) in Fig. 2(b). (a)(c) Simulation test-benches for pMOS and nPMOS transistor, respectively. (b)(d) Simulated phase shifts for pMOS and nPMOS transistor, respectively, for $V_{DD} = 0.8$V (phase degrees are calculated from cosines).

and switched-capacitor (sw-cap) banks [see Fig. 2(a)], modeled by C_{diff} and the parasitic single-ended capacitance C_{se} (shown in both ON and OFF modes). The C_{decap}, L_{decap}, and L_{bond} components model the decoupling capacitor with its parasitic inductance, and bonding-wire inductance, respectively. Two off-chip supplies are used: VDD_$A_{off\text{-}chip}$, VDD_$D_{off\text{-}chip}$, sharing the global ground $VSS_{off\text{-}chip}$. The "analog" power domain (VDD_A/VSS_A) is for the G_m transistors, while the "digital" power domain (VDD_D/VSS_D) is for the sw-cap banks. The separation of two power domains intends to avoid unwanted coupling from the sw-cap banks to the oscillator's core when incorporating this oscillator in a PLL. It could further improve thermal PN by reducing parasitic CM capacitance of sw-cap banks seen by an nMOS-only oscillator's CM path [10].

A. CM Return Path in Complementary Oscillators

Since the non-resistive terminations of CM currents (e.g., I_{H2}) are the main contributor to the flicker noise upconversion in nMOS-only class-B oscillators [10], [44], it would be interesting to study the CM return path in its complementary counterparts by figuring out the relationship between the CM currents generated by the pMOS and nMOS coupled-pairs.

A test-bench [see Fig. 3(a) and (c)] is set up where the pMOS and nMOS transistors [modeling M3 & M1 in Fig. 2(b)] are given similar operating conditions as in Fig. 2(b). For example, assuming $V_D \approx 0.5V_{DD} + V_{H1}\cos(\omega_0 t)$ and $V_G \approx 0.5V_{DD} + V_{H1}\cos(\omega_0 t + \pi)$, Fig. 3(b) and (d) reveal the phase of each harmonic current at the drain nodes of pMOS and nMOS (i.e., $\angle I_{H1-3,pMOS}$ and $\angle I_{H1-3,nMOS}$), respectively. Due to the oscillator's complementary configuration in Fig. 2, V_{H1} is saturated at around $0.5V_{DD}$ (i.e., ≈ 0.4V), resulting in a rail-to-rail output swing for the single-ended output of $V_{out,p}$ or $V_{out,n}$. As shown in Fig. 3(b) and (d), when $V_{H1} = 0.4$ V, both $I_{H1,pMOS}$ and $I_{H1,nMOS}$ in the pMOS and nMOS coupled-pairs are out-of phase of V_{DS}, demonstrating that the coupled-pairs will behave like "negative" G_m in the oscillator. Interestingly, the phase $\angle I_{H2,pMOS}$ is around 0° (see Fig. 3(b)), while phase $\angle I_{H2,nMOS}$ is −180° (see Fig. 3(d)), when $V_{H1} = 0.4$V. With the consideration of their own opposite reference directions, their CM current will be ultimately in-phase, as shown in Fig. 2(e). In other words, the CM current generated by the nMOS cross-coupled pair will be almost entirely absorbed by the pMOS cross-coupled pair with proper sizing of the transistor width ratio W_{pMOS}/W_{nMOS}.

Furthermore, the complementary oscillator provides a well-defined CM return path due to the short physical distance between the local supplies of VDD_A and VSS_A, resulting in the parasitic inductance (i.e., L_{decap}) of decoupling capacitor (i.e., C_{decap}) close to zero. Considering that C_{decap} can be large and also thanks to the low impedance of $1/G_m$ of M1–M4, the CM voltage (e.g., V_{H2}) is an order-of-magnitude smaller than in an nMOS-only oscillator. Thus, the ill-behaved V_{H2} is no longer the main contributor to the flicker noise upconversion, while the I_{H3} entering the capacitive path[1] (see Fig. 2(d)), generating V_{H3}, now starts playing a critical role.

B. Flicker Noise Upconversion and Numerical Verification

To quantitatively study how V_{H3} affects the flicker noise upconversion in the complementary oscillator of Fig. 2, we increase the width W_{nMOS} from 20 μm to 100 μm, while properly sizing W_{pMOS}/W_{nMOS} to fully suppress V_{H2} and reducing the power supply level [see Fig. 4(a)] to maintain the same power consumption. As shown in Fig. 4(b), the V_{H3}/V_{H1} ratio increases from 4% to 13%, but V_{H2}/V_{H1} remains much lower than 1% and V_{H1} keeps relatively constant [around $V_{DD}/2 = 0.4$ V, see subfigure (a)]. The waveform shaping of V_{DS} caused by I_{H3} entering the capacitive nature of the DM tank can be modeled by [12] and [13]

$$V_{DS} \approx V_{H0} + V_{H1}\cos(\omega_0 t) + V_{H3}\cos(3\omega_0 t + \frac{\pi}{2}) \qquad (1)$$

which models V_{DS} at the representative point: $W_{nMOS} = 100\,\mu$m [see Fig. 4(d)]. Obviously, the strong V_{H3} will cause steeper falling edges and less steep rising edge, introducing waveform asymmetries. The actual simulated V_{GS} and V_{DS} of M1 in Fig. 4(e) (including all harmonics) for the point confirm the observation.

Fig. 4(c) shows that PN at 10 kHz offset gets worsened significantly with the increase in V_{H3}/V_{H1}. Thus, the claim in [9] and [45] that the capacitive terminations of I_{H3} do

[1] Interestingly, I_{H1} will partially enter the inductive path (see Fig. 2(c)), generating a little positive imaginary energy to balance the negative imaginary energy due to I_{H3} entering capacitive path (i.e., "Law of Conservation of Energy").

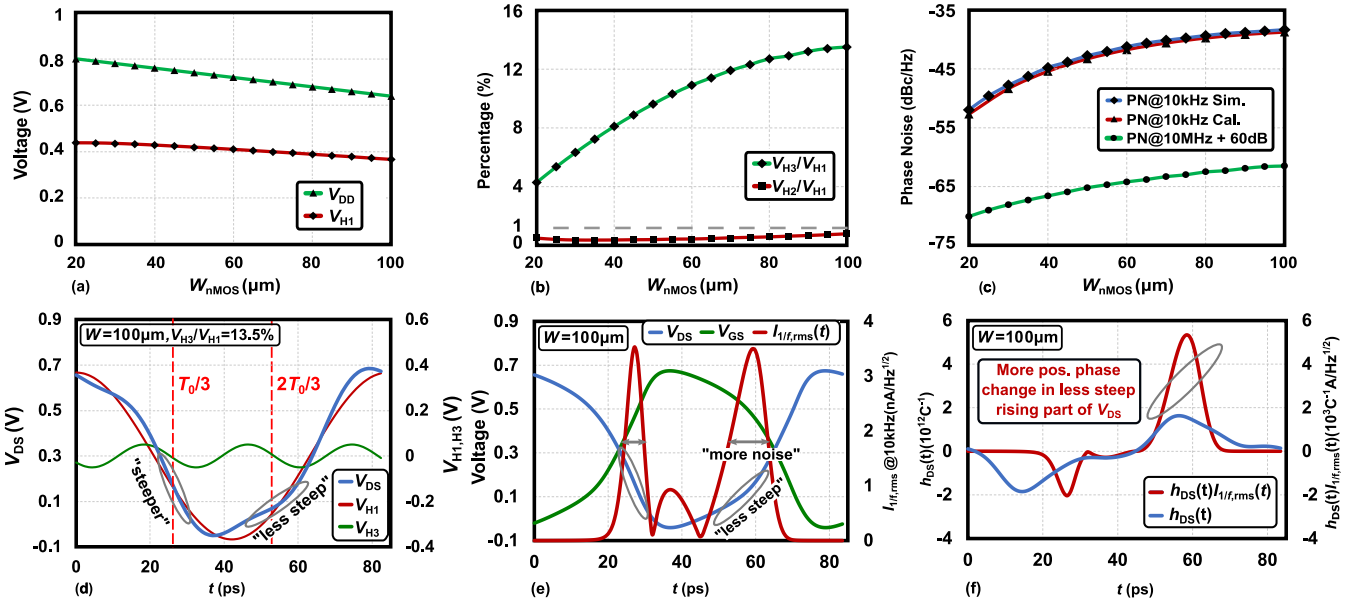


Fig. 4. (a) Simulated V_{H1} and corresponding V_{DD} that keeps the power consumption constant, (b) simulated harmonic contents at the drain nodes, and (c) calculated and simulated PN at 10 kHz offset with increasing W_{nMOS} (Conditions: for each W_{nMOS}, W_{pMOS} is sized properly to suppress V_{H2}). (d) Characterization of V_{DS} using only V_{H1} and V_{H3} [see (1)]. (e) Waveforms of V_{GS}, V_{DS} (including all harmonics) and the corresponding rms value of flicker current noise $I_{1/f,\mathrm{rms}}(t)$ at a 10 kHz offset. (f) Non-normalized ISF h_{DS} and $h_{DS} \cdot I_{1/f,\mathrm{rms}}$.

not contribute to the flicker noise upconversion is clearly not applicable to the complementary oscillator. To quantitatively study the flicker noise upconversion, we employ the theory framework in [10]–[13], where the flicker PN could be calculated by

$$\mathcal{L}_{1/f^3}(\Delta\omega) = \left(\frac{1}{2} \cdot \frac{\sqrt{2}}{\Delta\omega T_0} \int_0^{T_0} h_{\mathrm{DS}}(t) \cdot I_{1/f,\mathrm{rms}}(t) dt\right)^2 \quad (2)$$

where $I_{1/f,\mathrm{rms}}(t)$ is the periodically modulated rms value of flicker noise current at a low offset frequency $\Delta\omega$ (e.g., $2\pi \times 10$ kHz), T_0 $(= 2\pi/\omega_0)$ is the oscillation period, and $h_{\mathrm{DS}}(t)$ is the non-normalized ISF associated with V_{DS} of M1–M4 in Fig. 2(b). As shown in Fig. 4(f), the "less steep" rising part of V_{DS} is more vulnerable to the noise impulse injection than is its falling part. Thus, the flicker noise $I_{1/f,\mathrm{rms}}(t)$ introduces more positive phase change in its rising part (i.e., more positive area of effective non-normalized ISF $h_{\mathrm{DS}}(t) \cdot I_{1/f,\mathrm{rms}}(t)$) than in its falling part, leading to the flicker noise upconversion. The above analysis is numerically verified with simulations covering different transistor widths of W_{nMOS} and W_{pMOS}, as shown in Fig. 4(c), thus proving the effectiveness of the method.

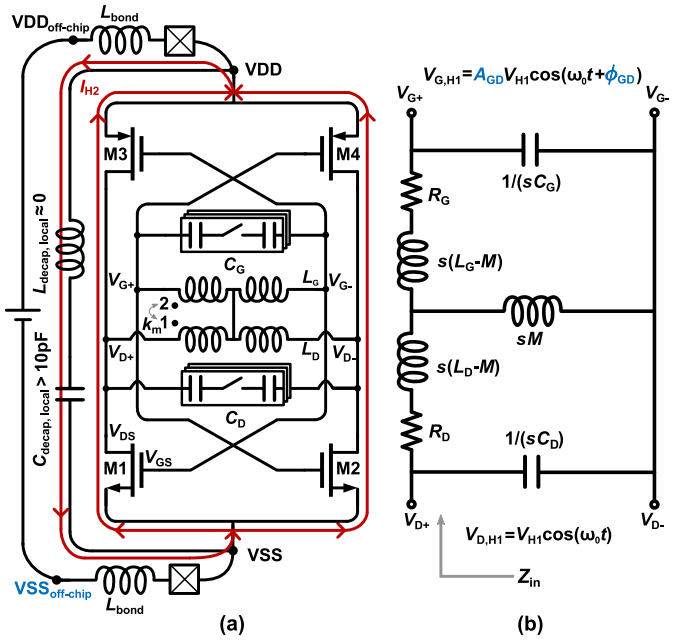


Fig. 5. (a) Schematic of the proposed transformer-based complementary oscillator and its CM return path. (b) T-model of the transformer-based resonator for the DM signal ($M = k_m\sqrt{L_D L_G}$).

III. Gate–Drain Phase Shift in Transformer-Based Complementary Oscillators

To be able to further improve both the thermal and flicker PN in the complementary oscillator, we replace the inductor in the conventional topology of Fig. 2(b) with a transformer (e.g., its turns ratio = 1:2), as shown in Fig. 5(a). A "2-port" topology is employed to avoid two possible oscillation modes (i.e., low-frequency mode at ω_L and high-frequency mode at ω_H) in a transformer-based "1-port" topology [46]–[49]. That is, the drain tank (i.e., L_D, C_D) is connected to the drain-nodes of M1–4, while the gate tank (i.e., L_G, C_G) is cross-connected to their gate-nodes. Both tanks are coupled by a coupling factor k_m. L_{bond}, $C_{decap,local}$, and $L_{decap,local}$ (≈ 0) model the wire-boning inductance, local decoupling capacitor and its parasitic inductance, respectively. To provide the dc operating points for M1–4, the center taps of the primary coil L_D and of the secondary coil L_G are connected. The oscillation frequency ω_0 $(= \omega_L)$ of the proposed topology can be

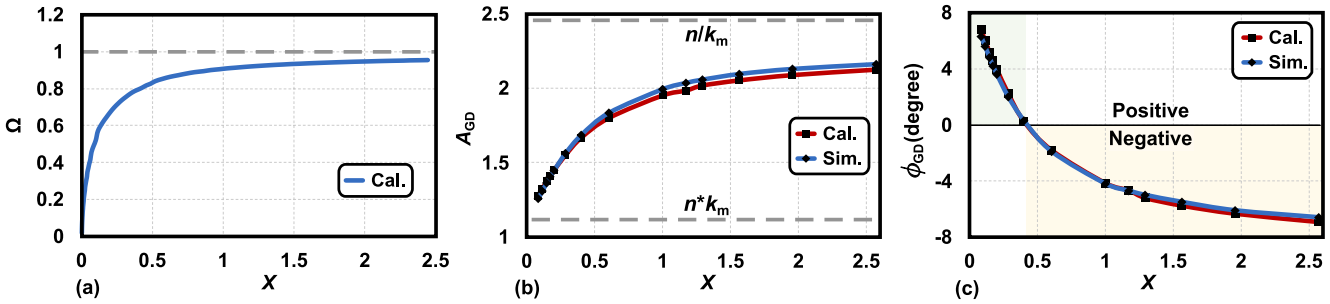


Fig. 6. (a) Calculated normalized oscillation frequency Ω. Calculated and simulated (b) gate–drain passive gain A_{GD} and (c) phase shift ϕ_{GD} of the proposed transformer-based resonator ($n \approx 1.65$, $k_m \approx 0.67$).

expressed as [50], [51]

$$\omega_0 = \sqrt{\frac{1+n^2X-\sqrt{(1+n^2X)^2-4n^2X(1-k_m^2)}}{2(1-k_m^2)}}\omega_G \quad (3)$$

where ω_G ($= 1/\sqrt{L_G C_G}$) represents the resonating frequency of the gate tank (i.e., secondary tank),

$$n = \sqrt{\frac{L_G}{L_D}} \quad (4)$$

is the "effective turns ratio" (different from the "turns ratio"), and

$$X = \frac{C_G}{C_D} \quad (5)$$

is the gate–drain capacitance ratio, which adds a degree-of-freedom and a critical "knob" to affect the oscillator's performance for a given transformer and oscillating frequency range. For example, some specific X will enable a class-F operation [52] for third-harmonic extraction to generate low-PN mmW carrier [10], [53]. Besides, the passive gain A_{GD} and gate–drain phase shift ϕ_{GD} for the fundamental oscillating waveform in the transformer-based resonator [see Fig. 5(b)] also depend on X, which has a large influence on both thermal PN and flicker PN of oscillators.

A. Gate–Drain Passive Gain A_{GD}

Compared with an inductor-based oscillator, the passive gain in a transformer-based oscillator could amplify the effective negative resistance "$-G_m$" by A_{GD} times. Thus, for the same start-up condition, the thermal PN part caused by $4kT\gamma g_m$ noise in a transformer-based oscillator is A_{GD} times smaller than that in an inductor-based oscillator. The relationship between A_{GD} and X is derived based on a T-model [54] of the transformer-based resonator [see Fig. 5(b)], where M ($= k_m\sqrt{L_D L_G}$) is the mutual inductance, $V_{G\text{-}}$ and $V_{D\text{-}}$ are assumed as DM ac ground. Applying Kirchhoff's law, the voltage transfer function of V_G/V_D can be derived as [52]

$$H(s) = \frac{V_G}{V_D} = \frac{Ms}{\alpha_3 s^3+\alpha_2 s^2+\alpha_1 s+\alpha_0} \quad (6)$$

where $\alpha_3 = C_G L_D L_G(1-k_m^2)$, $\alpha_2 = C_G(L_G R_D + L_D R_G)$, $\alpha_1 = L_D + C_G R_D R_G$, and $\alpha_0 = R_D$.

Substituting $s = j\omega_0$ and the quality factors of two coils at ω_0 as $Q_D = \omega_0 L_D/R_D$ and $Q_G = \omega_0 L_G/R_G$ into (6), the frequency response of the transformer-based resonator for the drain fundamental waveform $V_{D,H1}$ can be written as

$$H(j\omega_0) = \frac{nk_m}{(1-k_m^2-\frac{1}{Q_D Q_G})\Omega^2 - 1 + j(\frac{1}{Q_D}-\frac{Q_D+Q_G}{Q_D Q_G}\Omega^2)} \quad (7)$$

where

$$\Omega(X) = \frac{\omega_0}{\omega_G} = \sqrt{\frac{1+n^2X-\sqrt{(1+n^2X)^2-4n^2X(1-k_m^2)}}{2(1-k_m^2)}} \quad (8)$$

is the normalized oscillation frequency on ω_G, and[2]

$$\begin{cases} \lim\limits_{X\to 0}\Omega(X) = 0 \\ \lim\limits_{X\to\infty}\Omega(X) = 1. \end{cases} \quad (9)$$

Fig. 6(a) shows the relationship between Ω and X for the given transformer's n (e.g., $\sqrt{L_G/L_D} \approx 1.7$) and k_m (≈ 0.7). Once X is large enough (e.g., > 2), Ω is close to 1, meaning the oscillation frequency will be dominated by the resonance frequency of the gate tank (i.e., $\omega_0 \approx \omega_G$). Accordingly, the amplitude response A_{GD} for the drain's fundamental waveform $V_{D,H1}$ is given by [see Fig. 5(b)]

$$\begin{aligned} A_{GD}(X) &= |H(j\omega_0)| \\ &= \frac{nk_m}{\sqrt{\left(\left(\frac{1}{Q_D Q_G}+k_m^2-1\right)\Omega^2+1\right)^2+\left(\frac{1}{Q_D}-\frac{Q_D+Q_G}{Q_D Q_G}\Omega^2\right)^2}} \\ &\approx \frac{nk_m}{1-(1-k_m^2)\Omega^2} \end{aligned} \quad (10)$$

where the terms related to $1/Q_D^2$, $1/Q_G^2$, and $1/(Q_D Q_G)$ could be disregarded since they are inversely proportional to the square of the quality factors of the coils. It can be proven that A_{GD} would increase with Ω and X, and

$$\begin{cases} \lim\limits_{X\to 0,\,\Omega\to 0} A_{GD} \approx nk_m \\ \lim\limits_{X\to 1/n^2,\,\Omega\to 1/\sqrt{1+k_m}} A_{GD} \approx n \\ \lim\limits_{X\to\infty,\,\Omega\to 1} A_{GD} \approx \dfrac{n}{k_m}. \end{cases} \quad (11)$$

[2]See Appendix for the proof of $\lim_{X\to\infty}\Omega(X) = 1$.

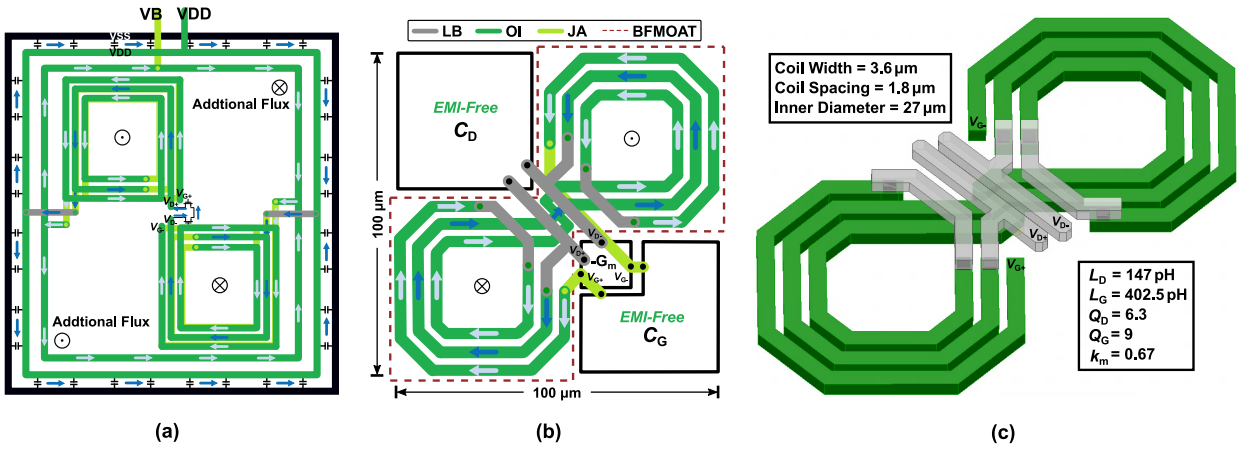


Fig. 7. (a) Transformer layout introduced in [40]. (b) Proposed triple-8-shaped transformer layout and (c) its 3-D illustration with parameters.

Fig. 6(b) visualizes (10) for a given n and k_m of the transformer. Note that when $X > 2$, A_{GD} is almost saturated. The transformer-based oscillator can thus operate in the passive gain saturation region.

B. Gate–Drain Phase Shift ϕ_{GD}

The transformer could also introduce a phase shift ϕ_{GD} between $V_{G,H1}$ and $V_{D,H1}$ [see Fig. 5(b)], which is associated with a potential reduction in the flicker PN in [14]. ϕ_{GD} can be expressed as

$$\begin{aligned}\phi_{GD}(X) &= \angle H(j\omega_0)\\ &= \arctan\left(\frac{\frac{1}{Q_D}-\frac{Q_D+Q_G}{Q_DQ_G}\Omega^2}{\left(\frac{1}{Q_DQ_G}+k_m^2-1\right)\Omega^2+1}\right). \quad (12)\end{aligned}$$

Similarly, we get

$$\begin{cases}\lim\limits_{X\to 0,\,\Omega\to 0}\phi_{GD} = \arctan\left(\dfrac{1}{Q_D}\right) > 0\\ \lim\limits_{X\to X_0,\,\Omega\to\Omega_0}\phi_{GD} = 0\\ \lim\limits_{X\to\infty,\,\Omega\to 1}\phi_{GD} \approx -\arctan\left(\dfrac{1}{k_m^2Q_G}\right) < 0\end{cases} \quad (13)$$

where

$$X_0 = \frac{k_m^2Q_G{}^2+Q_DQ_G}{n^2(Q_D{}^2+Q_DQ_G)} \approx \frac{1}{n^2}\frac{1+k_m^2}{2} \le \frac{1}{n^2} \quad (14)$$

with an assumption of $Q_D \approx Q_G$.

Clearly, the transformer-induced phase shift is mainly caused by its limited quality factors of Q_D and Q_G achievable in CMOS radio-frequency integrated circuits (RFICs). As shown in Fig. 6(c) and (13), either a positive or negative phase shift of ϕ_{GD} can be implemented in the transformer by tuning X. Intuitively, with large capacitance at the gate nodes, the phase of the fundamental waveform is delayed from the primary coil coupling to the secondary coil. In summary, for a given transformer, A_{GD} and ϕ_{GD} can be well-controlled by gate–drain capacitance ratio X (i.e., $= C_G/C_D$) in the resonator, which is independent of the tuned oscillation frequency ω_0. Simulation (based on EMX S-parameter model) and theoretical results reach a good agreement as shown in Fig. 6, demonstrating the efficacy of the above analysis.

IV. Proposed Oscillator With a Compact Triple-8-Shaped Transformer

In this section, we propose an ultra-compact complementary oscillator based on a triple-8 shaped transformer. Its flicker PN is suppressed by inducing a positive phase shift in the transformer.

A. Design of Triple-8 Shaped Transformer With Compact Area

An 8-shaped transformer was proposed in [38] and [40] to substantially reduce the DCO area. However, its actual DM return path, including its V_{DD}, V_B lines, was neglected in the analysis in [40], see Fig. 7(a). The excessively long V_{DD}, V_B lines significantly limit the DM quality factors of both the primary and secondary coils. Furthermore, they may also introduce an additional magnetic flux, as shown in Fig. 7(a).

The proposed 1:2 triple-8-shaped transformer-based oscillator is revealed in Fig. 7(b). 3D view and parameters of the transformer are shown in Fig. 7(c). There are no surrounding V_{DD} and V_B lines, thereby ensuring a well-defined DM return path and high Q for the compact occupied area (i.e., 0.01 mm^2). The proposed transformer is constructed in a coplanar interwound manner with three thick metal layers (called JA, OI, and LB in FDSOI), and a native layer (BFMOAT) is used to increase the high resistivity of the substrate, decreasing the eddy currents and further increasing the Q. Its coil width of 3.6 μm and inner space of 1.8 μm are optimized in a $100 \times 100\,\mu$m^2 area, yielding the primary quality factor $Q_p \approx 9$, the secondary quality factor $Q_s \approx 6.5$, and $k_m \approx 0.7$ for the intended frequency range. Two sw-cap banks are placed on the EMI-suppressed area, where the magnetic fluxes cancel each other due to the property of 8-shaped coils.

To further save the area and provide a defined local CM return path, the required minimum capacitance for the on-chip decoupling capacitors should be considered. For a ring oscillator, a large decoupling capacitance (e.g., $\sim$100 pF) may

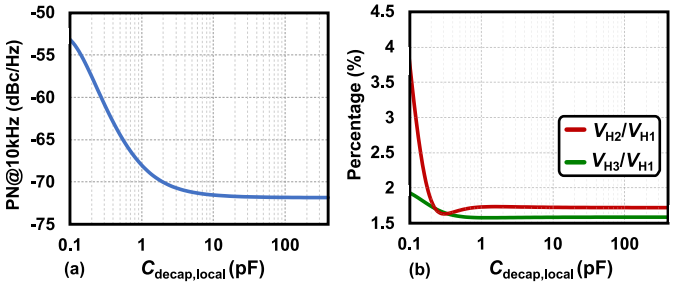


Fig. 8. Simulated (a) PN at 10 kHz and (b) V_{H2}/V_{H1}, V_{H3}/V_{H1} with different local decoupling capacitance $C_{decap,local}$ for $X = 0.2$.

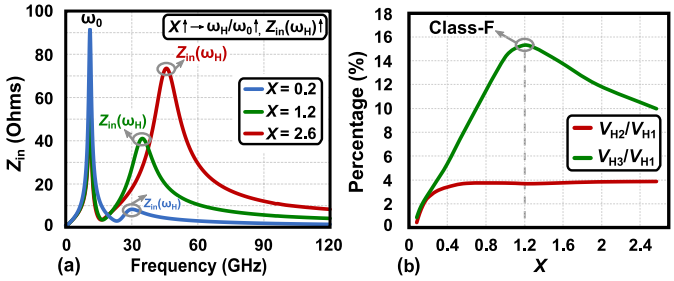


Fig. 9. (a) Simulated input impedance Z_{in} of the transformer-based resonator with different X. (b) Simulated V_{H3}/V_{H1}, V_{H2}/V_{H1} with different X.

be required to prevent the supply noise (especially, low-frequency components) from converting to PN due to the ring oscillator's considerable supply pushing effects (typically, several GHz/V) [15], [55], [56]. However, in transformer-based oscillators, since they naturally feature low supply pushing (typically <100 MHz/V) [52], [57], the on-chip decoupling capacitance is mainly to provide the local CM return path. Fig. 8 suggests that once the local decoupling capacitance $C_{local,decap}$ for the proposed transformer-based complementary oscillator is larger than ~10 pF, it can effectively suppress the second-harmonic voltage V_{H2} (also resulting in lower V_{H3}), thus improving the flicker PN.

B. $1/f^3$ Phase Noise in Complementary Class-F Oscillators

As per conclusions in Section II, the flicker PN in complementary oscillators is mainly caused by the third-harmonic current entering the capacitive path, while V_{H2} is suppressed by the complementary operation itself. Thus, to reduce the flicker PN, we *may* force the third-harmonic current I_{H3} to enter a resistive load, resulting in a complementary class-F topology (i.e., $\omega_H \approx 3\omega_0$). The additional resonance frequency ω_H of the transformer-based resonator as [48]

$$\frac{\omega_H}{\omega_0} = \sqrt{\frac{1+n^2X+\sqrt{(1+n^2X)^2-4n^2X(1-k_m^2)}}{1+n^2X-\sqrt{(1+n^2X)^2-4n^2X(1-k_m^2)}}}. \quad (15)$$

To study how X affects the PN of the proposed oscillator, we sweep X from 0.2 to 1.6 while maintaining the same oscillation frequency ω_0 and power consumption for a fair PN comparison. Fig. 9(a) plots the resonator's input impedance Z_{in} for three values of X while Fig. 9(b) shows the harmonic voltage ratios (i.e., V_{H2}/V_{H1}, V_{H3}/V_{H1}) across X. Both ω_H and $Z_{in}(\omega_H)$ increase with rising X; specifically, when $X \approx 1.2$, the class-F operation is achieved. The simulated thermal PN (e.g., PN at 10 MHz offset) and flicker PN (e.g., PN at 10 kHz offset) across X are plotted in Fig. 10(e).

Interestingly, the exact class-F operation (i.e., $\omega_H = 3\omega_0$) is not necessary to help improve PN, but it will be useful for the third harmonic extraction at mm-wave frequencies [10], [29], [53]. As shown in Fig. 10(e), the PN at 10 MHz offset keeps almost constant from $X = 0.6$ to $X = 1.6$, not significantly improved by enhancing V_{H3} (i.e., $X = 1.2$). This phenomenon can be explained by our analysis in the previous section that the improvement of thermal PN in the transformer-based oscillators depends on the reduction in $4kT\gamma g_m$ noise by the gate–drain passive gain A_{GD} (rather than by class-F itself), which would be saturated when X is large enough. On the other hand, there is a sudden, and rather unexpected, flicker PN degradation in the complementary class-F oscillator, even though its V_{DS} waveform becomes squarish and symmetric [see Fig. 10(a)] due to the class-F operation and the ill-behaved V_{H2} (the main contributor of flicker noise upconversion in nMOS-only class-F oscillators [9], [10]) being minimized by the complementary topology. To understand this special $1/f$ noise upconversion mechanism, we simulate the corresponding $I_{1/f,rms}$ and the effective non-normalized ISF $h_{DS} \cdot I_{1/f,rms}$ when $X = 1.2$ (i.e., class-F operation), as shown in Fig. 10(c) and (d). Due to the negative phase shift ϕ_{GD} of V_{GS} against V_{DS} by the transformer [i.e., $\phi_{GD} = -4°$, see Fig. 6(c) and Fig. 10(a)], the peak of V_{GS} moves a bit closer to the rising edge of V_{DS}, leading to the higher $I_{1/f,rms}$ [see Fig. 10(c)] getting exposed to the rising edge of V_{DS}. Ultimately, it causes more positive area of effective ISF, $h_{DS} \cdot I_{1/f,rms}$, see Fig. 10(d), resulting in the flicker noise upconversion.

C. $1/f^3$ Phase Noise Reduction by the Deliberate ϕ_{GD}

To compensate for the more positive phase change caused by $I_{1/f,rms}$ in the complementary class-B [see Fig. 4(f)] or class-F oscillator [see Fig. 10(d)], we could introduce a positive gate–drain phase shift[3] (i.e., ϕ_{GD}) in the transformer (see Fig. 6(c)). Per (12), with X decreasing, the peak of V_{GS} moves towards the falling edges of V_{DS} [see Fig. 10(b)], increasing the exposure of $I_{1/f,rms}$ to the falling edges of V_{DS} [see Fig. 10(b)], consequently resulting in a null area of effective ISF $h_{DS} \cdot I_{1/f,rms}$ [i.e., no flicker noise upconversion, see Fig. 10(d) and (e)]. It is worth noting that to get a positive drain-to-gate phase shift, some passive gain needs to be sacrificed (see Fig. 6(b) and (c)), which is the reason that PN at 10 MHz offset is worsened in the small X region (e.g. $X < 0.15$). Practically, the proposed complementary oscillator operates in the region of $X < 0.3$, achieving low PN, low flicker PN, and wide TR, simultaneously. Fig. 10(e) also illustrates the numerical verification of PN at 10 kHz with different X. The agreement between the calculations based on (2) and simulations demonstrates the efficacy of the above analysis. Furthermore, Fig. 11 shows the post-layout simulated

[3]Further, we predict that a negative phase shift of V_{GS} against V_{DS} could suppress the $1/f^3$ PN in an oscillator with steeper rising edges of V_{DS} (e.g. I_{H2} entering the inductive termination) [12].

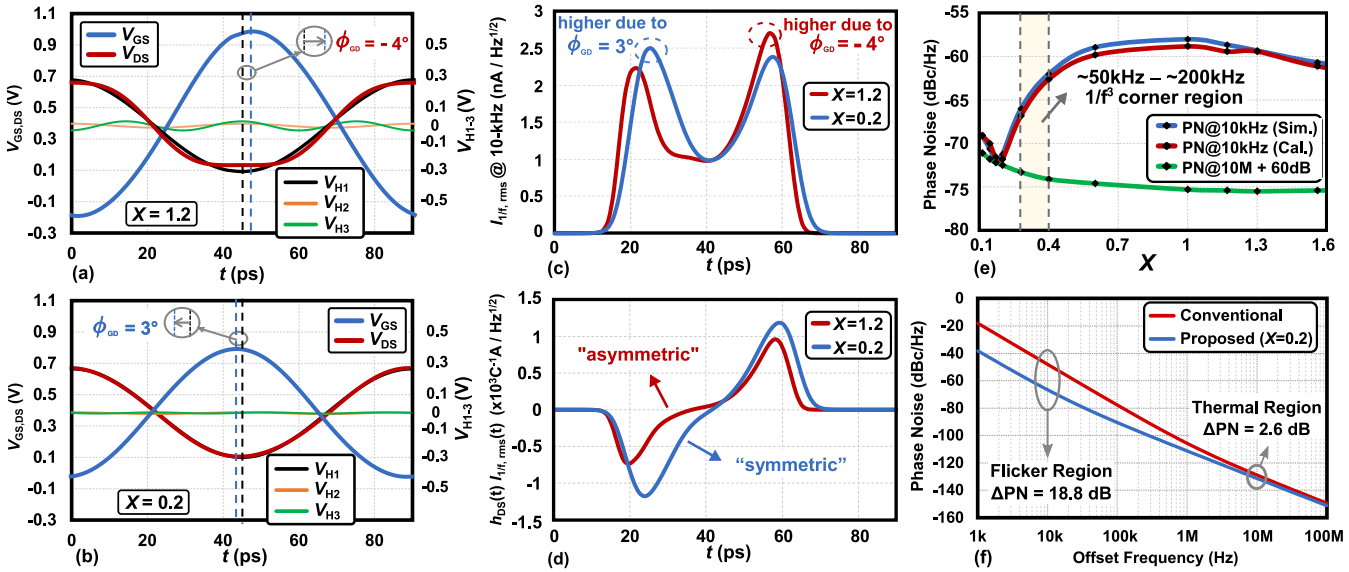
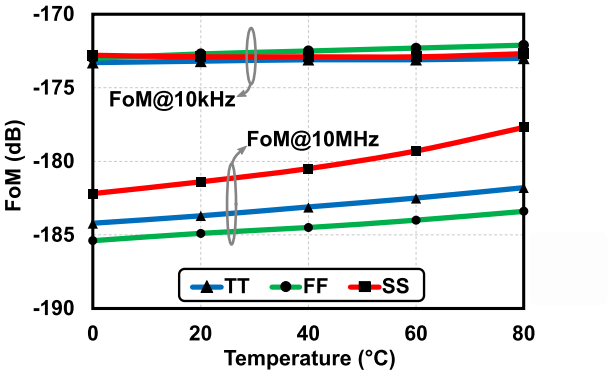


Fig. 10. Simulated full cycle of V_{GS}, V_{DS} of M1/2, and the harmonic contents of V_{DS} with: (a) $X = 1.2$ (i.e., class-F operation) and (b) $X = 0.2$. (c) Simulated rms value of periodically modulated flicker current noise at 10 kHz, $I_{1/f,\mathrm{rms}}(t)$. (d) Effective non-normalized ISF, $h_{DS}(t) \cdot I_{1/f,\mathrm{rms}}(t)$. (e) PN vs. X (keeping the same frequency and power consumption) and its numerical verification. (f) Simulated PN profile comparison between the conventional complementary class-B oscillator and the proposed oscillator.



*FoM = PN - $20\log_{10}(f_0/\Delta f) + 10\log_{10}(P_{DC}/1\mathrm{mW})$; V_{DD} = 1V for SS corner, 0.9V for other corners

Fig. 11. Post-layout simulations of FoM at 10 kHz and FoM at 10 MHz with different process corners and temperature.

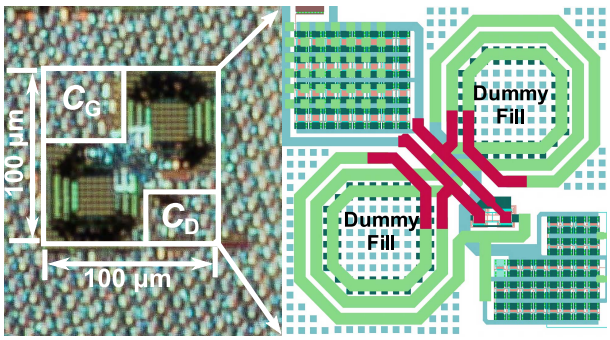


Fig. 12. Chip micrograph and zoomed-in view of the layout.

FoM at 10 kHz and at 10 MHz with different process corners and across temperature. FoM at 10 kHz varies much less than FoM at 10 MHz, demonstrating the robustness of the proposed flicker phase noise suppressing technique against process and temperature variations.

To further demonstrate the benefits of the proposed technique, the simulated PN profile comparison between the proposed transformer-based complementary oscillator and the conventional inductor-based complementary oscillator is shown in Fig. 10(f). The proposed oscillator can achieve 19 dB better PN in the flicker PN region (e.g., PN at 10 kHz), while 2.6 dB improvement in the thermal PN region (e.g., PN at 10 MHz).

V. Experimental Results

The prototype of the proposed oscillator is fabricated in GlobalFoundries 22-nm FDSOI. The chip microphotograph is shown in Fig. 12, occupying a core area of 0.01 mm^2. Its PN is evaluated using an R&S 2-Hz–85-GHz FSW Signal and Spectrum Analyzer. The 5-bit coarse tuning bank at the drain nodes of the oscillator, covering the measured TR from 9 to 13.34 GHz (39%), while the fine-tuning bank locates at the gate nodes. When operating at 9 GHz [see Fig. 13(a)], the measured PN is −110.2 dBc/Hz at 1 MHz offset, with an excellent $1/f^3$ PN corner of 70 kHz, while consuming only 6 mW. At the highest frequency of 13.34 GHz, as shown in Fig. 13(b), it achieves −107.1 dBc/Hz at 1 MHz offset, with 250 kHz flicker PN corner, while consuming 5mW, consequently resulting in FoM of −182.6 dB at 1MHz offset. Compared with [40], the proposed oscillator achieves 9 dB improvement in the FoM at 10 MHz offset with occupying 30% smaller area.

Fig. 14(a) and (b) show the measured $1/f^3$ noise corner and PN at 1 MHz offset across the whole 39% TR, respectively, demonstrating that the proposed gate–drain phase shift technique is wide-band in suppressing the flicker PN. The measured $1/f^3$ PN corner and PN at 1 MHz offset versus

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

		This Work		[57] El-Aassar-*JSSC*'21	[42] Sharkia-*JSSC*'18	[40] Ximenes-*TMTT*'17	[15] Yin-*JSSC*'16		[56] Tohidian-*MWCL*'15	[55] Abdul-Latif-*JSSC*'12
Type		Transformer-Based		Dual-Core Tri-Band	Inductor-Based	Transformer-Based	Dual-Mode TI-RVCO		Series LC	Cyclic-Coupled Ring
EM Compatibility?		Yes		No	No	Yes	Yes		No	Yes
f_0 [GHz]		9 – 13.34 (39%)		8 – 17 (72%)	4.6 – 5.6 (20%)	9.4 – 14.8 (45%)	1.7 – 3.47 (69%)		2.66 – 4.97 (61%)	1 – 2.56, 3.16 – 12.8 (163%)
V_{DD} [V]		0.9		0.45	0.8	1	0.7 – 1		0.9 – 1.1	0.7
Power [mW]		5.98	5	17 – 33	0.53	12 – 20	0.65	2.51	8.5 – 16	13 – 200
1/f³ PNCorner [kHz]		**70**	**250**	3000[&]	200[&]	300[&]	90	150	3000[&]	N/A
Phase Noise [dBc/Hz]	**1 MHz**	-110.2	-107.1	-112.3 – -119.1	-108.3	-103.5	-100.4	-98.7	N/A	-105.5
	10 MHz	-130.1	-128.5	-134.7 – -143.1	N/A	-124	-120.5	-119.3	-132.2	N/A
FoM*[dB]	**1 MHz**	-181.5	-182.6	N/A	-185.1	N/A	-166.9	-161.7	N/A	-160 – -166
	10 MHz	-181.4	-184	-180.65 – -191.65	N/A	-175	-167	-165.6	-173 – -176.9	N/A
FoM_T ** [dB]	**1 MHz**	-193.3	-194.4	N/A	-191.1	N/A	-183.6	-178.4	N/A	-184.2 – -190.2
	10 MHz	-193.2	-195.8	-197.8 – -208.8	N/A	-188	-183.7	-182.3	-188.7 – -192.6	N/A
FoM_A * [dB]**	**1 MHz**	-201.5	-202.6	N/A	-205.1	N/A	-192.1	-186.9	N/A	-168 – -174
	10 MHz	-201.4	-204	-184.75 – -195.75	N/A	-193	-192.2	-190.8	-195 – -198.9	N/A
FoM_{TA} ** [dB]**	**1 MHz**	**-213.3**	**-214.4**	N/A	-211.1	N/A	-208.8	-203.6	N/A	-192.8 – -198.8
	10 MHz	**-213.2**	**-215.8**	-201.9 – -212.9	N/A	206.4	-208.9	-207.5	-210.7 – -214.6	N/A
Supply Pushing [MHz/V]		80		0 – 60	N/A	80	4070		N/A	18461
Core Area[mm²]		0.01		0.39	0.01[#]	0.0144	0.003		0.0063	0.145
Technology		22-nm FD-SOI		22-nm FD-SOI	65-nm CMOS	40-nm CMOS	65-nm CMOS		40-nm CMOS	90-nm CMOS

[&]Estimated from PN plot *FoM = PN – 20log(f_0/Δf) + 10log(P_{DC}/1mW), **FoM_T = FoM – 20log(TR/10)
FoM_A = FoM + 10log(Area/1mm²) *FoM_{TA} = FoM – 20log(TR/10) + 10log(Area/1mm²)
[#]Including the synthesizer underneath the inductor

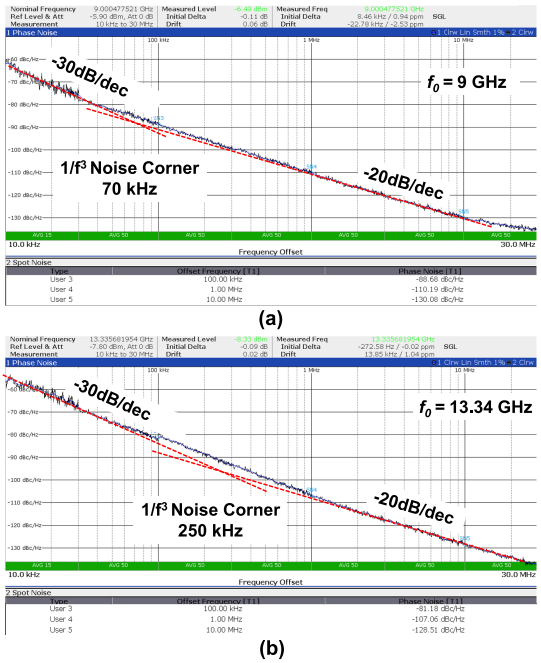


Fig. 13. Measured phase noise at (a) 9 GHz, and (b) 13.34 GHz.

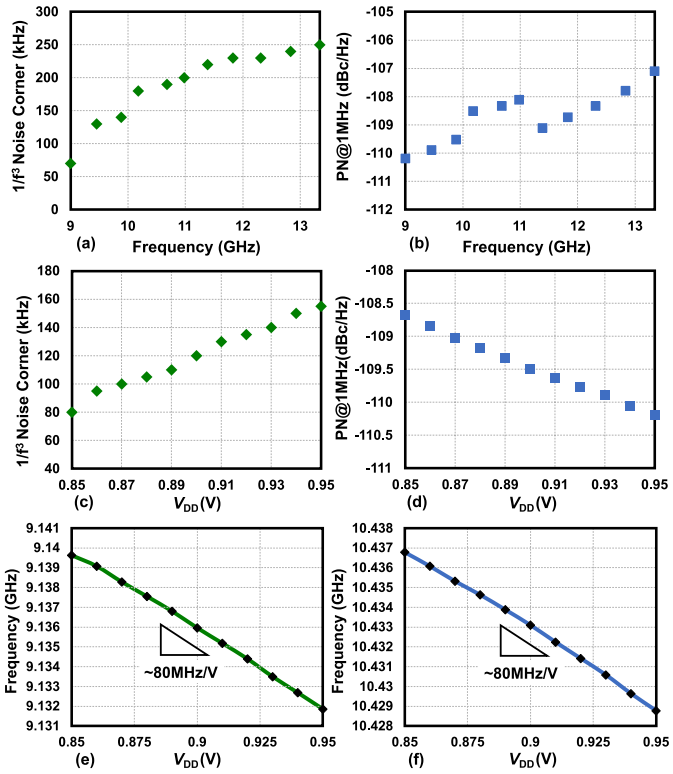


Fig. 14. Measured (a) $1/f^3$ PN corner, and (b) PN at 1 MHz offset over TR. Measured (c) $1/f^3$ PN corner, and (d) PN at 1 MHz offset over supply voltage at 9.13 GHz carrier. Measured frequency pushing (e) at 9.13 GHz carrier, and (f) 10.43 GHz carrier.

supply voltage are illustrated in Fig. 14(c) and (d), demonstrating its robustness against supply variation from 0.85 V to 0.95 V. The supply frequency pushing effect is measured at two carrier frequencies, as shown in Fig. 14(e) and (f). The proposed oscillator exhibits a great supply pushing around 80 MHz/V, which is two orders-of-magnitude better than that in any ring oscillator [15].

The performance of the proposed oscillator is summarized in Table I and compared with other recently published state-of-the-art oscillators featuring a small area. To the best of the authors' knowledge, it achieves a record FoM with normalized TR and area (FoM_{TA} [58], [59]) of −214 dB at 1 MHz offset.

VI. Conclusion

In this paper, we establish that in a complementary class-B oscillator, the ill-behaved second-harmonic voltage can be fully suppressed by the complementary operation itself, while the third-harmonic current entering the capacitive path is now the main contributor to the flicker noise upconversion. For the complementary class-F oscillator, it is the negative gate–drain phase shift causing excess of flicker noise $I_{1/f,\mathrm{rms}}$ exposure to the rising parts of V_{DS}, leading to the flicker phase noise. A robust and wide-band (39% TR) flicker PN suppressing technique was proposed, employing a gate–drain phase shift (adjusted by the capacitance ratio) in a compact (i.e., $0.01\,\mathrm{mm}^2$), triple-8-shaped transformer-based complementary oscillator. The prototype achieves best FoM with normalized TR and area ($\mathrm{FoM_{TA}}$) of -214 dB at 1 MHz offset, combining both benefits of LC-tank-based and inverter-ring-based oscillators.

Appendix: Proof of $\lim_{X\to\infty}\Omega(X)=1$

The upper limit of the numerator in the square root of (8) is expressed as

$$\lim_{X\to\infty}\left(1+n^2X-\sqrt{(1+n^2X)^2-4n^2X(1-k_{\mathrm{m}}^2)}\right)=\lim_{X\to\infty}\left(1+n^2X-(1+n^2X)\sqrt{1-\frac{4n^2X(1-k_{\mathrm{m}}^2)}{(1+n^2X)^2}}\right). \tag{16}$$

When $X\to\infty$, $4n^2X(1-k_{\mathrm{m}}^2)/(1+n^2X)^2\to 0$, we have the following Taylor series as:

$$\sqrt{1-\frac{4n^2X(1-k_{\mathrm{m}}^2)}{(1+n^2X)^2}}=1-\frac{1}{2}\frac{4n^2X(1-k_{\mathrm{m}}^2)}{(1+n^2X)^2}+\cdots. \tag{17}$$

Substituting (17) into (16), we get

$$\lim_{X\to\infty}\left(1+n^2X-(1+n^2X)\left(1-\frac{1}{2}\frac{4n^2X(1-k_{\mathrm{m}}^2)}{(1+n^2X)^2}+\cdots\right)\right)=\lim_{X\to\infty}\left(\frac{2n^2X(1-k_{\mathrm{m}}^2)}{1+n^2X}\right)=2(1-k_{\mathrm{m}}^2). \tag{18}$$

Therefore,

$$\lim_{X\to\infty}\Omega(X)=\sqrt{\frac{2(1-k_{\mathrm{m}}^2)}{2(1-k_{\mathrm{m}}^2)}}=1. \tag{19}$$

Acknowledgment

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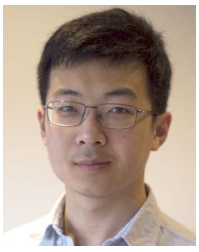

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