

Transmitter and Receiver for High Speed Polymer Microwave Fiber Communication at D-band

Frida Strömbeck, *Student Member, IEEE*, Zhongxia Simon He, *Senior Member, IEEE* and Herbert Zirath, *Fellow, IEEE*

Abstract—A chipset for high datarate polymer microwave fiber (PMF) communication is described. It consist of a PAM-4 RF-DAC and power detector (PD) and is fabricated using a commercial 130 nm SiGe BiCMOS process. A link measurement is performed over a one meter long PMF verifying that the link can support data rates up to 20 Gbps using PAM-4, with a bit error rate (BER) of $< 10^{-12}$. The RF-DAC covers frequencies between 120-160 GHz, with a peak output power of 4 dBm. It has a stacked transistor pair as core and includes a frequency doubler at the LO input and a three stage amplifier at the output. The PD includes an amplifier and an active balun to suppress the fundamental frequency. Both circuits occupy only 1.54 mm² combined, including pads. The high data-rate, energy efficiency, low cost and robustness of the link makes it suitable for short range (< 10 meters) device-to-device communication.

Index Terms—PAM-4, PD, PMF, RF-DAC, SiGe

I. INTRODUCTION

THE ability to process large amounts of data in a short amount of time has enabled several functions like machine learning and artificial intelligence (AI). The combination of AI and high precision robotics enables systems of fully automated factories and services. Solutions to transfer the data from the sensors and antennas to the central processing unit (CPU) at this high data rate is challenging and urgently needed. Fast data links between sensors and the CPU is essential. To be able to meet the demands of sensitivity and security, a high amount of data collection has to be done.

The development of autonomous vehicles is heavily relying on sensor fusion to make correct decision of the maneuvering. Sensors such as cameras, lidars, long range/short range radars inside and outside cabin, etc, are all connected to a CPU. With increasing number and with increasing resolution of the sensors, the capacity of data transmission in the vehicle has already exceeded 10 Gbps [1]. Primarily, fiber optics is considered as a good transmission solution due to high capacity, however, it is sensitive to the temperature condition of vehicle operation [2]. In addition, the focus of the short range in-cabin high speed communication systems is not only speed, but robustness, energy efficiency, reliability and cost.

Manuscript received 8 December 2021; revised 26 April 2022, 3 June 2022, and 8 June 2022; accepted 26 July 2022. Date of publication 17 August 2022; date of current version 26 October 2022.

F. Strömbeck, Z.S. He and H. Zirath are with Microwave Electronics Laboratory at Chalmers University of Technology, Gothenburg, Sweden.

The authors would like to thank Infineon Technologies for the fabrication of the chips.

The car2TERA project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 824962

For these reasons, polymer microwave fibers (PMF) have recently become an interesting alternative for short range (1-10 meters) links [3] [4] [5] [6] [7]. In a previous work, a PAM-4 radio frequency digital-to-analog converter (RF-DAC) in a 250 nm InP DHBT technology demonstrated that both high speed (40 Gbps) and high energy efficiency (1.2 pJ/bit) could be achieved using emitter coupled pairs as RF-DAC [8]. In this work, we demonstrate a PMF link based on a commercial automotive-certified 130 nm BiCMOS process. To the authors' knowledge it is the first PMF link using a SiGe BiCMOS process. In this process a stacked RF-DAC, with integrated local oscillator (LO) multiplier and power amplifier (PA) is proposed as transmitter and an active balun integrated power detector (PD) is used as receiver. The benefits of using an RF-DAC based PAM-4 modulator/PD for PMF communication is the high speed, no need for carrier recovery, low complexity and small circuits. The higher gain in the bipolar devices compared to CMOS makes it possible to use such an approach since PAM-4 requires higher SNR than QPSK for example. Real time transmissions of a PAM-4 signal are demonstrated which supports 20 Gbps with a bit error rate (BER) $< 10^{-12}$ at 138 GHz over a one meter PMF. This paper is organized as following; after introduction, in section II the technology and circuit design is described. Section III contains the measurement results, and section IV is the discussion and conclusion.

II. TECHNOLOGY AND CIRCUIT DESIGN

The proposed link consists of a transmitter which is based on a frequency doubler for the LO input, stacked RF-DAC as modulator, and a three stage single ended amplifier at the output. The receiver is a power detector (PD), which includes an amplifier at the input. Both circuits, transmitter (Tx) and Receiver (Rx), are designed and fabricated using a 130 nm SiGe BiCMOS process (B11HFC) that is offered by Infineon Technologies [9].

A block diagram of the RF-DAC can be seen in Fig. 1.

The core of the RF-DAC consists of a parallel stacked transistor pair, due to its energy efficiency. The schematic of the core of the RF-DAC can be seen in Fig. 2.

The function is as follows; if a voltage (1 V) is applied at the data input port, corresponding to logic value '1', it will turn on transistor Q2 for port D0 and Q4 for port D1. The current will flow through Q1 and Q3 which are connected to the LO input at the base, and the LO-signal is modulating the collector current. The output RF-signal is taken at the collector

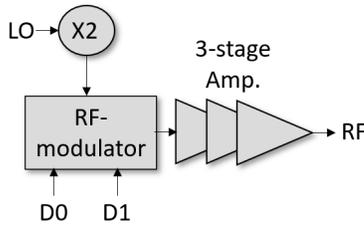


Fig. 1. Block diagram of the transmitter.

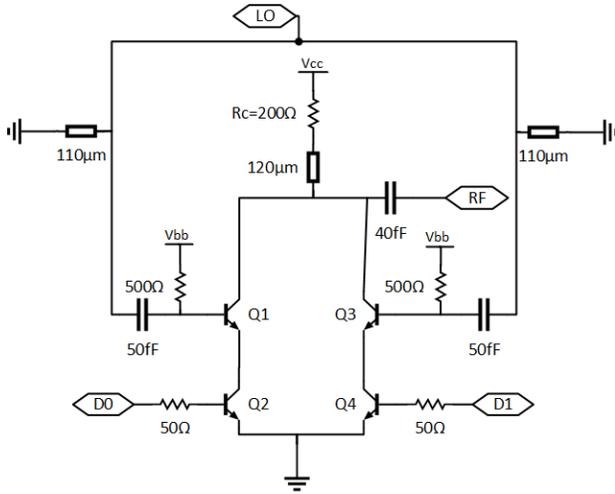


Fig. 2. Simplified schematic of the core of the RF-DAC. The shorted stubs at the LO input are $110 \mu\text{m}$ long with a width of $4.9 \mu\text{m}$. V_{cc} is 3 V and V_{bb} is internally biased using a resistor from V_{cc} and two stacked diodes to ground.

of Q1 and Q3 which are connected. For logic value '0', which in this case is 0 V applied at the data ports, Q2 and/or Q4 are turned off correspondingly, which in turn, turns off transistor Q1 and/or Q3, thus giving less power at the output. To create a most significant bit (MSB) and a least significant bit (LSB), transistor scaling is used. Q1 and Q2 have an emitter width of $6 \mu\text{m}$ while Q3 and Q4 have an emitter width of $3 \mu\text{m}$. The resistor R_c is 200Ω .

Simulation result of the output power for different data input voltages at the D0 port, can be seen in Fig. 3. D1 is set to 0 V and 1 V, and the carrier frequency is 140 GHz.

The RF-output is then amplified, the schematic of the amplifier can be seen in Fig. 4. The amplifier has three stages with increasing size of transistors ($6, 8$ and $10 \mu\text{m}$ emitter width). The interstage matching consist of a highpass network which counteracts the decreasing gain versus frequency for the transistor, resulting in a flat frequency response from 110 GHz to 150 GHz.

The LO is fed to the RF-DAC core via a frequency doubler. A simplified schematic of the doubler can be seen in Fig. 5. A Marchand balun at the input creates a differential signal, which is fed at the base of an emitter coupled pair. The output is then taken at the connected collectors which has a shorted stub for matching purposes. V_{cc} is 3 V and V_{bb} is internally biased using a resistor from V_{cc} and two stacked diodes to ground.

The fabricated RF-DAC is depicted Fig. 6. The circuit is

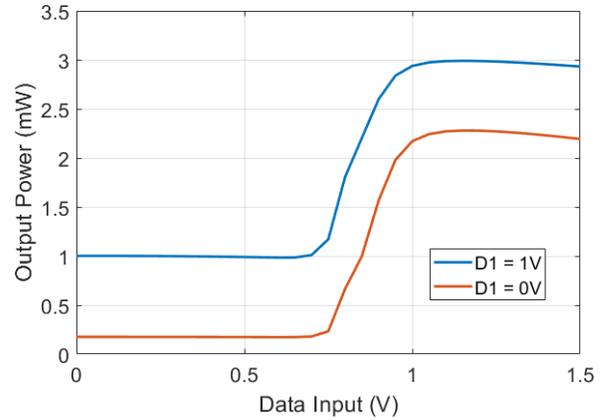


Fig. 3. Simulated output power for different voltage applied at the data ports. D1 was set to 0 V and 1 V, while D0 was swept between 0-1.5 V. The carrier frequency is 140 GHz and the input power is 3 dBm. The simulation was carried out using Cadence.

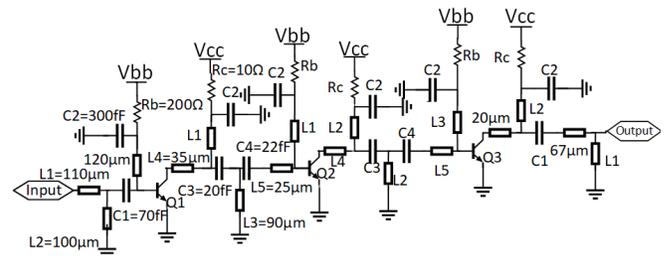


Fig. 4. Simplified schematic for the three stage amplifier used at the RF output. V_{cc} is 2 V and V_{bb} is internally biased using a resistor from V_{cc} and one stacked diode to ground.

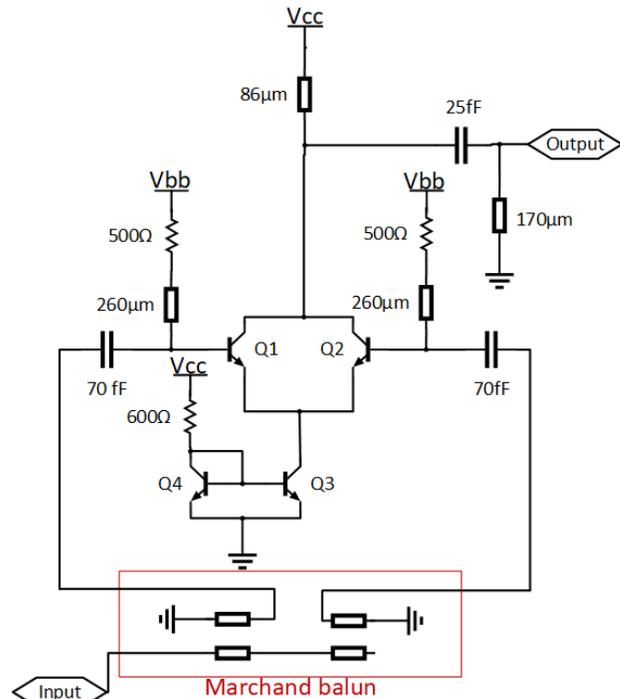


Fig. 5. Simplified schematic of the frequency doubler used at the LO input.

supplied by two DC bias of 2 V (V_{cc} for the amplifier) and 3 V (V_{cc} for the multiplier and RF-DAC core). The size of the circuit is $1.18 \times 0.72 \text{ mm}^2$ including pads.

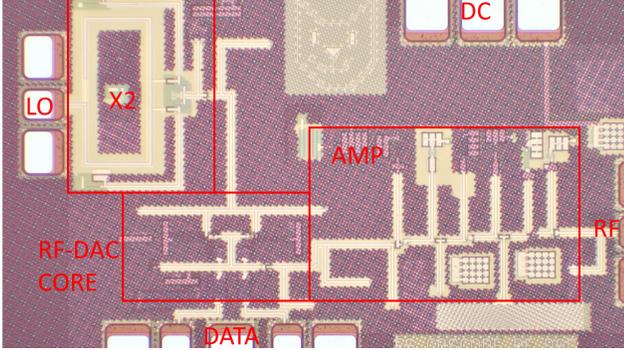


Fig. 6. Photograph of the transmitter.

The PD consists of a three stage common emitter amplifier at the input, with interstage matching, which is followed by two transistors, one which (Q7) is connected at the base configured as common emitter and one (Q8) that is connected at the emitter configured as common base. This acts as an active balun, at D-band, to cancel the odd harmonics of the carrier signal (from the transmitter), thus improving LO isolation. The combined output from these transistors are connected to the emitter of transistor at the output, which amplifies the data signal. Using an active balun compared to a passive balun can improve the bandwidth as well as gain. The schematic can be seen in Fig 7.

The fabricated PD can be seen in Fig. 8. The DC bias for the circuit is 1.5 V, 1.8 V, 2.3 V and 3 V for the PD. The size of the circuit is $1.25 \times 0.55 \text{ mm}^2$ including pads.

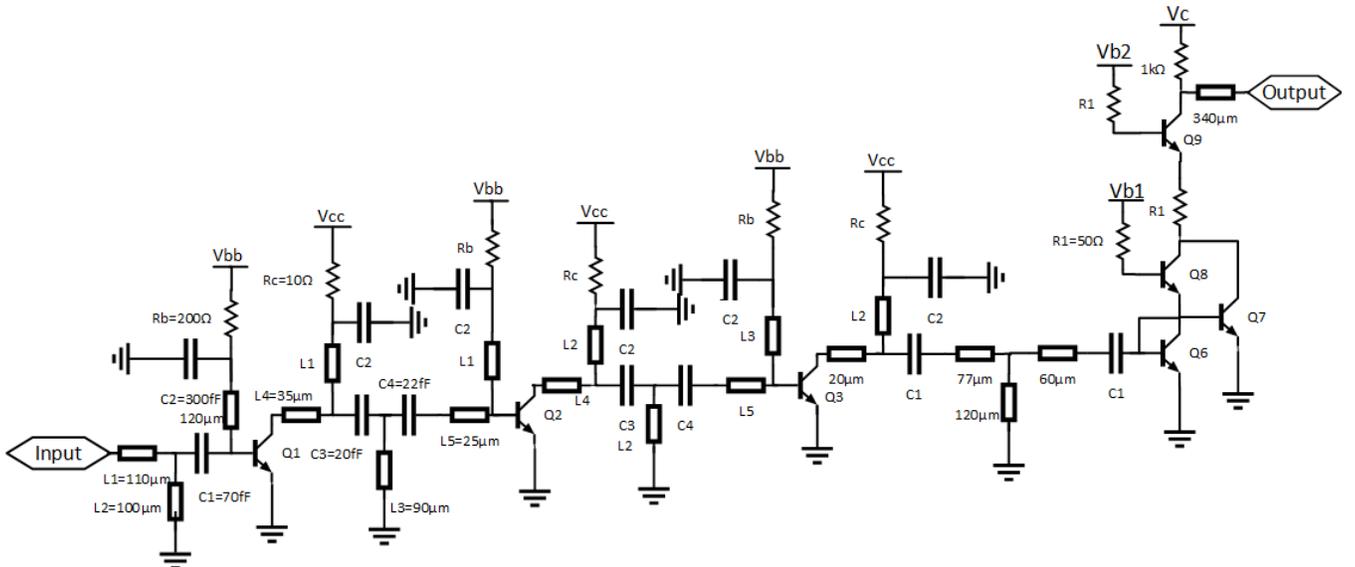


Fig. 7. Simplified schematic of the PD. Transistor Q6-Q8 have an emitter width of $3 \mu\text{m}$, and Q9 of $10 \mu\text{m}$.

III. MEASUREMENT RESULTS

A. Transmitter

The transmitter used as a PAM-4 modulator was measured in the frequency domain, on-wafer, using a probe station. The measurement of the output power, for different data input, was captured with a Keysight PNA-X (67 GHz N5247A), a VDI extender WR-6.5 was used at the output, and calibrated for absolute power measurements using the VDI calkit and an Erickson power meter (PM5). The input power to the LO-input was 5 dBm and was swept between 55 and 85 GHz. A VDI extender WR-12 was used to provide the input signal. The output power in the D-band (110 GHz-170 GHz) for different data input, both simulated and measured, can be seen in Fig. 9.

The DC power consumption of the RF-DAC is 132 mW, where the amplifier uses 78 mW, the doubler uses 42 mW and the RF-DAC core uses 12 mW.

B. Receiver

The PD was characterized by on-wafer measurements. The input power was provided by a Keysight PNA-X (67 GHz N5247A) through a D-band VDI extender WR-6.5, the output voltage was measured using a voltage meter. The voltage change for different input powers at 140 GHz, both simulated and measured can be seen in Fig. 10.

The LO leakage was measured by applying 0 dBm input power, and sweeping the frequency between 110 GHz and 170 GHz. The LO isolation of the signal was measured and is displayed in Fig. 11.

The DC power consumption of the PD is 59 mW, where the amplifier uses 55 mW.

C. Link Measurement

A link measurement was done over a one meter long PMF, provided by Lehrstuhl für Hochfrequenztechnik (LHFT),

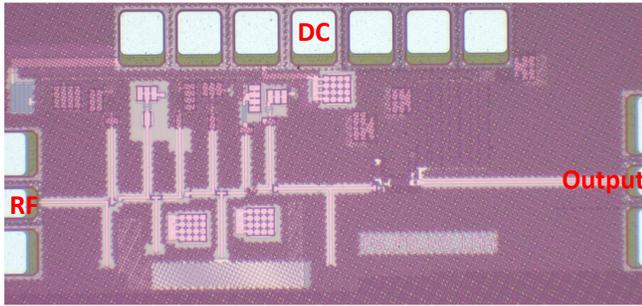


Fig. 8. Photograph of the PD.

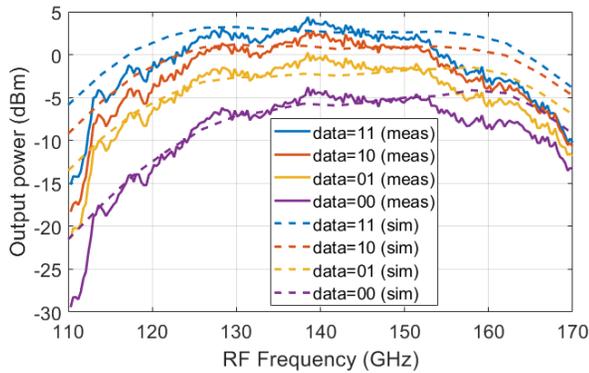


Fig. 9. Output Power for different output frequencies at 5 dBm LO input. Solid lines represent the measurements, while the dashed lines are the simulated values.

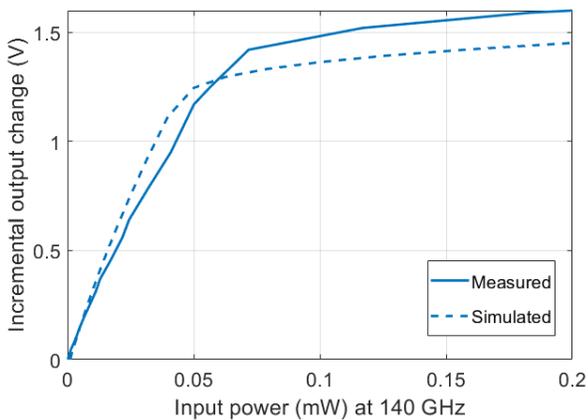


Fig. 10. Difference in output voltage for different input powers (W). The dashed lines represent the simulated values, and the solid lines is the measured values.

Germany, transferring data in real time. The output from the receiver was then connected using a coaxial cable to a Lecroy LabMaster 10-100Zi real-time oscilloscope where the signal could be analyzed. A photo of the fiber connecting the circuits on each probe station can be seen in Fig. 12.

The LO input signal for the RF-DAC was provided by a signal generator (PSG 20 GHz Agilent E8257D) through a VDI extender WR-12. The LO input frequency was set to 69 GHz, resulting in a center RF-frequency of 138 GHz. Two pseudorandom binary sequences (PRBS-9 and PRBS-10) was

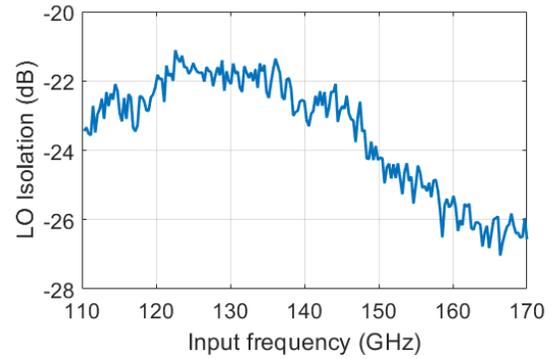


Fig. 11. Isolation of the fundamental frequency measured at 0 dBm input power.

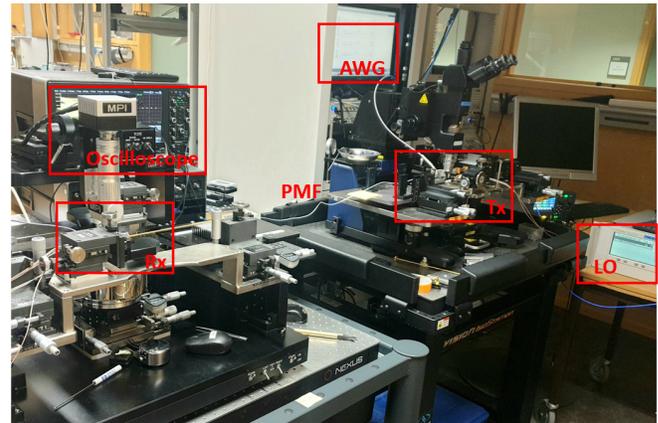


Fig. 12. The setup that was used during the link measurement.

provided by a Keysight M8195A arbitrary waveform generator (AWG) to generate the data. Different combinations of pulse shaping of the input stream, by the AWG, and equalization of the output stream, by the oscilloscope, were used. The equalizer is a Finite Impulse Response (FIR) equalizer, using 21 taps. An external DC block was used at the output of the PD during all measurements. De-emphasis (DE) of the input data stream was used to attenuate the lower frequency components of the signal to counter the dispersive effects of the PMF, and can be seen in Fig. 13.

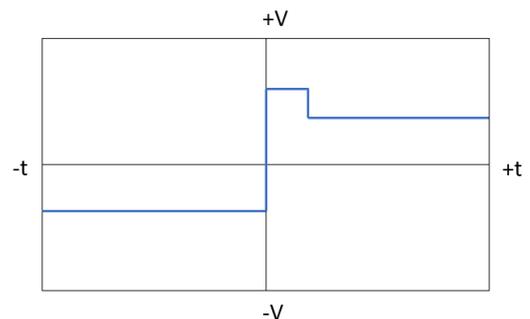


Fig. 13. De-emphasis with one negative post cursor tap.

In Fig. 14, eye diagrams of the output can be seen, using a

carrier frequency of 138 GHz. In Figure 14 A, both root-raised cosine (RRC) pulse shaping, with a roll-off factor of 1 and DE with one -5 dB post-cursor tap was used. Equalization is used at the output. In Figure B, the same pulse shaping as Figure A is used, but without equalization at the output. In Figure C no pulse shaping of the input bit stream is used, but equalization at the output of the PD. Data rates are 10 Gbaud (20 Gbps), 9 Gbaud (18 Gbps) and 8 Gbaud (16 Gbps), and the bit error rate (BER) of the transmissions are less than 10^{-12} .

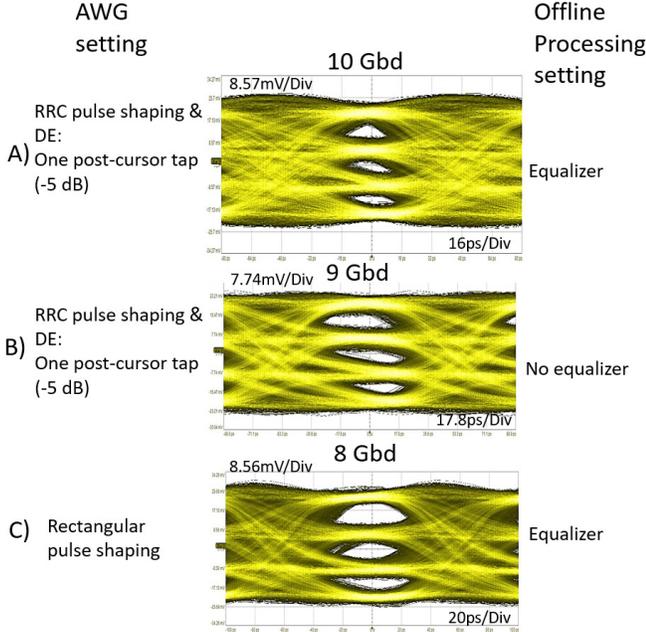


Fig. 14. Eye diagrams of the output from the PD at 69 GHz LO (138 GHz RF) for A) 10 Gbaud using RRC pulse shaping and DE with one -5 dB post-cursor tap. Equalization is also used at output. B) 9 Gbaud using RRC pulse shaping and DE with one -5 dB post-cursor tap. C) 8 Gbaud with no pulse shaping, but equalization is used at output. All transmissions have a BER $< 10^{-12}$.

In Fig. 15, eye diagrams for baud rates between 6 Gbaud and 4 Gbaud, corresponding to 12 Gbps and 8 Gbps, are shown. No equalization was used at the output of the PD, and all transmissions have a BER $< 10^{-12}$. In Figure D, de-emphasis with one -5 dB post-cursor tap is used, while in Figure E, de-emphasis with one -3 dB post-cursor tap is used. In Figure F, RRC pulse shaping with a roll-off factor of 1 is used. In Figure G, no pulse shaping is used of the input bit stream.

Baud rates up to 11 Gbaud were tested (using no pulse shaping, but equalization at output). The BER corresponding to different baud rates can be seen in Fig. 16. Less than 10^{-12} is displayed as 10^{-12} , which is considered "error free".

The link was also tested sending the same data at both data input ports (PRBS-10), in other words PAM-2 modulation. Figure 17 shows eye diagrams of data rates between 8 Gbps and 16 Gbps. In Fig. A (16 Gbps), no pulse shaping of the bit stream is used, but a DC block and equalization is used (by the oscilloscope) at the output of the PD. Fig. B (10 Gbps), an RRC filter (roll off factor=1) to shape the bit stream (by AWG) and a DC block at the output from the PD is used. Fig. C (8 Gbps), no pulse shaping is used, only a DC block at the output of the PD. The carrier frequency during the measurements was

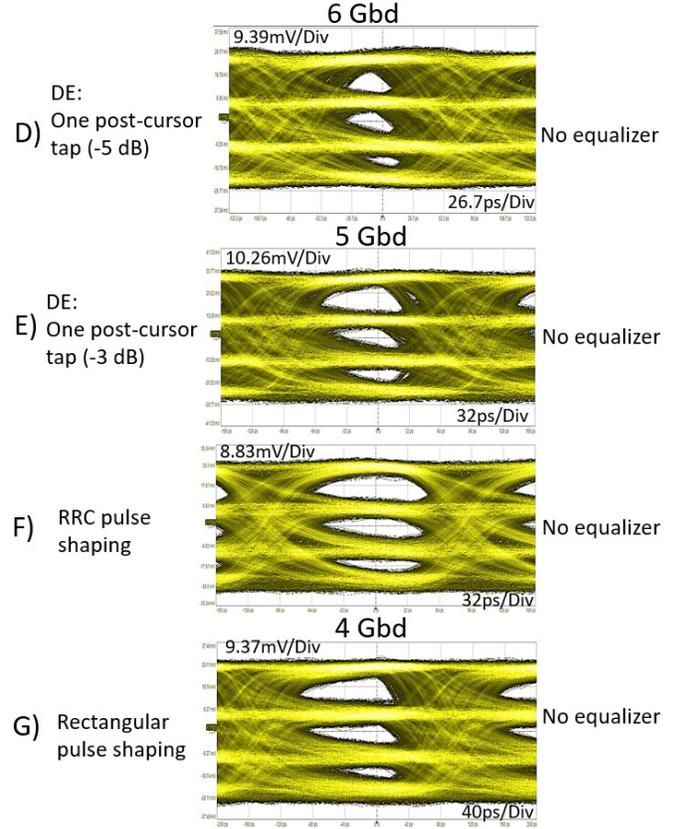


Fig. 15. Eye diagrams of the output from the PD at 69 GHz LO (138 GHz RF) for D) 6 Gbaud using DE with one -5 dB post-cursor tap. E) 5 Gbaud using DE with one -3 dB post-cursor tap. F) 5 Gbaud using RRC pulse shaping. G) 4 Gbaud with no pulse shaping. All transmissions have a BER $< 10^{-12}$.

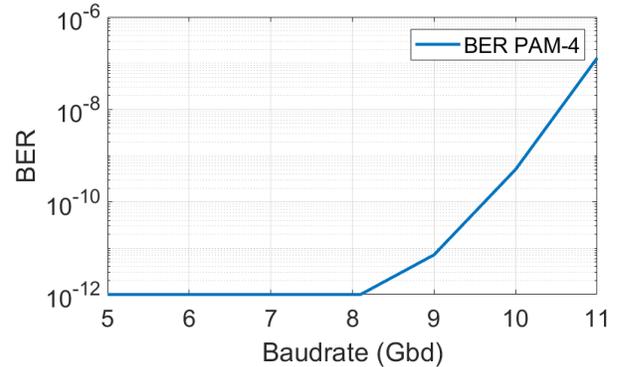


Fig. 16. BER for different baud-rates for PAM-4 link transmission at 138 GHz RF, using no pulse shaping, but equalization at output. ($< 10^{-12}$ is displayed as 10^{-12})

set to 138 GHz, and all transmissions had a BER of less than 10^{-12} .

Total DC power consumption for the link is 191 mW.

IV. THEORETICAL LIMIT

The effects of the fiber on the PAM-4 signal was simulated to understand the limitations and important parameters of the system. Matlab was used for the system simulations, and CST Studio Suite was used to simulate the fiber. The EM simulation

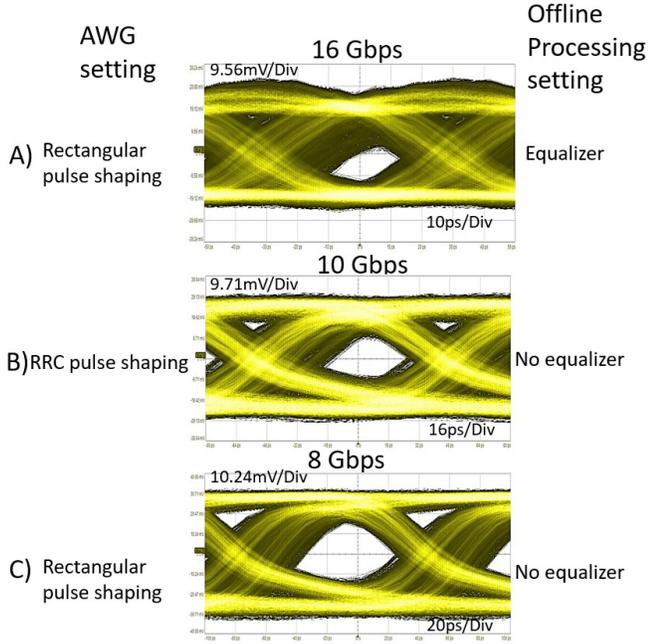


Fig. 17. Eye diagrams of the output from the PD at 69 GHz LO (138 GHz RF) for A) 16 Gbps using equalization at output. B) 10 Gbps using RRC pulse shaping. C) 8 Gbps with no pulse shaping. All transmissions have a BER $< 10^{-12}$.

showed the propagation of the signal (Fig. 18). A higher electric field density is displayed using warmer (red) colors.

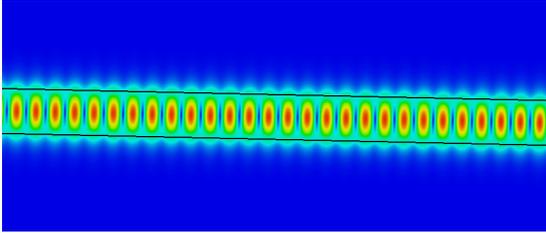


Fig. 18. CST was used to simulate the propagation of the signal through the fiber at D-band. The frequency was set to 140 GHz in this figure.

The simulated S21 and group delay can be seen in Fig. 19 and Fig. 20. The simulations of the fiber compare to the measurements (even if the transitions are not included).

Random data (D) is generated and up-sampled. An over-sampling of 400 per symbol was used during these simulations. The data was given an amplitude in voltage (A_V), a constant amplitude of leakage (A_I) was added, which is independent to the data. The amplitude is multiplied with the sinusoidal carrier, resulting in a modulated signal (y).

$$y = (A_I + A_V D) \sin(2\pi f_c t) \quad (1)$$

The signal is converted to frequency domain using fast fourier transform (FFT), and the transfer function generated from the s-parameters of the PMF is applied to the signal. The signal is then converted back to time domain, using inverse FFT. The envelope of the output signal is down-sampled, and the amplitude is compared to recover the output bitstream.

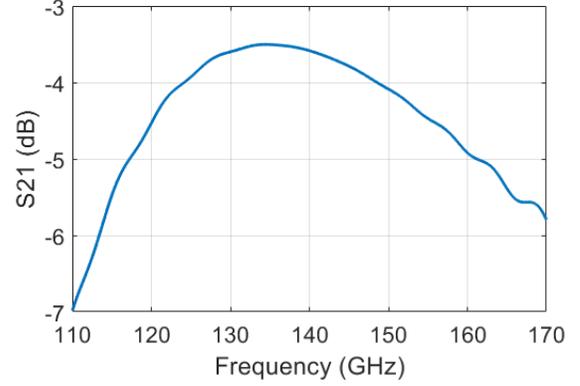


Fig. 19. CST simulated S21 of a 1 meter long Polytetrafluoroethylene (PTFE) fiber.

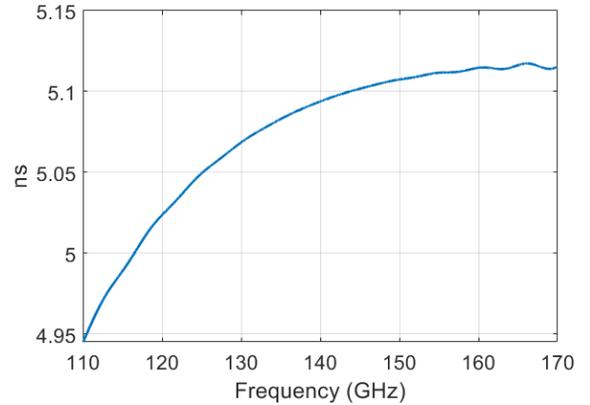
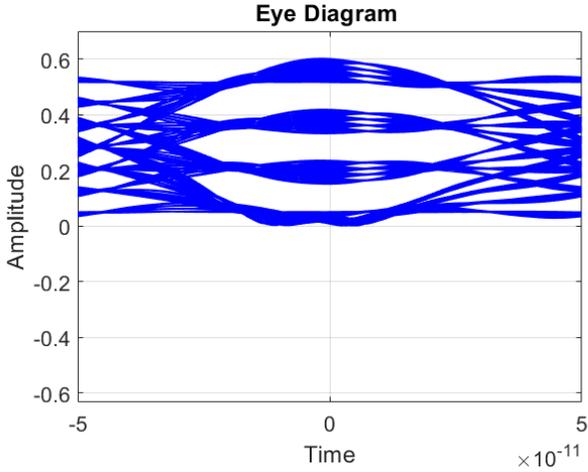


Fig. 20. CST simulated group delay of a 1 meter long PTFE fiber.

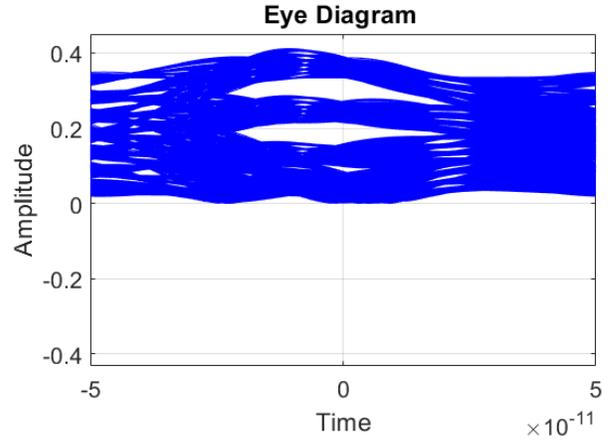
Simulations with a carrier frequency of 135 GHz, where the attenuation is the lowest, and the difference in attenuation over the bandwidth of the signal is minimized, was compared to simulations with 150 GHz as the carrier, where the group delay difference is significantly lower over the bandwidth of the signal. The eye diagrams of the demodulated PAM-4 signal for the different carrier frequencies can be seen in Fig. 21. The Baudrate was 10 GBd for both carriers, and the fiber was 1 meter long.

The difference in the shape of the eye diagrams is noticeable. More symbol interference can be seen for the lower carrier frequency, due to the larger difference in group delay. To get a clearer view of the effects, same simulations were made, but over a 2 meter long fiber. The eye diagrams can be seen in Fig. 22.

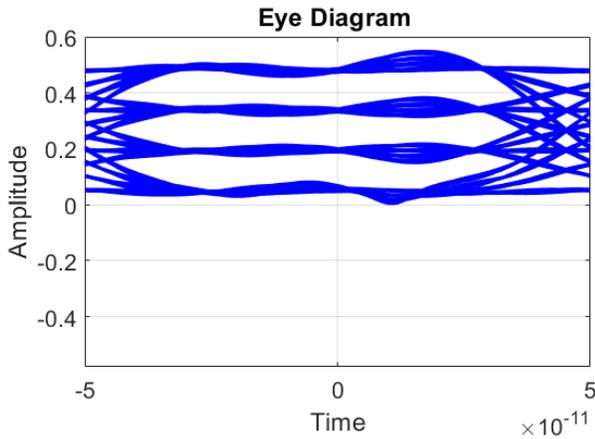
The difference in group delay for different frequencies (dispersion) of the fiber is a critical limitation. From the simulations one can see that the dispersive effects are lower at high carrier frequencies for this type of PMF. For PAM-4 modulation, the signal is more sensitive to change in group delay in the transmitted signals frequency band, than difference in attenuation. Difference in group delay leads to symbol interference, and for high speed, wide bandwidth communication this either needs to be minimized or compensated for. From that point of view, it is beneficial to use a high carrier



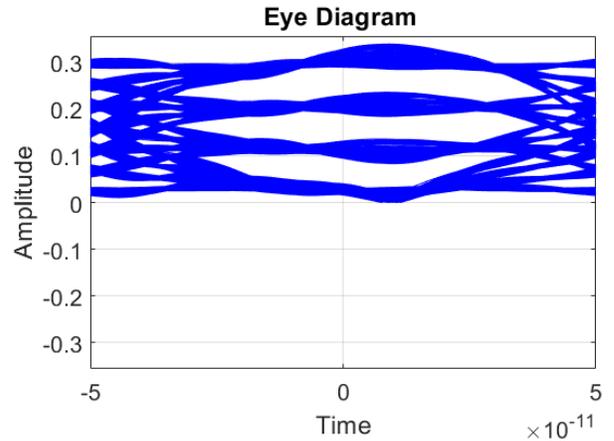
(a) Eye diagram of a demodulated 10 GBd PAM-4 signal using a carrier at 135 GHz over the simulated 1 meter long fiber.



(a) Eye diagram of a demodulated 10 GBd PAM-4 signal using a carrier at 135 GHz over the simulated 2 meter long fiber.



(b) Eye diagram of a demodulated 10 GBd PAM-4 signal using a carrier at 150 GHz over the simulated 1 meter long fiber.



(b) Eye diagram of a demodulated 10 GBd PAM-4 signal using a carrier at 150 GHz over the simulated 2 meter long fiber.

Fig. 21. Eye diagrams of a demodulated transmissions over 1 meter pmf. The amplitude unit is volt, and the time unit is seconds.

Fig. 22. Eye diagram of a demodulated transmissions over 2 meter PMF. The amplitude unit is volt, and the time unit is seconds.

frequency. Although other challenges, like power limitations, may be the limiting factor instead, which has to be considered like a trade-off.

V. DISCUSSION AND CONCLUSION

The results from this work is compared with previous work in Table I.

In this work a transmitter and receiver based on a PAM-4 modulator as well as a PD designed and measured using a commercial 130 nm SiGe BiCMOS process. Link measurements showed that the circuits can support up to 20 Gbps with BER $< 10^{-12}$. The circuits are area efficient, with a combined chip area of 1.54 mm² including pads. This type of

TABLE I
COMPARISON WITH OTHER PMF LINKS, WITH BER $< 10^{-12}$

Reference	[3]	[4]	[5]	[6]	[this work]
Technology	40 nm CMOS	28 nm CMOS	65 nm CMOS	28 nm CMOS	130 nm BiCMOS
Modulation	CP-FSK	CP-FSK	ASK	ASK	PAM-4
Frequency (GHz)	120	140	60	135	138
Data Rate (Gbps)	17.7	12	6	27	20
Fiber Length (m)	1.0	1.0	2.0	1	1.0
Energy Eff. (pJ/bit)	4.0*	19.2	4.7	4.8	9.55*
(*no LO included)					
Total chip area (mm ²)	N/A	2.31	N/A	1.94	1.54
Peak output power (dBm)	-1.9	6	N/A	-3	4

communication link is suitable for short distance, high speed communication, for example in-cabin vehicle communication for autonomous vehicles. It is shown that pulse shaping and/or equalization can be used with benefit to counteract the dispersive effects of the fiber.

REFERENCES

- [1] eeworldonline.com, "What high-speed data means for connected vehicles", 2019. [online]. Available: <https://www.eeworldonline.com/what-high-speed-data-means-connected-vehicles/> [Accessed 20-Jan-2021]
- [2] car2tera.eu, "Next Generation Smart Automotive Electronic Systems", 2020. [online]. Available: <https://car2tera.eu/about/> [Accessed 25-Nov-2020]
- [3] N. Van Thienen, Y Zhang, M. De Wit, and P. Reynaert, "An 18 Gbps Polymer Microwave Fiber (PMF) Communication Link in 40nm CMOS", *2016 European Solid-State Circuits Conference*, pp. 483-486, September 2016.
- [4] M. De Wit, Y. Zhang, P. Reynaert, "Analysis and Design of a Foam-Cladded PMF Link With Phase Tuning in 28-nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 54, no. 7, pp. 1960-1969, July 2019.
- [5] Y. Kim, L. Nan, J. Cong, and M.F. Chang, "High-Speed mm-Wave Data-Link Based on Hollow Plastic Cable and CMOS Transceiver", *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 12, pp. 674-676, December 2013
- [6] K. Dens, J. Vaes, S. Ooms, M. Wagner and P. Reynaert, "A PAM4 Dielectric Waveguide Link in 28 nm CMOS," *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, 2021, pp. 479-482.
- [7] P. Reynaert, M. Tytgat, W. Volkaerts, A. Standaert, Y. Zhang, M. De Wit and N. Van Thienen, "Polymer Microwave Fibers: a blend of RF, copper and optical communication ", *2016 European Solid-State Circuits Conference*, pp. 15-20, September 2016.
- [8] F. Strömbeck, Z. S. He, and H. Zirath, "A RF-DAC based 40 Gbps PAM Modulator with 1.2 pJ/bit Energy Efficiency at Millimeterwave Band", *2018 IEEE/MTT-S International Microwave Symposium - IMS*, pp. 931-933, June 2018.
- [9] J. Böck et al., "SiGe HBT and BiCMOS process integration optimization within the DOTSEVEN project", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 121-124, 2015.



Frida Strömbeck received the M.Sc. degree in engineering physics from Chalmers University of Technology, Göteborg, Sweden, in 2018.

She is currently working towards a Ph.D. degree at Microwave Electronics Laboratory, Chalmers University of Technology. Her research interests include high data rate millimeter wave communication and integrated circuit design.



Zhongxia Simon He (M'09) received the M.Sc. degree from the Beijing Institute of Technology, Beijing, China, in 2008, and the Ph.D. degree from the Chalmers University of Technology, Göteborg, Sweden, in 2014.

He is currently an Associate Professor with the Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology. His current research interests include high-data-rate wireless communication, modulation and demodulation, mixed-signal integrated circuit design, high-resolution radars, and packaging.



Herbert Zirath (M'86-SM'08-F'11) was born in Gothenburg, Sweden, in 1955. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Chalmers University of Technology, Gothenburg, in 1980 and 1986, respectively.

From 1986 to 1996, he was a Researcher with the Department of Radio and Space Science, Chalmers University of Technology, where he was responsible for developing GaAs- and InP-based HEMT technology, including devices, models, and circuits. In 1998, he joined the California Institute of Technology, Pasadena, CA, USA, as a Research Fellow, where he was engaged in the design of monolithic microwave integrated circuit (MMIC) frequency multipliers and class-E power amplifiers. In 2001, he joined the Chalmers University of Technology, as the Head of the Microwave Electronics Laboratory, where he has been a Professor of high speed electronics with the Department of Microtechnology and Nanoscience since 1996. Until 2020 he was Head of the Microwave Electronics Laboratory, building it up and developing it along with approximately 40 researchers in the area of high-frequency semiconductor devices and circuits. He is a Research Fellow with Ericsson AB, leading the development of a D-band (110 - 170-GHz) chipset for high data-rate wireless communication. He is a co-founder of Gotmic AB, Gothenburg, a company developing highly integrated front-end MMIC chip sets for 60 GHz and E-band wireless communication. He has authored or co-authored over 600 refereed journals/conference papers and has an H-index of 43 and holds 6 patents. His current research interests include MMIC designs for wireless communication and sensor applications based on III-V, III-N, graphene, and silicon devices.