# Optimized MASH-SR Divider Controller for Fractional- $N$ Frequency Synthesizers 

Dawei Mai ${ }^{( }$, Member, IEEE, and Michael Peter Kennedy ${ }^{( }$, Fellow, IEEE


#### Abstract

The divider controller in a conventional phase-locked loop fractional- $N$ frequency synthesizer modulates the instantaneous division ratio of the feedback divider. The divider controller is typically a digital circuit that performs quantization of its input signal. Multi-stage noise shaping digital delta-sigma modulators (MASH DDSMs) and successive requantizer (SRs) are two representative divider controller architectures offering lower complexity and better spur performance, respectively. The MASH-SR, as a hybrid of these two classes of divider controllers, can achieve both lower hardware cost than the SR and better performance against spurs than a MASH DDSM. In this work, we present an optimized MASH-SR hybrid and compare the design with its conventional MASH DDSM and SR counterparts.


Index Terms-Multi-stage noise shaping structure-successive requantizer (MASH-SR) divider controllers, MASH-SQ divider controllers, phase locked loops, phase noise, quantization noise, nonlinearity, spurious tones.

## I. Introduction

ADIVIDER-BASED phase-locked loop (PLL) is commonly used to implement fractional- $N$ frequency synthesis, as shown in Fig. 1. The divider controller output $y[n]$ modulates the instantaneous division ratio of the multi-modulus divider (MMD) around an integer value $N_{\text {int }}$ [1]. When the divider controller input $x[n]$ is constant, the expected value of the output of the divider controller is a desired fraction $\alpha$, giving:

$$
\begin{equation*}
E\left(N_{i n t}+y[n]\right)=N_{i n t}+\alpha \tag{1}
\end{equation*}
$$

The instantaneous integer division ratio deviates from the exact fractional value, but has the correct long-term average value. This modulation of the MMD introduces a phase noise contribution that can be observed in the output spectrum of the synthesizer.

The quantization error of the divider controller is typically required to be at least second-order high-pass shaped; this minimizes the in-band phase noise contribution from division ratio

[^0]modulation [2]. Conventionally, digital delta-sigma modulators (DDSMs) are used to generate the control sequence $y[n]$ for the divider [3]. A multistage noise shaping structure (MASH) is often preferred due to the inherent stability of higher-order DDSMs of this kind. MASH DDSM can be constructed using simple first-order accumulators.

Every physical PLL contains nonlinearities, e.g., the nonlinear transfer characteristic of the phase-frequency detector (PFD) and charge pump (CP) [4], [5], [6]. The phase deviation introduced by a DDSM-based divider controller will be distorted by the nonlinearity, resulting in spectral regrowth. This leads to additional noise and periodic components in the output phase noise [7], [8], [9]. The periodic components are termed spurious tones or spurs. These can cause unwanted noise in a communication system due to the additional upor down-conversion when the synthesizer is used as a local oscillator.

In order to optimize the spur immunity in the presence of nonlinear distortion, successive requantizers (SRs) ${ }^{1}$ were introduced as an alternative to DDSM-based divider controllers [10], [11], [12], [13]. SRs introduce a controlled and shaped quantization error that is tailored for the presence of know static nonlinearities based on prescribed state transition matrices. By choosing the state transition matrices appropriately, a SR can achieve different degrees of spur immunity as well as noise levels. Since a SR quantizes its input using identical cascaded stages and relatively complex structures are required to implement the quantization noise generator, it has a significantly higher hardware cost than the relatively simple conventional accumulator-based MASH DDSM divider controllers.

The MASH-SR is a hybrid between these two classes of divider controllers. It has a nested-cascaded structure that consists of a MASH DDSM and cascaded quantization blocks [14], [15], [16], [17]. The input to the divider controller is partitioned and quantized by a MASH and a SR. Consequently, fewer quantization blocks are needed to perform the quantization of the divider controller input. Due to the dominance of the phase noise contribution from the SR stages that quantize the most significant bits (MSBs) and the output of the MASH DDSM, the performance of the MASH-SR, both in terms of spur immunity and noise contribution, is close to that of the full-length cascaded SR [14], [15]. Similar to the SR, a MASH-SR can be optimized by choosing the state transition matrices.

[^1]

Fig. 1. Block diagram representation of a CP-PLL fractional- $N$ frequency synthesizer.

(b)


Fig. 2. (a) A MASH DDSM and (b) a constituent error feedback modulator.
In this work, we describe the design of a MASH-SR hybrid that achieves optimal spur performance in the presence of a static nonlinearity and low accumulated quantization noise at low frequencies. Simulation results for the MASH-SR divider controller are compared with DDSMs and SRs.

The architectures of MASH DDSM and SR are reviewed in Sec. II and the MASH-SR hybrid structure is described in Sec. III. The design methodology for the proposed MASH-SR is described in detail in Sec. IV. The simulated performance of the divider controllers is presented in Sec. V, followed by conclusions in Sec. VI.

## II. State-of-Art Divider Controller Architectures: MASH DDSM and SR

## A. MASH DDSM

The most commonly used MASH DDSM divider controller is shown schematically in Fig. 2. This MASH DDSM consists of identical first-order error feedback modulator (EFM1) stages, which are inherently stable. The input of the MASH DDSM $x[n]$ is applied to the first EFM1 stage. Each subsequent EFM1 stage accepts the quantization error signal $e_{i}[n]$, $i=1,2, \ldots, L$ from the previous stage as its input. The outputs of the stages are combined in the error cancellation network, which outputs the control signal $y[n]$.

The output of the MASH DDSM comprises the desired scaled input and a high-pass shaped quantization error. For an $L$ th-order MASH DDSM that consists of $L$ EFM1 stages


Fig. 3. Schematic of (a) a $K$-bit SR , (b) a quantization block.


Fig. 4. Block diagram of a $s_{d}[n]$ sequence generator which can generate first, second and third-order high-pass shaped $s_{d}[n]$.
and has an $N$-bit input, the output is

$$
\begin{equation*}
Y(z)=\left(\frac{X(z)}{M}-\left(1-z^{-1}\right)^{L} E_{L}(z)\right) \tag{2}
\end{equation*}
$$

where $Y(z), X(z), E_{L}(z)$ are the z-transform of the output signal, the input signal to the MASH DDSM, and the quantization error signal of the $L$ th EFM stage, respectively, and $M=2^{N}$ is the modulus. Since an EFM1 stage can be implemented using simple digital accumulators, the MASH DDSM has a low cost in terms of hardware and power. However, MASH DDSM-based divider controllers are prone to cause spurious tones in the output of the fractional- $N$ frequency synthesizer when nonlinearities are present [18].

## B. $S R$

The SR has been designed to quantize its input by introducing a controlled quantization error. A $K$-bit SR consists of $K$ identical cascaded quantization blocks, as shown in Fig. 3 [10], [13]. The quantization error signal of the $d$ th block $s_{d}[n]$ is derived from a sequence generator. The block diagram in Fig. 4 shows a general $s_{d}[n]$ sequence generator. This structure provides a quantization error signal $s_{d}[n]$ which can be first, second, or third-order high-pass shaped, based on the selection signal Order_SEL. The combinatorial logic output $v_{d}[n]$ is generated based on the past output $v_{d}[n-1]$, the parity control signal $o_{d}[n]$, and the output of the pseudo-random number generator (PRNG) $r_{d}[n]$. For different $d$ and $n$ values, $r_{d}[n]$ can be regarded as independent, identically, and uniformly distributed random variables. The combinatorial logic implements a pair of state transition matrices, $\mathbf{A}_{\mathbf{e}}$ and $\mathbf{A}_{\mathbf{0}}$, which dictate
the probabilities of its output when $o_{d}[n]$ is even and odd, respectively. Denoting the output range of the combinatorial logic as $\left[-N_{v}, N_{v}\right]$, the entries of $\mathbf{A}_{\mathbf{e}}$ and $\mathbf{A}_{\mathbf{0}}$ of a are defined as [13]

$$
\begin{align*}
& \mathbf{A}_{\mathbf{e}}(i, j)=P\left(v_{d}[n]=\mathbf{v}(j) \mid v_{d}[n-1]=\mathbf{v}(i), o_{d}[n]=0\right), \\
& \mathbf{A}_{\mathbf{0}}(i, j)=P\left(v_{d}[n]=\mathbf{v}(j) \mid v_{d}[n-1]=\mathbf{v}(i), o_{d}[n]=1\right), \tag{3}
\end{align*}
$$

where $\mathbf{A}_{\mathbf{x}}(i, j)$ is the element at $i$ th row and $j$ th column of matrix $\mathbf{A}_{\mathbf{x}}, \boldsymbol{x}=\boldsymbol{e}$ or $\boldsymbol{x}=\boldsymbol{o}$, and

$$
\begin{equation*}
\mathbf{v}=\left(-N_{v}-\left(N_{v}-1\right) \ldots N_{v}\right)^{T} \tag{5}
\end{equation*}
$$

The value of the 1-bit $o_{d}[n]$ sequence controls the parity of $v_{d}[n]$ : when $o_{d}[n]=0$, only values of the same parity as $v_{d}[n-1]$ are allowed; when $o_{d}[n]=1$, only values of the opposite parity to $v_{d}[n-1]$ are allowed. Thus,

$$
\begin{equation*}
o_{d}[n]=\left(v_{d}[n]-v_{d}[n-1]\right) \bmod 2 \tag{6}
\end{equation*}
$$

As the result [13],

$$
\begin{equation*}
\mathbf{A}_{\mathbf{e}}(i, j)=0 \forall i+j: \text { odd, } \mathbf{A}_{\mathbf{o}}(i, j)=0 \forall i+j: \text { even. } \tag{7}
\end{equation*}
$$

In Fig. 4, the outputs of the first-order difference blocks are denoted as $\nabla v_{d}[n], \nabla^{2} v_{d}[n]$, and $\nabla^{3} v_{d}[n]$, respectively; they can be expressed as

$$
\begin{align*}
\nabla v_{d}[n] & =v_{d}[n]-v_{d}[n-1],  \tag{8}\\
\nabla^{2} v_{d}[n] & =v_{d}[n]-2 v_{d}[n-1]+v_{d}[n-2],  \tag{9}\\
\nabla^{3} v_{d}[n] & =v_{d}[n]-3 v_{d}[n-1]+3 v_{d}[n-2]-v_{d}[n-3] . \tag{10}
\end{align*}
$$

For a $k$ th-order $s_{d}[n]$ generator, the quantization error $s_{d}[n]$ is generated by passing $v_{d}[n]$ through $k$ consecutive first-order difference blocks. When the generator is of first order, $s_{d}[n]=$ $\nabla v_{d}[n]$; for a second-order generator, $s_{d}[n]=\nabla^{2} v_{d}[n]$; when the generator is third-order, $s_{d}[n]=\nabla^{3} v_{d}[n]$. In a practical application as a divider controller, we require $s_{d}[n]$ to be at least second-order high-pass shaped in order to achieve a low in-band phase noise contribution.

For a first-order $s_{d}[n]$ generator, to achieve lossless quantization,

$$
\begin{align*}
& \left(x_{d}[n]+s_{d}[n]\right) \bmod 2  \tag{11}\\
& \quad=\left(x_{d}[n]+v_{d}[n]-v_{d}[n-1]\right) \bmod 2  \tag{12}\\
& \quad=\left(x_{d}[n]+o_{d}[n]\right) \bmod 2=0 . \tag{13}
\end{align*}
$$

It follows that, in a first-order $s_{d}[n]$ generator,

$$
\begin{equation*}
o_{d}[n]=\left(x_{d}[n]\right) \bmod 2 \tag{14}
\end{equation*}
$$

For a second-order $s_{d}[n]$ generator,

$$
\begin{align*}
& \left(x_{d}[n]+s_{d}[n]\right) \bmod 2  \tag{15}\\
& \quad=\left(x_{d}[n]+v_{d}[n]-2 v_{d}[n-1]+v_{d}[n-2]\right) \bmod 2  \tag{16}\\
& = \\
& \quad\left(x_{d}[n]+o_{d}[n]\right.  \tag{17}\\
& \left.\quad+v_{d}[n-1]+v_{d}[n-2]\right) \bmod 2=0 .
\end{align*}
$$

TABLE I
Naming Convention of Signals in $s_{d}[n]$ Sequence Generator [13]

|  | $v_{d}[n]$ | $\nabla v_{d}[n]$ | $\nabla^{2} v_{d}[n]$ | $\nabla^{3} v_{d}[n]$ |
| :---: | :---: | :---: | :---: | :---: |
| First-Order | $t_{d}[n]$ | $s_{d}[n]$ | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ |
| Second-Order | $u_{d}[n]$ | $t_{d}[n]$ | $s_{d}[n]$ | $\mathrm{N} / \mathrm{A}$ |
| Third-Order | $v_{d}[n]$ | $u_{d}[n]$ | $t_{d}[n]$ | $s_{d}[n]$ |

Therefore, in a second-order $s_{d}[n]$ generator

$$
\begin{equation*}
o_{d}[n]=\left(x_{d}[n]+v_{d}[n-1]+v_{d}[n-2]\right) \bmod 2 \tag{18}
\end{equation*}
$$

In a third-order $s_{d}[n]$ generator,

$$
\begin{align*}
& \left(x_{d}[n]+s_{d}[n]\right) \bmod 2  \tag{19}\\
& \quad=\left(x_{d}[n]+v_{d}[n]-3 v_{d}[n-1]\right. \\
& \left.\quad+3 v_{d}[n-2]-v_{d}[n-3]\right) \bmod 2 \\
& \quad=\left(x_{d}[n]+o_{d}[n]+v_{d}[n-2]+v_{d}[n-3]\right) \bmod 2=0 . \tag{20}
\end{align*}
$$

Thus, for a third-order $s_{d}[n]$ generator,

$$
\begin{equation*}
o_{d}[n]=\left(x_{d}[n]+v_{d}[n-2]+v_{d}[n-3]\right) \bmod 2 \tag{22}
\end{equation*}
$$

Since the generation of $o_{d}[n]$ is carried out by a modulo two operation, the LSBs of the signals involved are sufficient to generate $o_{d}[n]$.

In the literature, the naming of the internal signals of a $s_{d}[n]$ sequence generator differs, depending on its order [10], [12], [13]. This is because the signal of interest within a quantization block when the SR is used as a divider controller is the one that enters the last difference block to generate $s_{d}[n]$. This signal is conventionally denoted $t_{d}[n]$. Table I shows the naming convention for signals within the $s_{d}[n]$ sequence generators of different orders in the literature in reference to the general structure in Fig. 4 [13].

With an appropriate choice of the state transition matrices, the accumulated quantization error of the SR can be immune to a certain order of nonlinear distortion [12], [13]. Furthermore, the low-frequency accumulated quantization error, which corresponds to the low-frequency phase noise contribution when the synthesizer is linear, can be optimized [13].
Due to the complex structure that is required in every single quantization block, an SR divider controller has a much higher hardware cost than a MASH DDSM with the same input word length and noise shaping order. For example, the gate count and area of a 16-bit second-order SR are 12.5 and 6.5 times those of a DDSM with the same input word length and order [19].

## III. MASH-SR ARchitecture

## A. Nested MASH-SR Hybrid

The nested MASH-SR hybrid architecture can be represented by the block diagram in Fig. 5. The $N$-bit binary input $x[n]$ is partitioned into two parts. The $N_{2}$ LSBs of the input


Fig. 5. Schematic of an $N$-bit MASH-SR with $N_{1}$ cascaded quantization blocks and an $N_{2}$-bit MASH DDSM.
comprise the input to the MASH DDSM $x_{M}[n]$. The $N_{1}$ most significant bits (MSBs), represented by $x_{S}[n]$, are combined with the MASH DDSM output $y_{M}[n]$ and the sum is the input to the chain of $N_{1}$ quantization blocks. Denoting the modulus of the SR and the MASH DDSM within the MASH-SR as $M_{1}=2^{N_{1}}$ and $M_{2}=2^{N_{2}}$, respectively, the modulus of the divider controller is $M=M_{1} M_{2}$. The input can be expressed by a weighted sum of the inputs to the MASH DDSM and the SR as

$$
\begin{equation*}
x[n]=x_{M}[n]+M_{2} x_{S}[n] . \tag{23}
\end{equation*}
$$

The phase deviation caused by the divider controller is related to its accumulated quantization error in the analytical model for a fractional- $N$ frequency synthesizer [2]. The accumulated quantization error of a MASH-SR can be expressed as [15]

$$
\begin{equation*}
t[n]=\sum_{m=0}^{n}\left(y[m]-\frac{x[m]}{M}\right)=t_{M}[n]+t_{S}[n] \tag{24}
\end{equation*}
$$

where

$$
\begin{equation*}
t_{M}[n]=\frac{1}{M_{1}} \sum_{m=0}^{n}\left(y_{M}[m]-\frac{x_{M}[m]}{M_{2}}\right) \tag{25}
\end{equation*}
$$

and

$$
\begin{equation*}
t_{S}[n]=\sum_{m=0}^{n} \sum_{d=0}^{N_{1}-1} \frac{1}{2^{N_{1}-d}} s_{d}[m] \tag{26}
\end{equation*}
$$

are the accumulated quantization errors of the MASH DDSM and the SR, respectively. In a local oscillator (LO) application, $x[n]=X$ is a constant and this is assumed in the following analysis. This gives a fractional division ratio of $\alpha=X / M$.

Notice that the contribution of the accumulated quantization error from the MASH DDSM part is scaled by a factor $1 / M_{1}$. As a result, the accumulated quantization error from the SR typically dominates the spectral performance [15]. To achieve a $t[n]$ spectrum that is similar to that of a full SR implementing the same pair of state transition matrices, it is required that the order of the MASH DDSM be greater than or equal to that of the SR [15]. As simulations suggest, with a sufficient number of quantization blocks, the MASH-SR can achieve a similar effect in terms of the suppression of fixed spurs induced by the divider controller, when compared with a MASH DDSM divider controller [15].

## B. Advantages of MASH-SR Hybrid

A MASH-SR hybrid has several benefits over a full SR as a divider controller.

1) Spur Suppression With Less Hardware: Firstly, compared with the MASH DDSM of a similar order, the hybrid can achieve better spur suppression owing to the dominance of the spectral contribution of the SR [15]. Also, compared with a conventional SR, the MASH DDSM in a MASH-SR replaces the front quantization blocks, leading to a significant reduction in hardware. Considering a 20-bit divider controller, the MASH-SR implementation with a 16-bit MASH 1-1-1 DDSM and a 4-bit SR is estimated to require only about $22 \%$ the hardware of a full-length 20 -stage SR [15].
2) Phase Alignment/Adjustment: In modern synthesizer products, phase alignment/adjustment is a preferred function, especially for beam steering applications. Due to the implementation of the divide-by-two function in the SR, it is difficult to set an initial condition accurately to realize the phase adjustment function. Thanks to the MASH DDSM within the MASH-SR hybrid, phase adjustment can be carried out simply by setting the initial condition of the MASH.

When a MASH 1-1-1 DDSM is used in a MASH-SR hybrid, the accumulated quantization error contribution can be expressed as

$$
\begin{equation*}
t_{M}[n]=\frac{1}{M_{1} M_{2}}\left(e_{1}[-1]-e_{3}[n]+2 e_{3}[n-1]-e_{3}[n-2]\right), \tag{27}
\end{equation*}
$$

where $e_{1}[-1]$ is the initial condition of the register in the first stage EFM1. By setting the value of $e_{1}[-1]$, the DC offset of the accumulated quantization error of the MASH-SR can be adjusted. To achieve a change of unity in the DC value of $t[n]$, which corresponds to a phase offset value of $2 \pi$ or $360^{\circ}$, the initial condition should be able to change between 0 and $M_{1} M_{2}$. This range is greater than that of $e_{1}[n]$, which is $\left[0, M_{1}\right)$, implying that the corresponding bus widths in the MASH DDSM and the SR should be increased in order to perform this function.
3) Lower Latency: In the implementation of an SR quantization block, pipelining is typically applied due to the long propagation delay of the chain. This results in a latency that is proportional to the number of quantization blocks of the SR. Using a MASH-SR can decrease the number of SR stages needed; this reduces the delay caused by the quantization blocks compared to a standard SR structure.

## IV. Design of an Optimized MASH-SR Divider Controller

In this section, the design of an optimized 20-bit MASH-SR hybrid divider controller with second-order quantization blocks is presented. For convenience, we consider the signal notations of a second-order $s_{d}[n]$ signal generator as shown in Fig. 6, i.e., the notations in the second row of Table I. Thus,

$$
\begin{equation*}
u_{d}[n] \equiv v_{d}[n], t_{d}[n] \equiv \nabla v_{d}[n], s_{d}[n] \equiv \nabla^{2} v_{d}[n] \tag{28}
\end{equation*}
$$

To ensure the spectral dominance of the SR stages, a thirdorder MASH 1-1-1 DDSM is employed in the MASH-SR; this corresponds to the MASH DDSM in Fig. 2 with $L=3$. The output range of the MASH 1-1-1 is $y_{M}[n] \in[-3,4]$.


Fig. 6. Block diagram of a second-order $s_{d}[n]$ sequence generator.
The quantization error of the SR can be expressed as

$$
\begin{equation*}
s_{S}[n]=\sum_{d=0}^{N_{1}-1} \frac{1}{2^{N_{1}-d}} s_{d}[n] . \tag{29}
\end{equation*}
$$

For $u_{d}[n] \in\left[-N_{u}, N_{u}\right]$, we have $s_{d}[n] \in\left[-4 N_{u}, 4 N_{u}\right]$. The quantization error, which typically dominates the output, has the range $s_{s}[n] \in\left(-4 N_{u}, 4 N_{u}\right)$. For a moderate range of output and a sufficient number of pairs of state transition matrices for optimization, $N_{u}=2$ is chosen in this design. This leads to $5 \times 5 \mathbf{A}_{\mathbf{e}}$ and $\mathbf{A}_{\mathbf{o}}$ matrices.

For the consideration of hardware cost, each quantization block in the SR has a PRNG that generates a 4-bit $r_{d}[n]$ sequence, i.e., $M_{r}=16$ and $r_{d}[n] \in[0,15]$.

## A. Input Split of the Nested-Cascade Structure

As introduced in Sec. III, the MASH-SR exploits the spur immunity of the SR's accumulated quantization error contribution. In order to achieve this, a sufficient number of quantization blocks is needed. As discussed in [15], at least four quantization blocks are needed to ensure spectral separation between the SR contribution and the MASH DDSM-related contributions, in both the linear case and in the presence of a strong nonlinearity. Accordingly, the 20-bit MASH-SR is partitioned into a MASH 1-1-1 DDSM with a 16-bit input and four SR quantization blocks, i.e., $N_{1}=4$ and $N_{2}=16$. In this MASH-SR hybrid, the input to the SR has a range $y_{M}[n]+x_{S}[n] \in[-3,19]$. This, together with the range of SR quantization error of $S_{S}[n] \in(-8,8)$, gives an output range of

$$
\begin{equation*}
y[n]=\frac{y_{M}[n]+x_{S}[n]}{2^{4}}+S_{S}[n] \in[-7,8] . \tag{30}
\end{equation*}
$$

By comparison, the output ranges for a 20-bit MASH 1-1 DDSM and a second-order SR are $[-1,2]$ and $[-7,8]$, respectively.

## B. Finding State Transition Matrices

The state transition matrices can be designed to achieve spur immunity of $t_{S}[n]$ in the presence of nonlinear distortions. Such pairs of state transition matrices are of interest and the SR can be optimized by selecting state transition matrices among these candidates [13]. The quantization error $t_{S}[n]$ can be expressed as a weighted sum of $t_{d}[n]$ :

$$
\begin{equation*}
t_{S}[n]=\sum_{d=0}^{N_{1}-1} \frac{1}{2^{N_{1}-d}} t_{d}[n] \tag{31}
\end{equation*}
$$

with $t_{d}[n]=0$ for $n \leq 0$. Since the combinatorial logic does not directly generate $t_{d}[n]$, transition matrices from $u_{d}[n-1]$ to $t_{d}[n]$ are required and they are defined as [13]

$$
\begin{equation*}
\mathbf{T}_{\mathbf{e}}(i, j)=P\left(t_{d}[n]=\mathbf{t}(j) \mid u_{d}[n-1]=\mathbf{u}(i), o_{d}[n]=0\right) \tag{32}
\end{equation*}
$$

$$
\begin{equation*}
\mathbf{T}_{\mathbf{0}}(i, j)=P\left(t_{d}[n]=\mathbf{t}(j) \mid u_{d}[n-1]=\mathbf{u}(i), o_{d}[n]=1\right) \tag{33}
\end{equation*}
$$

where

$$
\begin{align*}
\mathbf{u} & =\left(-N_{u}-\left(N_{u}-1\right) \ldots N_{u}\right)^{T}  \tag{34}\\
\mathbf{t} & =\left(-2 N_{u}-\left(2 N_{u}-1\right) \ldots 2 N_{u}\right)^{T} \tag{35}
\end{align*}
$$

With (8) and (28), [13]
$\mathbf{T}_{\mathbf{x}}(i, j)$

$$
\begin{cases}\mathbf{A}_{\mathbf{x}}\left(i, i+j-2 N_{u}-1\right), & \text { if } 2 N_{u}+2-i \leq j \text { and }  \tag{36}\\ & j \leq 4 N_{u}+2-i \\ 0, & \text { otherwise }\end{cases}
$$

where $\mathbf{x}=\mathbf{e}$ or $\mathbf{x}=\mathbf{0}$. For $N_{u}=2, \mathbf{T}_{\mathbf{e}}$ and $\mathbf{T}_{\mathbf{0}}$ are $5 \times 9$ matrices.

Consider $t_{S}^{p}[n]$, which is the $t_{S}[n]$ sequence after distortion by a simple $p$ th-order nonlinearity. Two conditions, which are for odd and even order of distortion $p$ respectively, can ensure spurious-free performance for all $p$ less than or equal to an integer $h_{t}$ [13].

Firstly, for spur immunity to odd-order distortion, i.e., odd integer $p$, the $\mathbf{A}_{\mathbf{e}}$ and $\mathbf{A}_{\mathbf{o}}$ matrices are designed to be centrosymmetric, i.e., $\mathbf{A}_{\mathbf{x}}(i, j)=\mathbf{A}_{\mathbf{x}}\left(2 N_{u}+2-i, 2 N_{u}+2-j\right)$ for $\boldsymbol{x}=\boldsymbol{e}$ and $\mathbf{x}=\mathbf{0}$ [12], [13]. Each row of the matrices should have a sufficient number of non-zero terms. As (7) suggests, for a row vector in $\mathbf{A}_{\mathbf{e}}$ and $\mathbf{A}_{\mathbf{0}}$, every other entry is forced to be zero. For the $j$ th row of $\mathbf{A}_{\mathbf{x}}(i, j)$, if $\mathbf{A}_{\mathbf{x}}(i, j)=$ 0 for $i=1,3, \ldots$, then it is termed an even-entries row; if $\mathbf{A}_{\mathbf{x}}(i, j)=0$ for $i=2,4, \ldots$, then it is called an oddentries row. For an odd-entries row, there should be at least $\left\lfloor 1+\left(N_{u}+1\right) / 2\right\rfloor=2$ non-zero entries. For an even-entries row, there should be at least $\left\lfloor 1+N_{u} / 2\right\rfloor=2$ non-zero entries.

To ensure that the periodogram of $t_{S}^{p}[n]$ is immune to spurious tones for all even positive integer $p \leq h_{t}$, it is required that [10], [12], [13]

$$
\begin{align*}
\mathbf{A}_{\mathbf{e}} \mathbf{T}_{\mathbf{e}} \mathbf{t}^{(p)} & =\mathbf{A}_{\mathbf{e}} \mathbf{T}_{\mathbf{0}} \mathbf{t}^{(p)} \\
& =\mathbf{A}_{\mathbf{0}} \mathbf{T}_{\mathbf{e}} \mathbf{t}^{(p)}=\mathbf{A}_{\mathbf{0}} \mathbf{T}_{\mathbf{0}} \mathbf{t}^{(p)}=c_{p} \mathbf{1}_{2 N_{u}+1} \tag{37}
\end{align*}
$$

where $c_{p}$ is a constant, $\mathbf{1}_{2 N_{u}+1}$ is a vector of ones which has a length $\left(2 N_{u}+1\right)$, and

$$
\begin{equation*}
\mathbf{t}^{(p)}=\left(\left(-2 N_{u}\right)^{p}\left(-2 N_{u}+1\right)^{p} \ldots\left(2 N_{u}\right)^{p}\right)^{T} \tag{38}
\end{equation*}
$$

With the requirement for odd-order $t_{S}[n]$ spur immunity and (7), the $\mathbf{A}_{\mathbf{e}}$ and $\mathbf{A}_{\mathbf{o}}$ are populated with variables as (39), shown at the bottom of the next page.

For different $h_{t}$ values, the number of solutions is different. As proven in [12], the highest order of distortion to which $t_{S}[n]$ can be immune is $h_{t}=\left(4 N_{u}-3\right)=5$. In this case, we require (37) to hold for $p=2$ and $p=4$, given the spur immunity in odd- $p$ cases due to the structures of the $\mathbf{A}_{\mathbf{e}}$
and $\mathbf{A}_{\mathbf{0}}$. Two valid sets of state transition matrices are found using an algebraic equation solver, ${ }^{2}$ namely,

$$
\begin{align*}
\mathbf{A}_{\mathbf{e}} & =\left(\begin{array}{ccccc}
1 / 4 & 0 & 3 / 4 & 0 & 0 \\
0 & 5 / 8 & 0 & 3 / 8 & 0 \\
1 / 8 & 0 & 3 / 4 & 0 & 1 / 8 \\
0 & 3 / 8 & 0 & 5 / 8 & 0 \\
0 & 0 & 3 / 4 & 0 & 1 / 4
\end{array}\right), \\
\mathbf{A}_{\mathbf{o}} & =\left(\begin{array}{ccccc}
0 & 3 / 4 & 0 & 1 / 4 & 0 \\
3 / 16 & 0 & 3 / 4 & 0 & 1 / 16 \\
0 & 1 / 2 & 0 & 1 / 2 & 0 \\
1 / 16 & 0 & 3 / 4 & 0 & 3 / 16 \\
0 & 3 / 4 & 0 & 1 / 4 & 0
\end{array}\right) \tag{40}
\end{align*}
$$

and

$$
\begin{align*}
\mathbf{A}_{\mathbf{e}} & =\left(\begin{array}{ccccc}
3 / 4 & 0 & 1 / 4 & 0 & 0 \\
0 & 5 / 8 & 0 & 3 / 8 & 0 \\
3 / 8 & 0 & 1 / 4 & 0 & 3 / 8 \\
0 & 3 / 8 & 0 & 5 / 8 & 0 \\
0 & 0 & 1 / 4 & 0 & 3 / 4
\end{array}\right), \\
\mathbf{A}_{\mathbf{0}} & =\left(\begin{array}{ccccc}
0 & 11 / 12 & 0 & 1 / 12 & 0 \\
11 / 16 & 0 & 1 / 4 & 0 & 1 / 16 \\
0 & 1 / 2 & 0 & 1 / 2 & 0 \\
1 / 16 & 0 & 1 / 4 & 0 & 11 / 16 \\
0 & 1 / 12 & 0 & 11 / 12 & 0
\end{array}\right) . \tag{41}
\end{align*}
$$

The pair of matrices in (40) was presented in [10], [12], and [13]. Notice that (41) contains probabilities with a denominator of 12 . When quantizing to 4 bits based on the requirement imposed by $r_{d}[n]$, errors will be introduced. The limited number of pairs of $\mathbf{A}_{\mathbf{e}}$ and $\mathbf{A}_{\mathbf{0}}$ when $h_{t}=5$ does not permit efficient optimization.

[^2]In order to increase the number of candidate matrices for selection, we relax the requirement to $h_{t}=3$ and only consider the set of equations with $p=2$. By elimination and substitution, $\mathbf{A}_{\mathbf{e}}$ and $\mathbf{A}_{\mathbf{0}}$ can be represented by just two variables $x_{1}$ and $x_{2}$, as shown in (42) and (43), shown at the bottom of the page. Note that it still has to be ensured that each row of $\mathbf{A}_{\mathbf{e}}$ and $\mathbf{A}_{\mathbf{0}}$ contains at least two non-zero values. For (42) and (43), one can simply let $\mathbf{A}_{\mathbf{e}}(i, j) \in[0,1)$ and $\mathbf{A}_{\mathbf{0}}(i, j) \in[0,1)$ to satisfy this requirement.

Notice that $x_{1}$ and $x_{2}$ appear alone as entries in (42) and (43), respectively. To find valid state transition matrices, a brute-force search with a step size of $1 / M_{r}=1 / 16$ in $x_{1}$ and $x_{2}$ is performed. A thorough search can be conducted by applying the ranges $x_{1} \in[0,15 / 16]$ and $x_{2} \in[0,15 / 16]$. In total, 56 valid pairs of matrices are found. It should be noted that entries may not be integer multiples of $1 / 16$ in these matrices, e.g., $\mathbf{A}_{\mathbf{e}}(1,1)$ in (42). Further rounding may be needed in order to implement some of the matrices.

## C. Calculation of $t_{S}[n]$ Distribution

With a given pair of state transition matrices, the distribution of $t_{d}[n]$ can be estimated. Knowing the distribution of $t_{d}[n]$, the distribution of $t_{S}[n]$ can then be estimated.

Since $t_{d}[n]$ is the first-order difference of the $u_{d}[n]$ sequence in a second-order $s_{d}[n]$ generator, we consider the distribution of $u_{d}[n]$ first. The current state $u_{d}[n]$ is a function of the parity sequence $\left\{o_{d}[m], m=0,1, \ldots, n\right\}$, the pseudo-random sequence $\left\{r_{d}[m], m=0,1, \ldots, n\right\}$, and its initial condition $u_{d}[-1]$, which is assumed zero. As introduced in Sec. II, $r_{d}[n]$ and $r_{(d+\Delta)}[n]$ are independent sequences with $\Delta \neq 0$. Thus, $u_{d}[n]$ and $u_{(d+\Delta)}[n]$ are conditioned on independent

$$
\begin{align*}
\mathbf{A}_{\mathbf{e}} & =\left(\begin{array}{ccccc}
x_{e 1} & 0 & x_{e 2} & 0 & 1-x_{e 1}-x_{e 2} \\
0 & x_{e 3} & 0 & 1-x_{e 3} & 0 \\
x_{e 4} & 0 & 1-2 x_{e 4} & 0 & x_{e 4} \\
0 & 1-x_{e 3} & 0 & x_{e 3} & 0 \\
1-x_{e 1}-x_{e 2} & 0 & x_{e 2} & 0 & x_{e 1} \\
0 & x_{o 1} & 0 & 1-x_{o 1} & 0 \\
x_{o 2} & 0 & x_{o 3} & 0 & 1-x_{o 2}-x_{o 3} \\
0 & 1 / 2 & 0 & 1 / 2 & 0 \\
\mathbf{A}_{\mathbf{o}} & =\left(\begin{array}{ccccc} 
\\
1-x_{o 2}-x_{o 3} & 0 & x_{o 3} & 0 & x_{o 2} \\
0 & 1-x_{o 1} & 0 & x_{o 1} & 0
\end{array}\right)
\end{array},\right.
\end{align*}
$$

$$
\begin{align*}
& \mathbf{A}_{\mathbf{e}}=\left(\begin{array}{ccccc}
-\frac{8 x_{1}^{2}-16 x_{1}+8 x_{2}+7}{16\left(x_{1}-1\right)} & 0 & x_{1} & 0 & \frac{-8 x_{1}^{2}+16 x_{1}+8 x_{2}-9}{16\left(x_{1}-1\right)} \\
0 & 2 x_{1}+2 x_{2}-\frac{5}{4} & 0 & \frac{9}{4}-2 x_{2}-2 x_{1} & 0 \\
\frac{1}{2}-\frac{x_{1}}{2} & 0 & x_{1} & 0 & \frac{1}{2}-\frac{x_{1}}{2} \\
0 & \frac{9}{4}-2 x_{2}-2 x_{1} & 0 & 2 x_{1}+2 x_{2}-\frac{5}{4} & 0 \\
\frac{-8 x_{1}^{2}+16 x_{1}+8 x_{2}-9}{16\left(x_{1}-1\right)} & 0 & x_{1} & 0 & -\frac{8 x_{1}^{2}-16 x_{1}+8 x_{2}+7}{16\left(x_{1}-1\right)}
\end{array}\right),  \tag{42}\\
& 0 \tag{43}
\end{align*}
$$



Fig. 7. Estimated and simulated distribution of $t_{3}[n]$ and $t_{S}[n]$ of the SR within a 20-bit MASH-SR with a 16-bit MASH 1-1-1 and a 4-bit SR. State transition matrices in (40) are used.
sequences $\left\{r_{d}[m], m=0,1, \ldots, n\right\}$ and $\left\{r_{(d+\Delta)}[m], m=\right.$ $0,1, \ldots, n\}$. Since the value of $o_{d}[n]$ is partly determined by the quantization block input $x_{d}[n], u_{d}[n]$ and $u_{(d+\Delta)}[n]$ are not strictly independent; this imposes constraints on the analysis of the $t_{S}[n]$ distribution.

For a full SR structure, due to the constant input in the LO application, the $u_{d}[n]$ distributions are affected by the input $x[n]=X$ or the output of the preceding stage. However, in a MASH-SR, the input to the SR quantization blocks comprises two parts, namely the MASH DDSM output $y_{M}[n]$ and the MSBs of the input. The output $y_{M}[n]$ contains a high-pass shaped quantization error; as the result, the input of the SR is not constant. This gives alternating parities for all $x_{d}[n]$. Therefore, in the following analysis, it is assumed that the $o_{d}[n]$ sequence is a balanced 1-bit sequence with equal probabilities of zeros and ones with $\left\{o_{d}[n], \quad n=\right.$ $0,1, \ldots\}$ and $\left\{o_{(d+\Delta)}[n], \quad n=0,1, \ldots\right\}$ being statistically independent when $\Delta \neq 0$. Hence, $\left\{u_{d}[n], n=0,1, \ldots\right\}$ and its difference sequence $\left\{t_{d}[n], n=0,1, \ldots\right\}$ are independent of $\left\{u_{(d+\Delta)}[n], n=0,1, \ldots\right\}$ and $\left\{t_{(d+\Delta)}[n], n=0,1, \ldots\right\}$ when $\Delta \neq 0$ under this assumption, respectively.
The distribution of $u_{d}[n]$ is first estimated. Since the $o_{d}[n]$ sequence is assumed to have equal probabilities of zeros and ones, $P\left(o_{d}[n]=0\right)=P\left(o_{d}[n]=1\right)=0.5$. The overall state transition matrix A can be defined as [13]

$$
\begin{align*}
\mathbf{A}(i, j)= & P\left(u_{d}[n]=\mathbf{u}(j) \mid u_{d}[n-1]=\mathbf{u}(i)\right) \\
= & P\left(u_{d}[n]=\mathbf{u}(j) \mid u_{d}[n-1]=\mathbf{u}(i), o_{d}[n]=0\right) \\
& \times P\left(o_{d}[n]=0\right)+ \\
P\left(u_{d}[n]=\right. & \left.\mathbf{u}(j) \mid u_{d}[n-1]=\mathbf{u}(i), o_{d}[n]=1\right) P\left(o_{d}[n]=1\right) \\
= & \frac{\mathbf{A}_{\mathbf{e}}(i, j)+\mathbf{A}_{\mathbf{o}}(i, j)}{2} . \tag{44}
\end{align*}
$$

This definition implies that $\mathbf{A}$ is stochastic. The vector of stationary probabilities of the discrete-valued Markov random sequence $u_{d}[n]$, denoted $\mathbf{p}_{\mathbf{u}}$, can be found by solving

$$
\begin{equation*}
\mathbf{p}_{\mathbf{u}} \mathbf{A}=\mathbf{p}_{\mathbf{u}} \tag{45}
\end{equation*}
$$

Here $\mathbf{p}_{\mathbf{u}}(i)=P\left(u_{d}[n-1]=\mathbf{u}(i)\right)=P\left(u_{d}[n]=\mathbf{u}(i)\right)$. Similarly, the overall state transition matrix from $u_{d}[n-1]$ to
$t_{d}[n]$ can be defined as

$$
\begin{align*}
\mathbf{T}(i, j) & =P\left(t_{d}[n]=\mathbf{t}(j) \mid u_{d}[n-1]=\mathbf{u}(i)\right) \\
& =\frac{\mathbf{T}_{\mathbf{e}}(i, j)+\mathbf{T}_{\mathbf{0}}(i, j)}{2} \tag{46}
\end{align*}
$$

The probability distribution for $t_{d}[n]$, which is denoted $\mathbf{p}_{\mathbf{t}}$, can be evaluated by solving

$$
\begin{equation*}
\mathbf{p}_{\mathbf{t}}=\mathbf{p}_{\mathbf{u}} \mathbf{T} \tag{47}
\end{equation*}
$$

By definition, $\mathbf{p}_{\mathbf{t}}(i)=P\left(t_{d}[n]=\mathfrak{t}(i)\right)$.
Under the assumption that $t_{d}[n]$ of different stages are independent, the distribution of the output accumulated quantization error of the $\mathrm{SR} t_{S}[n]$ can be computed by the method described in Appendix A, based on (31). The probability vector $\mathbf{P}_{\text {tout }}$ for $t_{S}[n]$ can be expressed as

$$
\begin{array}{r}
\mathbf{P}_{\text {tout }}(i)=P\left(t_{S}[n]=-2 N_{u}\left(\frac{M_{1}-1}{M_{1}}\right)+\frac{i-1}{M_{1}}\right) \\
i \in\left[1,4\left(M_{1}-1\right) N_{u}+1\right] . \tag{48}
\end{array}
$$

Fig. 7 shows the estimated probability distributions for $t_{d}[n]$ $(d=3)$ and $t_{S}[n]$ and the simulation results of the 4-bit SR within the 20-bit MASH-SR. The estimated distributions match well with the simulation results.

## D. Spectra of $t_{d}[n]$ and $t_{S}[n]$

The spectral contribution of $t_{S}[n]$ dominates the accumulated quantization error of the divider controller. As (31) suggests, the $t_{d}[n]$ signals from quantization blocks, which are assumed to be independent, contribute to the $t_{S}[n]$ spectrum. Therefore, the spectrum of $t_{d}[n]$ is estimated first.

The power spectral density of the $u_{d}[n]$ is computed as

$$
\begin{equation*}
S_{u_{d}}(F)=\lim _{L \rightarrow \infty} \mathbf{E}\left(\sum_{m=-L+1}^{L-1} R_{u u, L}[m] e^{-j 2 \pi F m}\right) \tag{49}
\end{equation*}
$$

where $F=k / L, k=0,1, \ldots, L-1$ and

$$
\begin{equation*}
R_{u u, L}[m]=\frac{1}{L} \sum_{n=0}^{L-1} u_{d}[n] u_{d}[n+m] \tag{50}
\end{equation*}
$$



Fig. 8. Estimated (green) and simulated spectra of $u_{3}[n], t_{3}[n]$, and $t_{S}[n]$ of the SR within a 20 -bit MASH-SR with a 16 -bit MASH 1-1-1 and a 4-bit SR. State transition matrices in (40) are used.
is the autocorrelation of $u_{d}[n]$ and $L$ is the length of $u_{d}[n]$ sequence. Thus, $u_{d}[n]=0$ when $n<0$ and $n>L-1$. Furthermore, the limit for $\mathbf{E}\left(R_{u u, L}[k]\right)$ as $L \rightarrow \infty$ is [13]

$$
\begin{align*}
R_{u u}[m] & =\lim _{L \rightarrow \infty} \mathbf{E}\left(R_{u u, L}[m]\right)=\mathbf{E}\left(u_{d}[n] u_{d}[n+m]\right) \\
& =\sum_{l=1}^{2 N_{u}+1}\left(\mathbf{A}^{|m|} \mathbf{u}\right)(l) \cdot \mathbf{u}(l) \cdot \mathbf{p}_{\mathbf{u}}(l) \tag{51}
\end{align*}
$$

This gives

$$
\begin{align*}
S_{u_{d}}(F) & =\lim _{L \rightarrow \infty} \sum_{m=-L+1}^{L-1}\left(\lim _{L \rightarrow \infty} \mathbf{E}\left(R_{u u, L}[m]\right)\right) e^{-j 2 \pi F m} \\
& =\lim _{L \rightarrow \infty} \sum_{m=-L+1}^{L-1} R_{u u}[m] e^{-j 2 \pi F m} \tag{52}
\end{align*}
$$

Practically, a finite sequence length $L$ is used to estimate $S_{u_{d}}(k / L)$ :

$$
\begin{align*}
S_{u_{d}, L}\left(\frac{k}{L}\right)= & \sum_{m=-L+1}^{L-1} R_{u u}[m] e^{\frac{-j 2 \pi k m}{L}} \\
= & \sum_{m=-L+1}^{L-1}\left(\sum_{l=1}^{2 N_{u}+1}\left(\mathbf{A}^{|m|} \mathbf{u}\right)(l) \cdot \mathbf{u}(l) \cdot \mathbf{p}_{\mathbf{u}}(l)\right) \\
& \times e^{\frac{-j 2 \pi k m}{L}} \tag{53}
\end{align*}
$$

Since $u_{d}[n]$ is a Markov process that has a stationary distribution, the autocorrelation of $u_{d}[n]$ typically decreases in amplitude with the absolute value of the lag $m$. Therefore, $R_{u u}[m]$ can be approximated by an impulse at $m=0$ and the spectrum $S_{u_{d}}(F)$ can be approximated by white noise.

The spectrum of $t_{d}[n]$ can then be estimated by

$$
\begin{equation*}
S_{t_{d}, L}\left(\frac{k}{L}\right)=\left|1-e^{\frac{-j 2 \pi k}{L}}\right|^{2} S_{u_{d}, L}\left(\frac{k}{L}\right) \tag{54}
\end{equation*}
$$

Under the assumption that $t_{d}[n]$ sequences from different quantization blocks are independent, the cross-correlation between the $t_{d}[n]$ and $t_{(d+\Delta)}[n]$ is zero for $\Delta \neq 0$. The power spectral density for $t_{S}[n]$ can be estimated by

$$
\begin{equation*}
S_{t_{S}, L}\left(\frac{k}{L}\right)=\left(\sum_{d=0}^{N_{1}-1}\left(\frac{1}{2^{\left(N_{1}-d\right)}}\right)^{2}\right) S_{t_{d}, L}\left(\frac{k}{L}\right) \tag{55}
\end{equation*}
$$

In this particular design with $N_{1}=4$, the spectral contribution from $t_{S}[n]$ dominates the spectrum of $t[n]$,

$$
\begin{equation*}
S_{t, L}\left(\frac{k}{L}\right) \approx S_{t S}, L\left(\frac{k}{L}\right) \tag{56}
\end{equation*}
$$

Since a MASH 1-1-1 is employed in this MASH-SR design, first-order shaped LSB dither can be applied to it, which will lead to a flat spectral contribution of low amplitude at low frequencies in the $t[n]$ spectrum.

Examples of simulated and estimated spectra of $u_{d}[n], t_{d}[n]$, and $t_{S}[n]$ of the 4 -bit SR within the 20 -bit MASH-SR are shown in Fig. 8. The estimates (53), (54), and (55) can provide good predictions for the simulated spectra.

## E. Optimization of the SR Stages

In the linear case, the contribution of the SR to $t[n]$ is dominant, as (56) suggests. When a nonlinearity is present, the $t_{S}[n]$ related spectrum is expected to have a significant impact on the overall spectral performance. Consider a memoryless nonlinearity that can be approximated by a polynomial. The distorted $t[n]$ of the MASH-SR can be written as

$$
\begin{align*}
t^{N L}[n] & =\mathcal{N} \mathcal{L}(t[n])=\sum_{k=0}^{p} C_{k}(t[n])^{k} \\
& =\mathcal{N} \mathcal{L}\left(t_{S}[n]\right)+\mathcal{N} \mathcal{L}\left(t_{M}[n]\right)+r_{c}[n] \tag{57}
\end{align*}
$$

where $r_{c}[n]$ contains the cross terms. In the MASH-SR with at least four SR stages, the amplitude of $t_{S}[n]$ is significantly larger than that of $t_{M}[n]$. The autocorrelation of $\mathcal{N} \mathcal{L}\left(t_{S}[n]\right)$ is therefore a significant contribution to the autocorrelation of $t^{N L}[n]$, yielding a major spectral component associated with it. Optimizing the performance of $t_{S}[n]$ can hence improve the overall spectral performance of the MASH-SR hybrid.

With the valid state transition matrices found under the constraint $h_{t}=3$, the distributions as well as the spectra of $t_{d}[n]$ and $t_{S}[n]$ can be estimated when each pair of state transition matrices is applied. The SR stages are optimized by selecting the state transition matrices based on consideration of the performance in terms of spurs and noise.

The first aspect of the optimization is the distribution of $t_{d}[n]$ and $t_{S}[n]$. The range of $t_{S}[n]$ affects the potential immunity of the SR contribution to nonlinear distortion. The maximum order of nonlinear distortion to which $t_{S}[n]$ can be


Fig. 9. Estimated criteria for candidate state transition matrices: (a) $\operatorname{Var}\left(t_{d}[n]\right)$, (b) $\operatorname{Kurt}\left(t_{S}[n]\right)$ calculated from (58), (c) $C_{L F N}$ defined in (59), and (d) $C_{H F N}$ given in (60).
immune is related to its range [20]. However, $t_{S}[n]$ with the same range but different distributions can behave differently in the presence of nonlinear distortion. With a given length of the $t_{S}[n]$ sequence, the $t_{S}[n]$ with a distribution that has probabilities concentrated around zero will appear to have a lower range. This leads to a direct degradation of the performance in terms of spurs. Therefore, instead of selecting the state transition matrices for the range of $t_{S}[n]$, the variance of $t_{S}[n]$ is chosen as one of the criteria for optimization. Since $t_{d}[n]$ of different quantization blocks are assumed independent, (31) indicates that the ratio between the variances of $t_{d}[n]$ and $t_{S}[n]$ is a constant. This means that the variance of $t_{d}[n]$ can be used as a criterion without computing that of $t_{S}[n]$. Specifically, matrices giving larger variances of $t_{d}[n]$ and $t_{S}[n]$ are preferred.

The estimated variances of $t_{d}[n]$ for the valid state transition matrices, which are indexed based on the order in which they are found in the brute-force search, are shown in Fig. 9(a). Note that different pairs of matrices can lead to identical variances of $t_{d}[n]$ and $t_{S}[n]$. To have an identical variance, the distribution could have high probabilities for $t_{S}[n]$ values with small absolute values; alternatively, the probabilities for all values are more evenly distributed, which results in higher probabilities for $t_{S}[n]$ values with large absolute values. Fig. 10 shows the $t_{d}[n]$ and $t_{S}[n]$ distributions given by the pairs of matrices indexed 1 and 38, which both lead to $\operatorname{Var}\left(t_{d}[n]\right)=3.5$; they are examples of the two kinds. Therefore, the kurtosis of the $t_{S}[n]$ distribution is used as another criterion for the distribution. It is defined as

$$
\begin{equation*}
\operatorname{Kurt}\left(t_{S}[n]\right)=\frac{\mathbf{E}\left(\left(t_{S}[n]-\mathbf{E}\left(t_{S}[n]\right)\right)^{4}\right)}{\left(\operatorname{Var}\left(t_{S}[n]\right)\right)^{2}} . \tag{58}
\end{equation*}
$$



Fig. 10. Estimates of $t_{d}[n]$ and $t_{S}[n]$ distributions of the pairs state transition matrices with index 1 and 38 that give $\operatorname{Var}\left(t_{d}[n]\right)=3.5$.


Fig. 11. Simulated histograms of $t[n]$ of a MASH 1-1 and a MASH 1-1-1.
A $t_{S}[n]$ distribution with a low kurtosis value is less tailed and therefore tends to have more evenly distributed probabilities for $t_{S}[n]$ values. Such a distribution is hence preferred.

Typically, a lower-order MASH DDSM has a narrow range and the distribution of the accumulated quantization error with high probabilities for values with small absolute values. In contrast, a higher-order MASH DDSM has a wider distribution of the accumulated quantization error with higher probabilities for values with larger absolute values. Example $t[n]$ histograms of a MASH 1-1 and a MASH 1-1-1 DDSM are shown in Fig. 11. As the order of the MASH DDSM increases, the spur performance is improved. By selecting matrices based on the values of $\operatorname{Var}\left(t_{S}[n]\right)$ and $\operatorname{Kurt}\left(t_{S}[n]\right)$, the $t_{S}[n]$ can emulate the higher-order MASH DDSM in terms of its distribution.

Furthermore, the spectral traits of $t_{S}[n]$ will provide other criteria for optimization. The $t_{S}[n]$ spectral amplitude at low-frequencies is a concern since it determines the envelope of $t_{S}[n]$, given the white noise assumption for $S_{u_{d}}(F)$. Equation (54) suggests that, at a given frequency, the estimated amplitude of the spectrum of the $S_{t_{d}, L}(F)$ can be related to $S_{u_{d}, L}(F)$ by a fixed factor. The low-frequency noise of $S_{t_{d}, L}(F)$ can therefore be characterized by the criterion [13]

$$
\begin{equation*}
C_{L F N}=S_{u_{d}, L}(0) \tag{59}
\end{equation*}
$$

Also, the high-frequency noise of $t_{S}[n]$, which can be related to the noise floor due to folding [6], is considered as another criterion for the SR and it is defined as the amplitude of the spectrum around 0.5 normalized frequency, i.e.,

$$
\begin{equation*}
C_{H F N}=S_{u_{d}, L}\left(\frac{1}{2}\right) \tag{60}
\end{equation*}
$$

In this work, a $t_{S}[n]$ distribution which leads to better potential performance regarding spurs is preferred. According to the analysis presented, $t_{S}[n]$ distribution with a large variance and low kurtosis is desirable. Among the pairs of matrices that lead to similar $t_{S}[n]$ distribution, lower $t_{S}[n]$ power spectral density


Fig. 12. Figures of merit calculated using (61) for the candidate matrices.
at low frequencies is favored since it allows lower phase noise contribution from the divider controller around the synthesizer bandwidth. Therefore, the figure of merit used to select the valid candidate matrices is defined as

$$
\begin{equation*}
F o M=\frac{\operatorname{Var}\left(t_{d}[n]\right)}{\operatorname{Kurt}\left(t_{S}[n]\right) C_{L F N}} \tag{61}
\end{equation*}
$$

Values of the figure of merit for all candidate matrices are shown in Fig. 12. The matrices indexed 46, which are

$$
\begin{align*}
\mathbf{A}_{\mathbf{e}} & =\left(\begin{array}{ccccc}
5 / 48 & 0 & 5 / 8 & 0 & 13 / 48 \\
0 & 1 / 8 & 0 & 7 / 8 & 0 \\
3 / 16 & 0 & 5 / 8 & 0 & 3 / 16 \\
0 & 7 / 8 & 0 & 1 / 8 & 0 \\
13 / 48 & 0 & 5 / 8 & 0 & 5 / 48
\end{array}\right), \\
\mathbf{A}_{\mathbf{o}} & =\left(\begin{array}{ccccc}
0 & 1 / 6 & 0 & 5 / 6 & 0 \\
1 / 16 & 0 & 5 / 8 & 0 & 5 / 16 \\
0 & 1 / 2 & 0 & 1 / 2 & 0 \\
5 / 16 & 0 & 5 / 8 & 0 & 1 / 16 \\
0 & 5 / 6 & 0 & 1 / 6 & 0
\end{array}\right), \tag{62}
\end{align*}
$$

yield the highest value of this figure of merit. In order to implement the probabilities with a 4-bit pseudo-random number, the matrices are rounded as

$$
\begin{align*}
\mathbf{A}_{\mathbf{e}} & =\left(\begin{array}{ccccc}
1 / 8 & 0 & 5 / 8 & 0 & 1 / 4 \\
0 & 1 / 8 & 0 & 7 / 8 & 0 \\
3 / 16 & 0 & 5 / 8 & 0 & 3 / 16 \\
0 & 7 / 8 & 0 & 1 / 8 & 0 \\
1 / 4 & 0 & 5 / 8 & 0 & 1 / 8
\end{array}\right), \\
\mathbf{A}_{\mathbf{0}} & =\left(\begin{array}{ccccc}
0 & 3 / 16 & 0 & 13 / 16 & 0 \\
1 / 16 & 0 & 5 / 8 & 0 & 5 / 16 \\
0 & 1 / 2 & 0 & 1 / 2 & 0 \\
5 / 16 & 0 & 5 / 8 & 0 & 1 / 16 \\
0 & 5 / 6 & 0 & 1 / 6 & 0
\end{array}\right), \tag{63}
\end{align*}
$$

Notice that this pair of matrices leads to the highest highfrequency noise, as shown in Fig. 9(d). The power spectral density of $t_{S}[n]$ around the Nyquist frequency can be related to the noise floor caused by folding in the presence of nonlinearity [6]. Therefore, the selected state transition matrices may incur high nonlinearity-induced in-band noise.

## V. Comparison of Simulated Performance

In this section, the simulated performances of the MASH-SR with the optimized state transition matrices and


Fig. 13. The $t[n]$ spectra of a MASH 1-1 DDSM, a MASH 1-1-1 DDSM, and MASH-SR with state transition matrices with index 5 and index 46.
its counterparts are presented. For the purpose of comparison, the matrices giving the minimum figure of merit, which are indexed 5, namely

$$
\begin{align*}
\mathbf{A}_{\mathbf{e}} & =\left(\begin{array}{ccccc}
29 / 32 & 0 & 0 & 0 & 3 / 32 \\
0 & 5 / 8 & 0 & 3 / 8 & 0 \\
1 / 2 & 0 & 0 & 0 & 1 / 2 \\
0 & 3 / 8 & 0 & 5 / 8 & 0 \\
3 / 32 & 0 & 0 & 0 & 29 / 32
\end{array}\right), \\
\mathbf{A}_{\mathbf{0}} & =\left(\begin{array}{ccccc}
0 & 15 / 16 & 0 & 1 / 16 & 0 \\
15 / 16 & 0 & 0 & 0 & 1 / 16 \\
0 & 1 / 2 & 0 & 1 / 2 & 0 \\
1 / 16 & 0 & 0 & 0 & 15 / 16 \\
0 & 1 / 16 & 0 & 15 / 16 & 0
\end{array}\right), \tag{64}
\end{align*}
$$

are also considered. To permit the use of a 4-bit $r_{d}[n]$, the $\mathbf{A}_{\mathbf{e}}$ matrix is rounded to

$$
\mathbf{A}_{\mathbf{e}}=\left(\begin{array}{ccccc}
15 / 16 & 0 & 0 & 0 & 1 / 16  \tag{65}\\
0 & 5 / 8 & 0 & 3 / 8 & 0 \\
1 / 2 & 0 & 0 & 0 & 1 / 2 \\
0 & 3 / 8 & 0 & 5 / 8 & 0 \\
1 / 16 & 0 & 0 & 0 & 15 / 16
\end{array}\right)
$$

A 20-bit second-order $\operatorname{SR}$ in [13] implementing state transition matrices quantized for a 10 -bit $r_{d}[n]$

$$
\begin{align*}
\mathbf{A}_{\mathbf{e}} & =\left(\begin{array}{ccccc}
0 & 0 & \frac{333}{512} & 0 & \frac{179}{512} \\
0 & \frac{7}{128} & 0 & \frac{121}{128} & 0 \\
\frac{179}{1024} & 0 & \frac{333}{512} & 0 & \frac{179}{1024} \\
0 & \frac{121}{128} & 0 & \frac{7}{128} & 0 \\
\frac{179}{512} & 0 & \frac{333}{512} & 0 & 0
\end{array}\right) \\
\mathbf{A}_{\mathbf{o}} & =\left(\begin{array}{ccccc}
0 & \frac{7}{1024} & 0 & \frac{1017}{1024} & 0 \\
\frac{1}{512} & 0 & \frac{333}{512} & 0 & \frac{89}{256} \\
0 & \frac{1}{2} & 0 & \frac{1}{2} & 0 \\
\frac{89}{256} & 0 & \frac{333}{512} & 0 & \frac{1}{512} \\
0 & \frac{1017}{1024} & 0 & \frac{7}{1024} & 0
\end{array}\right) \tag{66}
\end{align*}
$$

is also simulated as a reference.

## A. Spectra of $t[n]$

The spectra of $t[n]$ of a MASH 1-1 DDSM, MASH 1-1-1 DDSM, and MASH-SR with matrices index 5 and 46 are show in Fig. 13. The MASH-SR with state transition matrices indexed 5 has high low-frequency noise in comparison to the other architectures. The $t[n]$ spectrum of the MASH-SR


Fig. 14. The spectra when $t_{A C}[n]$ of MASH 1-1, MASH 1-1-1, and MASH-SR with state transition matrices indexed 5 and 46 experience third-order distortion, a PWL nonlinearity with $1 \%$ mismatch, and a PWL nonlinearity with $8 \%$ mismatch.
with matrices indexed 46 is about 3.8 dB higher than that of a MASH 1-1 at mid and low frequencies. Comparing the case where matrices with index 5 are applied, the optimized MASH-SR has a low-frequency $t[n]$ power spectral density that is about 14.5 dB lower. Notice the $-20 \mathrm{~dB} /$ decade spectral contribution of the zeroth-order shaped LSB dither at very low frequencies in the spectrum of the MASH 1-1. The MASH-SR with matrices indexed 46 has the highest power spectral density around the 0.5 normalized frequency, even higher than that of the third-order MASH 1-1-1.

## B. Spectra of $t[n]$ in the Presence of Nonlinear Distortions

Next, we consider $t[n]$ in the presence of nonlinear distortions. It should be noted that the $t[n]$ of a MASH DDSM and MASH-SR will contain a DC component as the effect of the initial condition. In a practical synthesizer, the DC component will have no effect or only affect the local nonlinearity with which the phase deviation caused by the divide controller interacts [5]. To avoid the extra effect of the DC component, the nonlinearity consider is only applied to the AC component of $t[n]$, which is

$$
\begin{equation*}
t_{A C}[n]=t[n]-\mathbf{E}(t[n]) \approx t[n]-\frac{1}{n+1} \sum_{m=0}^{n} t[m] \tag{67}
\end{equation*}
$$

The range $t_{A C}[n]$ of the MASH-SRs is $(-3.875,3.875)$. For the full $\mathrm{SR}, t_{A C}[n] \in(-4,4)$. The ranges of $t_{A C}[n]$ of the MASH $1-1$ and the MASH $1-1-1$ are $(-1,1)$ and $(-2,2)$, respectively.

Two types of nonlinearities are considered in the simulations. Since the optimized state transition matrices were selected from those that are immune to third-order distortion, spectra of $t_{A C}^{3}[n]$ for all divider controllers are presented. The mismatch of charge pump current sources generally exists and the transfer characteristic of a PFD/CP can be modeled
by a piecewise-linear (PWL) nonlinearity [4]. To represent minor and severe nonlinearity, mismatches of $1 \%$ and $8 \%$ are considered. The simulated PWL nonlinearity can be expressed by

$$
\begin{equation*}
t_{A C}^{N L}[n]=t_{A C}[n]+\frac{\epsilon}{2}\left|t_{A C}[n]\right| \tag{68}
\end{equation*}
$$

where $\epsilon$ is the mismatch and $t_{A C}^{N L}[n]$ is the nonlinearly distorted $t_{A C}[n]$. Fig. 14 shows the nonlinearly distorted $t_{A C}[n]$ spectra.

In the presence of a third-order nonlinear distortion, the second and third-order MASH DDSM both lead to obvious spurs. In contrast, the MASH-SR hybrid with matrices indexed 5 shows a spur with low amplitude due to the rounding error of the matrix, while the MASH-SR with matrices indexed 46 does not shown any obvious spurs. When a PWL nonlinearity with $1 \%$ mismatch is present, the MASH-SR with matrices indexed 46 leads to a most significant spur that is more than 15 and 3 dB lower than those induced by a MASH $1-1$ and MASH 1-1-1 respectively, with no harmonic spurs observed. Compared with the MASH-SR hybrid with matrices indexed 5, the application of optimized matrices indexed 46 reduces the most significant spur by about 10 dB . When the mismatch of the PWL nonlinearity is increased to $8 \%$, the spur reduction observed in the $1 \%$ case is preserved. The noise floor introduced by the MASH-SR with matrices indexed 46 increases by about 18 dB as the mismatch is increased. In the presence of the PWL nonlinearity of $1 \%$ and $8 \%$ mismatches, the optimized MASH-SR has a noise floor that is about 3.8 dB higher that that of a MASH 1-1-1 DDSM. Comparing with the standard 20-bit SR , the spur performance of the MASH-SR is not compromised. Due to a lower power spectral density around 0.5 normalized frequency, the noise floor caused by the MASH-SR is about 1.5 dB lower that of the SR .


Fig. 15. Simulated synthesizer output phase noise spectra (blue) when a MASH $1-1$, a MASH $1-1-1$, SR, and a MASH-SR with the optimized state transition matrices (index 46) is employed, respectively. Output phase noise contribution from the divider controller (red) is overlapped on top. Divider controllers are 20 -bit and the input is $X=605$. Square markers highlight the overlapped spurs in the output phase noise spectra.

## C. Fractional-N Mode Fixed Spurs

The spur performance of the optimized MASH-SR divider controller and its counterparts was simulated using a closed-loop behavioral model [15], [21]. A Type-II synthesizer with a third-order loop filter has the parameters listed in Table II has been simulated and results are shown in Fig. 15 [13].

When the MASH 1-1 is used in the synthesizer, a primary integer boundary spur of -49 dBc and harmonic tones of -61 and -68 dBc are observed in the output phase noise spectrum. The integer boundary spur is reduced to -62 dBc with an insignificant harmonic spur at -70 dBc when a MASH $1-1-1$ is employed. When an optimized MASH-SR is applied, the corresponding integer boundary spur is -65 dBc , with no apparent harmonic tones; this spur performance is equivalent to that of the full 20 -bit SR in the simulation. Simulations indicate that MASH-SR divider controller will cause a higher noise floor compared to its MASH DDSM counterparts. Hence, in a wideband synthesizer whose in-band noise is significantly affected by the output phase noise contribution from the MASH-SR divider controller, appropriate linearization techniques should be applied to obtain the optimum spectral performance.

## D. Wandering Spurs

Wandering spurs is a time-varying phenomenon observed in the short-term output spectrum of a DDSM-based fractional- $N$ frequency synthesizer [22], [23]. Wandering spurs arise from the double accumulation of a constant in the DDSM-based divider controller [21].

Since the SR quantization block does not perform accumulation, the quantization error of a SR is free of wandering spurs. The dominance of the noise contribution of the SR quantization blocks in the proposed MASH-SR divider controller


Fig. 16. Spectrograms of $t_{A C}[n]$ of 20-bit MASH 1-1-1 DDSM and the optimized MASH-SR with state transition matrices index 46 in the presence of PWL nonlinearity with $8 \%$ mismatch when input $X=1$.

TABLE II
Table of Simulation Parameters

| Parameter | Value |
| :---: | :---: |
| Reference Frequency | 26 MHz |
| Up/Down Current Mismatch | $1 \%$ |
| Nominal Charge Pump Current | 1 mA |
| Loop Bandwith | 45 kHz |
| Loop Gain | $4.6425 \times 10^{8}$ |
| Pole 1 Frequency | 111.20 kHz |
| Pole 2 Frequency | 719.84 kHz |
| Zero Frequency | 9.0876 kHz |
| VCO Gain | $5 \mathrm{MHz} / \mathrm{V}$ |
| Division Ratio, Integer Part | 137 |
| Reference Phase Noise | $-150 \mathrm{dBc} / \mathrm{Hz}$ |
| VCO Phase Noise at 1 MHz offset | $-125 \mathrm{dBc} / \mathrm{Hz}$ |

structure leads to similar spectral performance. Moreover, the MASH 1-1-1 DDSM in the MASH-SR has a smaller number of bits for its input, which leads to faster-moving, loweramplitude wandering spurs compared with those arise from a standard MASH 1-1-1 with a similar input. Fig. 16 shows the simulated spectrogram of $t_{A C}[n]$ in the presence of a PWL nonlinearity of $8 \%$ mismatch when the MASH 1-1-1 DDSM input is $X=1$. The proposed MASH-SR with the optimized state transition matrices does not exhibit any wandering spurs.

## VI. Conclusion

A MASH-SR divider controller is a hybrid of a conventional MASH DDSM and an SR and it possesses the advantages of both structures. It can achieve similar spur performance to a full SR implementing identical state transition matrices with sufficient number of SR quantization blocks present in the structure. Compared with a full SR, a MASH-SR counterpart reduces the amount of hardware needed. Furthermore, a MASH-SR can be used to perform phase alignment and adjustment, which cannot be done with a conventional full length SR. Also, a MASH-SR can also lead to less latency compared to a full SR.

The spur performance of a MASH-SR can be optimized by selecting an appropriate pair of state transition matrices. In this work, the state transition matrices are optimized for 4-bit pseudorandom number generators which are included in a 20 -bit MASH-SQ that consists of a 16 -bit MASH 1-1-1 DDSM and four second-order SR quantization blocks. The selection of the state transition matrices is based on estimates for the distribution and spectrum of the accumulated quantization noise contribution of the SR quantization blocks. The state transition matrices that lead to an accumulated quantization noise contribution that is of greater variance and ketosis
are preferred. In terms of accumulated quantization noise, pairs of matrices that give less low-frequency accumulated quantization noise are favored.

As simulations indicate, the optimized state transition matrices achieve similar performance in terms of spur and noise floor to the state-of-art full SR implementing state transition matrices for 10 -bit pseudorandom number generators. It reduces the primary integer boundary spur by about 15 and 3 dB when compared to a standard MASH 1-1 and MASH 1-1-1 DDSM in the spectra of the distorted accumulated quantization error in the presence of a PWL nonlinearity. Closedloop behavior model simulations confirm the effectiveness of the proposed MASH-SR divider controller. The simulated spectral performance of the proposed MASH-SR is close to that of a reference standard full SR. Furthermore, the proposed MASH-SR hybrid can effectively mitigate wandering spurs that occur when using MASH DDSM divider controllers.

## Appendix A

## Computing the Distribution of $t_{S}[n]$

Consider two independent discrete random variables $X$ and $Y$ which have sample space

$$
\begin{equation*}
X \in\left\{x_{1}, x_{2}, \ldots, x_{M}\right\}, Y \in\left\{y_{1}, y_{2}, \ldots, y_{N}\right\} \tag{69}
\end{equation*}
$$

where

$$
\begin{equation*}
x_{k}-x_{k-1}=y_{l}-y_{l-1}=c>0, k \in[1, M], l \in[1, N] . \tag{70}
\end{equation*}
$$

The sample space of $X+Y$ is then

$$
\begin{equation*}
X+Y \in\left\{x_{1}+y_{1}, x_{1}+y_{1}+c, \ldots, x_{M}+y_{N}\right\} . \tag{71}
\end{equation*}
$$

The probability of the sum of two variables can be evaluated by the convolution of stochastic vectors

$$
\begin{equation*}
\mathbf{V}_{\mathbf{x}}=\left(P\left(X=x_{1}\right) \quad P\left(X=x_{2}\right) \quad \ldots \quad P\left(X=x_{M}\right)\right) \tag{72}
\end{equation*}
$$

and

$$
\begin{equation*}
\mathbf{V}_{\mathbf{y}}=\left(P\left(Y=y_{1}\right) P\left(Y=y_{2}\right) \ldots P\left(Y=y_{N}\right)\right) . \tag{73}
\end{equation*}
$$

Thus,

$$
\begin{align*}
& P\left(X+Y=x_{1}+y_{1}+(l-1) c\right) \\
& \quad=\sum_{k=\max \{l+1-M, 1\}}^{\min \{l, N\}} \mathbf{V}_{\mathbf{x}}[l+1-k] \mathbf{V}_{\mathbf{y}}[k], \\
& \quad l \in[1, M+N-1] . \tag{74}
\end{align*}
$$

The distribution of $t_{S}[n]$ can be computed by repeatedly applying this conclusion. Equation (31) can be written as

$$
\begin{align*}
t_{S}[n]= & \left(\cdots\left(\left(\frac{t_{K-1}[n]}{2^{1}}+\frac{t_{K-2}[n]}{2^{2}}\right)+\frac{t_{K-3}[n]}{2^{3}}\right)\right. \\
& \left.+\cdots+\frac{t_{1}[n]}{2^{K-1}}\right)+\frac{t_{0}[n]}{2^{K}} . \tag{75}
\end{align*}
$$

Define

$$
\begin{equation*}
t_{c, d}[n]=\frac{t_{d}[n]}{2^{K-d}} \tag{76}
\end{equation*}
$$

and the stochastic describing it as

$$
\begin{align*}
\mathbf{V}_{d}= & \left(P\left(t_{c, d}[n]=-\frac{N_{t}}{2^{K-d}}\right) \quad P\left(t_{c, d}[n]=-\frac{N_{t}+1}{2^{K-d}}\right)\right. \\
& \left.\ldots P\left(t_{c, d}[n]=\frac{N_{t}}{2^{K-d}}\right)\right)=\mathbf{p}_{\mathbf{t}} \tag{77}
\end{align*}
$$

where $N_{t}=2 N_{u}$ for a second-order $s_{d}[n]$ generator.
To start the iteration of the convolution, a vector to represent the sum that is to be added to $t_{c, d}[n]$ in the $(K-1-d)$ th set of brackets starting from inside in (75) is defined as $\mathbf{V}_{t,(K-1-d)}$. Therefore, $\mathbf{V}_{t, 1}=\mathbf{V}_{K-1}=\mathbf{p}_{\mathbf{t}}$.

Consider the sum in the first set of brackets starting from inside in (75). To establish sample spaces that have identical increments, padding of zeroes is performed to $\mathbf{V}_{t, 1}$ :

$$
\begin{align*}
& \mathbf{V}_{t, 1}^{\prime} \\
&=\left(P\left(t_{c,(K-1)}[n]=-\frac{2 N_{t}}{4}\right)\right. \\
& P\left(t_{c,(K-1)}[n]=-\frac{2 N_{t}-1}{4}\right) \\
&\left.\ldots P\left(t_{c,(K-1)}[n]=\frac{2 N_{t}}{4}\right)\right) \tag{78}
\end{align*}
$$

where $P\left(t_{c,(K-1)}[n]=\left(-2 N_{t}+k\right) / 4\right)=0$ for all odd integers $k$. Now the sum of $\mathbf{V}_{t, 1}^{\prime}$ and $\mathbf{V}_{K-2}$, which is by definition $\mathbf{V}_{t, 2}$, can be computed by convolution following (74):

$$
\begin{align*}
& \mathbf{V}_{t, 2}(l) \\
& =P\left(t_{c,(K-1)}[n]+t_{c,(K-2)}[n]=\frac{-3 N_{t}+l-1}{4}\right) \\
& =\sum_{k=\max \left\{l-2 N_{t}, 1\right\}}^{\min \left\{l, 2 N_{t}+1\right\}} \mathbf{V}_{K-2}[l+1-k] \mathbf{V}_{t, 1}^{\prime}[k], \\
& l \in\left[1,6 N_{t}+1\right] . \tag{79}
\end{align*}
$$

The step is repeated to compute the distribution of $t_{S}[n]$. Consider the summation in the $(m-1)$ th set of brackets. The zero-padded vector $\mathbf{V}_{t,(m-1)}^{\prime}$ can be expressed as

$$
\begin{align*}
\mathbf{V}_{t,(m-1)}^{\prime}= & \left(P\left(\sum_{p=1}^{m-1} t_{c,(K-p)}[n]=-\frac{\left(2^{m}-2\right) N_{t}}{2^{m}}\right)\right. \\
& P\left(\sum_{p=1}^{m-1} t_{c,(K-p)}[n]=-\frac{\left(2^{m}-2\right) N_{t}-1}{2^{m}}\right) \\
& \left.\ldots P\left(\sum_{p=1}^{m-1} t_{c,(K-p)}=\frac{\left(2^{m}-2\right) N_{t}}{2^{m}}\right)\right) \tag{80}
\end{align*}
$$

$\mathbf{V}_{t,(m-1)}^{\prime}$ is convolved with $\mathbf{V}_{K-m}$ to generate $\mathbf{V}_{t, m}$ :

$$
\begin{aligned}
\mathbf{V}_{t, m}(l) & =P\left(\sum_{p=1}^{m} t_{c,(K-p)}[n]=\frac{\left(2^{m}-1\right) N_{t}+l-1}{2^{m}}\right) \\
& =\sum_{k=\max \left\{l-2 N_{t}, 1\right\}}^{\min \left\{l,\left(2^{m+1}-4\right) N_{t}+1\right\}} \mathbf{V}_{K-m}[l+1-k] \mathbf{V}_{t,(m-1)}^{\prime}[k],
\end{aligned}
$$

$$
\begin{equation*}
l \in\left[1,\left(2^{m+1}-2\right) N_{t}+1\right] . \tag{81}
\end{equation*}
$$

The distribution of the $t_{S}[n]$ is found when $m=K$, i.e.,

$$
\begin{equation*}
\mathbf{P}_{\text {tout }}=\mathbf{V}_{t, K} \tag{82}
\end{equation*}
$$

and it can be expressed as (48).

## REFERENCES

[1] B. Miller and R. J. Conley, "A multiple modulator fractional divider," IEEE Trans. Instrum. Meas., vol. 40, no. 3, pp. 578-583, Jun. 1991.
[2] M. Perrott, M. Trott, and C. Sodini, "A modeling approach for $\Sigma-\Delta$ fractional $-N$ frequency synthesizers allowing straightforward noise analysis," IEEE J. Solid-State Circuits, vol. 37, no. 8, pp. 1028-1038, Aug. 2002.
[3] T. A. D. Riley, M. A. Copeland, and T. A. Kwasniewski, "Delta-sigma modulation in fractional- $N$ frequency synthesis," IEEE J. Solid-State Circuits, vol. 28, no. 5, pp. 553-559, May 1993.
[4] H. Arora, N. Klemmer, J. C. Morizio, and P. D. Wolf, "Enhanced phase noise modeling of fractional- $N$ frequency synthesizers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 2, pp. 379-395, Feb. 2005.
[5] M. P. Kennedy and V. S. Sadeghi, "Observations concerning PFD/CP operating point offset strategies for combatting static charge pump mismatch in fractional- $N$ frequency synthesizers with digital delta-sigma modulators," Nonlinear Theory Appl., vol. 5, no. 3, pp. 349-364, 2014.
[6] B. Razavi, "An alternative analysis of noise folding in fractional$N$ synthesizers," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2018, pp. 1-4.
[7] B. De Muer and M. S. J. Steyaert, "On the analysis of $\Delta-\Sigma$ fractional- $N$ frequency synthesizers for high-spectral purity," IEEE Trans. Circuits Syst. II, Analog Digital Signal Process., vol. 50, no. 11, pp. 784-793, Nov. 2003.
[8] P.-E. Su and S. Pamarti, "Mismatch shaping techniques to linearize charge pump errors in fractional- $N$ PLLs," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 6, pp. 1221-1230, Jun. 2010.
[9] K. Hosseini, B. Fitzgibbon, and M. P. Kennedy, "Observations concerning the generation of spurious tones in digital delta-sigma modulators followed by a memoryless nonlinearity," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 58, no. 11, pp. 714-718, Nov. 2011.
[10] A. Swaminathan, A. Panigada, E. Masry, and I. Galton, "A digital requantizer with shaped requantization noise that remains well behaved after nonlinear distortion," IEEE Trans. Signal Process., vol. 55, no. 11, pp. 5382-5394, Nov. 2007.
[11] K. J. Wang, A. Swaminathan, and I. Galton, "Spurious tone suppression techniques applied to a wide bandwidth 2.4 GHz fractional- $N$ PLL," IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2787-2797, Dec. 2008.
[12] E. Familier, C. Venerus, and I. Galton, "A class of quantizers with DC-free quantization noise and optimal immunity to nonlinearityinduced spurious tones," IEEE Trans. Signal Process., vol. 61, no. 17, pp. 4270-4283, Sep. 2013.
[13] E. Familier and I. Galton, "Second and third-order noise shaping digital quantizers for low phase noise and nonlinearity-induced spurious tones in fractional-N PLLs," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 6, pp. 836-847, Jun. 2016.
[14] Z. Li, H. Mo, and M. P. Kennedy, "Comparative spur performance of a fractional- $N$ frequency synthesizer with a nested MASH-SQ3 divider controller in the presence of memoryless piecewise-linear and polynomial nonlinearities," in Proc. Irish Signals Syst. Conf. ChinaIreland Int. Conf. Inf. Commun. Technol. (ISSC/CIICT), Jun. 2014, pp. 374-379.
[15] D. Mai and M. P. Kennedy, "A design method for nested MASH-SQ hybrid divider controllers for fractional- $N$ frequency synthesizers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 10, pp. 3279-3290, Oct. 2018.
[16] M. P. Kennedy et al., "16.9 4.48 GHz $0.18 \mu \mathrm{~m}$ SiGe BiCMOS exactfrequency fractional- $N$ frequency synthesizer with spurious-tone suppression yielding a -80 dBc in-band fractional spur," in IEEE Int. SolidState Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2019, pp. 272-274.
[17] Y. Donnelly et al., "4.48-GHz fractional- $N$ frequency synthesizer with spurious-tone suppression via probability mass redistribution," IEEE Solid-State Circuits Lett., vol. 2, no. 11, pp. 264-267, Nov. 2019.
[18] D. Mai, A. Dahlan, and M. P. Kennedy, "MASH DDSM-induced spurs in a fractional- $N$ frequency synthesizer," in Proc. 26th IEEE Int. Conf. Electron., Circuits Syst. (ICECS), Nov. 2019, pp. 13-16.
[19] E. Familier and I. Galton, "Second and third-order successive requantizers for spurious tone reduction in low-noise fractional- $N$ PLLs," in Proc. IEEE Custom Integr. Circuits Conf. (CICC), Apr. 2017, pp. 1-4.
[20] E. Familier and I. Galton, "A fundamental limitation of DC-free quantization noise with respect to nonlinearity-induced spurious tones," IEEE Trans. Signal Process., vol. 61, no. 16, pp. 4172-4180, Aug. 2013.
[21] D. Mai and M. P. Kennedy, "Analysis of wandering spur patterns in a fractional- $N$ frequency synthesizer with a MASH-based divider controller," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 3, pp. 729-742, Mar. 2020.
[22] D. Mai, H. Mo, and M. P. Kennedy, "Observations and analysis of wandering spurs in MASH-based fractional- $N$ frequency synthesizers," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 5, pp. 662-666, May 2018.
[23] D. Mai, X. Li, and M. P. Kennedy, "Experimental confirmation of wandering spurs in a commercial fractional- $N$ frequency synthesizer with a MASH 1-1-1 divider controller," in Proc. 30th Irish Signals Syst. Conf. (ISSC), Jun. 2019, pp. 1-6.


Dawei Mai (Member, IEEE) received the B.E. and M.E. degrees in electrical and electronic engineering from University College Cork (UCC) in 2015 and 2018, respectively, and the Ph.D. degree from University College Dublin (UCD) in 2021. He is currently a Post-Doctoral Research Fellow at UCD. His research interests include the design, analysis, and modeling of high-performance frequency synthesizers.


Michael Peter Kennedy (Fellow, IEEE) received the B.E. degree in electronics from the National University of Ireland, Dublin, in 1984, the M.S. and Ph.D. degrees from the University of California at Berkeley (UC Berkeley), Berkeley, in 1987 and 1991, respectively, the D.Eng. degree from the National University of Ireland in 2010, and the D.Sc. (Eng.) (Hons.) from Queen's University Belfast in 2020.

He has been a Professor in microelectronic engineering at University College Dublin since 2017. He was elected as a fellow of IEEE in 1998 for his contributions to the study of neural networks and nonlinear dynamics. He was elected to membership of the Royal Irish Academy (RIA) in 2004, served as the RIA Policy and International Relations Secretary from 2012 to 2016, and as the President from 2017 to 2020. He was the Vice President for Region 8 of the IEEE Circuits and Systems Society (CASS) from 2005 to 2007, a CASS Distinguished Lecturer from 2012 to 2013 and in 2022, and the Chair of the CASS Distinguished Lecturer Program from 2017 to 2020. He served on the IEEE Fellows Committee and the IEEE Gustav Robert Kirchhoff Award Committee. He received the Honoris Causa Award for D.Sc. (Eng.) degree.


[^0]:    Manuscript received 24 August 2022; revised 14 November 2022; accepted 5 December 2022. Date of publication 26 December 2022; date of current version 27 February 2023. This work was supported in part by the Science Foundation Ireland and Enterprise Ireland under Grant 20/FFP-A/8371 and Grant TC-2015-0019. This article was recommended by Associate Editor H. Sjoland. (Corresponding author: Dawei Mai.)

    The authors are with the School of Electrical and Electronic Engineering, University College Dublin, Belfield, Dublin 4, D04 V1W8 Ireland, and also with the Microelectronic Circuits Centre Ireland (MCCI), Dublin 4, D04 V1W8 Ireland (e-mail: dawei.mai@ucd.ie; peter.kennedy@ucd.ie).

    Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2022.3230634.
    Digital Object Identifier 10.1109/TCSI.2022.3230634

[^1]:    ${ }^{1}$ Successive requantizer was originally abbreviated as SQ in [10] and later as SR in [11].

[^2]:    ${ }^{2}$ For this work, the MATLAB solve function was used for solving and simplifying the sets of equations. -

