Power-Efficient Single-Stage Class-AB OTA Based on Non-Linear Nested Current Mirrors

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***Abstract*—A novel approach to design low-power area-efficient rail-to-rail output single-stage class-AB operational transconductance amplifiers (OTAs) with enhanced large- and small-signal performance to drive large capacitive loads is presented. It is based on a non-linear nested current mirror at the active load of a splitted differential input pair biased in weak inversion that boosts dynamic currents beyond their quiescent value directly at the output branch. As a result, slew rate, DC gain, gain-bandwidth product, settling time and noise performance are improved without additional circuit elements or power consumption. An OTA prototype has been fabricated in a 180-nm CMOS process, consuming a quiescent power of 2.9 µW from a supply voltage of ±0.5 V and a silicon area of 0.001 mm². Measurement results validate the advantages of the proposal, exhibiting positive and negative slew rates of 110 V/ms and −58 V/ms, respectively, and a gain-bandwidth product of 136 kHz with a phase margin of 90º for a capacitive load of 160 pF.**

***Index Terms*—Class-AB, non-linear nested current mirror, single-stage amplifier, rail-to-rail output, area efficiency.**

I. Introduction

LOW-POWER design is a crucial task which continuously requires novel techniques to satisfy the industry demands. Within this context, the OTA is a key element that still plays an important role due to its versatility in a wide variety of applications. Due to the proliferation of battery-operated devices and energetically autonomous systems in general, OTAs should operate with low-voltage and low-power constraints as well as exhibiting high-performance features, such as overall transconductance (G_m), gain-bandwidth product (GBW), slew rate (SR), settling time (ST), area, input-output swing and noise.

Single-stage amplifiers constitute the best-balanced option in terms of power efficiency, performance and area as the number of branches where current flows are minimum and because they are load compensated, avoiding the use of frequency compensation schemes that may increase both area and power. Conversely, their main drawback is their limited gain, especially in modern submicron CMOS processes [1]. For this reason, various techniques have been proposed to improve not only gain, but also GBW, SR or ST while keeping power consumption as low as possible.

Power efficiency is also achieved by class-AB operation. A limitation of class-A OTAs is that the maximum load current is bounded by the bias current, leading to a power vs performance trade-off. Class-AB topologies can improve large-signal performance without increasing quiescent current, yielding larger SR with the same static consumption as their class-A counterpart. These features are particularly useful in several applications, such as: LCD displays requiring a large number of amplifiers driving large capacitive loads (from hundreds of pF up to tens of nF) with restricted constraints of output swing, power budget and area per channel [2]-[5]; multichannel processing architectures employing power- and area-efficient switched-capacitor circuits where the class-AB behavior is mandatory to rapidly charge/discharge the capacitors [6], [7]; sigma-delta modulators [8], [9]; or low-dropout regulators in which large capacitive loads and fast transients are required [10], [11].

Over the years, different class-AB solutions have been presented. The use of flipped voltage followers as adaptive biasing floating batteries [12], [13] overcomes the tail current limitation in differential pairs by making bias current adaptive. However, the input range is limited, requiring additional circuit elements. The quasi-floating gate transistor [14] is another solution that provides both independent DC biasing and AC driving. However, the increased area and the inherent RC high-pass filtering may not be suitable for certain applications. Local common mode feedback [15] with passive resistors has been used in the active load of OTAs to increase both SR and GBW at the cost of extra area and reduced phase margin. Finally, SR enhancer circuits that inject an extra amount of driving current [16], [17] have also been proposed, with the penalty of increasing power and area.

An alternative strategy to obtain class-AB operation is to use non-linear current mirrors [18]-[21]. In DC conditions, the operation is similar to a linear current mirror; however, under dynamic operation, circuit enters a non-linear regime that boosts input pair's current beyond its quiescent value. Moreover, if the dynamic boosting occurs at the output branch so that no internal dynamic current replication exists, a nearly optimal current efficiency factor (CE), i.e., the ratio between the load and supply currents, $CE = I_{out}/I_{supply} \approx 1$ can be achieved.

The approach in [18] is using a current mirror at the active load where the input transistor is biased on the edge between saturation and triode regions. Under large-signal transitions, current mirror input transistor enters a non-linear deep triode region, thus boosting output current. The triode state is achieved by a relatively large dynamic input current, which is supplied by an adaptively biased pair in this case. Consequently, its usability is limited since the working principle requires an adaptive biasing pair, or very large bias currents. Reference [19] employs dynamic non-linear current mirrors, whose gain is changed by

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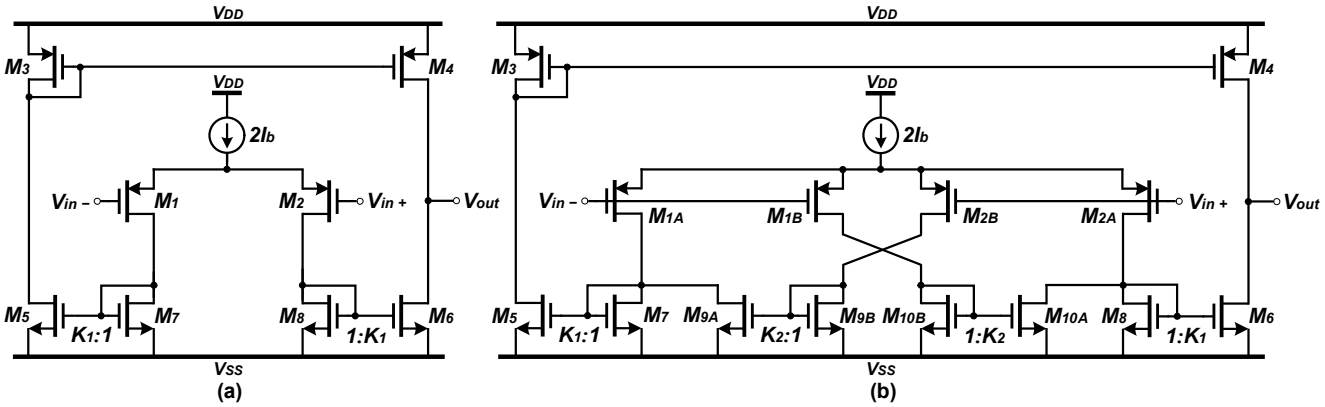

Fig. 1. Existing single-stage class-A amplifier topologies: (a) current mirror (CM) OTA and (b) nested current mirror (NCM) OTA.

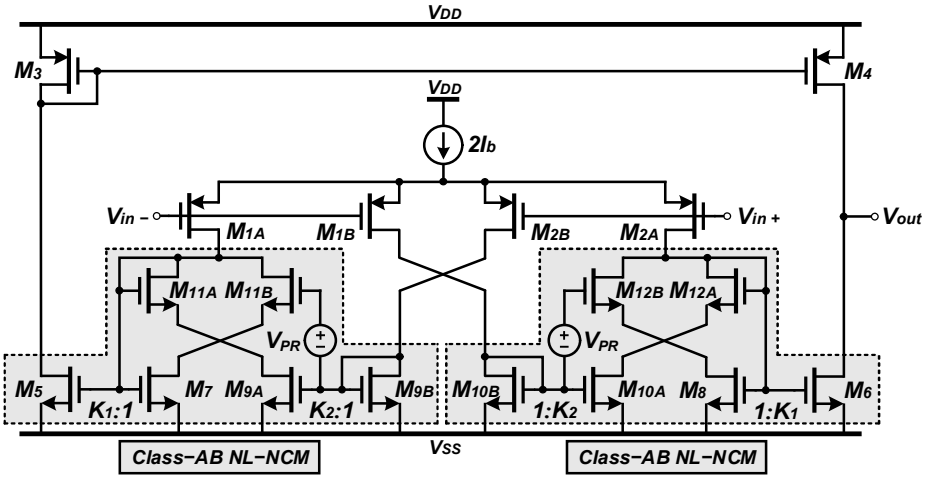

Fig. 2. Proposed class-AB non-linear nested current mirror (NL-NCM) OTA.

a cross-coupled local partial-positive feedback. However, the DC static power consumption is in the order of mW, and despite driving a large capacitive load, phase margin is low. The proposed technique in [20] combines again an adaptive biasing differential pair with a non-linear current mirror based on two cross-coupled cascode transistors. This connection dynamically biases output transistors between saturation and triode regions, achieving current boosting. However, only simulation results are provided, and adaptive biasing is still used at input pair. Finally, reference [21] employs an adaptive biasing input scheme with a non-linear current mirror as active load, which combines local common mode feedback with local partial-positive feedback. Despite the outstanding large-signal results obtained, local-common mode feedback resistors consume significant areas, reducing its applicability in area-efficient scenarios.

This paper presents a novel solution to design power and area efficient rail-to-rail output single-stage class-AB OTAs based on non-linear nested current mirrors (NL-NCM) with enhancements of SR, DC gain, GBW, ST and noise. The NL-NCM is based on a current-mode squarer/divider circuit previously published by some of the authors in [22] that dynamically bias output transistors under dynamic conditions, generating a boosted non-linear output current under large-signal transients whereas keeping a low DC power consumption. The proposed approach leads to high output currents avoiding the use of additional circuit elements. Therefore, the consumed area is low. Due to high driving capability, low power and low area, the proposed OTA is highly suitable for those applications that require high-performance transient responses for large capacitive output loads, limited power budgets and area constraints.

The paper is organized as follows. Section II introduces the NL-NCM while Section III presents a detailed analysis of the amplifier. Section IV compares analytically the proposed OTA with two preceding current mirror amplifiers that have inspired the NL-NCM, highlighting the improved features, as well as the benefits and drawbacks of each topology. Measurement results for a 180-nm CMOS implementation are given in Section V. Concluding remarks are drawn in Section VI.

II. Proposed Non-Linear Nested Current Mirror

The current mirror (CM) OTA is one of the most widely used single-stage amplifiers. Shown in Fig. 1(a), it offers an almost rail-to-rail output swing, and the current mirror ratio K_1 provides flexibility, controlling features such as G_m, GBW, SR and ST. However, it operates in class-A since the maximum output current cannot exceed the tail bias current unless K_1 >1, but a larger K_1 increases power and area, and also degrades stability.

An enhanced CM OTA is depicted in Fig. 1(b). Known as nested current mirror (NCM) OTA [23], [24] it splits the differential pair into N sub-transistors ($N = 2$ in this case). Subsequently, their outputs are cross-coupled via current mirrors $M_{9A,9B}$ and $M_{10A,10B}$ with a ratio K_2. This produces an in-phase

AC sum of input pair's transconductances, enhancing G_m [25] while preserving the CM OTA power consumption if K_1 is properly chosen.

Despite having better features, the NMC OTA still operates in class-A since the maximum output current is still proportional to the tail current. Hence a power-performance trade-off still exists limiting its use in those scenarios requiring large SRs and low STs. To circumvent these limitations, an improved class-AB version is proposed, which is shown in Fig. 2 where the shaded areas emphasize the novel contribution. Coined as non-linear nested current mirror (NL-NCM) OTA, the solution rearranges the active load to improve amplifier's performance. This is achieved adding extra transistors $M_{11A,11B}$ and $M_{12A,12B}$ in a stacked configuration at the drains of $M_{7,8}$ and $M_{9A,10A}$, allowing transistors M_7-M_8 to alternately operate between saturation and triode regions in large-signal operation. As a result, output current is non-linearly related to input currents coming from $M_{1A,2B}$ and $M_{1B,2A}$. This produces under large dynamic variations a boosted output current much larger than $2I_b$, no longer bounded by the scaled tail current. In addition to improved large-signal operation, small-signal performance can be enhanced by properly setting the NL-NCM bias point, increasing current gain. This can be controlled by the quiescent current through the splitted input pair M_1-M_2, and the drain-to-source voltage of M_7-M_8, which in turn is set by the aspect ratio of transistors $M_{11A,11B}$ and $M_{12A,12B}$ and/or through the voltage source V_{PR}, respectively. In order to save power, the circuit is designed for quiescent operation in weak inversion. Floating sources V_{PR} provide extra design flexibility and will be included in the following analysis, although they were not implemented in the fabricated OTA to minimize power and area.

A. DC Static Behavior

The DC behavior of NL-NCM can be described in two steps. The first one is to split the differential pair transistors $M_{1,2}$ of the CM OTA into two sub-transistors (see Fig. 2). Hence, the aspect ratios of $M_{1A,2A}$ and $M_{1B,2B}$ are defined as $(W/L)_{1A,2A} = \alpha(W/L)_{1,2}$ and $(W/L)_{1B,2B} = (1-\alpha)(W/L)_{1,2}$, where α is the splitting factor with $0.5 < \alpha < 1$, and $(W/L)_{1,2}$ is the aspect ratio of the non-splitted CM OTA pair. In order to simplify the description, the half circuit of Fig. 2 is redrawn in Fig. 3. The behavior of the other half circuit is the same due to the OTA's symmetry. In Fig. 3, I_{B1} and I_{B2} are DC static currents, and i_1 and i_2 are the small-signal input currents, being both supplied by the differential pair. In this way, DC currents are $I_{B1} = \alpha I_b$ and $I_{B2} = (1-\alpha)I_b$. Note that $I_{B1} > I_{B2}$ for proper circuit operation, which is achieved with $(W/L)_{1A,2A} > (W/L)_{1B,2B}$, i.e., $\alpha > 0.5$. Next, outputs of the splitted input pair are combined via current mirrors $M_{9A,9B}$. Consequently, DC current through M_7 is $I_7 = I_{B1} - I_{B2}K_2$ assuming that M_{9A} is in saturation, and $K_2 = (W/L)_{9A}/(W/L)_{9B}$.

Since the circuit operates in weak inversion, the well-known exponential current-voltage relationship is considered

$$I_d \approx I_o \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nV_t}} \left(1 - e^{\frac{-V_{DS}}{V_t}}\right) \quad (1)$$

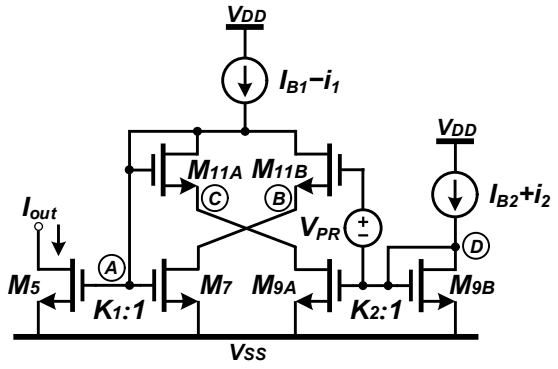

Fig. 3. Non-linear nested current mirror (NL-NCM).

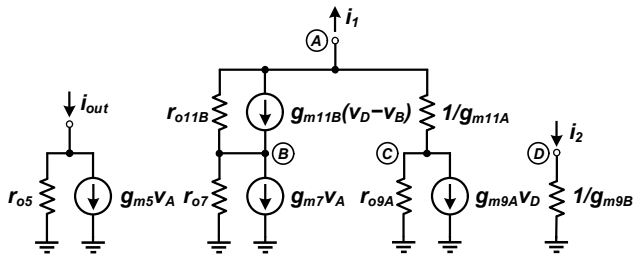

Fig. 4. Small-signal equivalent circuit.

where I_o is the specific current, V_{GS} (V_{DS}) is the gate-to-source (drain-to-source) voltage, V_{TH} is the threshold voltage, $V_t \approx 26$ mV is the thermal voltage and $n \approx 1.5$ is the slope factor. Implicitly, V_{TH} depends on V_{DS} through the drain-induced barrier lowering (DIBL) effect as well as V_{BS} through the body effect, expressed by $V_{TH} = V_{TH0} - \lambda_{DS}V_{DS} - \lambda_{BS}V_{BS}$, where V_{TH0} is the zero-bias threshold voltage and λ_{DS} and λ_{BS} are positive technology-dependent coefficients [26].

The output current varies depending on whether M_7 is in saturation or triode region. For $V_{DS} \geq 100$ mV, the device operates in saturation. By contrast, under low values of $V_{DS} < V_t$ [26], it can be modelled as a linear resistor operating in triode. Assuming that M_7 can be in saturation or triode, that M_5 is always in saturation and neglecting DIBL effect for simplicity, the quiescent output current is defined as

$$I_{out}^{Q} = K_1(I_{B1} - I_{B2}K_2)\left(\frac{1}{1 - e^{-V_{DS7}/V_t}}\right) \quad (2)$$

where $I_{B1} > I_{B2}K_2$ for a proper DC operation and $K_1 = (W/L)_5/(W/L)_7$. Note the non-linear dependence on V_{DS7}. When M_7 is biased in saturation, the non-linear term can be neglected, and $I_{out}^{Q} \approx K_1(I_{B1} - I_{B2}K_2)$, i.e., the same as for the NCM OTA. However, when it is in triode, I_{out}^{Q} increases non-linearly. Interestingly, this property can be used to enhance the small-signal performance. To exploit this feature, V_{DS7} should be set on the edge between saturation and triode regions, that is, $V_{DS7} \approx V_t = 26$ mV. This bias point allows exploiting the NL-NCM, increasing current gain with little power degradation. Note that (2) is only valid for those V_{DS7} that leads to $V_{GS5,7} < V_{TH}$ in order to maintain the weak inversion operation as well as the system stability. Later, it will be shown how to properly set this variable.

Equation (2) can be developed to relate I_{out}^{Q} to I_b, which is particularly useful to model the DC static power consumption.

Noting that $V_{DS7} = V_{GS9A} + V_{PR} - V_{GS11B}$, $I_{B1} = \alpha I_b$ and $I_{B2} = (1-\alpha)I_b$, where $V_{GS9A} = V_{TH9A} + nV_t \cdot \ln([K_2 I_{B2}]/[I_o(W/L)_{9A}])$ and $V_{GS11B} = V_{TH11B} + nV_t \cdot \ln([I_{B1} - I_{B2}K_2]/[I_o(W/L)_{11B}])$; and assuming M_{9A}, M_{9B}, M_{11A} and M_{11B} in saturation, and $V_{TH9A} = V_{TH11B}$ for simplicity, (2) can be rewritten as

$$I_{out}^{Q} = I_b K_1(\alpha - [1-\alpha]K_2)\left(1 + \frac{1}{e^{\frac{V_{PR}}{V_t}}\left(\frac{x[1-\alpha]K_2}{\alpha - [1-\alpha]K_2}\right)^n - 1}\right) \tag{3}$$

where $x = (W/L)_{11A,11B}/(W/L)_{7,9A}$. For higher accuracy, second order effects such as DIBL, body and channel-length modulation effects should be considered.

The bias currents can be properly chosen to operate transistors in weak inversion in order to maximize the g_m/I_d ratio [16], improving power efficiency, signal swing and linearity if the application does not require a very large bandwidth.

B. Small-Signal Performance

When two complementary small-signal currents i_1 and i_2 are supplied by the differential pair, an in-phase AC current sum is generated at the output, as seen in the small-signal equivalent circuit of Fig. 3 shown in Fig. 4. Depending on whether M_7 is in saturation or triode, the circuit operation changes. To model it, the transistor intrinsic gain $g_m r_o$ deserves to be analyzed. Defining $g_m = \partial I_d/\partial v_{GS}$ and $r_o = (\partial I_d/\partial v_{DS})^{-1}$, as well as considering the DIBL effect, $g_m r_o$ of a MOS transistor in weak inversion is

$$g_m r_o = \frac{1}{\lambda_{DS} + \frac{n}{e^{V_{DS}/V_t} - 1}}. \tag{4}$$

Note that $g_m r_o$ varies considerably with V_{DS}. In saturation, (4) can be approximated to $g_m r_o \approx 1/\lambda_{DS}$ and the assumption $g_m r_o \gg 1$ is often considered. In triode $g_m r_o$ is reduced, and the latter assumption is no longer valid. In the limit, when V_{DS} approaches to 0 V, $g_m r_o \approx 0$. For intermediate V_{DS}, values (4) must be used.

To obtain the current gain expression, all devices are assumed in saturation except M_7 (which can be in saturation or triode), thus $g_m r_o \gg 1$ will be considered for all transistors but M_7. Also, output resistances of M_5, M_{9A} and M_{11B} will be neglected. The small-signal output current is

$$i_{out} = \frac{g_{m5}}{g_{m7} g_{m11B} r_{o7}}\left(i_1[1 + g_{m11B} r_{o7}] + i_2\left[\frac{g_{m9A}}{g_{m9B}} + \frac{g_{m11B}}{g_{m9B}}[1 + g_{m9A} r_{o7}]\right]\right). \tag{5}$$

Since $i_1 = \alpha i_{in}$ and $i_2 = (1-\alpha) i_{in}$, where i_{in} is the small-signal non-splitted input current, from (4) current gain is

$$A_I = \frac{i_{out}}{i_{in}} = \frac{K_{1eff}}{g_{m11B} r_{o7}}\left(\alpha[1 + g_{m11B} r_{o7}] + [1-\alpha]\left[K_2 + \frac{g_{m11B}}{g_{m9B}}[1 + g_{m9A} r_{o7}]\right]\right) \tag{6}$$

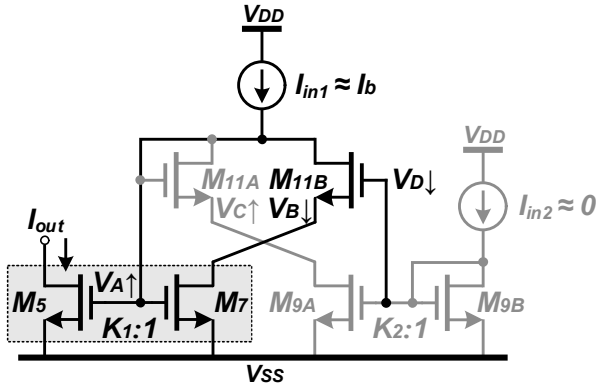

Fig. 5. Large-signal performance when $I_{in1} \gg I_{in2}$.

where $K_{1eff} = g_{m5}/g_{m7} = K_1/(1 - e^{-V_{DS7}/V_t})$ represents the effective gain of current mirror M_5-M_7. Note that V_{DS7} increases K_{1eff} maintaining area. When all transistors are in saturation, $g_{m7} r_{o7} \gg 1$ and $A_I \approx K_1(\alpha + [1-\alpha]K_2)$ with $K_{1eff} \approx K_1$, as for the NCM. Conversely, when M_7 is in triode, $g_{m7} r_{o7} < 1$ and $A_I \approx (K_{1eff}/g_{m11B} r_{o7})(\alpha + [1-\alpha][K_2 + g_{m11B}/g_{m9B}])$, so A_I is boosted as V_{DS7} and r_{o7} decrease.

C. Large-Signal Performance for Class-AB operation

Let's assume a large differential current $I_{id} = I_{in1} - I_{in2}$ in Fig. 3. When $I_{in1} \gg I_{in2}$, M_{9A}, M_{9B} and M_{11A} are nearly off since almost no current flows through them. On the other hand, current in M_7 and M_{11B} is $I_{7,11B} = I_{in1} - K_2 I_{in2} \approx I_{in1}$. As I_{in2} reduces, $V_{gs9A,9B}$, and consequently, V_{g11B}, are reduced. Therefore, since M_{11B} acts as a source follower, V_{ds7} is decreased, entering M_7 in deep-triode region. In order to keep its drain current, V_{gs7} is boosted, increasing V_{gs5} and achieving class-AB operation with a notable output current boosting. The working principle is illustrated in Fig. 5. As $V_{gs5,7} \gg V_{TH}$ in dynamic conditions, $M_{5,7}$ enter strong inversion. Moreover, M_7 is in triode and M_5 is in saturation. Defining the strong inversion currents in both triode and saturation as $I_d = \beta(V_{gs} - V_{TH})V_{ds}$ and $I_d = (\beta/2)(V_{gs} - V_{TH})^2$ respectively, with $\beta = \mu_n C_{ox}(W/L)$,

$$I_{out} = \frac{\beta_5}{2}\left(\frac{I_{in1} - K_2 I_{in2}}{\beta_7 V_{ds7}}\right)^2 \approx \frac{K_1}{2\beta_7}\left(\frac{I_{in1}}{V_{ds7}}\right)^2 \tag{7}$$

yielding class AB operation by a quadratic current boosting. Moreover, as M_7 is in triode, V_{ds7} is reduced further increasing I_{out} since the denominator of (7) tends to zero. In practice V_{gs} values are limited by the supply voltages. Rewriting (7) as $I_{out} \approx K_1(\beta_7/2)(V_{gs7} - V_{TH})^2$ for $V_{ds7} \approx 0$ V, $V_{g7} \approx V_{DD}$ then, $V_{gs\ ,max} \approx V_{DD} - V_{SS} = 2V_{DD}$, and

$$I_{out}^{MAX} \approx K_1 \frac{\beta_7}{2}(2V_{DD} - V_{TH})^2 \cdot \tag{8}$$

Note that (8) is just an approximated expression based on the simple MOS square law. In practice a more complex modeling

including second-order effects is required to accurately model large-signal behavior.

By contrast, when $I_{in1} \ll I_{in2}$, $I_{7,11B} \approx -K_2 I_{in2}$, transistors M_5 and M_7 are off, and no current flows in the output branch. In this case the large output current in (8) is yielded by the other half circuit in Fig. 2, reaching the OTA output with opposite sign.

D. Design Considerations

Note that V_{DS7} is a key design parameter in the NL-NCM OTA, hence it is important to set it properly to get an optimal bias point. The first approach consists of choosing an adequate aspect ratio of M_{11A} and M_{11B}. If M_{11A}-M_{11B} are chosen x times larger than M_7-M_{9A}, since $V_{DS7} = V_{GS9} - V_{GS11B}$, then

$$x = \frac{(W/L)_{11A,11B}}{(W/L)_{7,9B}} = \frac{I_{B1} - I_{B2}K_2}{I_{B2}K_2} \cdot e^{\left(\frac{V_{DS7}}{nV_t}\right)} \tag{9}$$

where body effect has been neglected and perfect matching and operation in saturation of M_{9A} and M_{11B} has been assumed. It is worth mentioning how the dependence on V_{TH} is cancelled due to the subtraction of both V_{GS}, improving the robustness against process variations. Note that choosing x the quiescent V_{DS7} is set. For instance, to set M_7 in the limit of saturation and triode regions, $V_{DS7} \approx V_t$ (26 mV). If $I_{B1} = 2I_{B2}K_2$ with $K_2 = 1$, $x = 1.9477 \approx 2$.

The drawback of this method is the inherent dependence on temperature through V_t as well as the mismatch, especially for low values of V_{DS7}. Matching is required not only for transistors in Fig. 3 but also for the input pair transistors as they set α and hence I_{B1} and I_{B2}. To improve matching large transistors lengths can be used, at the cost of degrading area and bandwidth. Also, proper layout techniques (e.g., interdigitation) should be used. This method to set $V_{DS7}$is simple and optimal in terms of power and area since no additional circuit elements are required, despite the aforementioned drawback.

The second approach utilizes the floating voltage battery V_{PR} in Fig. 2. Analyzing the current mirror using the translinear principle [27], by inserting a voltage source into the translinear loop, the circuit behavior can be easily altered [28]. In this way, $V_{DS} = V_{GS9A} + V_{PR} - V_{GS11}$. Assuming perfect matching

$$V_{PR} = V_{DS7} - nV_t \cdot ln\left(\frac{xI_{B2}K_2}{I_{B1} - I_{B2}K_2}\right). \tag{10}$$

The potential advantage is that V_{PR} can be set either internally or externally and thus it can be modified after fabrication, yielding a versatile amplifier design. Examples of voltages source implementations can be found in [29]-[33]. Another advantage is that V_{PR} can make the circuit more robust, compensating temperature variations (e.g., by a proper PTAT voltage) and mismatch. Automatic on-chip tuning techniques [34]-[37] can be applied to electronically adjust V_{DS} during calibration. However, the V_{PR} implementation could increase power consumption, area and circuit complexity. For this reason, only the first method will be considered here in the amplifier implementation. Of course, both methods can be combined.

Note from (6) and (7) that low V_{DS7} values allow exploiting the non-linear NCM behavior, increasing K_{1ef} as well as output driving capability. By contrast, power, stability, mismatch and thermal dependence are degraded. On the other hand, a larger V_{DS7} reduces sensitivity to mismatch and temperature, but it exploits less the non-linear NCM behavior. Therefore, the circuit designer should consider this trade-off depending on the required performance of the target application.

III. Single-Stage Class-AB NL-NCM OTA

A. Small-Signal Performance

When a small-signal differential input voltage v_{id} is applied, the differential input pair provides two complementary currents $i_1 = (v_{id}/2)g_{m1A,1B}$ and $i_2 = -(v_{id}/2)g_{m2A,2B}$ that enter into the NL-NCM. Transconductances of the differential input pair are defined as $g_{m1A,2A} = \alpha g_{m,in}$ and $g_{m1B,2B} = (1-\alpha)g_{m,in}$, being $g_{m,in}$ the transconductance of the non-splitted input pair, which is equal to $g_{m,in} = g_{m1A,2A} + g_{m1B,2B}$. By considering $i_1 = \alpha i_{in}$ and $i_2 = (1-\alpha)i_{in}$ with $i_{in} = (v_{id}/2)g_{m,in}$, once substituted in (5), the OTA transconductance is

$$\begin{aligned} G_m &= \frac{i_{out}}{v_{id}} = A_I \frac{i_{in}}{v_{id}} = A_I g_{m,in} \\ &= \frac{g_{m,in}K_{1eff}}{g_{m11B}r_{o7}}\Bigg(\alpha[1 + g_{m11B}r_{o7}] + \\ &\quad (1-\alpha)\left[K_2 + \frac{g_{m11B}}{g_{m9B}}[1 + g_{m9A}r_{o7}]\right]\Bigg) \end{aligned} \tag{11}$$

Regarding stability, the dominant pole is located at the output, and depends on both load capacitance and output resistance $\omega_d = 1/(r_{out}C_L)$. According to Fig. 3, A, B, C and D represent the nodes of the non-dominant poles, which are defined as

$$\begin{aligned} \omega_{pA} &\approx \frac{g_{m7}g_{m11B}}{(g_{m11B} + 1/r_{o7})C_A} \\ \omega_{pB} &\approx \frac{1 + g_{m7}g_{m11B}r_{o7}r_{o11B}}{r_{o7}C_B} \\ \omega_{pC} &\approx \frac{g_{m11A}}{C_C} \\ \omega_{pD} &\approx \frac{g_{m9B}}{C_D} \end{aligned} \tag{12}$$

where C_i represents the parasitic capacitance associated to the i-th node. An advantage of the proposed OTA is that all non-dominant poles are located at low impedance nodes within the signal path, allowing to position them beyond the gain-bandwidth product $\omega_{GBW} = A_{OL}\omega_d = G_m/C_L$, where $A_{OL} = G_m r_{out}$ is the open-loop gain. Consequently, no frequency compensation is required, extending the range of capacitive loads [24].

By inspection, it can be seen how ω_{pA} and ω_{pB} have a strong dependence on the biasing of M_7. In saturation, $\omega_{pA} \approx g_{m7}/C_A$ and $\omega_{pB} \approx g_{m7}g_{m11B}r_{o11B}/C_B$. However, in deep triode state, $r_{o7} \to 0$ therefore $\omega_{pA} \to 0$ and $\omega_{pB} \to \infty$. Intuitively, when r_{o7} is reduced, the RC time constant associated to node B is also reduced. The lower bound $r_{o7} = 0$ makes that node B is virtually connected to ground, shifting the pole towards very high frequencies. Since poles ω_{pC} and ω_{pD} remain unchanged, and

C_A is the highest parasitic contribution, it is assumed that pole at node A is the non-dominant one at lowest frequency.

In addition, two zeros appear in the system. The first one ω_{z1} is associated with the feedforward input pair stages $M_{1A,1B}$ and $M_{2A,2B}$. The other one is produced by current mirrors $M_{9A,9B}$ and $M_{10A,10B}$, generating a pole-zero doublet with ω_{pD} defined as $\omega_{z2} = (K_2 + 1)\omega_{pD}$ [25]. These zeros are located beyond the non-dominant poles, and depending on the design conditions, it can be beneficial to compensate for the phase shift of ω_{pC} and ω_{pD} [24].

Using the phase margin expression $PM = 90º - tg^{-1}(\omega_{GBW}/\omega_{pA})$ and considering $G_m = A_I g_{m,in}$,

$$PM \approx 90° - tg^{-1}\left(\frac{A_I g_{m,in}[g_{m11B} + 1/r_{o7}]}{g_{m7} g_{m11B}} \cdot \frac{C_A}{C_L}\right). \quad (13)$$

Notice how phase margin is degraded as M_7 enters in triode when V_{DS7} is reduced, that in turn increases A_I and reduces $g_{m7} r_{o7}$, thus demonstrating the stability vs performance trade-off. Once amplifier small-signal properties fixed for a target phase margin of $PM = 70º$, or equivalently for $\omega_{pA} = 3\omega_{GBW}$, which is a typical value that optimizes the 1% settling time [38], [39], the minimum load capacitance under this condition is

$$C_{L,min} \approx \frac{A_I g_{m,in}[g_{m11B} + 1/r_{o7}]}{g_{m7} g_{m11B}} \cdot \frac{C_A}{tg(20°)}. \quad (14)$$

Because the amplifier is load compensated, it will be unconditionally stable for those loads larger than $C_{L,min}$, avoiding frequency compensation schemes and extending the range of capacitive loads, with no upper limitation in terms of stability.

B. Linear Small-Signal Settling

To compute the influence on the linear settling response, the time constant τ is calculated. For simplicity, a single-pole system is considered [40] with $H(s) = A_{OL}/(1 + s/\omega_d)$. Defining $A_{CL}(s) = H(s)/(1 + \beta H(s))$ the closed-loop transfer function with β the feedback factor, once substituted $H(s)$ becomes

$$A_{CL}(s) = \frac{A_{OL}}{1 + \beta A_{OL}} \cdot \frac{1}{\frac{s}{(1 + \beta A_{OL})\omega_d}} \quad (15)$$

were $\tau = 1/(1 + \beta A_{OL})\omega_d$. For a unity-gain feedback factor $\beta = 1$, $\tau \approx 1/\omega_{GBW} = C_L/G_m$, and the time constant is

$$\tau \approx \frac{C_L}{A_I g_{m,in}} \quad (16)$$

where the output response for a unity input step $V_{in} = u(t)$ can be expressed as

$$V_{out}(t) \approx \frac{A_{OL}}{1 + A_{OL}}(1 - e^{-t/\tau}). \quad (17)$$

C. Non-Linear Large-Signal Settling

To evaluate the non-linear settling performance, the slew rate is analyzed. Upon application of a large input step $V_{id} = V_{in+} - V_{in-}$, two differential currents are delivered by the input pair, which are defined in weak inversion as

$$I_{d1} = I_{1A} - I_{2A} = 2\alpha I_b tanh\left(\frac{V_{id}}{2nV_t}\right) \quad (18)$$

$$I_{d2} = I_{1B} - I_{2B} = 2(1 - \alpha) I_b tanh\left(\frac{V_{id}}{2nV_t}\right). \quad (19)$$

When $V_{id} > 0$, both differential currents can be approximated by $I_{d1} \approx I_{1A}$ and $I_{d2} \approx I_{1B}$, with $I_{2A} \approx I_{2B} \approx 0$, turning off transistors M_{9A}, M_{9B} and M_{11A} as well as the right-side circuit. Consequently, I_{d1} flows through M_7 and M_{11B}. Last conditions reduce $V_{gs9A,9B}$ and consequently, V_{gs11B} and V_{ds7}, boosting V_{gs5} and output current I_5, where $I_6 \approx 0$. Thus, the output current is $I_{out} = I_5 - I_6 \approx I_5$. In a similar manner, when $V_{id} < 0$, $I_{d1} \approx -I_{2A}$ and $I_{d2} \approx -I_{2B}$, with $I_{1A} \approx I_{1B} \approx 0$, boosting V_{gs6} and output current I_6, where $I_5 \approx 0$ and $I_{out} = I_5 - I_6 \approx -I_6$. Consequently, once substituted equation (18) as input current in (7), the approximated slew rate for the non-linear strong inversion region is

$$SR = \frac{I_{out}}{C_L} \approx \pm \frac{2\alpha^2 {I_b}^2 K_1}{\beta_7 {V_{ds7}}^2 C_L} tanh^2\left(\frac{V_{id}}{2nV_t}\right) \quad (20)$$

where $I_{out} > 0$ when $V_{id} > 0$ and $I_{out} < 0$ when $V_{id} < 0$. Since the current boosting is produced at the output branch, current efficiency, which is expressed as $CE = |I_{out}|/(|I_{out}| + 2I_b)$ [13], is near its optimal value of 1 since $|I_{out}| \gg 2I_b$ under dynamic conditions.

D. Noise

Both thermal and flicker noise are considered, whose spectral densities are defined in a MOS device as

$$\overline{V_n^2}(f) = \frac{4kT\gamma}{g_m} + \frac{K_{P/N}}{C_{ox} WLf} \quad (21)$$

where k is the Boltzmann's constant, T is the temperature, γ is equal to $1/3$ in weak inversion and $2/3$ in strong inversion [41], $K_{P/N}$ is the flicker noise coefficient for a PMOS or NMOS transistor, respectively, and f is the frequency. The first and second terms corresponds to the thermal and flicker noise densities, respectively. Assuming all noise sources are uncorrelated, the input referred thermal and flicker noise density expressions are

$$\overline{V_{T,in}^2} = \frac{8kT\gamma}{g_{m,in}}\left[1 + \frac{g_{m3}}{g_{m,in}}\frac{1}{{A_I}^2} + \frac{g_{m5}}{g_{m,in}}\left(\frac{1}{{A_I}^2} + \frac{1}{K_{1eff}}\right) + \frac{g_{m9B}}{g_{m,in}}(1 + K_2) + \frac{g_{m11A} + g_{m11B}}{g_{m,in}}\right] \quad (22)$$

$$\overline{V_{F,in}^2(f)} = \frac{2K_P}{C_{ox} f}\left[\frac{1}{W_{in}L_{in}} + \frac{1}{{A_I}^2}\left(\frac{g_{m3}}{g_{m,in}}\right)^2 \frac{1}{W_3 L_3} + \frac{K_N}{K_P}\left(\frac{1}{{A_I}^2} + \frac{K_1}{{K_{1eff}}^2}\right)\left(\frac{g_{m5}}{g_{m,in}}\right)^2 \frac{1}{W_5 L_5} + \frac{K_N}{K_P}(1 + K_2)\left(\frac{g_{m9B}}{g_{m,in}}\right)^2 \frac{1}{W_{9B} L_{9B}} + \frac{K_N}{K_P}\left(\frac{g_{m11A} + g_{m11B}}{g_{m,in}}\right)^2 \frac{1}{W_{11A} L_{11A}}\right]. \quad (23)$$

In the above analysis, and with the intention of simplifying the equations, it has been assumed that both left and right circuit parts are perfectly symmetrical: $g_{m1A} = g_{m2A}$, $g_{m1B} = g_{m2B}$,

$g_{m3} = g_{m4}$, $g_{m5} = g_{m6}$, $g_{m7} = g_{m8}$, $g_{m9A} = g_{m10A}$, $g_{m9B} = g_{m10B}$, $g_{m11A} = g_{m12A}$ and $g_{m11B} = g_{m12B}$. These conditions allow calculating noise for a half-circuit and subsequently, doubling its value to model the full noise response. Symmetry can be enforced by proper layout techniques, such as interdigitation, common-centroid strategies or dummy devices, among others. In addition, by increasing transistor lengths, the mismatch robustness is improved. Regarding the splitted differential input pair: $W_{1A}L_{1A} = \alpha W_{in}L_{in}$ and $W_{1B}L_{1B} = (1-\alpha)W_{in}L_{in}$ where $W_{in}L_{in}$ is the non-splitted input pair channel area and $L_{1A} = L_{1B} = L_{in}$. For the inner current mirrors of NL-NCM: $g_{m5} = K_{1eff} \cdot g_{m7}$ and $W_5L_5 = K_1 \cdot W_7L_7$ where $L_5 = L_7$ (it is should be pointed how K_{1eff} is the effective aspect ratio that in turn depends on NL-NCM bias point as well as the aspect ratio K_1); and $g_{m9A} = K_2 \cdot g_{m9B}$ and $W_{9A}L_{9A} = K_2 \cdot W_{9B}L_{9B}$ where $L_{9A} = L_{9B}$. Finally, $W_{11A}L_{11} = W_{11B}L_{11}$ with $L_{11A} = L_{11B}$. Remark how in those matching conditions, transistor lengths are selected to be equal to simplify the calculations and increase mismatch robustness, as previously mentioned. As expected, input-referred noise is minimized by maximizing transconductance and channel area of input transistors. Note also that due to the small-signal current gain A_I and the effective aspect ratio K_{1eff} of non-linear nested current mirror, output branch transistors have less influence on input-referred noise.

E. Amplifier Trade-Offs

As seen, variable V_{DS} is very useful to extend the properties of NL-NCM OTA. In general terms, it controls current gain A_I, which in turn is related with the overall transconductance $G_m = A_I g_{m,in}$, gain-bandwidth product $\omega_{GBW} = G_m/C_L$, settling time constant $\tau \approx C_L/G_m$ and DC gain $A_V = G_m r_{out}$ where r_{out} is the OTA output resistance. Note also how input-referred noise is reduced when A_I increases. As V_{DS7} is reduced, gain A_I increases due to non-linear current mirror behavior, thus improving last characteristics. On the contrary, power consumption increases with A_I. In addition, the amplifier's phase margin PM also depends on A_I, compromising its closed-loop stability. In conclusion, a reduction in V_{DS7} implies an increment in A_I, thus G_m, ω_{GBW}, ST, A_V and noise are improved, whereas DC static power consumption and PM are degraded. Under dynamic conditions, as V_{DS7} approaches zero, output current is at its maximum driving capability.

An important consideration is the mismatch and PVT variations of V_{DS7}. For high values (e.g., $V_{DS7} = 100$ mV, in which M_7 is in saturation), the OTA is more robust but potential for small-signal performance enhancement is not fully exploited. By contrast, for low values (e.g., $V_{DS} = 26$ mV, in which M_7 is in the limit between saturation and triode) sensitivity to PVT and mismatch is worse but small-signal behavior is improved. Hence, V_{DS7} leads to a trade-off between small-signal performance, power consumption and PVT and mismatch sensitivity. Concerning large-signal performance, it is similar for both V_{DS} configurations as large V_{DS7} swings take place.

F. PVT and Mismatch Considerations

As mentioned previously, a trade-off between performance, PVT and mismatch exists in the circuit that the designer should handle. Regarding the process variations, it can be seen from (9) how the circuit is robust to them as V_{DS7} does not depend on process parameters. Since a translinear loop is applied in the NL-NCM, the dependence on V_{TH} is cancelled thus improving robustness against process variations. However, parametric and geometric mismatch may modify V_{DS} , thus influencing small-signal performance (mainly GBW). Moreover, dependence of temperature through V_t may alter both DC static as well as small-signal conditions. In addition, the bulk effect in M_{11A}-M_{11} and M_{12} -M_{12B} can also degrade performance.

As a conclusion, the circuit is robust against process variations but exhibits variability in terms of temperature and mismatch. Simulation results are provided in Section V validating this conclusion.

Large enough channel areas in transistors, as well as interdigitation or common centroid techniques and dummy devices in those transistors requiring matching allow minimizing such mismatch. The use of a properly calibrated PTAT voltage V_{PR} can compensate for temperature variations.

G. Design Guidelines

The procedure followed to design the OTA is described here (referring to the left-half circuit for simplicity). Tail current $2I_b$ is chosen so that all transistors operate in weak inversion. Due to the splitted differential pair, DC currents are $I_{1A} = \alpha I_b$ and $I_{2B} = (1-\alpha)I_b$. Since $I_7 = I_{1A} - K_2 I_{2B}$ and $I_7 > 0$ to properly bias NL-NCM OTA, therefore $I_{1A} > K_2 I_{1B}$ or equivalently, $\alpha > K_2(1-\alpha)$. Hence $K_2 < \alpha/(1-\alpha)$ is required. A simple choice is $K_2 = 1$, so that pole associated to node D is at high frequencies, well-beyond ω_{pA} and ω_{pB}. Moreover, if $K_2 = 1$, then $I_{9A} = I_{9B} = I_{11A}$, so poles at nodes C and D are similar ($\omega_{pC} \approx \omega_{pD}$) Additionally, this choice keeps a low area and improves matching if high-performance layout techniques are employed.

Once selected $K_2 = 1$, then $\alpha > (1-\alpha)$, i.e., $\alpha > 0.5$, which can be achieved by $(W/L)_{1A} > (W/L)_{2B}$. Defining $\delta = (W/L)_{1A}/(W/L)_{2B} = \alpha/(1-\alpha)$, this condition is satisfied for $\delta > 1$. To keep DC current symmetry in the inner NL-NCM branches, $I_7 = I_{9A}$ is chosen. Since $K_2 = 1$, $I_{9A} = I_{9B} = I_{2B} = (1-\alpha)I_b$.

Hence $I_{1A} = I_7 + I_{9A} = 2I_{2B}$, leading to $\delta = 2$ and $\alpha = 2/3$. Next, since K_1 increases both A_i (thus G_m, ω_{GBW}, ST, A_V and noise) and SR, but also increases the quiescent current at the output branch, area and phase margin, a tradeoff on the choice of K_1 arises. The optimal value depends on the design constraints of the target application. Here $K_1 = 2$ is selected.

The final design parameter is V_{DS7}.The choice of $V_{DS} = 26$ mV sets the transistor between saturation and triode regions, yielding a high A_I with little power degradation. Besides, it leads to spaced poles at nodes A and B ($\omega_{pB} > \omega_{pA}$), thus preserving closed-loop stability. As mentioned above, its value can be properly set by the ratio $x = (W/L)_{11\ ,11B}/(W/L)_{7,9A}$. As $I_{1A} = 2I_{2B}$, $x = 1.9477 \approx 2$ according to (9). This design

TABLE I
ANALYTICAL COMPARISON BETWEEN CM, NCM AND NL-NCM OTAS

Parameter	CM	NCM	NL-NCM
$g_{m,in}$	$g_{m1,2}$	$g_{m1A,2A}+g_{m1B,2B}=\alpha g_{m1,2}+(1-\alpha)g_{m1,2}$	$g_{m1A,2A}+g_{m1B,2B}=\alpha g_{m1,2}+(1-\alpha)g_{m1,2}$
A_I	K_1	$K_1(\alpha+[1-\alpha]K_2)$	$\frac{K_{1eff}}{g_{m11B}r_{o7}}\left(\alpha[1+g_{m11B}r_{o7}]+[1-\alpha]\left[K_2+\frac{g_{m11B}}{g_{m9B}}[1+g_{m9A}r_{o7}]\right]\right)$ $\begin{cases}A_{I,SAT}=K_1(\alpha+[1-\alpha]K_2) & , \quad g_{m7}r_{o7}\gg 1\\ A_{I,TRI}=\frac{K_{1eff}}{g_{m11B}r_{o7}}\left(\alpha+[1-\alpha]\left[K_2+\frac{g_{m11B}}{g_{m9B}}\right]\right), & g_{m7}r_{o7}<1\end{cases}$
I_{DC}^{Q}	$2I_b+2I_bK_1$	$2I_b+2I_bK_1(\alpha-[1-\alpha]K_2)$	$2I_b+2I_bK_1(\alpha-[1-\alpha]K_2)\left(\frac{1}{1-e^{-V_{DS7}/V_t}}\right)$
I_{out}	$2I_bK_1$	$2\alpha I_bK_1$	$\frac{K_1}{2\beta_7}\left(\frac{2\alpha I_b}{V_{DS7}}\right)^2$
CE	$K_1/(1+K_1)$	$\alpha K_1/(1+K_1(\alpha-[1-\alpha]K_2))$	$\lvert I_{out}\rvert/(\lvert I_{out}\rvert+2I_b)\approx 1$

† I_{DC}^{Q} refers to the total current dissipation and σ_{PVT} to mismatch robustness.

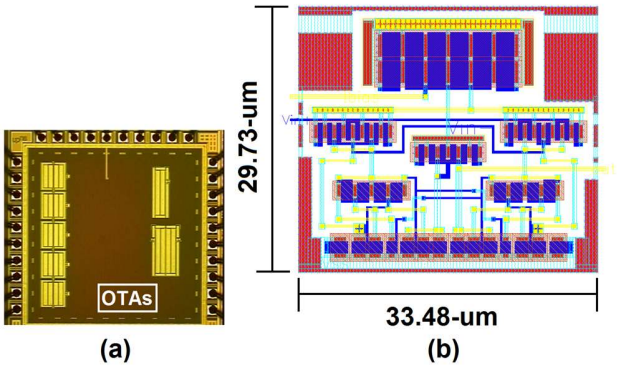

Fig. 6. (a) Test chip microphotograph and (b) OTA layout.

TABLE II
TRANSISTOR ASPECT RATIOS

Transistor	Dimension (μm/μm)
M_{1A}, M_{2A}	4x(1.50/0.50)
M_{1B}, M_{2B}	2x(1.50/0.50)
M_3, M_4	2x(1.30/0.65)
M_5, M_6	2x(1.30/1.30)
M_7, M_8, M_{9A}, M_{9B}, M_{10A}, M_{10B}	1x(1.30/1.30)
M_{11A}, M_{11B}, M_{12A}, M_{12B}	2x(1.30/1.30)

method has been used in the fabricated chip. Remember that V_{DS7} should satisfy a $V_{GS5,7}<V_{TH}$ to maintain the weak inversion operation in DC static conditions. In order to improve the mismatch robustness, the channel area of the transistors should be increased.

IV. COMPARISON BETWEEN CM, NCM AND NL-NCM OTAS

Once described the NL-NCM OTA, it is important to compare it with the CM and NCM OTAs, which are the starting point of the proposed OTA.

Table I summarizes the main performance parameters of CM, NCM and NL-NCM OTAs. The amplifiers have the same bias current $2I_b$, as depicted in Figs. 1 and 2. Despite the distributed nature of the nested OTAs differential pairs, note how the three OTAs have the same non-splitted $g_{m,in}$. Regarding current gain A_I, note the improvement in NCM and NL-NCM OTAs with respect to CM OTA. This is due to the in-phase AC sum of input pair's splitted transconductances, which improves small-signal performance for the same power consumption as the CM OTA.

Regarding NL-NCM, it extends the properties of NCM since it includes the additional V_{DS7} design variable. If M_7 is in saturation, the small-signal performance is the same as NCM. However, as M_7 enters triode region, A_I is boosted, at the cost of degrading power consumption and PM.

Another important aspect is the static DC current dissipation. Notice how both NCM and NL-NCM OTAs have a lower dissipation than CM OTA (for $\alpha>0.5$ and a well-balanced A_I for the non-linear amplifier). This allows increasing K_1 to equalize power consumptions, with the corresponding increment in A_I. Regarding output current drivability, note the class-A nature of CM and NCM OTAs since output current is bounded by $2I_b$ (or the scaled version by K_1), limiting its usability in high-performance driving scenarios. If high output currents are desired, K_1 should be increased, degrading static power consumption. By contrast, NL-NCM OTA operates in class AB, avoiding the current limitation with the same static power. This aspect can be quantified by the current efficiency CE, defined as the maximum output current with respect to the total current. This is very important in low-power scenarios as not only considers the static power dissipation, but also the dynamic current utilization. In both CM and NCM OTAs, the only way to improve CE is by increasing K_1, which in general terms degrades power, as mentioned. The main benefit of NL-NCM OTA is that maximum output current under dynamic conditions is much higher than the class-A cases, while having the same DC power consumption. What is more, boosting is produced at the output branch, leading to a highly power-efficient topology since no internal dynamic current replications are employed.

The main drawback of NL-NCM OTA is the inherent process and temperature variability of V_{DS7}, especially if low values are desired. The variability may alter A_I, and hence G_m, GBW, PM, ST, A_V, noise, and DC power. By this reason, it should be well-controlled as discussed in Section II.D.

As a final remark, note that both NCM and NL-NCM OTAs can be extended with additional nested stages. This is discussed in [24] for the NCM, extending the number of nested stages to three and four, and hence, generalizing the nested principle with additional in-phase AC sums. The proposed solution could be used in [24] also in these cases, turning them into class-AB OTAs.

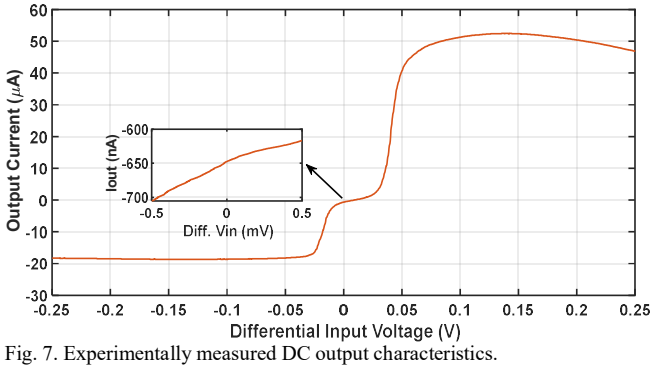

Fig. 7. Experimentally measured DC output characteristics.

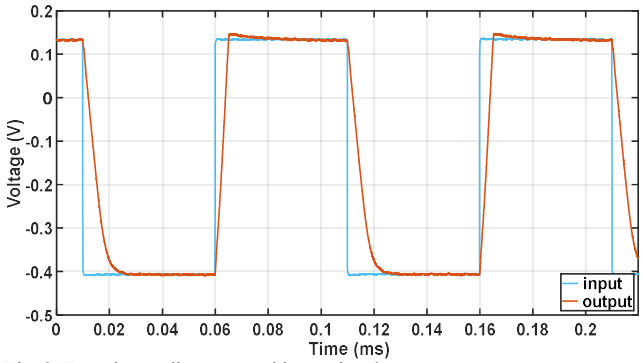

Fig. 8. Experimentally measured large-signal response.

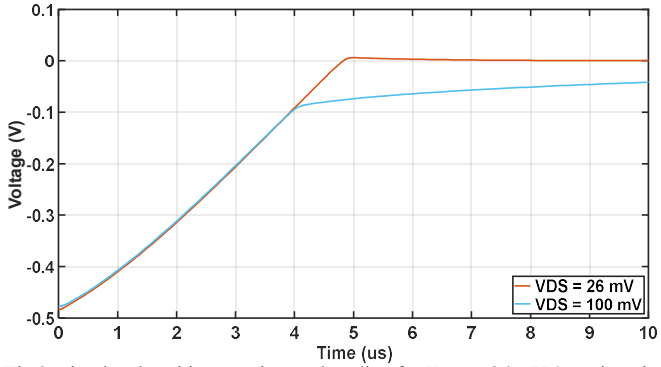

Fig.9. Simulated positive transient and settling for $V_{DS7} = 26$ mV (transistor in triode) and $V_{DS7} = 100$ mV (transistor in saturation). $V_{DS7} = 100$ mV was controlled by an ideal V_{PR} in simulations.

V. Measurement and Simulation Results

A test chip prototype was fabricated in UMC 180-nm CMOS process that contains the proposed NL-NCM OTA to validate experimentally the design. The device was loaded off-chip with 160 pF, which includes the pad, breadboard, and test probe capacitance, respectively. The chip microphotograph and layout are shown in Fig. 6.

The OTA was fabricated in open-loop and unity-gain closed-loop configurations in order to fully characterize it. The transistor aspect ratios are shown in Table II. In order to increase the robustness against mismatch and PVT variations, the transistor lengths have been increased in the inner NL-NCM. The supply voltage was ±0.5 V and I_b was 500 nA. In this way, all transistors were biased in weak inversion. The differential pair was splitted by a factor $\delta = 2$ ($\alpha = 2/3$), and the current mirror ratios were $K_1 = 2$ and $K_2 = 1$. Finally, V_{DS} was set to 26 mV in the limit of saturation and triode regions to exploit non-linear behavior of current mirror, which was achieved by selecting $x = 2$. For simplicity, and with the aim of reducing the static power consumption, area and circuit complexity, the programmable voltage source V_{PR} was not included in the fabricated device, therefore $V_{PR} = 0$ V.

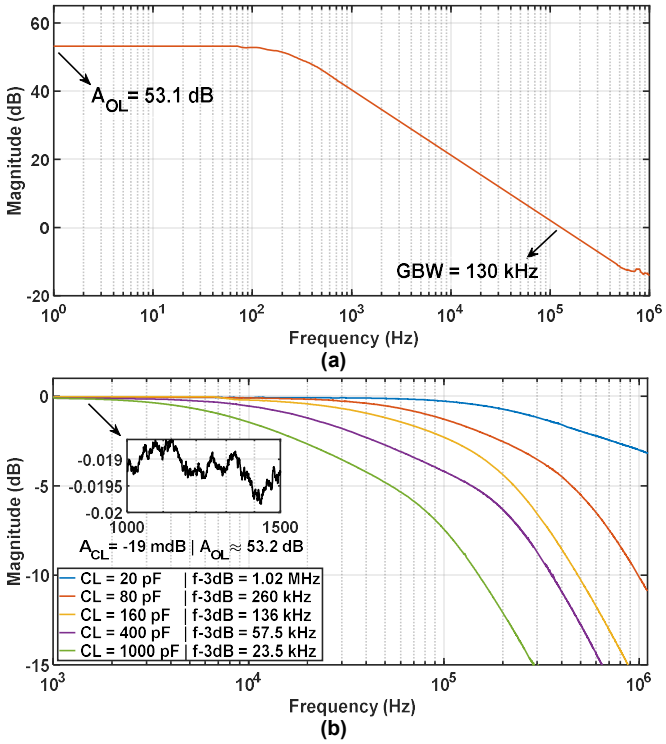

Fig. 10. Experimentally measured (a) open-loop for $C_L = 160$ pF and (b) closed-loop unity-gain frequency response for different capacitive loads.

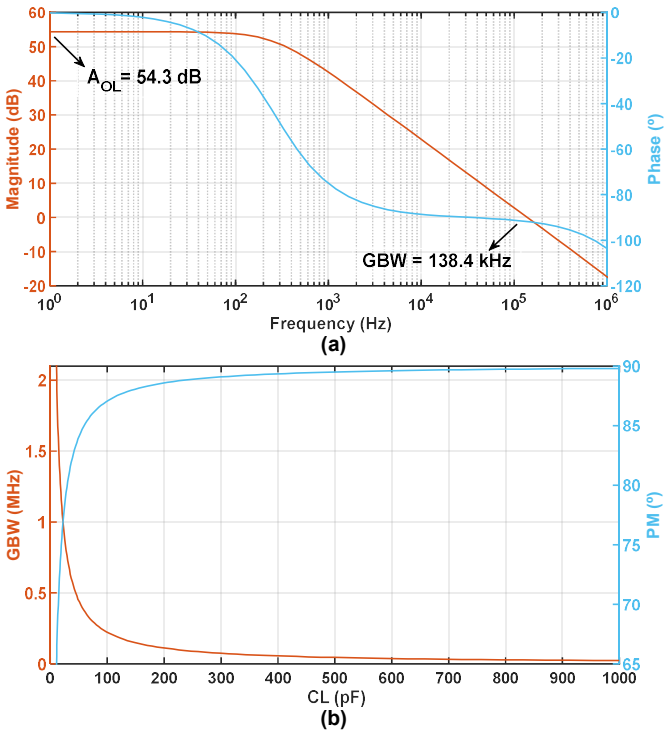

Fig. 11. Simulated (a) open-loop for $C_L = 160$ pF and (b) $GBW|PM$ vs C_L.

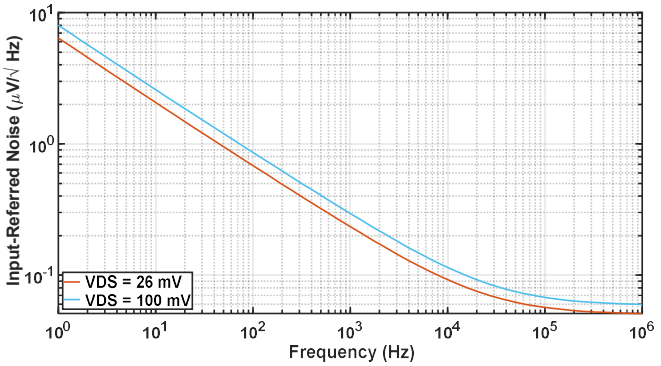

Fig. 12. Simulated input-referred noise for different V_{DS7} values. V_{DS7} = 100 mV was controlled by an ideal V_{PR} in simulations.

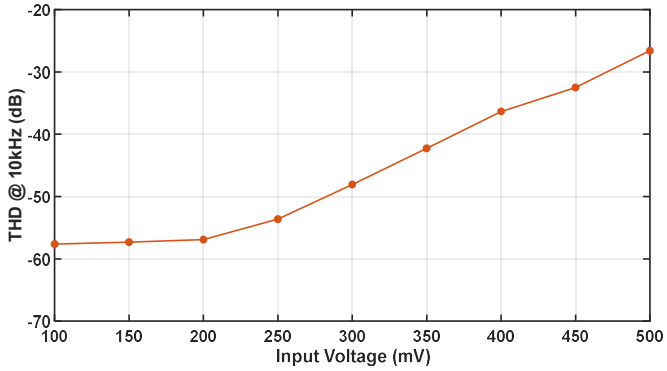

Fig. 13. Experimentally measured THD vs V_{in}.

TABLE III
MEASUREMENT OF 5 SAMPLES UNDER SUPPLY VARIATIONS

Supply Voltage	Parameter	Min	Avg.	Max
±0.45 V	SR+ [V/μs]	70.3	72.9	74.5
	SR− [V/μs]	30.4	32.6	34.3
	GBW [kHz]	100.9	108.6	127.4
±0.5 V	SR+ [V/μs]	102.3	104.8	110.6
	SR− [V/μs]	50.1	54.3	58.0
	GBW [kHz]	129.2	132.8	139.8
±0.55 V	SR+ [V/μs]	142.5	145.2	147.8
	SR− [V/μs]	82.6	86.5	91.9
	GBW [kHz]	148.6	157.3	168.0

† C_L = 160 pF .

Fig. 7 shows the measured DC open-loop output current vs differential input voltage generated by an Agilent 33522A arbitrary waveform generator. In order to measure it, a transimpedance amplifier was connected to the output for current-to-voltage conversion [42]. The resulting response was measured in a Tektronix MSO44 oscilloscope. Notice the class-AB operation, with an output current not limited by the bias current. This way, the current boosting factor (CB), i.e. the ratio between the maximum output current and bias current, $CB = I_{out}^{MAX}/2I_b \approx 52$, that is computed with the maximum output current $I_{out}^{MAX} \approx 52$ μA and the tail current $2I_b$ = 1 μA. Maximum current is limited by supply rails due to the large gate-to-source voltages of output transistors M_5 and M_7, as modelled in equation (8).

In order to characterize the slew rate, the unity-gain configuration was used with a 540 mV, 10 kHz square input signal. Fig. 8 shows the measured response. The positive and negative slew rates were 110 V/ms and −58 V/ms, respectively. Notice the asymmetry in both values, being consistent with the open-loop DC current response.

TABLE IV
CORNER SIMULATIONS FOR PROCESS AND TEMPERATURE VARIATIONS

T = 27º

Parameter	TT	FF	SS	SF	FS
SR+ [V/ms]	108.2	134.4	85.7	109.4	103.1
SR− [V/ms]	54.2	55.0	51.9	38.5	67.3
GBW [kHz]	138.4	137.2	141.7	141.9	136.6
PM [º]	88.2	88.3	88.0	88.1	88.3
DC gain [dB]	54.3	54.0	54.7	54.4	54.2
CMRR (DC) [dB]	108.0	111.3	104.0	116.0	104.5
PSRR+ (DC) [dB]	54.5	54.2	54.9	54.6	54.4
PSRR− (DC) [dB]	91.2	91.0	91.4	91.0	94.2
Power [μW]	≈2.9	≈2.9	≈2.9	≈2.9	≈2.9

T = 120º

Parameter	TT	FF	SS	SF	FS
SR+ [V/ms]	96.1	116.8	77.9	90.1	95.8
SR− [V/ms]	41.6	42.2	40.0	31.1	53.4
GBW [kHz]	109.3	106.9	111.9	110.7	107.5
PM [º]	88.4	88.5	88.2	88.3	88.4
DC gain [dB]	53.5	53.0	54.0	53.5	53.5
CMRR (DC) [dB]	123.5	140.8	116.7	110.0	110.9
PSRR+ (DC) [dB]	53.7	53.2	54.2	53.7	53.7
PSRR− (DC) [dB]	90.3	90.0	90.6	89.6	90.6
Power [μW]	≈2.9	≈2.9	≈2.9	≈2.9	≈2.9

T = −40º

Parameter	TT	FF	SS	SF	FS
SR+ [V/ms]	117.7	147.4	91.7	125.1	108.9
SR− [V/ms]	69.3	70.4	66.7	50.2	80.9
GBW [kHz]	165.8	162.7	169.3	169.7	161.9
PM [º]	88.2	88.3	88.0	88.1	88.2
DC gain [dB]	54.4	54.1	54.7	54.5	54.3
CMRR (DC) [dB]	102.0	105.6	96.7	105.8	99.0
PSRR+ (DC) [dB]	54.6	54.3	54.9	54.7	54.5
PSRR− (DC) [dB]	90.9	90.8	91.0	90.9	90.8
Power [μW]	≈2.9	≈2.9	≈2.9	≈2.9	≈2.9

Fig. 9 compares the simulated settling response for two cases: V_{DS7} = 26 mV (transistor on the edge of saturation and triode) with $A_i \approx 10.1$; and V_{DS7} = 100 mV (transistor in saturation) with $A_i \approx 1.1$ to see the effect of V_{DS} in amplifier's performance. It can be seen how current gain is increased approximately 10 times for a reduced V_{DS7}. For the case of V_{DS7} = 26 mV, it was controlled by x = 2 with V_{PR}= 0 V, whereas the case of V_{DS7} = 100 mV employed x = 2 as well as V_{PR} = 100 mV, which was implemented by an ideal voltage source in simulations. Notice how, as predicted in Sections II and III, a smaller V_{DS} enhances both A_i and G_m, reducing the time required by the output to reach a final value closer to the input. Therefore, the settling time is reduced, and the settling accuracy is increased. Note also how slew rate remains almost equal for both cases, mainly produced by $V_{DS7} \approx 0$ V under large-signal conditions.

The measured open-loop frequency response is shown in Fig.

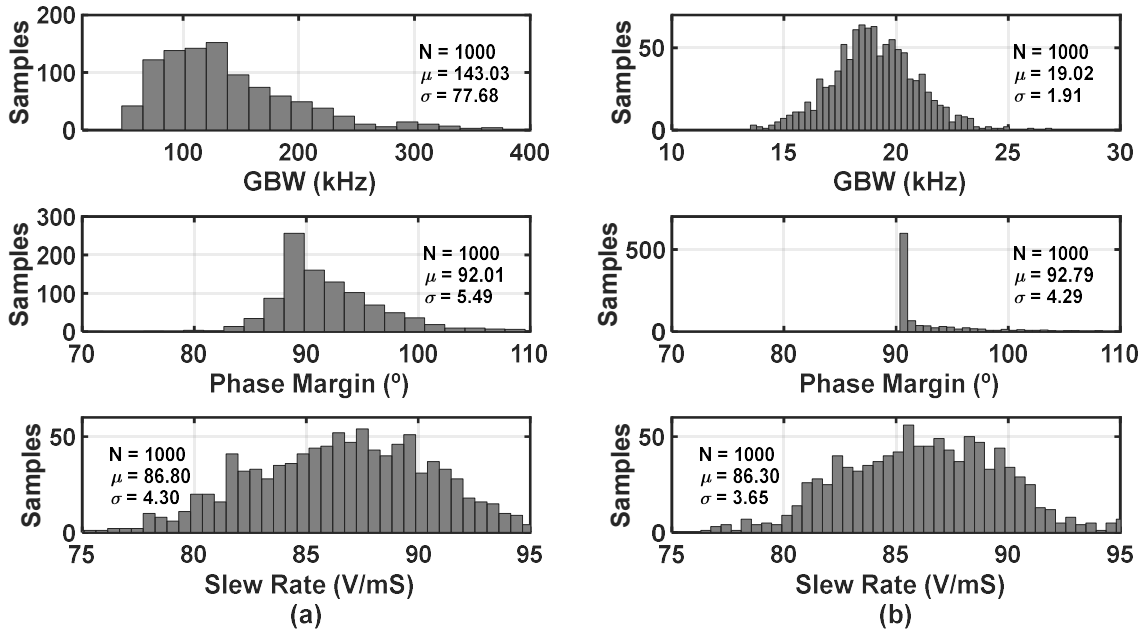

Fig. 14. GBW, PM and SR process and mismatch Monte-Carlo simulations for (a) $V_{DS7} = 26$ mV and (b) $V_{DS7} = 100$ mV. $V_{DS7} = 100$ mV was controlled by an ideal V_{PR} in in simulations.

10(a) for $C_L = 160$ pF. The open-loop gain was $A_{OL} \approx 53.1$ dB and $f_{GBW} = 130$ kHz, which were obtained by the method proposed in [43]. The measured closed-loop unity-gain frequency response for different capacitive loads is shown in Fig. 10(b). The closed-loop unity gain was $A_{CL} \approx -19$ mdB. Since $A_{CL} \approx A_{OL}/(1 + A_{OL})$, the extrapolated open-loop gain is 53.2 dB, both open- and extrapolated closed-loop gains being consistent with each other. For $C_L = 160$ pF, the closed-loop −3 dB bandwidth was 136 kHz with an approximate phase of −45º. Therefore, the extrapolated phase margin is 90º. This is a good approximation to GBW and PM due to the strongly dominant pole at the output terminal.

To confirm last results, the simulated open-loop frequency response for $C_L = 160$ pF is given in Fig. 11(a), in which $A_{OL} \approx$ 54.3 dB and $f_{GBW} = 138.4$ kHz with $PM = 88.2$º. The simulated open-loop GBW and PM for different capacitive loads is shown in Fig. 11(b), demonstrating the wide driving capability of the proposed OTA.

Regarding power, current gain and gain-bandwidth product, the fabricated device with $V_{DS} = 26$ mV has $P = 2.9$ µW, $A_i \approx$ 10.1 and $f_{GBW} \approx 136.0$ kHz, respectively. By contrast, when $V_{DS7} = 100$ mV, $P = 1.9$ µW, $A_i \approx 1.1$ and $f_{GBW} \approx 18.0$ kHz, demonstrating how the NL-NCM improves the amplifier's performance mainly due to the increase in current gain. In order to equalize the GBW performance of both devices, the bias current should be increased 10 times in last case, leading to $P = 26.6$ µW, $A_i \approx 1.1$ and $GBW \approx 132$ kHz. It can be seen how GBW is increased at the cost of degrading power consumption.

The simulated input-referred noise for different V_{DS7} values is depicted in Fig. 12. Notice how noise is reduced when $V_{DS} = 26$ mV, which is due to the increase in current gain. This confirms the theoretical prediction in equations (22) and (23). Remember that $V_{DS} = 100$ mV was set by an ideal V_{PR} in simulations.

Fig. 13 shows the measured total harmonic distortion (THD) for an input sinusoid of 10 kHz and peak-to-peak input amplitudes ranging from 100 mV to 500 mV, obtained with the unity-gain closed-loop configuration. It can be seen how linearity is degraded for higher input values, mainly produced by the limited input range.

In Fig. 14, a Monte-Carlo simulation shows the effects of process and mismatch variations in terms of GBW, PM and SR for different V_{DS7} (26 mV and 100 mV) obtained for a run of 1000 simulations. As seen, the GBW variability for $V_{DS7} = 26$ mV is higher due to the increased sensitivity. By contrast, phase margin exhibits less variations, mainly due to the high capacitive load that approximates OTA to a single-pole amplifier, as mentioned. It is worth mentioning how both average GBW and PM mean values are in good agreement with measurements and simulations. When $V_{DS7} = 100$ mV, the GBW mismatch robustness is higher. However, the GBW achieved is reduced, demonstrating the performance vs mismatch sensitivity trade-off. In the case of SR, the variability is low, with practically equal values in both cases. This is produced by the non-linear large-signal behavior that leads to $V_{DS7} \approx 0$ V under dynamic conditions in both configurations. Finally, the standard deviations of input offset for $V_{DS7} = 26$ mV and $V_{DS} = 100$ mV are 3.27 mV and 4.10 mV, respectively, for a run of 1000 simulations. In order to confirm the Monte-Carlo simulations, the measurement of 5 die samples for $C_L = 160$ pF are given in Table III, where the supply voltage has been varied ±10% around its nominal value. In this case, simulations correspond to the unity-gain closed-loop configuration. Finally, the simulated corner of the circuit variability against process and temperature is summarized in Table IV.

Several conclusions can be obtained with both corner and Monte-Carlo simulations. The corner analysis reveals how the

TABLE V
MEASURED CLASS-AB NL-NCM OTA PERFORMANCE PARAMETERS AND COMPARISON

Parameter	[18]	[24]	[19]	[44]	[45]	[42]	[46]	[47]	This work
Year	2007	2015	2016	2016	2018	2018	2020	2021	2022
CMOS process [µm]	0.5	0.18	0.18	0.18	0.5	0.5	0.18	0.18	0.18
Supply voltage [V]	± 1	1.2	1.8	1.1	± 1	± 1	0.8	0.5	± 0.5
Capacitive load [pF]	80	150	200	100	70	70	130	150	160
Stage Type	Single	Nested-Single	Single	Pseudo-Single	Single	Single	Single	Single	Nested-Single
Class Type	Super-AB	A	AB	AB	AB	Super-AB	Super-AB	Digital-AB	AB
Pos. Slew Rate [V/µs]	20	0.0256	74.1	8.7	9.8	13.2	1.24	0.019	0.110
Neg. Slew Rate [V/µs]	-54	--	--	--	-7.6	-25.3	-0.826	--	-0.058
Pos. settling (1%) [µs]	--	20.8	--	1.2	0.096	0.12	0.55	--	17.3
Neg. settling (1%) [µs]	--	--	--	--	0.074	0.10	0.56	--	16.2
GBW [MHz]	3.46	0.283	86.5	1.7	4.75	3.4	1.12	0.0575	0.136
PM [º]	58	86.4	50	69	60	75.1	67.9	90	90
THD [dB]	-41.0 @100 kHz 900 mV_{pp}	--	--	--	-41.0 @100 kHz 1 V_{pp}	-55.5 @25 kHz 500 mV_{pp}	-56.3 @10 kHz 100 mV_{pp}	-40.0 @2.5 Hz 75 mV_{pp}	-48.0 @10 kHz 300 mV_{pp}
Eq. Input Noise [nV/√Hz]	44.7 @100 kHz	430 @0.1 kHz	0.8 @100 kHz	--	35 @1 MHz	35 @1 MHz	68.8 @100 kHz	--	86.3 @100 kHz
DC gain [dB]	39	72	72	100	81.7	76.8	102.7	73.0	56.1
CMRR (DC) [dB]	70	--	--	--	78	112	137.7	65.0	103.1
PSRR+ (DC) [dB]	37	--	--	--	72	92	114.8	50.0	56.7
PSRR− (DC) [dB]	70	--	--	--	74	113	136.9	--	90.1
Input offset [mV]†	--	--	--	--	6	--	1.24	--	5.3
Power [µW]	140	3.6	11900	7.4	120	100	36	0.1075	2.9
Area [mm^2]	0.054	0.0013	0.070	0.0021	0.024	0.030	0.021	0.00098	0.0010
FOM_L [(V/µs)(pF/µW)]	21.14	1.07	1.25	117.57	5.08	13.48	3.73	26.5	4.63
FOM_S [(MHz)(pF/µW)]	1.98	11.79	1.45	22.97	2.77	2.38	4.04	80.2	7.50
FOM_{AL} [FOM_L/mm^2]	391.53	820.51	17.79	55985	211.46	449.17	177.63	27040	4630
FOM_{AS} [FOM_S/mm^2]	36.61	9071	20.77	10940	115.45	79.33	192.59	81836	7500

† Averaged with 10 chips.
* All performance parameters have been experimentally measured.

circuit is robust against process variations. For a given temperature, the performance does not suffer large deviations. This is due to the translinear loop in NL-NCM that cancels the dependence on V_{TH}, as mentioned. Regarding temperature, as expected from (9), it alters the thermal voltage V_t, thus modifying V_{DS7} and therefore the global performance between the three selected temperatures (−40º, 27º and 120º). The Monte-Carlo analysis considers both process and mismatch variations. As the circuit is robust against process variations, it can be concluded that the device is only sensitive to mismatch. The temperature variations can be compensated by making V_{PR} PTAT, and the geometric mismatch by increasing the channel lengths of transistors. Since the circuit exhibits a small area with transistors requiring a very close matching and interdigitation, large geometric mismatch is avoided. This has been corroborated in Table III with the measure of 10 fabricated devices, exhibiting all amplifiers similar characteristics.

Table V summarizes the main experimentally measured parameters and compares them with other existing OTAs. In order to compare quantitatively the OTA performance with other reported designs, the following well-known two couples of figures-of-merits are used

$$FOM_L = SR\frac{C_L}{P} \tag{24}$$

$$FOM_S = GBW\frac{C_L}{P}. \tag{25}$$

The equations reflect the amplifier's performance in terms of large- and small-signal operation for a given capacitive load C_L and power P, respectively. Note that large-signal behavior of the proposed OTA is improved when it is compared to the original NCM amplifier [24]. This is due to the class A nature of the original circuit, in contrast to the proposed class-AB approach. GBW in [24] is higher as three nested-stages are employed, increasing bandwidth by an additional nested current mirror aspect ratio. Regarding other reported designs, they have been selected since they employ the class-AB approach for driving large capacitive loads. Although [18], [42] and [45] present higher FOM_L, their supply voltages are twice the proposed OTA, so node excursions are wider and boosted driving currents are subsequently higher. In addition, the CMOS process is different. Reference [44] shows the best results in terms of large-signal performance. However, the circuit includes an additional gain-booster circuit as well as several bias branches. For those applications requiring a large number of amplifiers, this would result in a significant increment in DC static power. Finally, the amplifier proposed [47] reports the best small-signal performance. This is due to ultra-low quiescent current dissipation as the OTA architecture is digital, reducing substantially the power consumption. However, the amplifier requires Muller-C elements often not found in standard digital libraries and suitable calibration strategies to combat sensitivity to PVT variations and mismatches [48].

As the proposed OTA has a low area, a couple of figure-of-merits that relate both large- and small-signal properties with area are included [24], defined as

$$FOM_{AL} = \frac{SR \cdot C_L}{P \cdot area} = \frac{FOM_L}{area} \quad (26)$$

$$FOM_{AS} = \frac{GBW \cdot C_L}{P \cdot area} = \frac{FOM_S}{area} \quad (27)$$

showing that the proposed amplifier can achieve competitive results with little silicon area, only surpassed by [24], which is the class-A nested current mirror OTA that extends the concept to three nested stages and thus increasing bandwidth by an additional aspect ratio; by [44], that includes the gain-booster circuit and several bias branches; and by [47] that is the OTA digital version. Note that the three devices exhibit areas similar to the proposed OTA.

VI. Conclusions

A novel power-efficient class-AB technique and its application to rail-to-rail output single-stage OTAs has been presented. It is based on a NL-NCM at the active load of a splitted differential pair biased in weak inversion that boosts the pair's tail current beyond its quiescent value directly at the output node, achieving a nearly ideal current efficiency. In addition to large-signal, a proper DC bias point can be set to enhance the small-signal properties of the amplifier. Operation in weak inversion allows optimal g_m/I_D operation, further improving gain and reducing power consumption. Due to low quiescent currents, high driving capability and reduced silicon area, the OTA is highly suitable for those applications requiring a high number of amplifiers such as multichannel architectures with high capacitive loads or in switched-capacitor applications.

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