Guest Editorial Special Issue on the IEEE Latin American Symposium on Circuits and Systems (LASCAS 2023)

THIS Special Issue of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS (TCAS-I) includes papers presented at the IEEE Latin American Symposium on Circuits and Systems (LASCAS). This annual symposium provides a high-quality exchange and networking forum for researchers, professionals, and students, gathering an international audience with experts from all over the world. The symposium is a space where the Circuits and Systems (CAS) community can present new concepts and innovative approaches, learn about new trends and solutions, and receive feedback from specialists in diverse fields. The 14th IEEE Latin American Symposium on Circuits and Systems (LASCAS 2023) was held in person from February 28 to March 3 in Quito, Ecuador. A subset of top-rated papers was selected for this Special Issue among all the contributions presented at the conference in poster and oral sessions. The invited papers brought new technical results and underwent a peer-review process consisting of expert reviewers on the related topics. A brief description of the two selected papers is as follows.

In [A1], Stanger et al. overview and analyze transistor operation at cryogenic temperatures and how it influences digital circuit design targeted to this regime. With these effects in mind, the use of dynamic logic families, including the classical dynamic (NORA) logic and the recently introduced dual mode logic (DML) and dual mode pass logic (DMPL) families, are examined under cryogenic operation, showcasing improved performance and power efficiency. Measurements conducted on a 16-nm FinFET test chip validate their operation at low temperatures down to 4 K, with supply voltages ranging 0.4–0.8 V. Furthermore, the considered dual mode logic families exhibit performance enhancements of up to 26% in dynamic mode and power efficiency increases up to 53% in static mode, compared with CMOS.

In [A2], da Rosa et al. investigate the design of approximate arithmetic operator units used in the calibration procedure for radio astronomy light sensors—the so-called statistically efficient and fast calibration (StEFCal) method. The StEFCal algorithm comprises arithmetic operations like a divider, square accumulate (SAC), and multiply–accumulate (MAC) units. The StEFCal circuit of this work explores the following arithmetic operators: 1) two approximate squarer units from the literature, i.e., radix-4 (AxRSU) and SquASH; 2) two approximate iterative based Newton-Raphson (NR) and Goldschmidt (GLD) dividers; 3) one approximate parallel prefix adder (AxPPA); and 4) a new approximate radix-4 multiplier (AxRMU), proposed in this work, explored in the StEFCal multiply-accumulate circuit design. The AxRSU utilizes the parameters K1 and K2 to represent the number of exact encoders for squarer- and conventional-partial products, respectively, subsequently replaced with approximate encoders. The same principle applies to AxRMU, where the parameter K indicates the number of exact encoders for conventional-partial products, subsequently exchanged with approximate encoders. We demonstrate the efficiency of StEFCal using the approximate arithmetic operators from the Pareto-optimal front that express the area and power-quality trade-off. The results show that using the AxRSU with $K1 = 4$ and $K2 = 6$, AxRMU, and AxPPA with $K = 16$ and NR with one iteration has an MSE equal to 89.98 dB and offers up to 158× energy-savings compared with the exact StEFCal, and up to 25× more energy-savings and 3.33× area-savings compared with our previous work, 440× energy-savings compared with the accurate state-of-the-art, and 258× compared with the approximate state-of-the-art.

To conclude this guest editorial, we would like to express our gratitude to all authors contributing to this Special Issue, for their interesting research and hard work in writing their papers. Moreover, we would like to thank the reviewers involved in the different review rounds, who contributed constructive feedback and recommendations to increase the papers' readability and quality. Finally, the Organizing Committee of LASCAS 2023 also deserves special recognition for their generous work, comments, and valuable suggestions to make the symposium successful. To the readers, we hope you will enjoy these papers and find them helpful for your future work.

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ALEXANDRA ZIMPECK, *Guest Editor*
Center of Social and Technological Sciences, Catholic University of Pelotas (UCPEL)
Pelotas 96015-560, Brazil

ALEXANDER FISH, *Guest Editor*
Faculty of Engineering
Bar-Ilan University
Tel Aviv, Ramat Gan 5290002, Israel

APPENDIX: RELATED ARTICLES

[A1] I. Stanger et al., "Revisiting dynamic logic—A true candidate for energy-efficient cryogenic operation in nanoscaled technologies," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 3, pp. 987–999, Mar. 2024.

[A2] M. M. A. da Rosa, P. Ü. L. da Costa, E. A. C. da Costa, R. I. Soares, and S. Bampi, "VLSI architectures of approximate arithmetic units applied to parallel sensors calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 3, pp. 1000–1013, Mar. 2024.