A Time-Constant Calibrated Phase-Locked Loop With a Fast-Locked Time

Sung-Rung Han, *Student Member, IEEE*, Chi-Nan Chuang, *Student Member, IEEE*, and Shen-Iuan Liu, *Senior Member, IEEE*

***Abstract*—A time-constant calibrated phase-locked loop with a fast-locked time is presented. A variable capacitance multiplier (VCM) is developed to adjust the equivalent capacitance in the loop filter. And a calibration circuit is used to allow the time constant of the loop filter to track with the reference clock. By using the proposed time-constant calibration circuit and the VCM, the fast acquisition time is achieved and the loop capacitance is also multiplied. A prototype has been fabricated in a 0.35-μm CMOS process to demonstrate the proposed circuit.**

***Index Terms*—Fast locked, phase-locked loop (PLL), time-constant calibration, variable capacitance multiplier (VCM).**

I. Introduction

FOR a typical phase-locked loop (PLL), the jitter performance and the transient behavior mainly depend on the dynamic parameters, i.e., damping factor and natural frequency. Moreover, in order to reduce the external components and avoid the undesired noise coupling, the on-chip loop filter is preferred. However, the process and temperature variations alter the dynamic parameters away from the desired values. To tolerate the process and temperature variations, a technique [1] with digitally switched capacitors has been developed to calibrate the loop filter in a PLL. It may have either a complex switched-capacitor array or limited resolution. In this brief, an analog time-constant calibration circuit is proposed to precisely control the time constant of the loop filter. In order to adjust the equivalent capacitance in the loop filter, a variable capacitance multiplier (VCM) is also developed. To save the power, the clock generator will be stopped and be re-started once the demand is active [2]. By using the proposed time-constant calibration circuit and the VCM, a fast acquisition time for a PLL is achieved. Moreover, the loop capacitance is multiplied and the active area is reduced.

This brief is organized as follows. Section II describes the time-constant calibration circuit. The fast-locking acquisition is discussed in Section III. Section IV illustrates the experimental results. The conclusions are given in Section V.

II. Circuit Description

A conventional charge pump PLL is shown in Fig. 1. It is composed of a phase detector, a charge pump, a loop filter, a voltage-controlled oscillator, and a divider. The second-order loop filter is composed of the resistor R_1 and the capacitors C_1 and C_2. Assume that C_2 is much less than C_1. The damping factor ζ and natural frequency ω_n are approximately expressed as [3], [4]

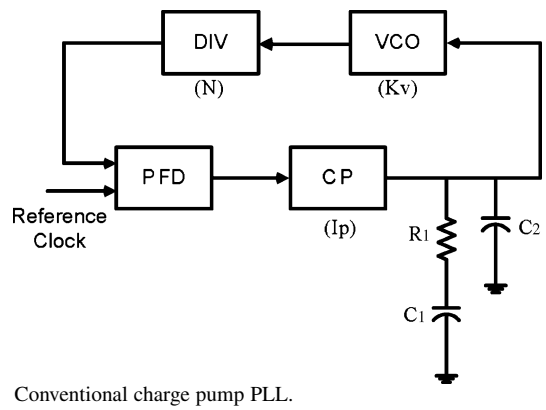

Fig. 1. Conventional charge pump PLL.

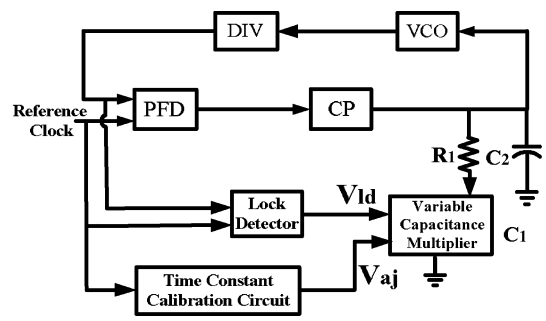

Fig. 2. PLL with a time-constant calibration circuit.

$$\zeta = \frac{R_1}{2} \cdot \sqrt{\frac{I_p \cdot K_v \cdot C_1}{N}} \text{ and } \omega_n = \sqrt{\frac{I_p \cdot K_v}{N \cdot C_1}} \qquad (1)$$

where N is the ratio of the divider, K_v is the gain of the VCO, and I_p is the charge pump current. Based on the damping factor and the natural frequency, the jitter performance and transient response of a PLL can be estimated. Since the passive components, such as R_1 and C_1, vary owing to the process and temperature variations, the damping factor and the natural frequency deviate from the designed values, too. To overcome this problem, an analog time-constant calibration circuit for a PLL is developed.

Assume that the divider's ratio N and the gain of the VCO K_v in a PLL are known. Let the charge pump current I_p be inversely proportional to R_1. According to (1), the damping factor and the natural frequency are proportional to $\sqrt{R_1 \cdot C_1}$ and $1/\sqrt{R_1 \cdot C_1}$, respectively. Fig. 2 presents a PLL with a time-constant calibration circuit, a VCM, and a lock detector.

Manuscript received December 19, 2005; revised May 24, 2006. This paper was recommended by Associate Editor G.-Y. Wei.

The authors are with Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10617, R.O.C. (e-mail: lsi@cc.ee.ntu.edu.tw).

Digital Object Identifier 10.1109/TCSII.2006.883826

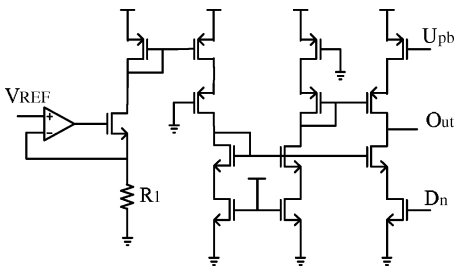

Fig. 3. Charge pump circuit.

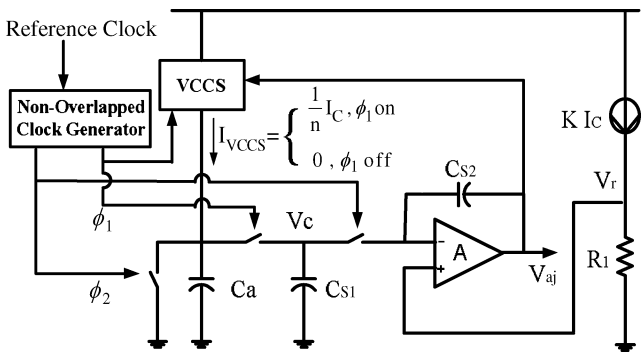

Fig. 4. Time-constant calibration circuit.

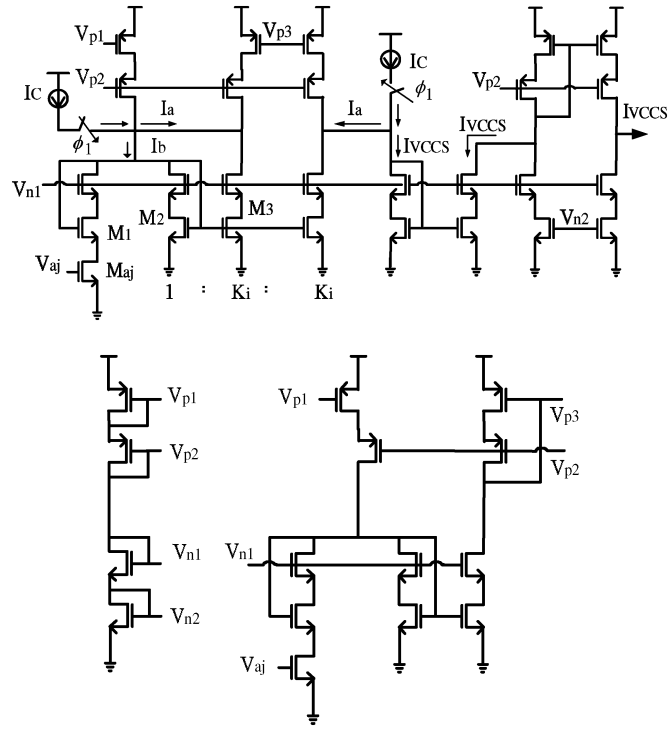

Fig. 5. (a) VCCS. (b) Bias circuits of the VCCS.

The time-constant calibration circuit adjusts the VCM to track the time constant, R_1C_1, of the loop filter with the period T of the reference clock. Thus, the damping factor and natural frequency also track with the period of the reference clock. The detailed circuit descriptions are discussed below.

A. Charge Pump Circuit

The charge pump circuit is shown in Fig. 3. A reference voltage and a replica resistor, which is equal to the resistor in the loop filter, are connected to the inputs of the amplifier, respectively. Therefore, the charge pump current is inversely proportional to the resistor in the loop filter. This charge pump current is designed around 50 μA.

B. Time-Constant Calibration Circuit

Fig. 4 shows the proposed analog time-constant calibration circuit which precisely control the time constant of the loop filter. The replica resistor R_1 and the replica capacitor C_a are equal to the resistor in the loop filter and the capacitor in the VCM, respectively. Two nonoverlapped clocks ϕ_1 and ϕ_2 and the capacitor C_a are used to realize an equivalent resistor [5]. The capacitors C_{s1} and C_{s2} in the switched-capacitor amplifier are used to sample and integrate the input voltage, respectively. To operate correctly, the capacitor C_a must be much larger than C_{s1}. The output current of the voltage-controlled current source (VCCS), I_{VCCS} is expressed as

$$I_{\mathrm{VCCS}} = \begin{cases} \frac{I_C}{n}, & \phi_1 \text{ on} \\ 0, & \phi_1 \text{ off.} \end{cases} \tag{2}$$

By the VCCS, the inverting input voltage of the amplifier, V_c, is approximated to $(I_c \cdot T)/(2 \cdot n \cdot C_a)$ and the noninverting input voltage of the amplifier V_r is equal to $K \cdot I_c \cdot R_1$ where K is a constant. If there is a difference between these two voltages, the output voltage of the amplifier V_{aj} is altered to adjust the multiplying factor n in the VCCS and the VCM. The effective capacitance C_1 of the VCM is designed to be equal to nC_a. As this circuit reaches its steady state, V_c is equal to V_r and the time constant R_1C_1 of the loop filter is guaranteed as $T/(2 \cdot K)$. Thus, the time constant will track with the period of the reference clock.

C. VCCS

The VCCS used in the time-constant calibration circuit is shown in Fig. 5(a) and its bias circuits are shown in Fig. 5(b).

In Fig. 5(a), consider only the ac currents. When ϕ_1 is on, the multiplying factor is defined as $n = I_C/I_b$ and it is variable as in (2). Thus, the ac currents $I_a = (1 - (1/n))I_C$ and $I_{\mathrm{VCCS}} = I_C/n$ are generated. In Fig. 5(a), the transistor M_{aj} is biased in the triode region to act as a voltage-controlled resistor. g_{m1}, g_{m2}, R_{aj}, and K_i are the transconductances of M1, M2, the effective resistance of M_{aj}, and the transistor ratio between M3 and M2, respectively. The ac current I_b multiplied by the equivalent resistance $((1/g_{m1}) + R_{aj})//(1/g_{m2})$, the transconductance g_{m2} and the factor K_i should be equal to the ac current I_a. The multiplying factor is derived as

$$n = 1 + \frac{K_i \cdot g_{m2} \cdot (1 + g_{m1} \cdot R_{aj})}{g_{m1} + g_{m2} + g_{m1} \cdot g_{m2} \cdot R_{aj}}. \tag{3}$$

Since R_{aj} is controlled by the voltage V_{aj} from the time-constant calibration circuit, the multiplying factor n is also variable. The nominal value of n is realized around 10.

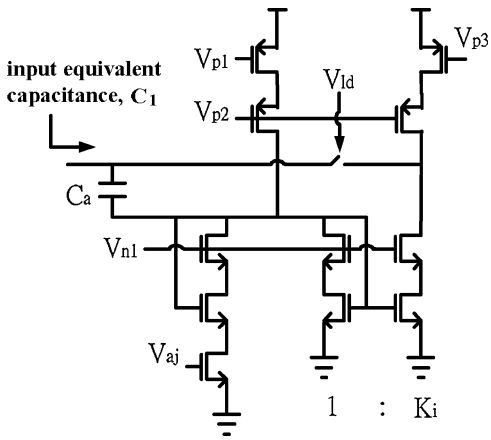

Fig. 6. VCM.

D. VCM

The VCM is a voltage-controlled capacitor as shown in Fig. 6. The capacitance multiplication technique is similar to [6], but our VCM is voltage controlled. It acts as the serial capacitor C_1 in the loop filter of Fig. 1. When the lock detector [7] is active (i.e., V_{ld} is on), a portion of the input current is bypassed to reduce the current flowing into the capacitor, C_a. Similar to the VCCS, it results in the effective capacitor C_1 equal to nC_a. Also, the voltage V_{aj} adjusts this factor n, and therefore, the effective capacitance of $C_1 = nC_a$ in the loop filter is also adjusted. When the lock detector is off (i.e., V_{ld} is off), the effective capacitor $C_1 = C_a$ in the loop filter is not multiplied. The capacitor C_a is designed as 15 pF and the effective capacitor C_1 is varied within 120–175 pF.

The multiplying factor n is affected by the supply noise. However, if g_{m1}, g_{m2}, and R_{aj} are chosen carefully, this issue is greatly reduced. Practically, K_v may vary owing to the process and supply variations. The simulated variation of K_v is around $\pm 50\%$. The simulated variation of the damping factor and natural frequency is around $+/-30\%$ if the time constant is fixed. To cover the full range of the process variations, the calibration range of this method should be increased. Moreover, this method will save the chip area, compared with a conventional PLL using an on-chip passive loop filter.

III. Fast-Locking Acquisition

In general, a PLL is designed with the overdamped transient characteristic to obtain a flat jitter transfer function without peaking. However, in this situation, a long transient time is needed in the acquisition. Thus, if a wide loop bandwidth is used in the transient response, the acquisition time is greatly reduced. To have a low jitter, a narrow–loop bandwidth is desired once the loop is locked. The implementation of this method is discussed as follows. When the lock detector is off, an effective capacitor, $C_1 = C_a$, (i.e., V_{ld} is off) is realized in the loop filter. It equivalently enlarges the loop bandwidth of the PLL. Thus, the fast-locking acquisition is achieved in the transient response. When the lock detector is on, the effective capacitor, $C_1 = nC_a$, is multiplied. It results in a small loop bandwidth and the low jitter performance is obtained. In this design, the capacitor C_2 is fixed. To avoid the instability issue, the lock window (i.e., the threshold phase difference) of the lock detector is designed to be wide enough.

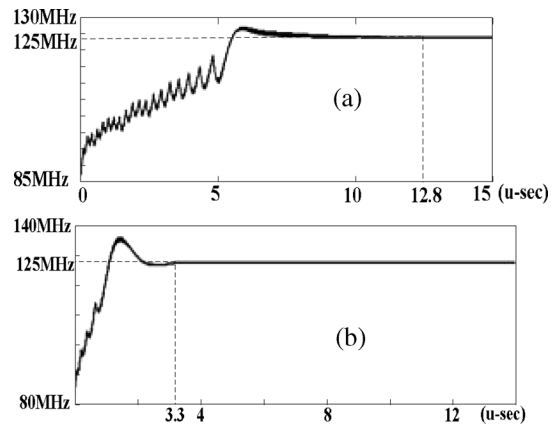

Fig. 7. (a) Simulated transient of the conventional PLL (b) Simulated transient of the proposed PLL.

TABLE I
Performance Summary

Technology	0.35um CMOS
Supply voltage	3.3V
Reference clock	25MHz
VCO's frequency range	88-162MHz with Kv=30MHz/V
Divider	5
Charge pump current	50uA
R1 in loop filter	15k
$C_1(=n\cdot C_a)$ in the loop filter	150pF
C_2 in the loop filter	10pF
Calibration range for the time constant variation	±15%
Simulated lock time for phase acquisition (@ 2.25% UI phase error)	12.8 us (conventional) 3.3 us (proposed)
Measured locked time (@ ±2% frequency error)	7 us (conventional) 2.5 us (proposed)
Measured rms and peak-to-peak jitters	25.4ps and 222ps
Chip size	1.7mmx1.7mm
Power consumption	200mW

Fig. 7(a) and (b) shows simulated transient responses for the conventional PLL and the proposed one, respectively. The circuit parameters are listed in Table I. In Fig. 7(a), the locked time is 12.8 us for the phase error less than 2.25% reference clock period in the conventional PLL. Under the same error criterion, the locked time for the proposed PLL is reduced to be 3.3 μs.

IV. Experimental Results

To demonstrate the proposed PLL, a prototype has been fabricated in a 0.35-μm CMOS technology. Fig. 8 shows the die photograph. The total area is 1.7×1.7 mm^2 with pads and on-chip loop filter. The reference clock is 25 MHz. The operation rang of this VCO is 88–162 MHz, and the measured K_v is 30 MHz/V. The supply voltage is 3.3 V and the power consumption is 200 mW including I/O buffers.

The measured rms jitter and peak-to-peak one of the proposed PLL in Fig. 9 is 25.4 and 222 ps, respectively. In Fig. 10, the resistor in the loop filter is manually varied with $0.85R_1$, R_1, and

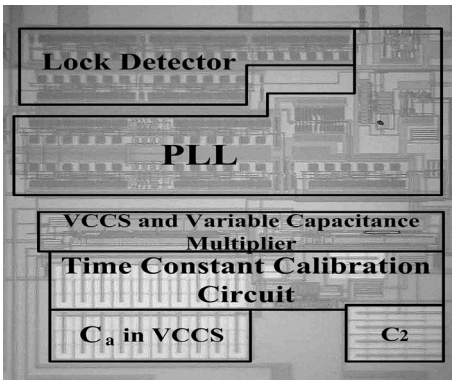

Fig. 8. Die photograph.

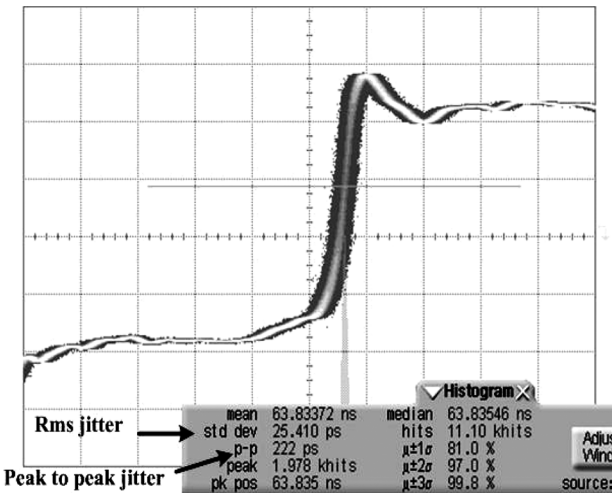

Fig. 9. Measured jitter histogram.

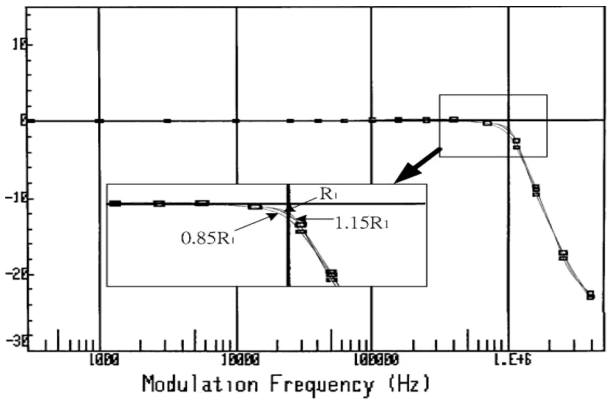

Fig. 10. Measured jitter transfer curves corresponding to different resistances in the loop filter.

$1.15R_1$, respectively. The measured jitter transfer curves corresponding to these resistances are almost the same. It demonstrates that the time constant of the loop filter is calibrated.

Fig. 11 shows the measured transient responses for the conventional PLL and the proposed one to demonstrate the frequency acquisition. The measured locked time within $\pm 2\%$ frequency error for the conventional PLL and the proposed one is 7 us and 2.5 μs, respectively. Performance summaries of this work are also listed in Table I.

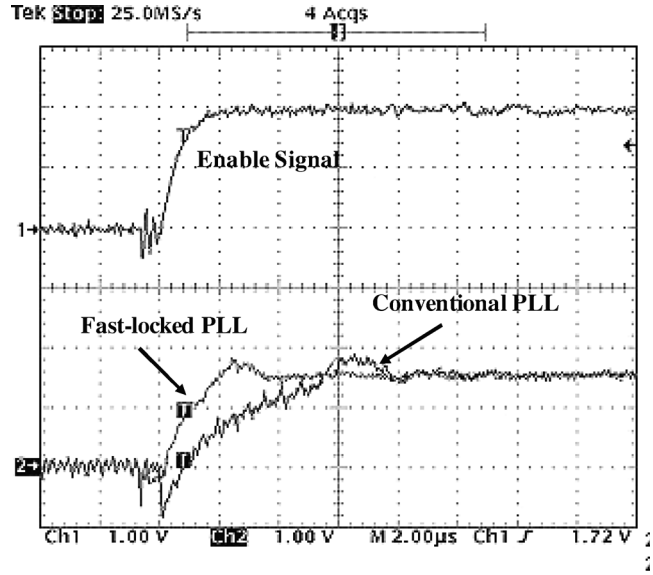

Fig. 11. Measured transient response for the conventional PLL and the proposed one.

V. Conclusion

In this brief, a time-constant calibrated PLL with a fast-locked time is presented. By using the time-constant calibration circuit and the VCM, the time constant of the loop filter and the dynamic parameters of the PLL track with the period of the reference clock. Moreover, a fast locking acquisition is also achieved and the loop capacitance is multiplied. The measurement results demonstrate the proposed circuits.

Acknowledgment

The authors would like to thank National Chip Implementation Center (CIC), Taiwan, R.O.C., for fabricating this chip.

References

[1] H. Darabi, S. Khorram, H. M. Chien, M. A. Pan, S. Wu, S. Moloudi, J. C. Leete, J. J. Rael, M. Syed, R. Lee, B. Ibrahim, M. Rofougaran, and A. Rofougaran, "A 2.4-GHz CMOS transceiver for Bluetooth," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2016–2024, Dec. 2001.

[2] Y. Saisaki, N. Kato, and H. Nakaya, "Constant-ratio-coupled multi-grain digital synchronizer with flexible input-output delay selection for versatility in low-power applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1092–1099, May 2006.

[3] J. Kim, M. Horowitz, and G. Y. Wei, "Design of CMOS adaptive-bandwidth PLL/DLLs: a general approach," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 11, pp. 860–869, Nov. 2003.

[4] Z. Wang, "An analysis of charge-pump phase-locked loops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 10, pp. 2128–2138, Oct. 2005.

[5] P. Roo, S. Sutardja, S. Wei, F. Aram, and Y. Cheng, "A CMOS transceiver analog front-end for Gigabit Ethernet over CAT-5 cables," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2001, pp. 310–311.

[6] K. Shu, S. S. Edgar, S. M. Jose, and S. H. K. Embabi, "A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 866–873, Jun. 2003.

[7] G. K. Dehng, J. W. Lin, and S. I. Liu, "A fast-lock mixed -mode DLL using a 2-b SAR algorithm," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1464–1471, Oct. 2001.