A Frequency-Translating Hybrid Architecture for Wideband Analog-to-Digital Converters

by

Shahrzad Jalali Mazlouman

B.Sc., Amirkabir University of Technology (Tehran Polytechnic), 2001
M.Sc., Amirkabir University of Technology (Tehran Polytechnic), 2003

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ABSTRACT

Many emerging applications call for wideband analog-to-digital converters and some require medium-to-high resolution. Incorporating such ADCs allows for shifting as much of the signal processing tasks as possible to the digital domain, where more flexible and programmable circuits are available. However, realizing such ADCs with the existing single stage architectures is very challenging. Therefore, parallel ADC architectures such as time-interleaved structures are used. Unfortunately, such architectures require high-speed high-precision sample-and-hold (S/H) stages that are challenging to implement.

In this thesis, a parallel ADC architecture, namely, the frequency-translating hybrid ADC (FTH-ADC) is proposed to increase the conversion speed of the ADCs, which is also suitable for applications requiring medium-to-high resolution ADCs. This architecture addresses the sampling problem by sampling on narrowband baseband subchannels, i.e., sampling is accomplished after splitting the wideband input signals into narrower subbands and frequency-translating them into baseband where identical narrowband baseband S/Hs can be used. Therefore, lower-speed, lower-precision S/Hs are required and single-chip CMOS implementation of the entire ADC is possible.

A proof of concept board-level implementation of the FTH-ADC is used to analyze the effects of major analog non-idealities and errors. Error measurement and compensation methods are presented. Using four 8-bit, 100 MHz subband ADCs, four 25 MHz Butterworth filters, two 64-tap FIR reconstruction filters, and four 10-tap FIR compensation filters, a total system with an effective sample rate of 200 MHz is implemented with an effective number of bits of at least 7 bits over the entire 100 MHz input bandwidth.

In addition, one path of an 8-GHz, 4-bit, FTH-ADC system, including a highly-linear mixer and a 5^{th}-order, 1 GHz, Butterworth G_m-C filter, is implemented in a 90 nm CMOS technology. Followed by a 4-bit, 4-GHz subband ADC, the blocks consume a total power of 52 mW from a 1.2 V supply, and occupy an area of 0.05 mm^2. The mixer-filter has a THD $\leq$ 5% (26 dB) over its full 1 GHz bandwidth and provides a signal with a voltage swing of 350 mV_{pp} for the subsequent ADC stage.

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LIST OF ABBREVIATIONS

ADC: Analog-to-Digital Converter

CML: Current-Mode Logic

CMFB: Common-Mode Feedback

CMOS: Complementary Metal-Oxide Semiconductor

CT: Continuous-Time

DAC: Digital-to-Analog Converter

DSP: Digital Signal Processing

ENOB: Effective Number of Bits

FBD: Frequency-band Decomposition

FFT: Fast Fourier Transform

FIR: Finite Impulse Response

FPGA: Field Programmable Gate Array

FTH: Frequency-Translating Hybrid

HFB: Hybrid Filter Bank

LNA: Low-Noise Amplifier

LO: Local Oscillator

NMOS: Negative-Channel Metal-Oxide Semiconductor

OSR: Over-Sampling Ratio

PMOS: Positive-Channel Metal-Oxide Semiconductor

PMR: Perfect Magnitude Reconstruction

QMF: Quadrature Mirror Filter

S/H: Sample-and-Hold

SFDR: Spurious-Free Dynamic Range

SNR: Signal-to-Noise Ratio

SNDR: Signal-to-Noise-and-Distortion Ratio

THD: Total Harmonic Distortion

TI: Time-Interleaved

UWB: Ultra Wide-Band

VLSI: Very Large-Scale Integrated

VNA: Vector Network Analyzer

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DEDICATION

To My Parents:

Nayyereh Nouyan

and

Dr. Rahim Jalali Mazlouman

1 INTRODUCTION

1.1 Motivation

Physical signals such as audio and video are analog in nature. However, all of these signals undergo several processing stages in electronic systems. By virtue of the significant advances in very large-scale integration (VLSI) and digital signal processing (DSP) techniques, most of the signal processing task is usually accomplished in the digital domain. Therefore, analog to digital converters (ADC) are inevitable and an essential block in many systems, including almost any recent integrated wireless communication receiver.

Advantages of digital VLSI and DSP techniques compared to analog signal processing, have accelerated the trend in shifting as much of the signal processing tasks as possible from the analog domain to the digital domain, where more flexible and programmable circuits are available [1]. In addition, if implemented in CMOS technology, further advantages, such as higher levels of integration, higher yield, lower cost, and potentially lower power can be exploited.

In many receiver architectures, the ADC block is located after the RF-front-end (RF front-ends usually include low-noise amplifier (LNA), down-conversion mixer and analog filtering stages). The new trend calls for placing the ADC in the early stages of the receiver

front-end. For example, in many emerging integrated wireless applications, such as software-defined radio or direct digital receivers, the goal is to remove most of the analog pre-processing blocks and to move the ADC as close as possible to the antenna, so that the signal is converted into digital as soon as possible, as shown in Figure 1.1.

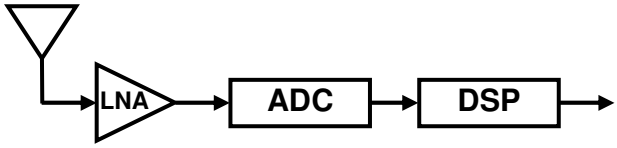


Figure 1.1: Generic receiver architecture with the ADC moved after the LNA.

However, moving the ADC closer to the antenna imposes more stringent requirements on ADC performance metrics such as dynamic range (resolution) and bandwidth. This is mainly due to the fact that in such designs, various analog signal processing stages such as gain control and filtering are either removed or simplified.

Wideband digital radio receivers, for example, need to simultaneously digitize strong and weak signals, as well as to provide excellent signal-to-noise ratios (SNRs), to avoid losing the weak signal to distortions, such as thermal and quantization noise [1]. Wideband, medium-to-high resolution ADCs for such systems are therefore essential.

Applications such as software-defined radio, multi-standard systems, direct digital wireless receivers, wideband radar, as well as ultra-wideband (UWB) transceivers, require ADCs with signal bandwidths on the order of several gigahertz along with medium-to-high resolutions (8-10 bits). Besides, wideband, medium-to-high resolution ADCs are required in broadband communication data links and high-speed measurement and test instruments such as real-time high-speed oscilloscopes [2]-[5].

1.2 Trade-off: Bandwidth vs. Resolution

A study of different ADC architectures reveals a trade-off between the resolution and the signal bandwidth of ADCs [6]: While it is possible to achieve high-speed analog-to-digital conversion for low resolution, the bandwidth decreases dramatically for higher resolutions. Reported state-of-the-art CMOS ADCs indicate resolutions of 4 to 6 bits with sampling rates of up to 4 GHz for Nyquist-rate single flash ADCs, that are practically the fastest single (non-parallel) ADCs available with this range of resolution [7]-[9]. The bandwidth, however, falls to a few tens of megahertz for higher resolutions, e.g., for delta-sigma modulators, that are practically the highest-resolution ADCs available [10] .

Flash ADC architectures are based on an array of parallel comparators, the number of which grows exponentially with resolution. A simplified, generic schematic of a flash ADC is shown in Figure 1.2. As can be seen in the figure, in this type of ADC the analog input signal is compared against an array of resistors that generate the reference voltages. The output of the comparators including several amplification and latching stages, are then delivered as an array of digital bits to the encoder. This resulting codeword is called a thermometer code, due to the special appearance of 1s and 0s in it. Finally, the encoder converts the thermometer code to a gray or a binary code [7].

Therefore, the number of required comparators in an N-bit flash ADC will be 2^N. Also, the separation of adjacent reference voltages for these comparators becomes smaller exponentially [6]. Consequently, flash ADCs require large area and power for higher resolutions. It is difficult to match components in their parallel comparator array. Finally, increasingly large input capacitance reduces the analog input bandwidth in flash ADCs.

Therefore, it is very challenging to achieve resolutions of more than 6 bits in GHz speeds with single flash ADCs.

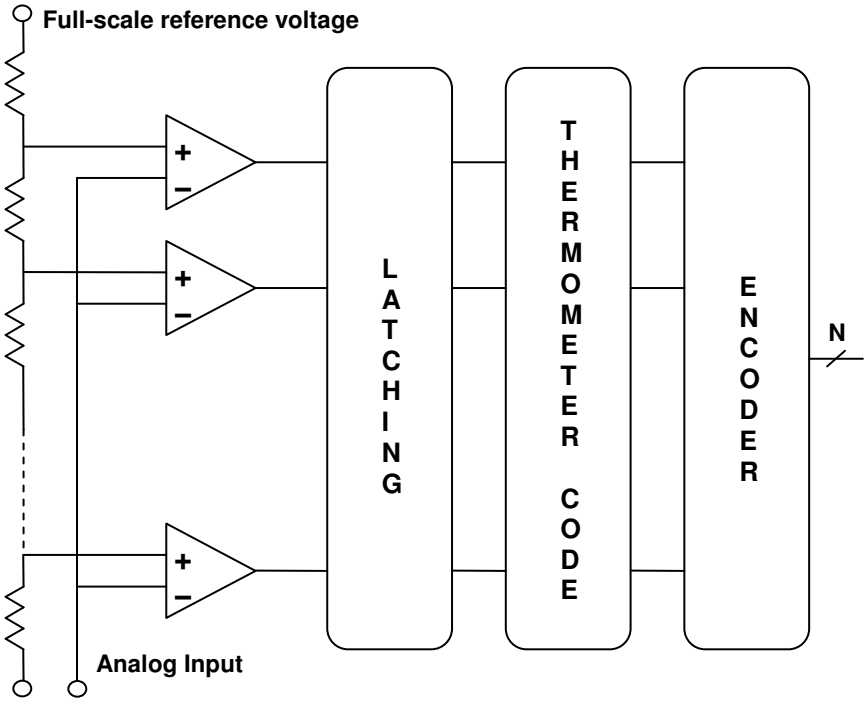


Figure 1.2: Simplified generic flash ADC architecture.

From another point of view, sigma-delta converters trade speed for resolution. In these converters, large oversampling ratios, compared to the Nyquist sample rates, are used to sample the analog input signal. Figure 1.3 shows a simplified generic schematic of a sigma-delta modulator.

As can be seen in this figure, the analog input signal is fed into a quantizer via an integrator. The quantized output is fed back and compared with the input to adjust for the differences such that the average of the quantized signal tracks the average of the analog input signal. These stages shape and suppress the quantization noise in the lower portions of the spectrum relative to the converter sampling frequency, so that a higher resolution can be achieved [11]-[12].

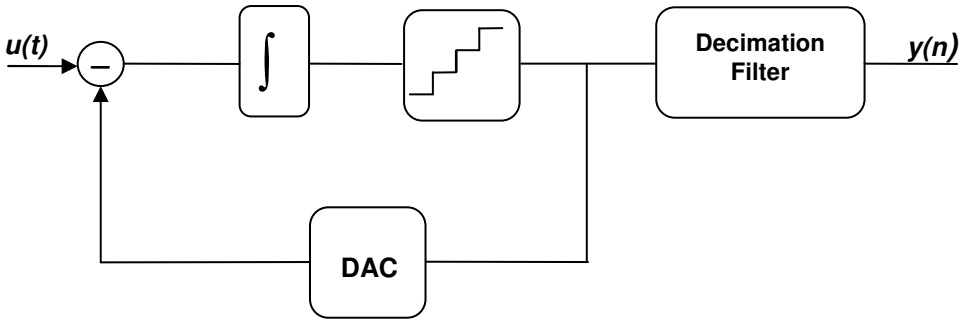


Figure 1.3: Simplified generic sigma-delta converter architecture.

In high-bandwidth applications where the oversampling ratio (OSR) is constrained by technology limitations, however, alternative techniques should be used to obtain relatively large noise suppression with low oversampling ratio requirements.

One approach to reduce the OSR requirement of delta-sigma modulators for high-frequency applications, is to increase the order of the modulator (order of the loop filter) to improve the noise shaping capability [13]. Nonetheless, higher order modulators are difficult to stabilize [14]-[15], and are sensitive to component mismatch [13]. Besides, the effect of increasing the loop order diminishes to a large extent at low oversampling ratios unless multi-bit quantization is also used [16]. Designing a multi-bit, linear digital-to-analog converter (DAC), which is a major part in the feedback loop of delta-sigma converters is however difficult [11]-[12]. The nonlinearity of these DACs contributes directly to nonlinearity in the response of the modulator.

Another approach is to use cascaded stages. The use of multiple cascaded noise-shaping stages makes it possible to achieve a high degree of quantization noise suppression at very low oversampling ratios. Since each stage can employ single-bit quantization, the linearity and stability problems associated with high-order or multi-bit single-stage

modulators can be avoided. However, the number of stages that can be cascaded usefully is limited [16].

It should be noted that various calibration methods [17]-[18], and dithering [12], can usually be used to improve the performance of almost any ADC architecture to some extent after the design has been implemented. Such methods are out of the scope of this context and are not discussed herein.

1.3 Solution: Parallel ADC Architectures

A more efficient approach to design wideband ADCs with medium-to-high resolution is to exploit more than one ADC through parallelism. A generic figure of parallel ADCs is shown in Figure 1.4.

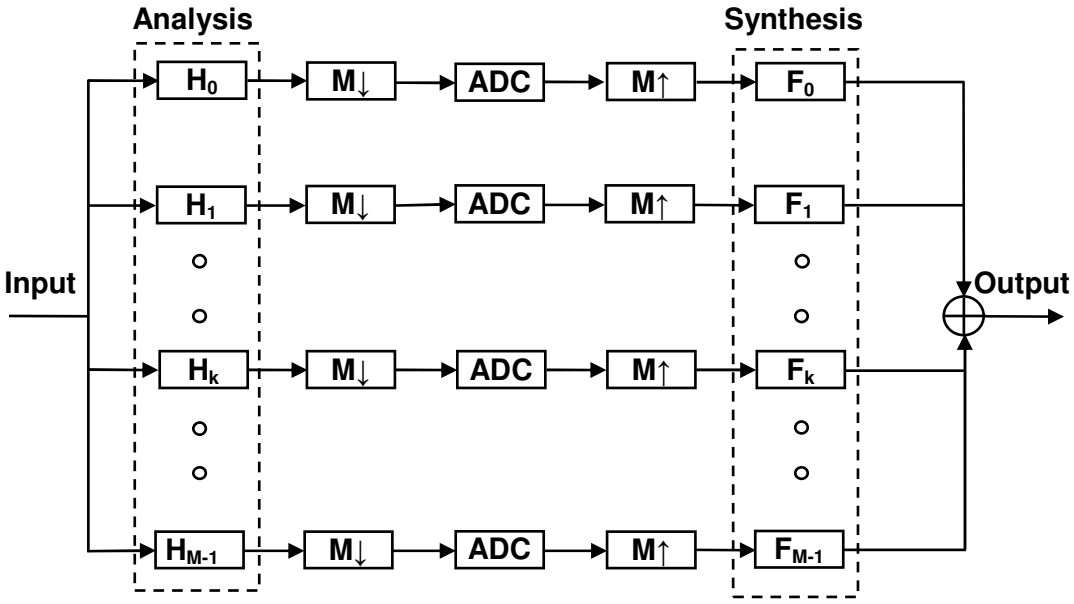


Figure 1.4: Generic parallel ADC architectures.

In parallel ADCs, the main idea is to take a wideband analog input signal, split it into a number of channels (in time or frequency domain) using an array of analysis filters, and

convert each channel data into digital using lower-bandwidth ADCs in each channel. Decimation stages shown in Figure 1.4 reduce the sampling rate by a factor M, keeping every other *M* of their input samples and discarding the *M*-1 samples between them. These downsampling stages may or may not exist explicitly. Finally, the digital subband data samples are up-sampled using the upsampler stages that increase the sampling rate by a factor of *M*, by interpolating *M*-1 zero samples between each two consecutive input samples. The up-sampled subband data are then recombined to reconstruct the digitized representation of the original wideband analog input signal, using an array of synthesis filters. The benefit of such architecture lies in the fact that using lower-bandwidth ADCs in parallel, a system with a higher overall bandwidth can be achieved.

Some drawbacks of parallelism are increased hardware and power consumption. Besides, compensating for errors due to analog non-idealities and mismatch between parallel channels can be challenging.

Some of the most popular conventional parallel architectures will be reviewed and compared in Chapter 2.

1.4 Objective and Outline of the Thesis

The main objective of this thesis is to propose a new parallel approach to increase the conversion speed of ADCs, which is also suitable for applications requiring medium-to-high resolution. Specifically, the proposed approach can make integrated single-chip CMOS ADC solutions for gigahertz conversion speeds with about 8-10 bits of resolution realizable. However, this approach is not limited to a specific technology, application or performance

metrics and can be used as a general approach for increasing the conversion speed of any ADC architecture.

Compared to the conventional parallel ADCs as will be discussed in Chapter 2, the new proposed ADC architecture is the only approach that can be implemented in fully single-chip CMOS technology for state-of-the-art gigahertz conversion speeds with medium-to-high resolution.

The organization of the thesis is as follows. A background review of conventional parallel ADC architectures with their advantages and disadvantages is presented in Chapter 2. The new parallel system is introduced and designed in Chapter 3. A proof-of-concept board-level implementation is then used in Chapter 4 to analyze performance metrics of the proposed architecture in the presence of major analog non-idealities and errors as well as approaches to measure and compensate for these errors. One channel of a four-channel system is designed, implemented and measured in 90 nm CMOS technology in Chapter 5 to study CMOS-integrated implementation challenges of the proposed system. Finally, Chapter 6 is devoted to summary, conclusion and future work suggestions.

1.5 List of Contributions

1.5.1 Proposing the New Frequency-Translating Hybrid ADC (FTH-ADC) Architecture

The proposed architecture is a parallel filter-bank-based hybrid ADC, namely the frequency-translating hybrid ADC (FTH-ADC). In this architecture, a wideband analog input signal is frequency-translated down to baseband and low-pass filtered before being converted into digital by subband ADC blocks. After conversion into digital, the subband

digital samples are upconverted and frequency-translated back to their original centre frequency. Therefore, unlike conventional parallel ADCs, low-bandwidth, baseband sample-and-hold (S/H) blocks are required for this architecture that are implementable on a single CMOS chip together with the rest of the circuit. Also, except for the digital reconstruction filter coefficients and the mixing frequencies, all blocks of this system are identical which adds flexibility and simplicity to the design of FTH-ADCs. These advantages provide for a fully-CMOS ADC solution with gigahertz conversion speed and medium-to-high resolution, which is very challenging to design with conventional ADC architectures.

1.5.2 Analysis, Design, and Optimization of the Digital Reconstruction Structure, including the Synthesis Filters for the Proposed FTH-ADC

In the proposed FTH-ADC system, the digital representation of the wideband analog input signal is reconstructed using digital FIR reconstruction filters. These filters are designed and optimized to compensate sufficiently for the aliasing terms that appear in the signal spectrum due to undersampling. A design approach is presented for these filters based on the measurements on the analog signal path including the analog low-pass filters frequency response. An optimization method is adopted herein to design these filters.

1.5.3 Analysis of the Effects of Major Analog Non-Idealities and Errors on the Performance of the FTH-ADC System, Using a Proof-of-Concept Board-Level Implementation

The FTH-ADC system analysis and digital reconstruction filters design is revisited in the presence of major analog non-idealities such as ADC and channel mismatch and offset errors and compensation approaches are presented based on the derived equations. The complexity of the system with regard to the performance metrics is also studied.

As a proof-of-concept, a 2-channel, 200 MHz, 7-bit prototype FTH-ADC system is implemented in board-level using off-the-shelf components for filters and splitters and two analog quadrature mixer boards and two Altera Stratix DSP development kits (FPGA boards). The proposed measurement and compensation techniques are implemented on this board to demonstrate their feasibility and effectiveness.

1.5.4 Proposing an I/Q Imbalance Compensation Method for the FTH-ADC System

In particular, using the board-level implementation, an approach is presented and implemented to measure and compensate for the I/Q mismatch error in the FTH-ADC system. The I/Q mismatch error includes the gain and phase-imbalance of the in-phase and quadrature paths of each channel. A compensation block is added to the digital reconstruction part of the system that includes a pair of FIR compensation filters per channel. The complexity of these filters is also discussed.

1.5.5 Circuit-Level Design and Implementation: A 4-bit, 4-GHz, 52 mW, Mixer-Filter-ADC Stage in CMOS 90 nm (One Channel of a 4-bit, 8-GHz FTH-ADC System)

In the circuit level, one path of a 2-channel, 4-bit, 8-GHz FTH-ADC system, with an analog bandwidth of 4 GHz, is designed and implemented in CMOS 90 nm technology. This path consists of a highly-linear mixer-filter-ADC block that can operate at sampling rates of up to 4 GHz with an SNDR of at least 26 dB. The block consists of a fully-differential 5^{th}-order Butterworth G_m-C filter, with a cutoff frequency of 1 GHz, and a passive, highly-linear, double-balanced mixer operating at 4 GHz with at least 26 dB of linearity. A fully-differential flash ADC architecture with 4 bits of resolution operating at 4 GS/s is adopted for this path.Therefore, the mixer-filter has a THD $\leq$ 5% (26 dB) over its full 1 GHz bandwidth and provides a signal with a voltage swing of 350 mV_{pp} for the subsequent ADC stage. The total path consumes a total measured power of 52 mW from a 1.2 V supply with an active area of 0.05 mm^2.

2 A REVIEW OF CONVENTIONAL PARALLEL ADC ARCHITECTURES

In this chapter, some of the most popular conventional parallel ADC architectures are reviewed and compared. In particular, the possibility of using each architecture for an integrated high-speed, medium-to-high resolution CMOS ADC solution is examined.

2.1 Time Interleaved ADC (TI-ADC)

Time-interleaved (TI) ADCs, dating back to the early 1980s [19], are perhaps the first ADCs that took advantage of parallelism. In this architecture, parallel lower-speed ADC converters, namely the subband converters, are interleaved in time to result in an overall higher-bandwidth ADC.

Figure 2.1 shows a four-channel time-interleaved ADC architecture and Figure 2.2 shows the clock signals applied to each channel. In this structure, a multiplexer selects the output of each ADC at the proper time, providing the output corresponding to each sample. When the clock signal of a channel is high, the sample and hold (S/H) circuit of that channel samples the input. When the clock signal of this channel goes low, the S/H circuit holds the value and the ADC begins to digitize it. At the same time, the clock signal of the following channel goes high to allow the next channel to acquire the next input sample. Digitized

subchannel data is then upsampled by M, where M is the number of channels (M=4 in this case). The multiplexer is controlled such that it selects each channel at the right time [20].

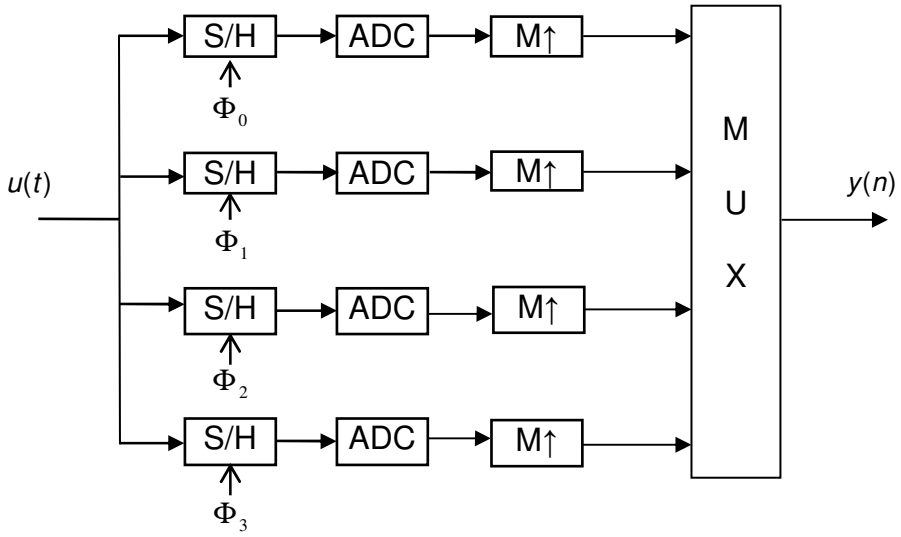


Figure 2.1: The time-interleaved (TI-ADC) architecture.

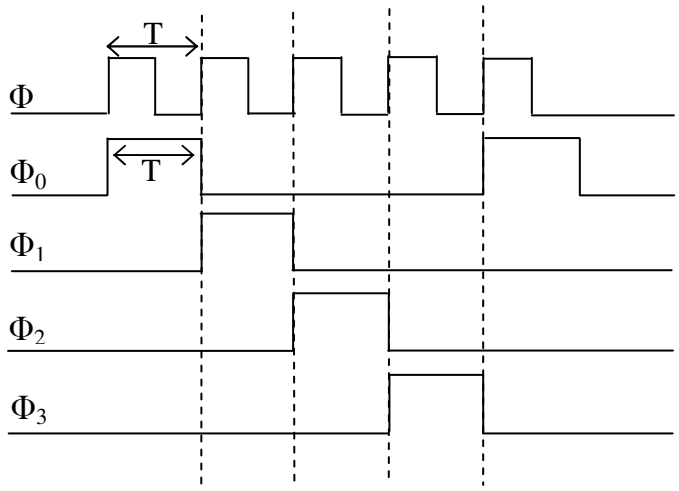


Figure 2.2: Time-multiplexing signals for the TI-ADC.

One of the main problems in the TI architectures is their sensitivity to the jitter (time uncertainty) of the S/H circuit preceding each ADC, which leads to a corresponding uncertainty in the stored data. To minimize the effects of jitter sensitivity, high-speed, high-precision, low-jitter S/H circuitry should be used at the first stage of the TI structures. Such blocks are very challenging to implement in CMOS technology for GHz rates.

One way to reduce the effect of sampling jitter is to use a two-rank S/H, as shown in Figure 2.3 [21]. In this structure, Φ is a clock at four times the rate of Φ_0 to Φ_3 (also shown in Figure 2.2). Each of the four ADC converters operates at one-quarter of the rate of the input sampling frequency.

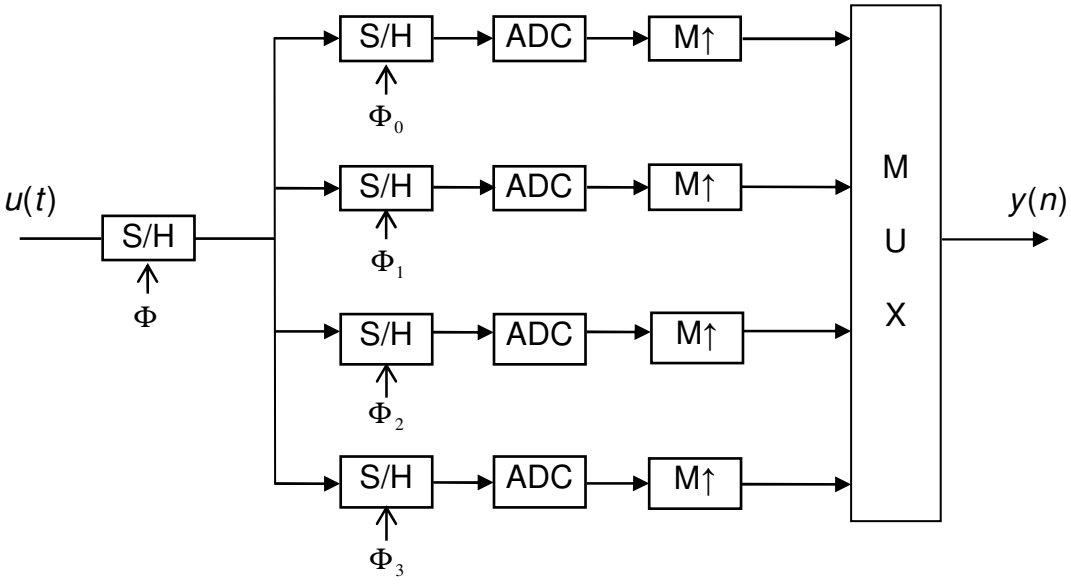


Figure 2.3: Two-rank S/H in the TI-ADC architecture.

Using this approach, the jitter of the input S/H clock (Φ) is critical, while the remaining four S/H converters can tolerate a considerable jitter since the signal is already sampled prior to those S/Hs. Therefore, low-jitter requirement is relaxed on the second array

of S/H circuitry. A different technology such as GaAs can be used for the first S/H stage while the remaining circuits are implemented in CMOS [5], [21].

The second significant problem with the time-interleaved architecture is that a high level of matching between the channel components is essential to minimize the total harmonic distortion and therefore to maximize the attainable effective number of bits (ENOB). Note that the relationship between ENOB and the output signal-to-noise-and-distortion (SNDR) of an ADC converter for a full-scale sinusoidal input is [22]:

$$\text{SNDR} = 6.02 \times \text{ENOB} + 1.76 \text{ (dB)} \tag{2.1}$$

Any offset or gain mismatch between the ADCs in the channels can produce tones at f_s/M, where $f_s = 1/T$ is the effective sampling frequency of the total system, and M is the number of channels. For example, in the four-channel system of Figure 2.1, a DC offset in one converter would result in a tone at $f_s/4$ [22]. These tones add up to the noise power and therefore decrease the SNDR and consequently the ENOB of the total converter system.

Laser trimming [23] and digital calibration methods [17] can be used to reduce the effects of component mismatch. Another approach is to exploit redundant channel components and random selection and averaging of the outputs [24]. However, such approaches can increase cost and complexity.

Time-interleaved architectures have been reported to have up to 8 bits of resolution at GHz speeds. An 8-GS/s, 8-bit time-interleaved ADC with a bandwidth of nearly 2 GHz is reported in [25]. A 40-GHz, 4-bit [5], an 8-bit, 8-GHz [26], and an 8-bit, 20-GHz [27] time-interleaved ADC have been reported. However, as explained before, none of these converters was implemented fully in CMOS. Recently, an 8-bit, 4-GHz TI-ADC was

implemented fully in CMOS using 32 time-interleaved ADCs, achieving an ENOB of up to 5 bits for input bandwidths around 2 GHz [28].

2.2 Digital Frequency-Band Decomposition ADC (QMF/FBD-ADC)

Petraglia and Mitra exploited quadrature mirror filter banks (QMFs) and the concept of multi-rate signal processing [29]-[31], to introduce a new parallel ADC architecture based on frequency-band decomposition, or FBD-ADCs [32]-[33].

An M-channel FBD-ADC architecture is shown in Figure 2.4. In this structure, the discrete-time input signal, $u(n)$, (denoted as $U(z)$ in the frequency domain) is passed through a filter bank consisting of an array of M bandpass filters, $H_k(z)$, (except for the first filter which is a low-pass filter) and is decomposed into a set of M subband signals. These bandpass filters, usually called the analysis filters, are frequency selective in contiguous frequency bands of width π/M each, as shown in Figure 2.5.

The subband signals are then down-sampled by a factor of M and digitized at $1/M$ rate of the original input signal. Next, the ADC outputs are upsampled by a factor of M and passed through a set of M bandpass digital filters, $F_k(z)$, to remove the extra terms due to undersampling, resulting in an output signal, $y(n)$, whose sampling rate is the same as that of the input, $u(n)$. These digital reconstruction filters are usually called the synthesis filters. The input/output relation for this system in the z-domain is given by [32],

$$Y(z) = \frac{1}{M}\sum_{l=0}^{M-1}\left[U(zW^l)\sum_{k=0}^{M-1}H_k(zW^l)F_k(z)\right] \qquad W = e^{j2\pi/M} \tag{2.2}$$

where $Y(z)$ is the output signal in the frequency domain. The analysis and synthesis filters can be designed to ideally achieve a perfect reconstruction at the output, implying that the output is a delayed and scaled replica of the input with complete aliasing cancellation. In this case, (2.2) reduces to

$$Y(z) = Az^{-d}U(z) \tag{2.3}$$

where d is a positive integer and A is a constant. Equation (2.3) is usually referred to as the perfect reconstruction (PR) condition [30].

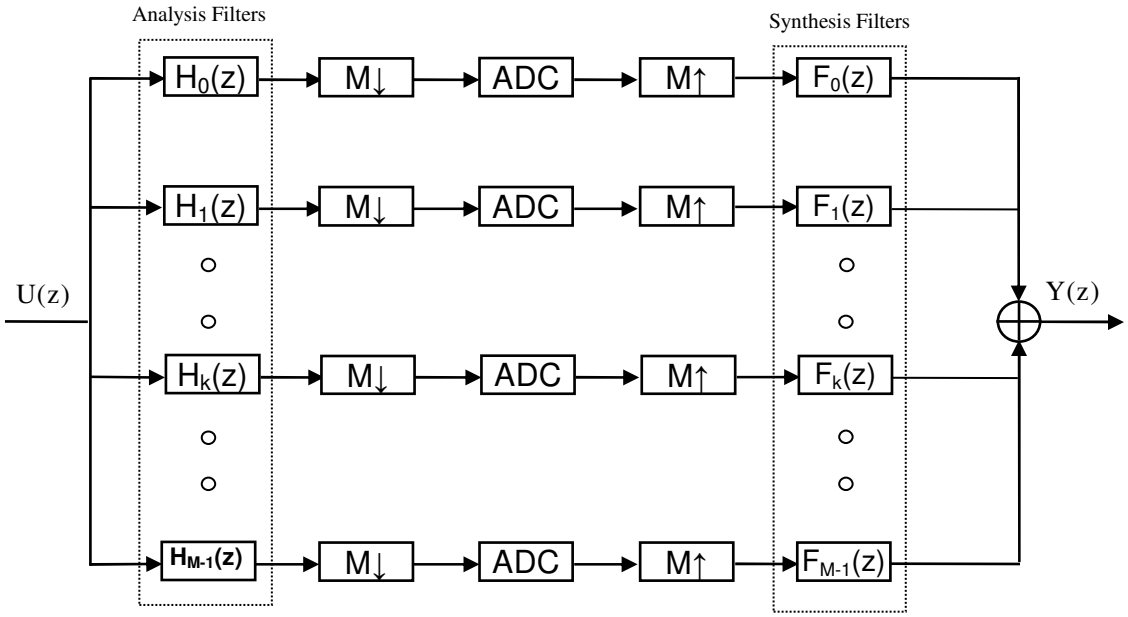


Figure 2.4: The Frequency-band decomposition (FBD-ADC) architecture.

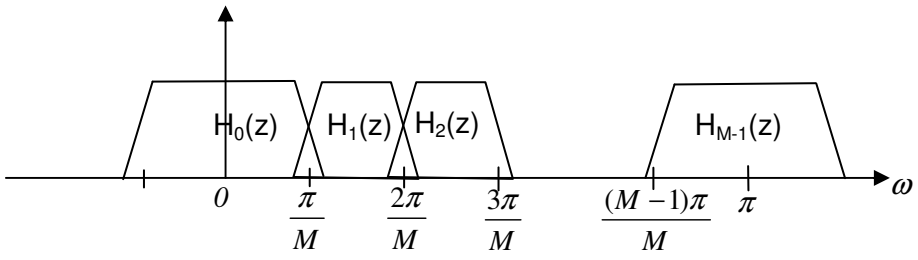


Figure 2.5: Filtering scheme in the FBD-ADC.

Perfect reconstruction can be simplified to perfect-magnitude reconstruction (PMR) depending on the application if no useful information is carried in the phase of the signal. In this case, (2.3) is simplified to

$$\left|Y(z)\right| = \left|Az^{-d}U(z)\right| = A\left|U(z)\right| \tag{2.4}$$

The frequency-band decomposition (FBD) architecture has many advantages over the time-interleaved architecture. It has been shown that this architecture is not as much sensitive to mismatch as time-interleaved structures [33]. This is basically due to the fact that the reconstruction filters can be designed by taking the channel component mismatches into account. The total harmonic distortion is therefore reduced in this architecture. Hence, a higher ENOB can be achieved as compared to the time-interleaved ADC architecture.

Also, jitter due to uneven sampling of high-frequency inputs is automatically reduced in QMFs because of the decimation stage (downsampling at S/H). This idea is quite similar to the two-rank S/H solution offered in [21]. In fact, in the QMF-FBD, each sampled-and-held output of each discrete-time analysis filter is passed to a down-sampler that acts as a second-rank S/H. When the down-sampler transition from sample to hold happens, its input signal remains constant [32].

In fact, each analysis filter (usually implemented as a discrete switched-capacitor filter) presents the already sampled and held input to the decimator, which can be seen as a second-rank S/H. Consequently, when the decimator transition from sample state to hold state occurs, its input signal is not changing [33].

From another point of view, the frequency-band decomposition architecture is relatively insensitive to sampling jitter since the input is sampled in all channels simultaneously and is therefore robust to clock skews [34].

However, the use of switched-capacitor filters as the discrete-time analysis filters for QMF architectures limits the speed of the system and introduces switching noise, which can limit the SNDR. Besides, the sample-and-hold circuit which is the first block to process the input signal in this architecture still has to process a wideband analog signal, since channelization is accomplished after this block. In other words, the whole parallel QMF-FBD system is operating with a discrete-time analog input signal which should be provided by the first sample-and-hold stage. The bandwidth of the overall system is therefore limited to the maximum implementable bandwidth for the front-end S/H circuit.

2.3 Delta-Sigma Filter Bank ADC

Delta-sigma modulation can be exploited together with the above mentioned parallel structures, i.e., the frequency-band decomposition structure or the time-interleaved architecture, to result in a high-bandwidth, high-resolution system [35]-[37].

For example, a fourth-order digitally programmable bandpass delta-sigma architecture has been shown in [35], with tunable null frequencies. By combining several of these modulators in parallel and programming each appropriately, a highly adjustable parallel ADC can be constructed.

As a proof-of-concept, a four-band system with a sampling frequency of 2.3 MHz and SNDR of 47 dB has been implemented on CMOS *2 μm* technology with this architecture. An additional advantage of such parallel modulator structure is the ability to vary the resolution of conversion across the input spectrum depending on the application [38].

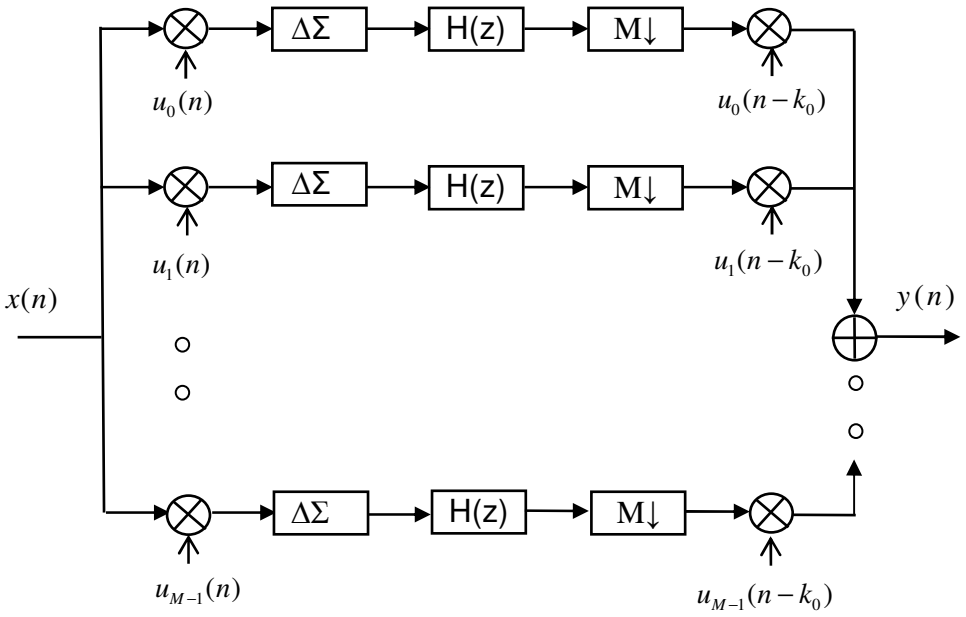


Figure 2.6: Hadamard-modulated ΠΔΣ-ADC.

In practice, however, the bandwidth of such systems is very limited. Note that the aliasing error of the FBD system can limit the resolution of the system, regardless of the resolution of the delta-sigma modulator used. Therefore, proper digital reconstruction filters should be designed for such structures.

2.4 Hadamard Modulated ADC (ΠΔΣ-ADC)

The Hadamard-modulated ADC, namely ΠΔΣ-ADC was first proposed in [39]. Channelization in this architecture, i.e., separation of signal and noise, is accomplished using Hadamard modulation. As shown in Figure 2.6, in each channel, the input sequence, $x(n)$, is multiplied by a channel-specific ±1 sequence (Hadamard matrices), $u_i(n)$, delta-sigma modulated, low-pass filtered, and multiplied by a delayed version of the same channel-

specific ±1 sequence, $u_i(n-k_0)$, where k_0 is the delay of the system. The outputs are finally summed to result in the overall system output, $y(n)$.

The advantage of using this architecture is that while keeping many of the attractive properties of the delta-sigma architecture, oversampling is not required [40]-[41]. Therefore, these structures can be implemented with higher conversion speeds.

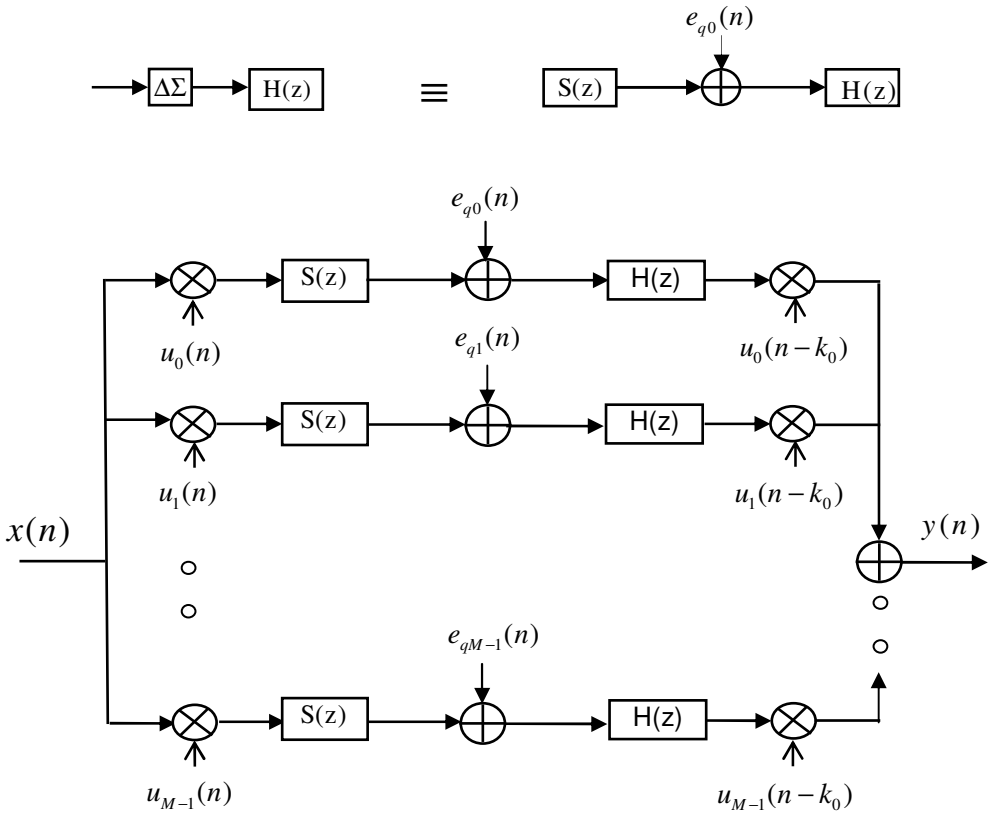


Figure 2.7: The quantization model for Hadamard-modulated ΠΔΣ-ADC.

Noise shaping in this architecture is based on the fact that the ΔΣ modulator quantization error components are not Hadamard-modulated at the input prior to filtering, and therefore the effect of filtering is not undone as in the case of the signal components. The low-pass filtering can thus be used to filter out the higher components of the

quantization noise. This is shown in Figure 2.7, where the delta-sigma modulator is modeled with a signal transfer function, $S(z)$, and an added quantization noise $e_{qi}(n)$.

In other words, in the conventional ΔΣ-ADC architecture, both the signal and the quantization noise pass through the same filter, and therefore, both are filtered by the same low-pass decimation filter. In contrast, the Hadamard-modulated ΠΔΣ-ADC amplitude-modulates the input to decouple the signal from the quantization noise such that the filtering of the signal is undone by amplitude demodulation. In effect, the signal is simply delayed while the noise is low-pass filtered.

Another advantage of this architecture is that it is easily implementable since it only needs multiplication by ±1 and therefore the signal is either passed or inverted. Note that M should be chosen such that an $M \times M$ Hadamard matrix exists.

A 16-channel, 1 MHz system with a resolution of 5.7 bits for no oversampling and resolution of 8.7 bits for an OSR of 3 implemented in CMOS *1.2 μm* has been reported in [39], [42]. Another 8-channel 1 MHz system with a bandwidth of 200 kHz and an OSR of 5 has been reported to have an SNR of 56.8 dB [43].

Component mismatch among the channels produces distortions in the ΠΔΣ ADC architecture [18]. As for jitter sensitivity, this architecture has a better performance than the TI but worse performance than the FBD. This is mainly due to the fact that higher-frequency sampling circuitry is needed in this architecture [34], [39].

In fact, since this architecture is also based on discrete data at the input, the need for a high-precision, high-speed S/H circuitry as the first stage is still the main bottleneck in exploiting the ΠΔΣ-ADC for high-speed, medium-to-high resolution ADC applications.

2.5 Hybrid Filter Bank ADC (HFB-ADC)

An alternative way to implement the bandpass frequency decomposition ADC system is to use an array of analog continuous-time (CT) analysis filters at the first stage rather than discrete-time analysis filters, as is the case for FBD systems. Therefore, the analog input signal is first decomposed into smaller subbands through filtering and then sample-and-held and converted into digital by subband ADCs. By moving the S/H stage after the filtering stage, this architecture simplifies the precision and speed requirements on the S/H stage to some extent compared to the previous parallel architectures.

This architecture is called a hybrid frequency-band decomposition ADC architecture, or briefly called hybrid filter bank ADC (HFB-ADC) and is shown in Figure 2.8. The name hybrid refers to the fact that the analysis filters are analog and the synthesis filters are digital [44], [45]. Note that the wideband analog input signal is a continuous-time analog signal, denoted as $U(s)$ in the frequency domain, whereas the output signal is a wideband digital representation of the input, denoted as $Y(z)$ in the frequency domain.

Figure 2.9 shows the filtering structure in this system. The HFB-ADC is very similar to the FBD architecture and therefore inherits all the advantages of it, including less sensitivity to channel mismatch and jitter compared to the TI. This architecture allows for standard analog filters (such as Butterworth, Bessel, etc.) to be used as the analysis filters. Digital synthesis filters can then be designed and optimized to compensate for these filters and potential component mismatches in a similar way to the one explained for FBD structures.

It should be noted that perfect reconstruction is not feasible for HFB structures due to the analog nature of the analysis filters [46]; however, with reasonable assumptions,

digital synthesis filters can be designed that provide sufficient SNDR for the total ADC system for medium-to-high resolution applications.

A board-level prototype using four Analog Devices AD9042, 12-bit, 40-MSps ADCs and a sampling frequency of 160 MSps with 90 dB dynamic range has been reported in [44]. The digital FIR filters for this system were optimized for a length of 64. However, due to the practical limitation of the measurement instruments, only 45 dB of SNDR was measured.

Although the requirements on the S/H stages of these ADCs are simplified, since this architecture still requires bandpass sampling, high-speed, high-precision S/H circuitry tuned at the channel centre frequency and bandpass ADCs are still the challenging part of the design for these converters.

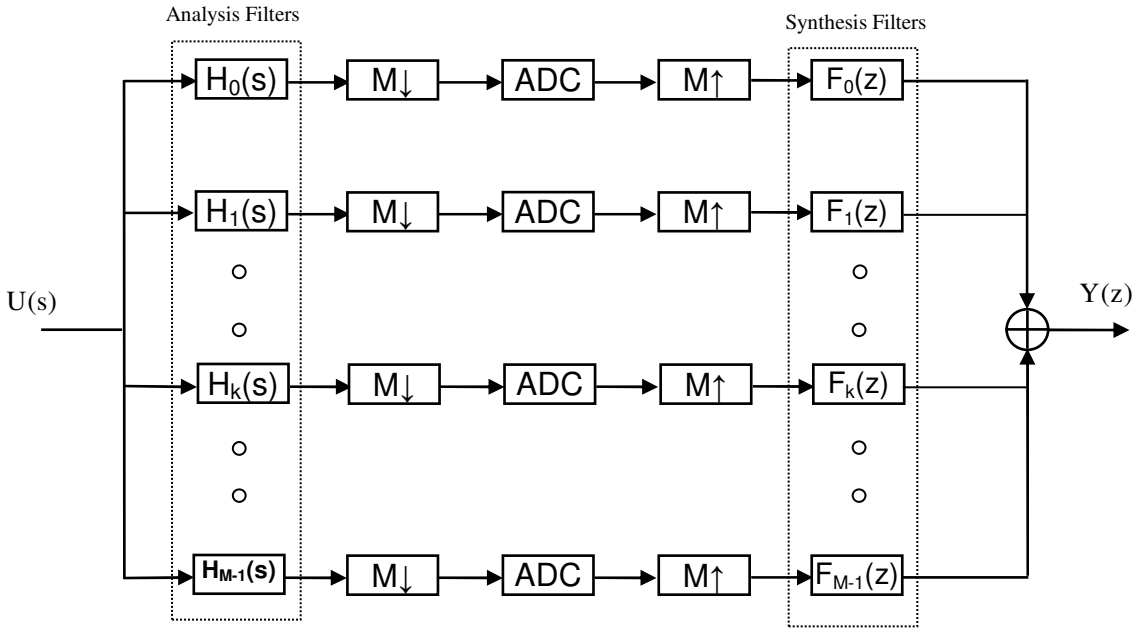


Figure 2.8: The hybrid filter bank ADC (HFB-ADC) architecture.

In this thesis, a new parallel ADC architecture is proposed for wideband medium-to-high resolution ADCs. This architecture addresses the sampling problem by performing all

of the sampling on the narrowband baseband signals. In this structure, sampling is accomplished after splitting the wideband input signals into narrower subbands and frequency-translating them into baseband, where identical narrowband baseband S/H blocks can be used. Therefore, lower-speed, lower-precision S/H stages are required. This will be further discussed in the following chapters.

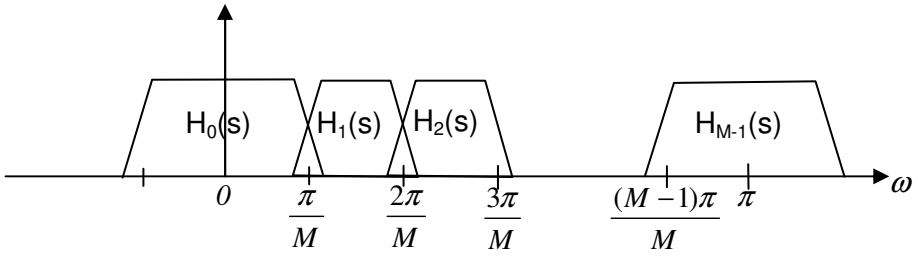


Figure 2.9: Filtering scheme in the HFB-ADC.

3 THE FREQUENCY-TRANSLATING HYBRID ADC

In this chapter, the proposed frequency-translating hybrid structure for wideband, medium-to-high resolution ADCs, is introduced and analyzed. The design of ideal digital reconstruction filters of this structure is presented. After calculating the required ideal digital reconstruction filters for this system, an optimization algorithm is adopted to design practical real FIR filters to reconstruct the digital representation of the original wideband analog input signal. Simulation results are reported to confirm the system-level analysis. Finally, the proposed structure is compared to the conventional parallel ADCs that were reviewed in Chapter 2.

3.1 The Structure

The proposed parallel ADC structure is a filter-bank-based hybrid structure, and is shown in Figure 3.1 [47]. In this system, a wideband analog input signal, $u_c(t)$ (denoted as $U_c(j\Omega)$ in the frequency domain), is fed simultaneously into multiple channels.

Assume a wideband baseband input signal with a bandwidth of Ω_B is being processed by this M-channel ADC. Each channel consists of a two-path system composed of quadrature downconversion mixers that frequency-translate the input signal down to baseband by

$$\Omega_k = \frac{(2k+1)\Omega_B}{2M} \tag{3.1}$$

where k is the channel index ($0 \leq k \leq M$-1). The signals in each path are then low-pass filtered using identical analog filters (analysis filters), $H_c(j\Omega)$, with a 3-dB bandwidth of

$$\Omega_c = \frac{\Omega_B}{2M} \tag{3.2}$$

At this stage, the signal has been decomposed into narrower band in-phase (I) and quadrature (Q) baseband subbands. Identical baseband ADCs in the following stage digitize the subband signals. Subband digital samples are then upconverted back to their corresponding (equivalent) digital center frequencies (ω_k), interpolated (upsampled), filtered through an array of digital reconstruction filters (synthesis filters), $F_k(e^{j\omega})$, and finally recombined in the digital domain to reconstruct the digital representation of the wideband analog input signal.

Since the analysis filters in this system are analog and the synthesis filters are digital, this system is a hybrid system. Furthermore, frequency translating is the key concept in this structure, therefore, the system is called a frequency-translating hybrid ADC, or FTH-ADC in short.

The overall system performs as a wideband ADC digitizing an input signal of bandwidth Ω_B using an M-channel structure with $2M$ identical parallel low-pass filters and $2M$ identical ADCs, each with a sampling period, T, of

$$T = \frac{M\pi}{\Omega_B} \tag{3.3}$$

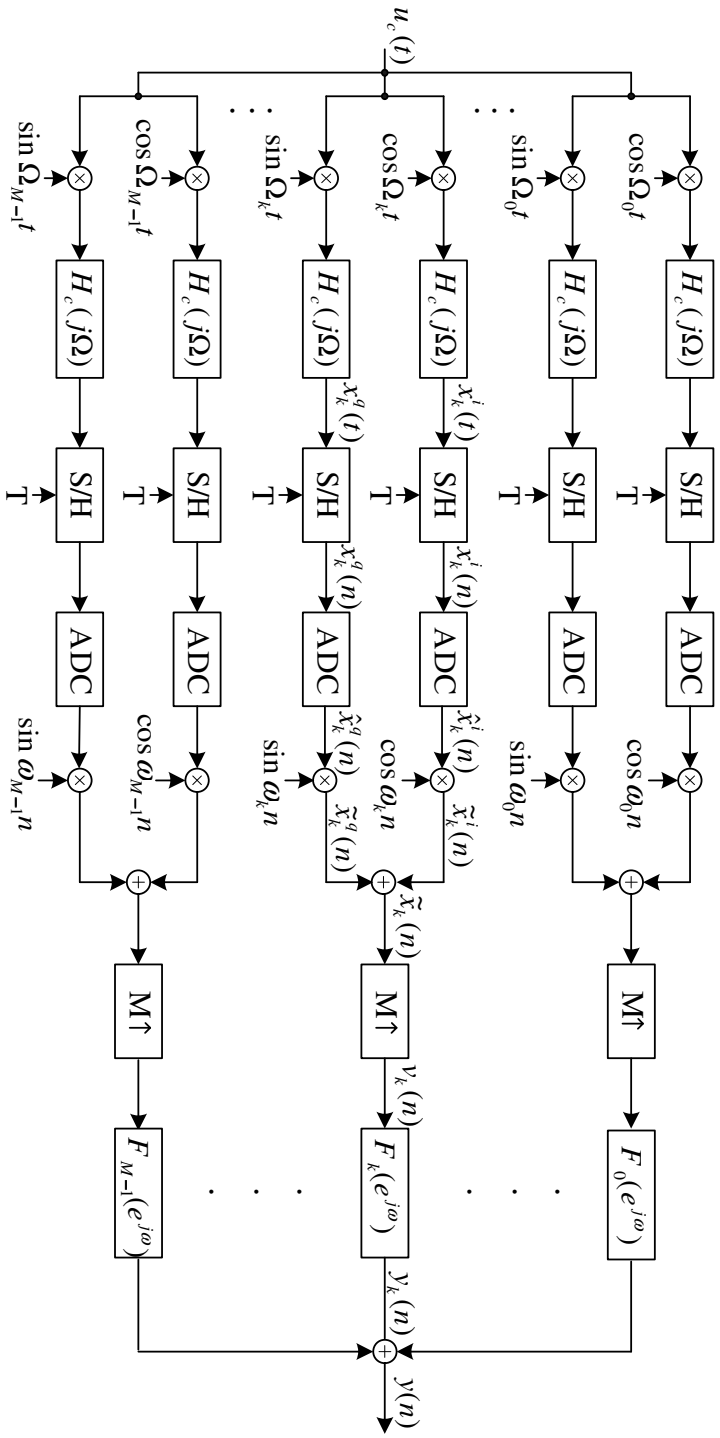


Figure 3.1: The frequency-translating hybrid analog-to-digital converter (FTH-ADC) structure.

An oversampling ratio (OSR) of 2 is chosen for each subband ADC, which reduces the complexity of the implementation of the digital upconverting mixers by reducing the multiplication coefficients to ±1s and 0s. Therefore, these mixers can be implemented using inverters and buffers instead of multiplier blocks.

Another option would be to use an ADC with a sample rate of Ω_B/M (Nyquist rate) together with an upsampler and a digital low-pass filter which is not used in this structure as it produces aliasing terms that may deteriorate the SNDR of the overall system, as will be discussed in the following subsection. In order to upconvert the digitized signal in each channel back to its corresponding center frequency in the digital domain, the second quadrature mixers should have a digital local oscillator with a frequency of $\omega_k = \Omega_k.T$, where T is the sampling period of each subband ADC as specified in (3.3).

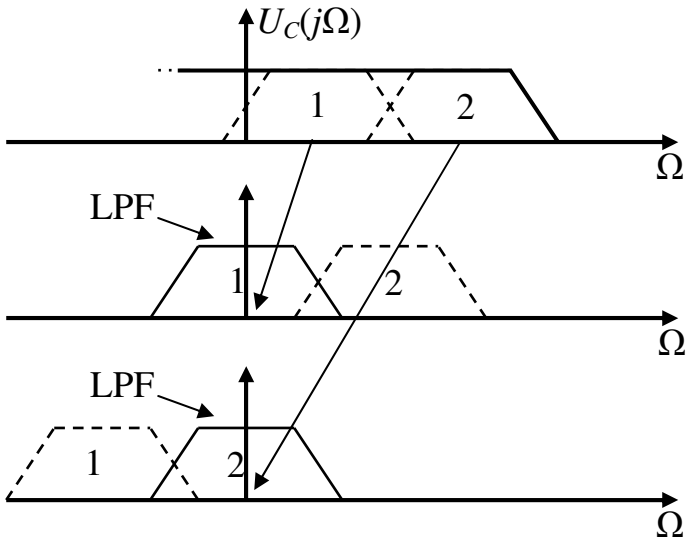


Figure 3.2: Shifting the wideband input signal into baseband in the FTH-ADC.

Figure 3.2 shows how the wideband analog input signal is mixed down and filtered in a 2-channel system. For simplicity, only the positive frequency portion of the spectrum is

shown. Numbered portions of the spectrum show the subband signal processed in each channel. It should be noted that similar ideas of parallel frequency-translation and filtering have previously been used in [48] for an ADC system and in [49] for a serial link receiver; however, these systems had different digital reconstruction structures and aimed for lower resolutions and different applications.

3.2 Digital Reconstruction Filter Design

3.2.1 The Distortion/Aliasing Terms

As stated before, assume the input signal is a wide, baseband signal limited to Ω_B. After the signal is downconverted by the quadrature mixers and low-pass filtered by the identical analysis filters with an impulse response of $h_c(t)$ and a transfer function of $H_c(j\Omega)$, the subband signal in the I and Q channels can be written as

$$X_k^i(j\Omega) = \frac{1}{2}\left[U_c(j\Omega - j\Omega_k)\cdot H_c(j\Omega) + U_c(j\Omega + j\Omega_k)\cdot H_c(j\Omega)\right] \tag{3.4}$$

for the in-phase component of channel k and

$$X_k^q(j\Omega) = \frac{1}{2j}\left[U_c(j\Omega - j\Omega_k)\cdot H_c(j\Omega) - U_c(j\Omega + j\Omega_k)\cdot H_c(j\Omega)\right] \tag{3.5}$$

for the quadrature component of channel k. Downsampling followed by analog-to-digital conversion yields (assuming ideal ADC converters),

$$\hat{X}_k^i(e^{j\omega}) = \frac{1}{2T}\sum_{m=-\infty}^{+\infty}\left[U_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} - j\Omega_k) + U_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} + j\Omega_k)\right] \cdot H_c(j\frac{\omega}{T} - j\frac{2\pi m}{T}) \tag{3.6}$$

and

$$\hat{X}_k^q(e^{j\omega}) = \frac{-j}{2T}\sum_{m=-\infty}^{+\infty}\left[U_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} - j\Omega_k) - U_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} + j\Omega_k)\right] \cdot H_c(j\frac{\omega}{T} - j\frac{2\pi m}{T}) \tag{3.7}$$

I and Q components are then digitized by the ADCs in each channel and frequency-translated back to their corresponding centre frequencies and finally added together, so that

$$\tilde{X}_k(e^{j\omega}) = \frac{1}{T}\sum_{m=-\infty}^{+\infty} U_c(j\frac{\omega}{T} - j\frac{2\pi m}{T})\cdot\left[H_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} - j\Omega_k) + H_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} + j\Omega_k)\right]. \tag{3.8}$$

The subband signal is then upsampled, and passed through the subband digital synthesis filters. Finally, the system output is the sum of the outputs of all the channels [47], (assuming M is the number of channels in the system)

$$\begin{aligned} Y(e^{j\omega}) &= \frac{M}{T}\sum_{k=0}^{M-1} Y_k(e^{j\omega}) \\ &= \frac{M}{T}\sum_{k=0}^{M-1}\sum_{m=-\infty}^{+\infty} F_k(e^{j\omega})\cdot U_c(\frac{j\omega M}{T} - \frac{j2\pi m}{T}). \\ &\left[H_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} - j\Omega_k) + H_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} + j\Omega_k)\right] \end{aligned} \tag{3.9}$$

Because of the effective subsampling by *M* in each channel. As shown in [50]-[51], the above equation can be reduced into

$$\begin{aligned} Y(e^{j\omega}) = \frac{M}{T}\sum_{m=0}^{M=1} U_c(\frac{j\omega M}{T} - \frac{j2\pi m}{T})\cdot\sum_{k=0}^{M-1} F_k(e^{j\omega})\cdot \\ \left[H_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} - j\Omega_k) + H_c(j\frac{\omega}{T} - j\frac{2\pi m}{T} + j\Omega_k)\right] \end{aligned} \tag{3.10}$$

where $U(.)$ and $H(.)$ are periodic frequency-domain representations of the sampled $u_c(t)$ and $h_c(t)$, respectively. The digital synthesis filters, $F_k(z)$, are designed such that the system output, $Y(e^{j\omega})$, should simply be a scaled, delayed version of the input, $U(j\Omega)$, i.e.,

$$\begin{aligned} Y(e^{j\omega}) &= \sum_{m=0}^{M-1} U\left(\frac{j\omega M}{T} - \frac{j2\pi m}{T}\right) \cdot T_m(e^{j\omega}) \\ &= Ce^{-j\omega d} U\left(j\frac{\omega M}{T}\right) \end{aligned} \tag{3.11}$$

where d is the system delay, C is a constant, and the distortion/aliasing functions, $T_m(e^{j\omega})$, $0 \le m \le M\text{-}1$, are,

$$\begin{aligned} T_m(e^{j\omega}) = \sum_{k=0}^{M-1} F_k(e^{j\omega}) [& H\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} + j\Omega_k\right) + \\ & H\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} - j\Omega_k\right)] \end{aligned} \tag{3.12}$$

Perfect reconstruction (as discussed in Chapter 1) will therefore occur when the first term, the distortion function, $T_0(e^{j\omega})$, ideally corresponds to a perfect delay and the following aliasing terms, $T_p(e^{j\omega})$, ideally equal to zero, i.e.,

$$T_0(e^{j\omega}) = Ce^{-j\omega d}, \qquad T_p(e^{j\omega}) = 0. \qquad 1 \le p \le M-1 \tag{3.13}$$

The ideal digital reconstruction filters should therefore be designed such that the above equations are met.

In practice, perfect reconstruction may not be achieved for various reasons, including the analog nature of the analysis filters, finite precision of the digital filter coefficients and the limited length of these filters. In fact, the aliasing terms need not be totally canceled. It is sufficient that these terms be small enough not to degrade the required SNDR for the resolution of the total ADC system.

It should be noted that the baseband assumption on the wideband analog input signal is only for brevity and simplicity in the equations and the same analysis holds for a bandpass analog input signal, with the difference that a frequency-offset term equal to the offset frequency of the baseband input signal would be added to all of the mixer frequencies used. This offset frequency term can be defined as the centre frequency or the lowest frequency of the baseband input signal and the equations can be adjusted accordingly.

For example, assuming Ω_B is the bandwidth of a wideband analog input signal with the lowest frequency of Ω_L and highest frequency of Ω_H ($\Omega_B = \Omega_H - \Omega_L$), an offset frequency of $\Omega_{offset} = \Omega_L$ can be added to the mixer frequencies defined in (3.1):

$$\Omega_k = \frac{(2k+1)\Omega_B}{2M} + \Omega_L \tag{3.14}$$

where k is the channel index ($0 \leq k \leq M$-1). Note that the digital mixer frequencies have to be updated accordingly.

To minimize the reconstruction error, an optimization method can be used to design the synthesis filters such that equations in (3.13) are approximately held with sufficiently small errors. One such optimization technique, that assumes that the synthesis filters are real and finite impulse response (FIR), is presented in [50] and [52], and will be briefly discussed in the following section.

3.2.2 Digital Filter Optimization

The mathematical optimization routine used in [50] and [52], is exploited herein to calculate the synthesis filters, $F_k(e^{j\omega})$. Given the low-pass standard analysis filter, $H(j\Omega)$, the routine calculates an initial guess for $F_k(e^{j\omega})$ using the distortion/aliasing terms equations in (3.13).

To do this, the analysis filter transfer function amplitude and phase data at *N* equally spaced frequency points are calculated. These values are then applied to (3.11)-(3.13) to derive values for $F_k(e^{j\omega})$, i.e., the target reconstruction filters frequency responses. The optimization routine calculates the best real, causal, finite impulse response (FIR) approximations of these filters in the time domain.

An efficient way to design FIR synthesis filters with length *L*,

$$\hat{F}_k(z) = \sum_{n=0}^{L-1} \hat{f}_k[n] \cdot z^{-n} \tag{3.15}$$

whose frequency responses, $\hat{F}_k\left(e^{j\omega}\right)$, optimally approximate the targeted filter frequency responses, $F_k\left(e^{j\omega}\right)$, in a squared error sense,

$$\varepsilon_k = \int_{-\pi}^{\pi} \left|\hat{F}_k(e^{j\omega}) - F_k(e^{j\omega})\right|^2 d\omega \tag{3.16}$$

is calculated as follows. As shown in [50] and [52], the impulse response of the synthesis filter that minimizes the squared error is simply the inverse Fourier transform of the ideal frequency response,

$$\hat{f}_k[n] = \frac{1}{2\pi} \int_{-\pi}^{\pi} F_k(e^{j\omega}) e^{j\omega n} d\omega \tag{3.17}$$

which can be calculated using the fast Fourier transform (FFT) algorithm.

When calculating the Inverse Fourier transform of these ideal frequency response expressions, it is important to ensure that the calculated synthesis filters coefficients are real. This means that the Fourier transforms of the filters must be conjugate-symmetric. The Fourier transforms of the ideal synthesis filters are specified over the interval $0 \le \omega \le \pi$ so the conjugate-symmetric Fourier transform of the ideal synthesis filters from $-\pi \le \omega \le \pi$ (or

equivalently $\pi \le \omega \le 2\pi$ as used in some FFT algorithms) can be formed by taking the complex conjugate of the Fourier transform on $0 \le \omega \le \pi$, reversing it in frequency, and moving it to $-\pi \le \omega \le 0$ (or $-\pi \le \omega \le 2\pi$).

Furthermore, the symmetry and 2π periodicity properties of the conjugate-symmetric Fourier transforms require the imaginary part of the transform to be zero at frequencies that are integer multiples of π. Since the ideal synthesis filter expressions are not guaranteed to meet this property, these criteria should be forced manually.

Using N samples of the ideal conjugate-symmetric synthesis filter Fourier transform, $F_k(e^{j\omega})\Big|_{\omega=\frac{2\pi p}{N}}$, $p = 0,...,N-1$, the N-point inverse FFT, $f_k^{(N)}[n]$, is the impulse response of the desired filter time-aliased every N points. N should be chosen large enough that the impulse response has sufficiently decayed so that the time aliasing is negligible (e.g., N = 1024 points), therefore,

$$f_k^{(N)}[n] \approx \frac{1}{2\pi}\int_{-\pi}^{\pi} F_K(e^{j\omega})e^{j\omega n}d\omega = f_k[n] \tag{3.18}$$

However, the resulting N-point impulse response is unnecessarily long. Therefore, it is windowed with a length L boxcar function,

$$\hat{f}_k[n] = f_k^{(N)}[n].\omega[n] \tag{3.19}$$

where the boxcar function is,

$$\omega[n] = \begin{cases} 1, & 0 \le n \le L-1 \\ 0, & L \le n \le N \end{cases} \tag{3.20}$$

Evaluating the error term defined in (3.16) is easier in time domain. By Parseval's relation, equation (3.16) can be rewritten as [52],

$$\varepsilon = \sum_{k=0}^{M-1} \varepsilon_k = \sum_{k=0}^{M-1} \int_{-\pi}^{\pi} \left| \hat{F}_k(e^{j\omega}) - F_k(e^{j\omega}) \right|^2 d\omega \tag{3.21}$$

and minimizing (3.24) is equivalent to minimizing

$$\varepsilon = \sum_{k=0}^{M-1} \sum_{n=-\infty}^{+\infty} \left(\hat{f}_k[n] - f_k[n] \right)^2 \tag{3.22}$$

so,

$$\varepsilon = \sum_{k=0}^{M-1} \sum_{n=L}^{N} \left(f_k^{(N)}[n] \right)^2 \tag{3.23}$$

The error is minimized by iteratively adjusting the system delay, *d*, recalculating the synthesis filters and repeating until the energy in the truncated coefficients is minimized. A standard minimization algorithm, the Nelder-Mead Simplex algorithm has been used [53].

This optimization is computationally efficient because it relies on iterated evaluations of the inverse FFT, and it can calculate optimal synthesis filters and system delay. Note that with the resulting filters, the distortion term should be as close as possible to a constant and the aliasing terms should not limit the resolution of the system.

3.2.3 The 2-channel Case

The special case of $M = 2$ will be used in the following chapter to implement a 2-channel frequency translating hybrid ADC at the board-level. Therefore, the ideal digital reconstruction filters frequency response for this 2-channel system ($M = 2$) will be calculated in this section.

For a 2-channel system, the output signal can be written as:

$$Y_k(e^{j\omega}) = \frac{2}{T}\left[U(j\frac{2\omega}{T}) T_0(e^{j\omega}) + U(j\frac{2\omega}{T} - j\frac{2\pi}{T}) T_1(e^{j\omega}) \right] \tag{3.24}$$

with the distortion/aliasing terms as

$$T_0(e^{j\omega}) = \left[H(j\frac{2\omega}{T} - j\Omega_0) + H(j\frac{2\omega}{T} + j\Omega_0) \right] \cdot F_0(e^{j\omega}) \\ \left[H(j\frac{2\omega}{T} - j\Omega_1) + H(j\frac{2\omega}{T} + j\Omega_1) \right] \cdot F_1(e^{j\omega}) = Ce^{-j\omega d} \tag{3.25}$$

$$T_1(e^{j\omega}) = \left[H(j\frac{2\omega}{T} - j\frac{2\pi}{T} - j\Omega_0) + H(j\frac{2\omega}{T} - j\frac{2\pi}{T} + j\Omega_0) \right] \cdot F_0(e^{j\omega}) \\ \left[H(j\frac{2\omega}{T} - j\frac{2\pi}{T} - j\Omega_1) + H(j\frac{2\omega}{T} - j\frac{2\pi}{T} + j\Omega_1) \right] \cdot F_1(e^{j\omega}) = 0. \tag{3.26}$$

Solving for the ideal digital reconstruction filters, we obtain:

$$F_0(e^{j\omega}) = \frac{Ce^{-j\omega d} \cdot \left[H(j\frac{2\omega}{T} - j\frac{2\pi}{T} + j\Omega_1) + H(j\frac{2\omega}{T} - j\frac{2\pi}{T} - j\Omega_1) \right]}{den} \tag{3.27}$$

and,

$$F_1(e^{j\omega}) = -\frac{Ce^{-j\omega d} \cdot \left[H(j\frac{2\omega}{T} - j\frac{2\pi}{T} + j\Omega_0) + H(j\frac{2\omega}{T} - j\frac{2\pi}{T} - j\Omega_0) \right]}{den} \tag{3.28}$$

where,

$$den = \{ [H(j\frac{2\omega}{T} + j\Omega_0) + H(j\frac{2\omega}{T} - j\Omega_0)] \times \\ [H(j\frac{2\omega}{T} - j\frac{2\pi}{T} + j\Omega_1) + H(j\frac{2\omega}{T} - j\frac{2\pi}{T} - j\Omega_1)] \\ -[H(j\frac{2\omega}{T} + j\Omega_1) + H(j\frac{2\omega}{T} - j\Omega_1)] \times \\ [H(j\frac{2\omega}{T} - j\frac{2\pi}{T} + j\Omega_0) + H(j\frac{2\omega}{T} - j\frac{2\pi}{T} - j\Omega_0)] \} \tag{3.29}$$

3.2.4 Simulation Results

Matlab and Simulink simulations were used to model a 2-channel system with a normalized bandwidth of BW_{eff} = 2 and four ideal identical 8-bit ADCs, each with a normalized bandwidth of BW_{sub} = 0.5 and a normalized sampling rate of f_{sub} = 2. Four

identical continuous-time 5th-order Butterworth low-pass filters, each with a normalized 3-dB cutoff frequency of f_{cutoff} = 0.5, are used as subband filters. For this system, the two normalized mixer frequencies are therefore 0.5 and 1.5, respectively, according to (3.1).

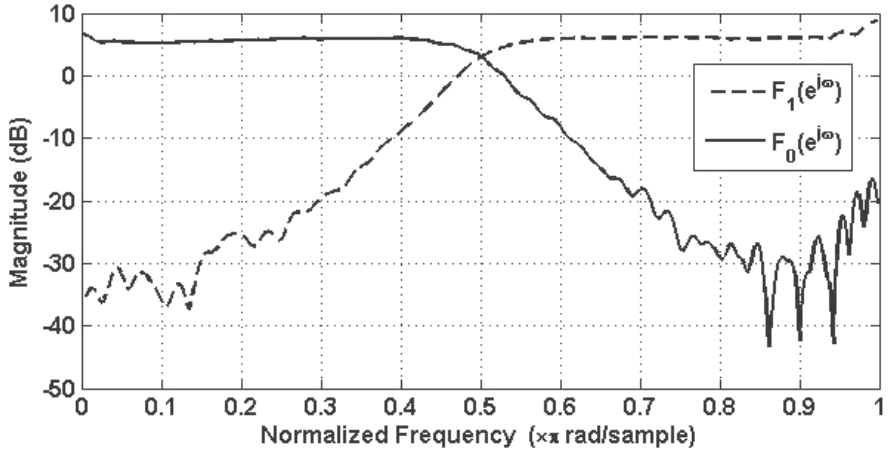


Figure 3.3: The digital, 12-bit 128-tap FIR reconstruction filters for a 2-channel FTH-ADC system with a normalized input BW of 2 (effective sampling rate of 4), and 5th-order Butterworth filters.

Butterworth filters are chosen for their maximally flat passband characteristic which results in less complex synthesis filters [50]. Other analog filters, however, can also be used, and appropriate digital filters can be designed accordingly with a proper optimization technique.

A normalized effective sampling rate of F_{eff} = 4 (Nyquist rate for the wideband input signal) is achieved for this system using digital 128-tap FIR reconstruction filters with 12-bit quantized coefficients. The synthesis filters are designed using the optimization techniques discussed in Section 3.2.2. The frequency responses of these filters are shown in Figure 3.3.

Figure 3.4 shows the output spectrum of the simulated FTH-ADC for a normalized input frequency of $f_{in} = 1.71$. As can be seen in this figure, an ENOB of more than 7.5 bits can be achieved using the designed filters shown in Figure 3.3.

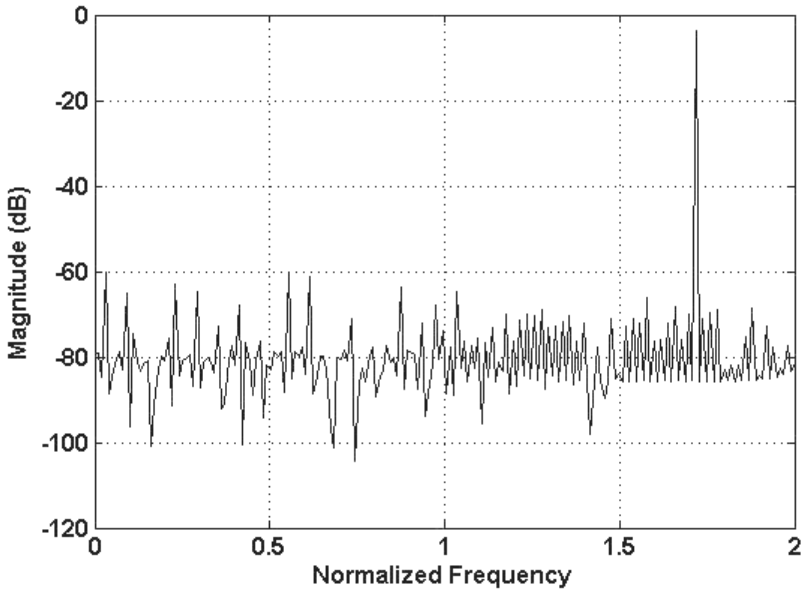


Figure 3.4: Simulated output spectrum of a 2-channel system with a normalized input BW of 2, and 8-bit subchannel ADCs and 128-tap 12-bit FIR reconstruction filters ($F_{in} = 1.71$).

As a multi-tone test to inspect the operation of the system in the presence of more than one tone, Figure 3.5 shows the output spectrum of the simulated FTH-ADC system for a multi-tone wideband analog input signal composed of $f_{in} = 0.51$, $f_{in} = 0.72$ and $f_{in} = 1.71$ with equal amplitudes. Again, it can be seen that more than 7.5 bits can be achieved for all the input test tones chosen anywhere on the input bandwidth.

Figure 3.6 shows the ENOB of the overall system over the entire normalized bandwidth of 2. As can be seen in this figure, an ENOB of at least 7.5 bits is attainable everywhere across the band.

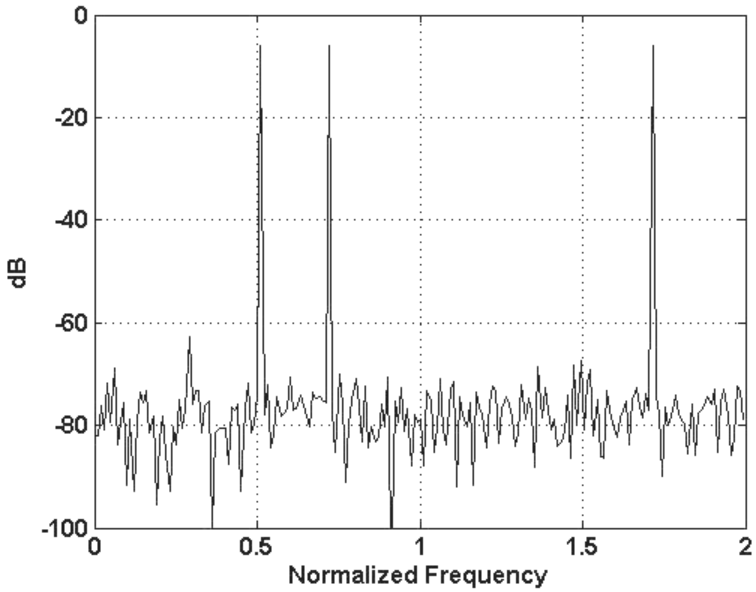


Figure 3.5: Simulated output spectrum of a 2-channel system with a normalized input BW of 2, and 8-bit subchannel ADCs and 128-tap 12-bit FIR reconstruction filters with multi-tone input (f_{in} = *0.51, 0.72* and *1.71*).

It should be noted that several sources of implementation error such as analog non-idealities and component mismatches can affect the performance of the FTH-ADC. These errors are not discussed in this chapter and therefore are not included in the simulations reported here. Also, depending on the sources of errors and the system performance metrics required, the complexity of the digital reconstruction may vary.

This will be further discussed in the following chapter where a board-level proof-of-concept implementation is used to study major sources of error and complexity in the board-level implementation of the FTH-ADC as well as techniques to measure and compensate for these errors.

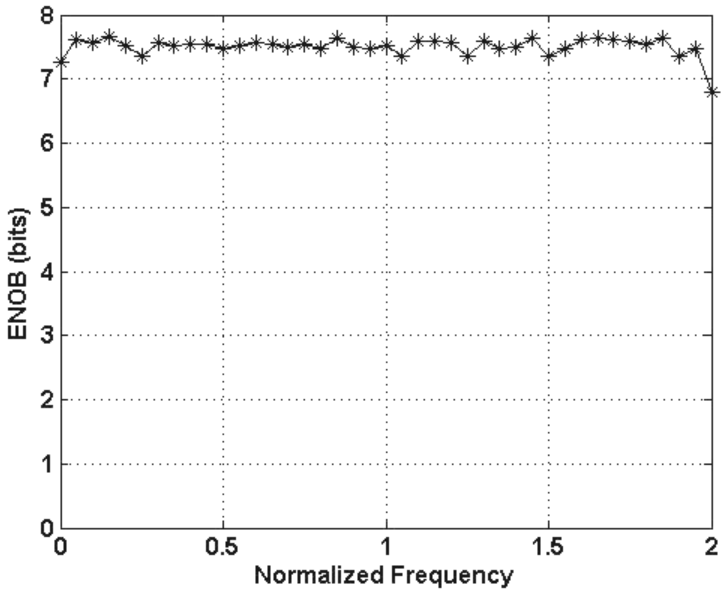


Figure 3.6: ENOB for a 2-channel system over the normalized input BW of 2, with 8-bit subchannel ADCs and 128-tap 12-bit FIR reconstruction filters.

3.3 Comparison with Conventional Parallel ADC Architectures

The proposed FTH-ADC system has many advantages compared to conventional parallel ADC structures discussed in Chapter 2. As stated before, the need for a high-precision, wideband, sample-and-hold (S/H) stage at the input stage of the time-interleaved (TI), Hadamard-modulated, and the QMF-FBD structures is one of the major challenges in the design of such systems. In the HFB structure, this problem is partly addressed, since signal sampling is performed after the wideband input signal is decomposed into narrower subbands. However, since this architecture does not frequency-translate high-frequency bands down to baseband, it still requires wideband S/H circuitry that needs to operate over

the corresponding frequency band of each channel and the analog bandpass filters should be tuned to the center frequency of each channel; both are challenging design tasks.

In the frequency-translating hybrid ADC, the above-mentioned problems associated with sampling are resolved by performing the sampling task on the narrowband baseband signal. Since sampling is done after the signal is filtered and quadrature-downconverted, i.e., after the wideband signal is decomposed into smaller baseband subbands, the S/H circuits needed for this structure are identical narrowband baseband circuits that can be implemented on a single CMOS chip together with the other blocks of the system. This is in contrast to the more costly solutions offered for TI structures, e.g., in [5], [21], that include using other technologies to implement the required high-speed, high-precision S/H stages.

In the proposed FTH-ADC architecture, the bandpass subband ADCs of each channel have been replaced by identical narrowband baseband ADCs with an OSR of *2*. The multiplication coefficients in the digital mixer array are therefore simplified to ±1s and 0s; i.e., no actual multipliers are therefore required.

Except for the centre frequency of the mixers and the coefficients of the digital reconstruction filters, the subband channel components in the FTH-ADC structure are identical which makes the overall system easier to design.

In addition, this structure is very similar to the FBD and the HFB architectures and inherits the lower sensitivity to jitter and channel component mismatch error characteristic of these architectures, compared to the time-interleaved structure.

Since the signal energy is distributed between the channels, the dynamic range requirement on the subband ADCs of the FTH-ADC structure is more relaxed as is the case in all frequency-decomposition based structures.

The main challenges to overcome in this structure include sensitivity to the mixers non-idealities such as linearity and I/Q phase and amplitude imbalance, local oscillators phase noise and ADC non-idealities such as gain mismatch and offset errors. Most of these errors can be sufficiently compensated in the digital domain as will be discussed in Chapter 4 for a 2-channel case. In addition, linearity, speed and power are main circuit issues that will be discussed in Chapter 5, in the circuit-level and CMOS implementation of one channel of a 2-channel FTH-ADC system.

It should also be noted that although the number of channels in the FTH-ADC system can be arbitrarily large in theory, as in many other parallel ADC structures, this number is limited in practice. This limitation is due to various implementation trade-offs and costs. For example, as the number of channel increases, to achieve higher ENOBs, higher reconstruction costs, e.g., in terms of filter lengths and number of bits per filter coefficients is required. Besides, the linearity of the front-end analog mixer stages can become a design bottleneck in very high speed systems and therefore limit the maximum attainable resolution or conversion speed.

4 PROOF-OF-CONCEPT: BOARD-LEVEL IMPLEMENTATION-ERROR AND COMPLEXITY SOURCES, MEASUREMENT AND COMPENSATION METHODS

In this chapter, the performance specifications of the FTH-ADCs in the presence of major analog non-idealities are analyzed and challenges and trade-offs in the practical realization of these systems as well as complexity trade-offs are discussed.

Sources of analog non-idealities and component mismatches that are discussed in this chapter include the subband ADC gain mismatch error and offset error, quadrature mixer I/Q channel gain and phase imbalance error, subband ADC clock and local oscillator (LO) jitter and analog analysis filter implementation errors.

Sources of complexity include the digital implementation cost, length and resolution of the digital synthesis filters and type and order of the analog analysis filters. It should be noted that any error that introduces changes in the aliasing terms appearing at the output spectrum (e.g., amplitude change) compared to (3.11), affects the SNDR and hence the total system resolution.

After discussing the effects of the error sources on the performance of the FTH-ADC, measurement and compensation techniques are presented to improve the performance in the presence of such errors. As a proof-of-concept, a 2-channel, 200 MHz, 7-bit prototype

FTH-ADC system is implemented using off-the-shelf mixer and DSP/FPGA boards. The proposed measurement and compensation techniques are implemented on this board to demonstrate their feasibility and effectiveness.

4.1 Sources of Error and Compensation Methods

4.1.1 Subchannel ADC Gain/Offset Mismatch Error

The subchannel ADC characteristic in the presence of gain mismatch and offset errors can be modeled as:

$$\hat{x}_k^{\{i,q\}}(n) = (1+a_k)\cdot x_k^{\{i,q\}}(n) + b_k \tag{4.1}$$

where a_k and b_k are the gain and offset errors of the k^{th} subband ADC [31]. By applying this model to the system, we have [47]:

$$\begin{aligned} Y(e^{j\omega}) &= \frac{M}{T}\sum_{m=0}^{M-1} U\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T}\right)\sum_{k=0}^{M-1}(1+a_k)F_k(e^{j\omega})\cdot \\ &\left[H\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} - j\Omega_k\right) + H\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} + j\Omega_k\right)\right] \\ &+\sum_{k=0}^{M-1} b_k.\delta\left(j\frac{\omega M}{T} - j\Omega_k\right)\cdot F_k(e^{j\omega}) \end{aligned} \tag{4.2}$$

ADC gain errors will therefore affect the SNDR of the output by scaling the magnitude of the distortion/aliasing terms by $(1+a_k)$. The mismatch between ADCs in different channels can be compensated by taking these gain mismatch coefficients into account when designing the digital reconstruction filters.

The gain mismatch of subband ADCs between two paths of one channel can be treated as I/Q path mismatch and can be measured and compensated as will be discussed in Section 4.1.2. As can be seen from (4.2), ADC offset errors, b_k, however, are frequency-

translated to the center frequency, ω_k, in each channel. To prevent these errors from adding unwanted terms to the output, these dc values are measured and subtracted from the output of each ADC.

4.1.2 I/Q Gain and Phase Imbalance

Using the complex signal notation, gain and phase mismatch errors between the I/Q channels in the local oscillators (LOs) can be modeled as [47], [48]:

$$LO_k(t) = \cos(\Omega_k t) + j(1+\varepsilon_k)\sin(\Omega_k t + \theta_k) \tag{4.3}$$

where ε_k and θ_k are the gain and phase mismatch errors in the k^{th} channel, respectively. Applying this model to the system discussed in Chapter 2, (3.5) can be re-written as:

$$\begin{aligned} X_k^q(j\Omega) = \frac{1+\varepsilon_k}{2j}\cdot\Big[& e^{j\theta_k}U(j\Omega - j\Omega_k)H(j\Omega) + \\ & e^{-j\theta_k}U(j\Omega + j\Omega_k)H(j\Omega)\Big] \end{aligned} \tag{4.4}$$

The output will therefore be:

$$\begin{aligned} Y(e^{j\omega}) = \frac{M}{2T}\sum_{k=0}^{M-1} F_k(e^{j\omega}).\Bigg\{ & \sum_{m=0}^{M-1} U\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T}\right) \\ & \Bigg[(1+A_k).H\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} + j\Omega_k\right) \\ & + (1+B_k).H\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} - j\Omega_k\right)\Bigg] + \\ & U\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} - j2\Omega_k\right).(1-A_k).H\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} - j\Omega_k\right) + \\ & U\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} + j2\Omega_k\right).(1-B_k).H\left(j\frac{\omega M}{T} - j\frac{2\pi m}{T} + j\Omega_k\right)\Bigg\} \end{aligned} \tag{4.5}$$

where,

$$\begin{cases} A_k = (1+\varepsilon_k)e^{j\theta_k} \\ B_k = (1+\varepsilon_k)e^{-j\theta_k} \end{cases} \tag{4.6}$$

As can be seen in (4.5), unwanted replicas of the input signal shifted by $2\Omega_k$ appear in the desired band due to the gain and phase mismatch errors in the quadrature paths.

Proper design can keep the corresponding errors small and many approaches have been suggested to cancel the image errors due to gain/phase imbalance in quadrature mixers [55]-[56]. In this chapter, a simple method is presented to measure the imbalances in the calibration mode. This method is described below. Then, the technique of [56] is modified and adopted for this system to compensate for imbalances.

4.1.3 The I/Q Imbalance Measurement and Compensation Technique

In an FTH-ADC system with I/Q imbalances, the output of Q path after passing through the subband ADCs and multiplying by the digital Sine can be written as:

$$\begin{aligned}\tilde{X}_k^q(e^{j\omega}) = \frac{1}{4T}\sum_{m=0}^{M-1} & K_1 U\left(j\left(\frac{\omega}{T}-\frac{2\pi m}{T}\right)\right)H\left(j\left(\frac{\omega}{T}-\frac{2\pi m}{T}-\Omega_k\right)\right) \\ & + K_2 U\left(j\left(\frac{\omega}{T}-\frac{2\pi m}{T}-2\Omega_k\right)\right)H\left(j\left(\frac{\omega}{T}-\frac{2\pi m}{T}-\Omega_k\right)\right) \\ & + K_3 U\left(j\left(\frac{\omega}{T}-\frac{2\pi m}{T}\right)\right)H\left(j\left(\frac{\omega}{T}-\frac{2\pi m}{T}+\Omega_k\right)\right) \\ & + K_4 U\left(j\left(\frac{\omega}{T}-\frac{2\pi m}{T}+2\Omega_k\right)\right)H\left(j\left(\frac{\omega}{T}-\frac{2\pi m}{T}+\Omega_k\right)\right)\end{aligned} \tag{4.7}$$

where,

$$\begin{cases} K_1 = -(1+\varepsilon_k)e^{-j\theta_k} \\ K_2 = (1+\varepsilon_k)e^{j\theta_k} \\ K_3 = -(1+\varepsilon_k)e^{j\theta_k} \\ K_4 = (1+\varepsilon_k)e^{-j\theta_k} \end{cases} \tag{4.8}$$

and $\tilde{X}_k^q(e^{j\omega})$ is the frequency-domain representation of $\tilde{x}_k^q(t)$, as shown in Figure 3.1.

The form of the equation for the I path ($\tilde{X}_k^i(e^{j\omega})$ corresponding to $\tilde{x}_k^i(t)$ in Figure 3.1) is identical to (4.7)-(4.8), except for the multiplication factors, K_n, that are all equal to 1. Note that in this model (refer to (4.3)), amplitude and phase mismatches are considered with reference to the I path.

Ideally, if ε_k and θ_k are zero, the signal component terms, corresponding to the terms with coefficients K_1 and K_3, would combine and the unwanted terms of the replica of the input signal shifted by $2\Omega_k$, corresponding to the terms with coefficients K_2 and K_4 would cancel each other after summing the I and Q paths data in each channel. Therefore, an approach should be used to measure and compensate for the extra unwanted terms so they still cancel each other, in the presence of the errors.

If ε_k and θ_k are known, a simple compensation method would be to multiply the digital samples in the Q path by $\sin(\omega_k n-\theta_k)$ rather than $\sin(\omega_k n)$. In this case, coefficients K_n of the Q path (see (4.8)), will change to:

$$\begin{cases} K_1 = -(1+\varepsilon_k)e^{-2j\theta_k} \\ K_2 = (1+\varepsilon_k) \\ K_3 = -(1+\varepsilon_k)e^{2j\theta_k} \\ K_4 = (1+\varepsilon_k) \end{cases} \tag{4.9}$$

Therefore, if the amplitude mismatch of $(1+\varepsilon_k)$ is adjusted, the unwanted replicas of the input signal shifted by $2\Omega_k$, corresponding to the terms with coefficients K_2 and K_4, can be eliminated after combing the I and Q paths data of the channel.

However, it can be seen that K_1 and K_3, that are the signal component coefficients, now include a phase distortion factor. This means that this method cannot be used to effectively compensate for the I/Q gain and phase imbalance unless no useful data is carried

in the phase of the signal; however, since the unwanted components are minimized, this method can be used to measure the phase error, θ_k, as follows:

To get an estimate of ε_k and θ_k, a single tone signal (with test tones swept across the bandwidth) is applied as an input to the FTH system. For a given input frequency, in each channel, the ratio of the RMS of the signal in the I and Q paths is used as an estimate of the amplitude mismatch, $(1+\varepsilon_k)$, at that frequency.

For each input frequency, the output of the Q path in each channel is multiplied by $\sin(\omega_k n-\varphi_k)$ and the value of φ_k is swept to minimize the unwanted image terms. The value of φ_k that minimizes the image terms is used as the estimate of θ_k. ε_k measurements can be included in the path mismatch measurements. It should be noted that ε_k and θ_k are in general frequency dependent.

To summarize, here is a step-by-step description of the proposed phase measurement method:

- Step (a): Apply a single-tone input signal.
- Step (b): Instead of multiplying the Q path data by the digital $\sin(\omega_k n)$, mutiply by $\sin(\omega_k n-\varphi_k)$, where φ_k is swept over the expected phase imbalance range (-5° to +5° in this case). Save the value of φ_k for which the unwanted terms appearing in the output spectrum are minimized. This value is used for θ_k.
- Step (c): Repeat Steps (a) and (b) for input tones across the entire input bandwidth of the system for the desired number of measurements.

Once these measurements are done, a method similar to [56] can be adopted to compensate for the I/Q gain and phase imbalance. In this compensation method, the signal samples in the I and Q paths are multiplied by two correction coefficient vectors, α_k and β_k,

that are implemented as two FIR filters per channel for the FTH-ADC system (since these vectors are also frequency-variant).

However, contrary to the system proposed in [56], in the FTH ADC, due to frequency-conversion and overlapping positive and negative frequency bands at the baseband, the correction stages should be placed after the second mixer stages; as shown in Figure 4.1 in the dashed blocks. This allows for the correction filtering stage to operate on the intended frequency band. Therefore, the α_k and β_k vector values for each channel of the FTH-ADC system should be calculated.

After writing the equations, the combined and compensated output of each channel ($v_k(n)$ in Figure 4.1), can be written as:

$$v_k(n) = \alpha_k \hat{x}_k^i(n)\cos(\omega_k n) + \left[\beta_k \hat{x}_k^i(n) + \hat{x}_k^q(n)\right]\sin(\omega_k n) \tag{4.10}$$

with α_k and β_k vector values for the k^{th} channel calculated as:

$$\begin{cases} \alpha_k = (1+\varepsilon_k)\cdot\cos(\theta_k) \\ \beta_k = (1+\varepsilon_k)\cdot\sin(\theta_k) \end{cases}, \tag{4.11}$$

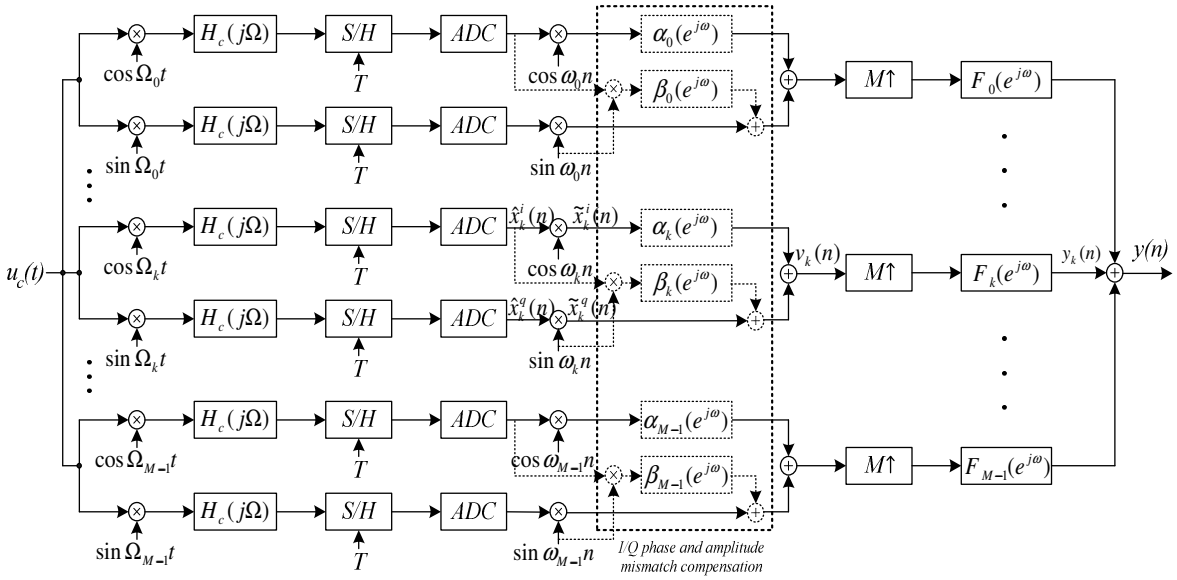


Figure 4.1: The frequency-translating hybrid architecture with the compensation blocks (shown with dashed lines).

4.1.4 ADC and LO Jitter

Similar to the FBD structure, since all channels are undersampled by the same clock signal, the system performance is less sensitive to sampling clock jitter compared to the TI ADC structure [33], [38].

Channel LOs that are used to perform the downconversions must, however, generate signals with low jitter. Phase noise (jitter) in the local oscillators (LO) and the subband ADCs can be modeled as [47]-[48]:

$$LO_k = \cos(\Omega_k t + \Phi(t)) + j\sin(\Omega_k t + \Phi(t)) \tag{4.12}$$

where $\Phi(t)$ is a random, zero-mean variable with Gaussian distribution with a standard deviation of σ_Φ. The jitter power adds up to and therefore increases the noise floor in each subband. If σ_Φ is high, the errors due to jitter may dominate the maximum noise level and therefore decrease the overall SNDR, thereby deteriorating the effective resolution. However, since the error due to this type of jitter is wideband in nature, some level of jitter is tolerable.

Figure 4.2 shows simulation results for the effective number of bits of a 2-channel system with a normalized bandwidth of 2 and four ideal identical 12-bit ADCs, each with a normalized bandwidth of 0.5 and a normalized sampling rate of 2. Four identical continuous-time 5^{th}-order Butterworth low-pass filters, each with a normalized 3-dB cutoff frequency of 0.5, were used as subband filters. The normalized mixer frequencies are therefore chosen as 0.5 and 1.5 for the first and second channels, respectively.

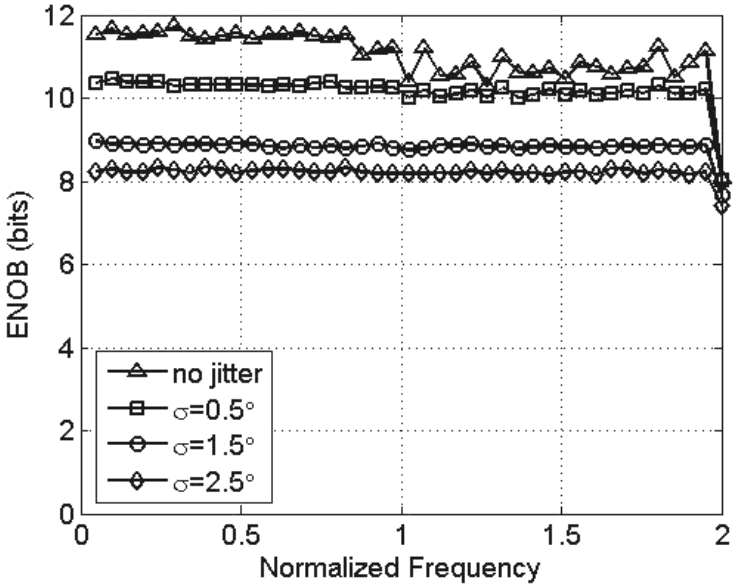


Figure 4.2: The effect of LO Gaussian jitter with σ = 0.5°, 1.5°, and 2.5° on the ENOB of a 2-channel FTH-ADC with 12-bit subband ADCs and 16-bit, 128-tap FIR reconstruction filters.

A normalized effective sampling rate of 4 (Nyquist rate for the wideband input signal) is achieved for this system using digital 128-tap FIR reconstruction filters with 16-bit coefficients. A Gaussian phase jitter with a zero mean and a standard deviation of σ = 0.5°, 1.5°, and 2.5° is added to the local oscillators.

As can be seen in this figure, up to 10 bits of resolution is attainable over the entire band, using the specified FTH-ADC system with low jitter. The performance, however, falls to a little above 8 bits for higher levels of jitter (σ = 2.5°).

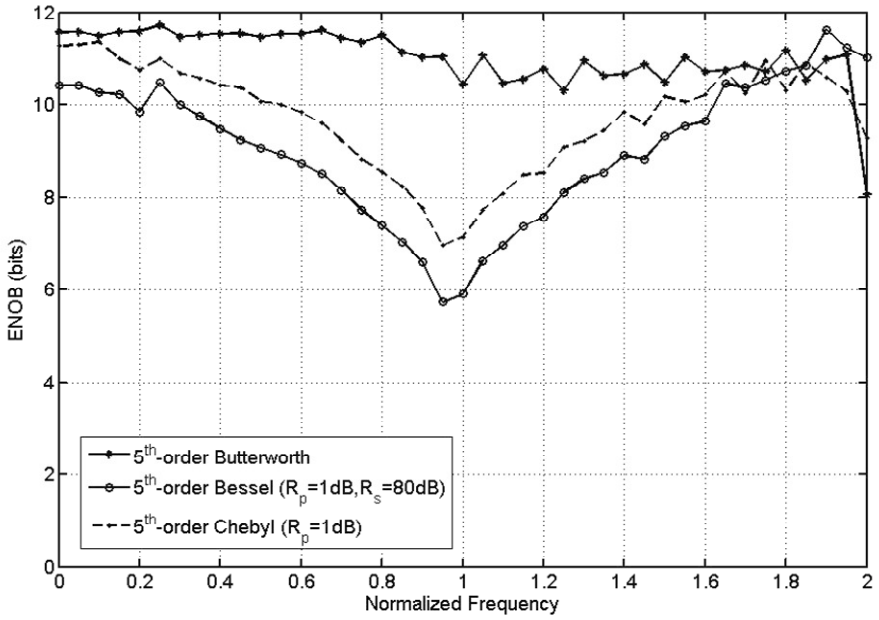


Figure 4.3: ENOB for a 2-channel system with analog 5th-order Butterworth, Chebychev I and Bessel filters with 12-bit ADCs and FIR filter lengths of 128. The best ENOB is attained for the flat characteristic of the Butterworth Filter.

4.1.5 Analog Analysis Filter Implementation Errors

Implementation errors can deteriorate the transfer function of the analog analysis filters. However, the filter mismatches in I and Q paths of each channel translate into I/Q imbalance in that channel and will be compensated as already discussed in Section 4.1.2, using the digital compensation filters. The filter mismatches among different channels can also be compensated by taking them into account in the design of the digital synthesis filters corresponding to those channels.

4.1.6 Analysis Filter Complexity (Type and Order)

To compare the effect of the type of the analysis filters on the system resolution, three 5th-order standard filters, namely, Butterworth, Chebychev and Elliptic filters are used as the analysis filters and the attainable resolution obtained for the 2-channel system with 12-bit subband ADCs and 128-tap FIR reconstruction filters are compared over the entire bandwidth, as shown in Figure 4.3.

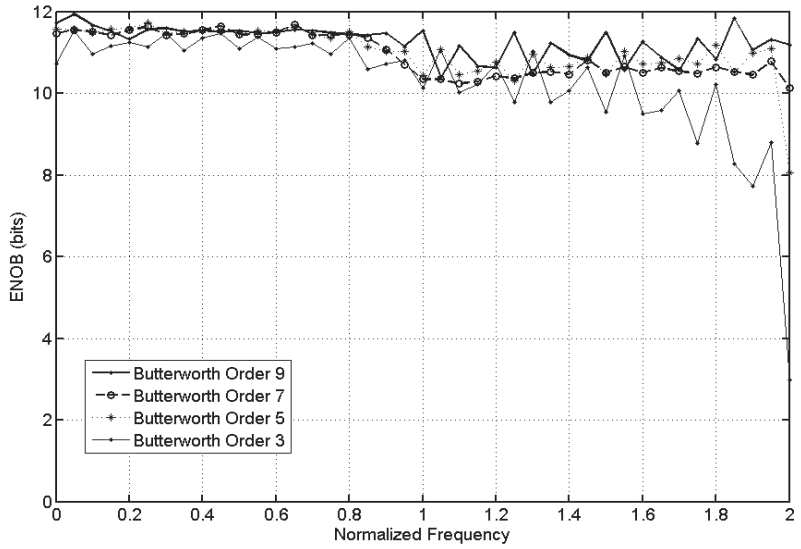


Figure 4.4: ENOB for a 2-channel system with analog Butterworth filters of order 3, 5, 7 and 9 with 12-bit ADCs and 128-tap FIR filters. The order of the analysis filters does not have much effect on the effective ENOB of the total system.

Note that R_p and R_s values are the passband ripple and stopband attenuation in dB scale, respectively. Based on the results presented in this figure and similar to the hybrid

filter bank structures ([43], [45]), Butterworth filters result in the highest attainable ENOB due to their flat passband characteristic.

To compare the effect of the order of analysis filters on the system resolution, Butterworth filters of orders 3, 5, 7 and 9 are incorporated in the 2-channel system with 12-bit subband ADCs and 128-tap FIR reconstruction filters. Figure 4.4 depicts the attainable ENOB over the entire band for these filters.

It can be seen that while a higher order filter can decrease the noise power by attenuating more out-of-band noise components, the overall worst-case attainable ENOB is almost independent of the order of the analysis filter, similar to the hybrid filter bank structures [43].

4.1.7 Synthesis Filter Complexity (Length and Resolution)

The digital reconstruction block of the system consists of upsamplers, digital multipliers, adders, and FIR filters. Since an OSR = 2 is used in each channel ADC, the upsampling and digital multiplication coefficients in the digital mixers are either 0s or ±1s. Therefore, no actual digital multiplier implementation is required for digital mixers. Hence, FIR filters are the main source of implementation complexity in the digital block.

The length (L) and coefficient resolution for the FIR synthesis filters can be chosen based on the trade-off between the overall system resolution and complexity. Figure 4.5 shows the ENOB achieved for a 2-channel system with 5^{th}-order analog Butterworth analysis filters, and 8-bit ADCs with FIR filter lengths of 32, 64, and 128, and 12-bit ADCs with FIR filter lengths of 64 and 128.

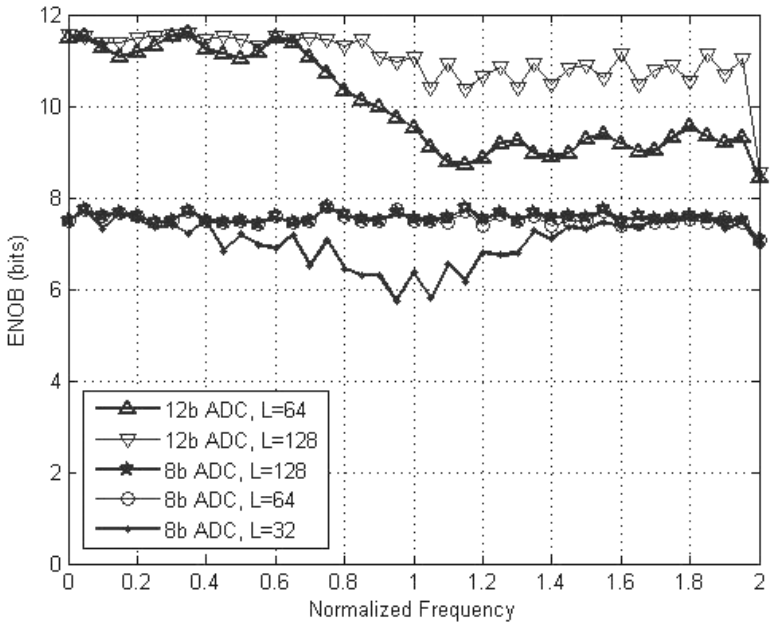


Figure 4.5: ENOB for a 2-channel system with analog 5th-order Butterworth filters with 8-bit ADCs with FIR filter lengths of 32, 64 and 128 and 12-bit ADCs with FIR filter lengths of 64 and 128.

Also, Figure 4.6 shows the ENOB achieved for a 2-channel system with 5th-order analog Butterworth analysis filters, and 8-bit ADCs with 8-bit and 12-bit FIR filters, and 12-bit ADCs with 12-bit and 16-bit FIR filters, all with FIR filter lengths of 128.

Based on Figure 4.5 and Figure 4.6, it can be concluded that depending on the desired resolution, the complexity of the system may vary. For example, as shown in Figure 4.5, there is not much of a difference between L = 64 and 128 for 8-bit resolution but the difference is apparent for 12-bit system resolution. Also, as shown in Figure 4.6, filters with 12-bit coefficients are suitable for 8-bit ADCs but not for 12-bit ADCs.

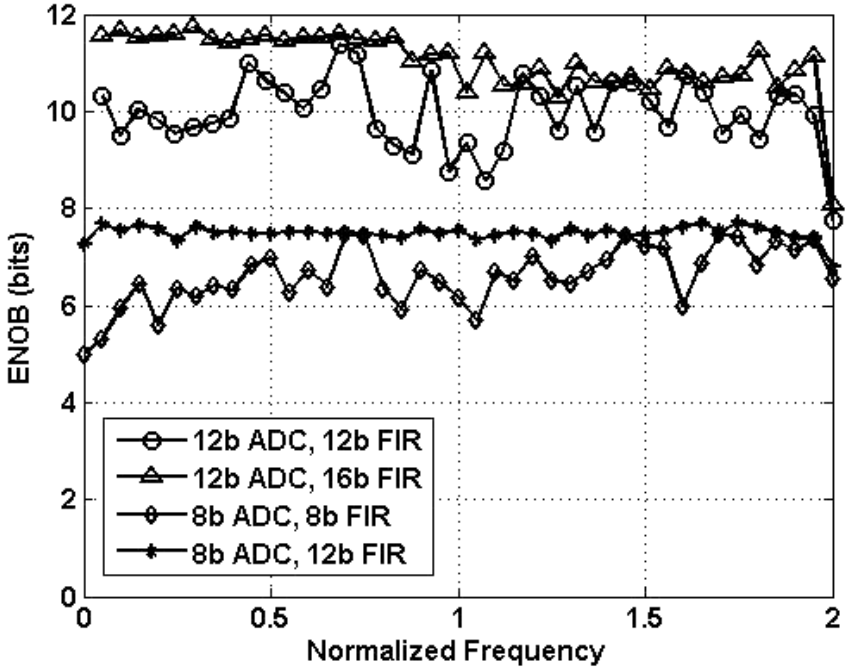


Figure 4.6: ENOB for a 2-channel system with analog 5th-order Butterworth filters with 8-bit ADCs with 8-bit and 12-bit FIR filter lengths of 128 and 12-bit ADCs with 12-bit and 16-bit FIR filter lengths of 128.

It should be noted that digital IIR reconstruction filters can also be used, however, these filters are out of the scope of this thesis. These filters may be harder to design due to their stability and phase distortion issues.

4.2 Measurement Results

4.2.1 The System Set-up

As a proof of concept, a 2-channel system is implemented at the board-level using off-the-shelf components for filters, splitters, two analog mixer boards and two Altera Stratix DSP development kits (EP1S80B956). A simplified block diagram of the set-up is

shown in Figure 4.7. A photo of the physical set-up is shown in Figure 4.8.

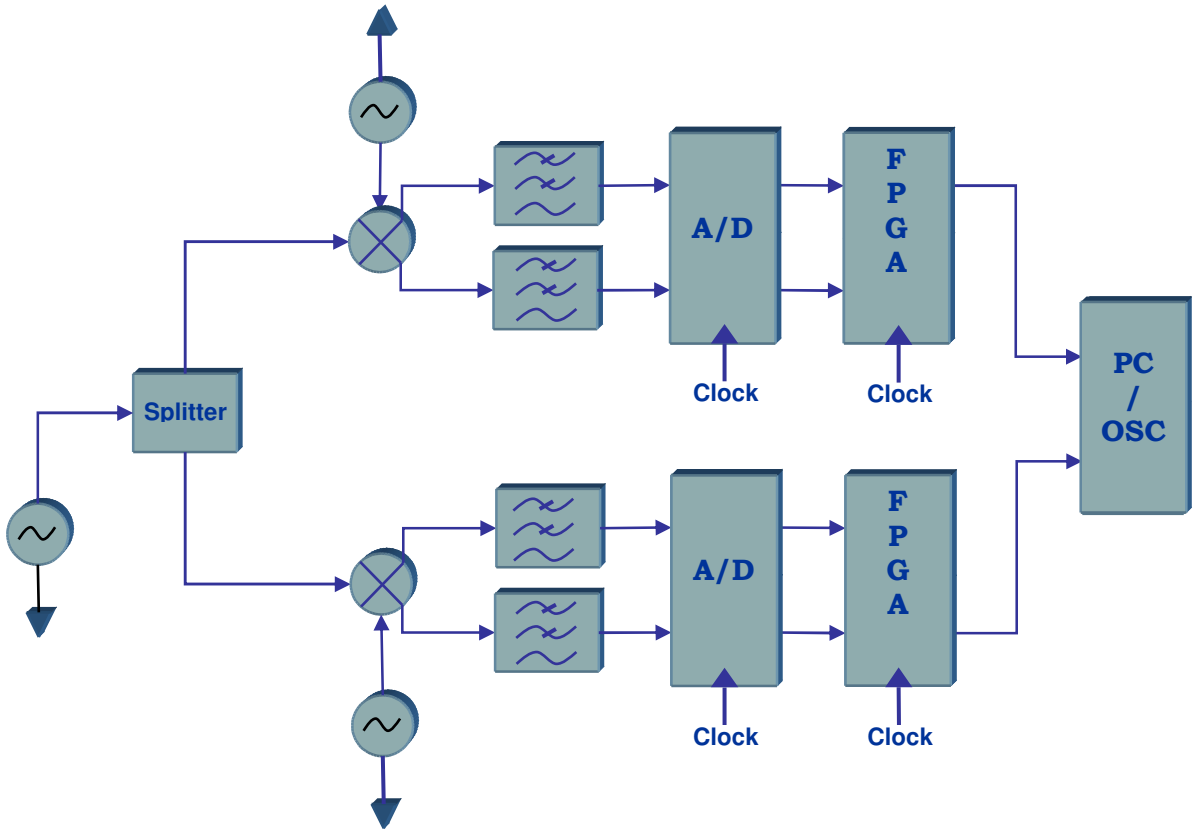


Figure 4.7: The board-level implementation set-up block diagram.

Two quadrature mixer boards (SRF1016-EVB) followed by four Minicircuits low-pass filters (SLP-21.4) with a cutoff frequency of 25 MHz constitute the analog part of the system. The analog input signal and the LOs are distributed into these mixer boards using a 0° splitter.

Each mixer board includes a double-balanced quadrature mixer with differential 50 Ω RF and LO inputs. Because of the frequency limitation of the existing matching circuits on the mixer boards, the input signal band of 200 to 300 MHz is chosen for the prototype system. (The mixer ICs are designed to operate in the 65 to 300 MHz band.) Note

that for this bandpass system, the analysis in Chapter 3 is valid except that an offset of 200 MHz should be added to all frequencies.

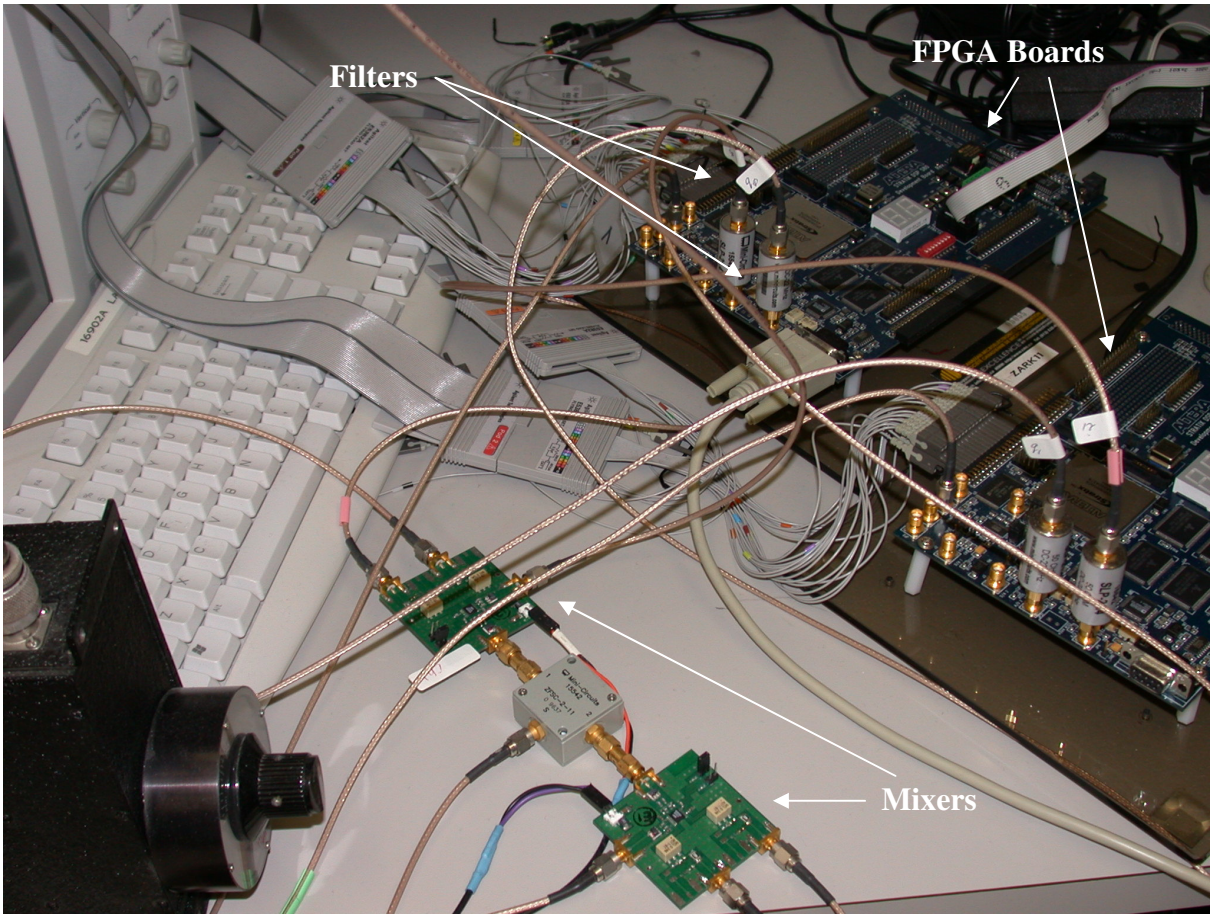


Figure 4.8: The board-level implementation set-up picture.

For the effective system bandwidth of 100 MHz, the LO frequencies Ω_0 and Ω_1 are calculated as 25 and 75 MHz, therefore, the mixer board LO signals are 225 and 275 MHz. These mixers translate input frequency components from 200 to 250 MHz (corresponding to Channel 0) and input frequency components from 250 to 300 MHz (corresponding to Channel 1), into two baseband channels with a low-pass filter bandwidth of 25 MHz.

Each Stratix FPGA board (DSP development kit), includes two 100/125 MHz AD9433 ADCs which are used as subband ADCs, as well as an FPGA that is used to realize

the digital reconstruction structure. The digital reconstruction structure includes all the stages as plotted in Figure 4.1, i.e., the digital mixers, the upsamplers, the digital reconstruction filters, the I/Q imbalance compensation filters and the digital summers. A 100 MHz clock is applied to the subband ADCs.

The analog mixers are set to a low-gain mode and low-swing signals are used at their input to reduce the nonlinearity effects in the mixers. It should be noted that the non-linearity of the mixer should not affect the required SNDR for the total ADC system.

Also, it should be noted that the analog input signal provided by the signal generator should also have a low noise level (good dynamic range), to accommodate the required SNDR for the total ADC system. For measurement purposes such as ENOB measurements on the ADCs, a pure single-tone Sine input is needed. Therefore, sharp filtering stages or precise signal generators are required for high-resolution measurements.

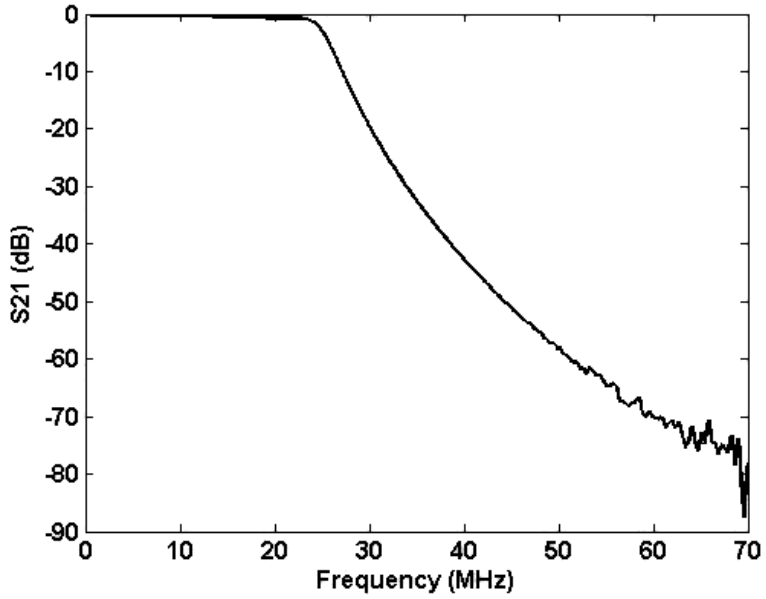


Figure 4.9: The frequency response of the measured analog low-pass filters.

With the limited input applied due to the limited dynamic range of the input signal generator and mixer nonlinearity, the SNDR of a single ADC path was measured to be 51.9 dB (equivalent to an ENOB of 8.3 bits for the resolution of one subband ADC). This will be used as the reference resolution for the subband ADCs when considering the resolution of the overall ADC system.

The analog low-pass filters are characterized using a vector network analyzer (VNA). Using the transfer function of the analog filters (S_{21} measurements), two 16-bit 64-tap FIR reconstruction filters are designed. The magnitude of the frequency response of the analog low-pass filters is shown in Figure 4.9.

The digital reconstruction filters designed for the FTH-ADC system using these filters are shown in Figure 4.10. Note that since 8 bits of resolution is targeted, a 64-tap FIR reconstruction filter should be sufficient, as discussed before. This will be further inspected in the reconstruction section. The output data of the system is captured using a real-time oscilloscope with a sampling frequency of 20 GS/s. The output spectrum is then analyzed using the FFT of the captured data.

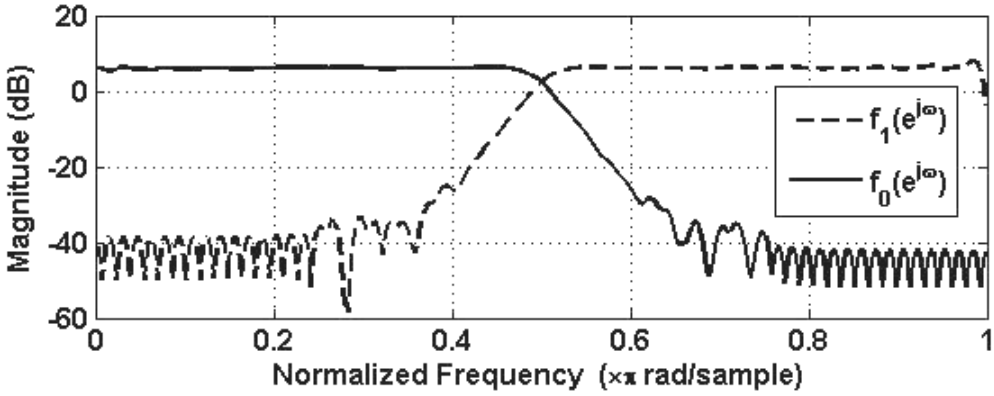


Figure 4.10: The frequency response of the designed digital reconstruction filters.

4.2.2 Analysis of the Mismatches

Spectrum analysis of the overall system output data reveals unwanted frequency components. As an example, the output spectrum for an input frequency of f_{in} = 261 MHz is shown in Figure 4.11 (a).

Six frequency components are distinguishable in this figure. Tone ① in this figure is the 261 MHz input tone that is translated into a 61 MHz tone in the output. As explained before, extra components due to amplitude and/or phase imbalance appear at $f_{in}\pm 2\Omega_{k.}$ Here, for Ω_0 = 25 and Ω_1 = 75 MHz, the 61±50 and 61±150 MHz frequencies are translated into 11 and 89 MHz (tones ② and ③ in Figure 4.11 (a)). Note that 89 = 200-(61+2×25) and 89 = -(61-2×75).

Amplitude mismatch of the two channels is a result of mismatch in the mixers, ADCs, and/or analog filters. The result of this error in here is a tone at 100-f_{in} (the system aliasing term due to undersampling), which is 39 MHz (tone ⑥ in Figure 4.11 (a)).

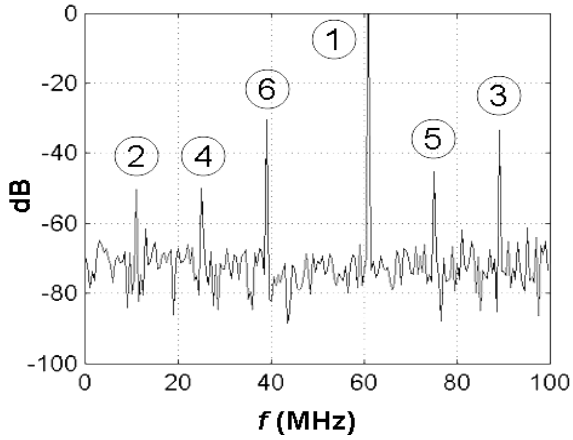
The two LO signal generators used in this application are phase-locked through their synchronization port. However, they have a phase offset that changes every time the system is turned on. This phase difference between the LOs of the two channels can be thought of as a phase mismatch between the channels and therefore is reflected in tone ⑥ of Figure 4.11 (a) as well. The last two undesired tones visible in Figure 4.11 (a) are the small tones ④ and ⑤, due to upconverted ADC dc-offsets, which appear at 25 and 75 MHz. Note that the mixers set up has been chosen such that they are sufficiently linear, by using their low-gain mode and applying a low input signal amplitude, i.e., the harmonic distortions of the mixers in the output spectrum are below the noise floor for the desired system resolution (which is targeted to be about 8 bits for this application).

4.2.3 Measurement of the Mismatches

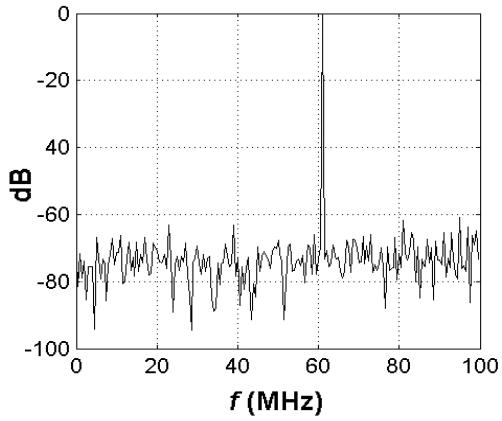
Mismatches to be measured are: I/Q phase and amplitude mismatch in each channel (path mismatch), amplitude mismatch of the two channels (channel mismatch), phase difference of the two LOs, and DC offsets of the ADCs output.

In order to measure the mismatches, the raw sampled data were processed according to the following steps:

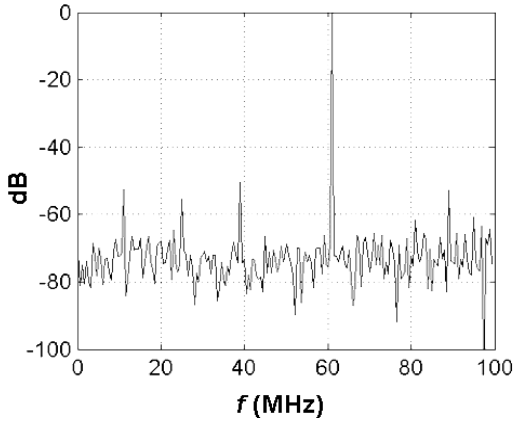
- Step (a): DC-offsets were measured and removed from the sampled data by digital subtraction after the subband ADCs.
- Step (b): The RMS of the data samples in the I/Q paths were used to measure the I/Q amplitude imbalance.
- Step (c): To measure the I/Q phase imbalance, as explained in Section 4.1.2, it suffices to multiply the sampled data by a digital sine with the same phase shift as the one it was already multiplied by in the analog domain. Therefore, sweeping the phase shift to minimize the amplitude of undesired tones (tones ② and ③ in Figure 4.11 (a)) in the output spectrum leads to the I/Q phase imbalance value.
- Step (d): The phase difference of the two LOs can be measured and removed by employing a similar technique as to Step (c) for measuring and removing the I/Q paths phase imbalance. Here, the phase shift is applied to both I and Q paths of one channel (e.g., Channel 0), while in Step (c), the phase shift is applied to one of the I and Q paths of each channel. Furthermore, in Step (c), the phase shift is limited by the mismatch specifications of the board (about -5° to 5°), whereas in this step, it is a uniform random variable in the range of -180° to 180°.



(a)



(b)



(c)

Figure 4.11: FFT of the measured output for an input frequency of 261 MHz

(a) before compensation (Section 4.2.2) (b) after compensation with codes (ideal compensation), and (c) after compensation with FIR implemented filters (Section 4.2.4).

- Step (e): For amplitude mismatch of the two channels, the RMS of the data in the two channels with inputs around the channels crosspoint (250 MHz) is used, as the power level of the signal in the different channels is not necessarily equal for other inputs. As the result of Steps (d) and (e), tone ⑥ in Figure 4.11 (a) is minimized.

Figure 4.12 depicts the compensated output results for a multi-tone input test. The input is comprised of two input frequencies, 221 MHz and 287 MHz, combined together using a power combiner. Note that the dynamic range of the input is smaller in this case compared to the single-tone test due to the limited dynamic range provided by the available filters and therefore the full resolution of the system is not available.

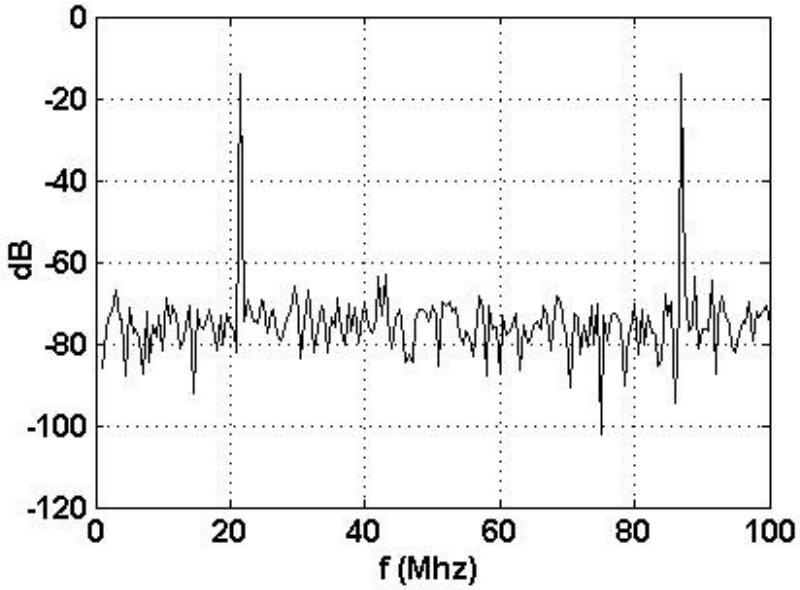


Figure 4.12: FFT of the compensated output for multi-tone input comprising of two frequency components.

Figure 4.13 shows the measured amplitude/phase mismatch values versus the input frequency for the implemented system. Note that due to the board components bandwidth limitations, measurements are only reported up to 291 MHz. The LO phase differences are not shown in this figure. Note that for each input frequency, the reported mismatch values are based on the measurements for the stronger channel, i.e., the channel where most of the input signal power is processed. Also, note that the reported values are based on

channel/path measurements, not the individual components (mixer, filter, etc) measurements. Most of the compensation parameters measured in the abovementioned steps are frequency dependent. However, in some of them, such as the DC offsets, the variations are small and can be ignored.

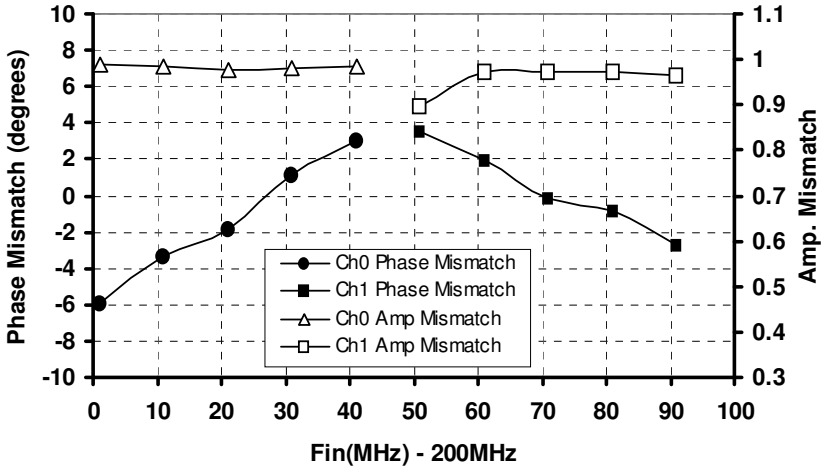


Figure 4.13: Measured amplitude/phase mismatch values for the implemented board based on the strong channel measurements.

4.2.4 Compensation of the Mismatches

ADC offset values are compensated by digital subtraction as the first block in the digital domain (not shown in Figure 4.1 for brevity). The total channel amplitude mismatch can also be accounted for in the design of the reconstruction filters. Next, in order to compensate for the I/Q phase and amplitude imbalance, two 10-tap linear-phase FIR filters are designed to implement the α_k and β_k values calculated using (4.11).

In the design of the FIR filters for the α_k and β_k vectors, it should be taken into account that these values are in fact intended to remove the corresponding image component

of each input frequency. Therefore, the vector values for each input should be mapped and implemented as the FIR filter response coefficient of the corresponding image frequency rather than the input frequency. For example, in this 2-channel system, the corresponding image for the input frequency of f_{in} = 261 MHz would be located at 11 MHz. So the calculated vector values for this input will be implemented at 0.22π (11 MHz sampled at a 100 MHz rate since these blocks are placed before the upsamplers).

Figure 4.11 (b) and Figure 4.11 (c) show the spectrum of the output after applying the compensation techniques to the system with 261 MHz input signal discussed in the previous section and shown in Figure 4.11 (a). In Figure 4.11 (b), the best attainable spectrum is shown by applying software codes for compensation ([54]). In Figure 4.11 (c), the output spectrum using 10- tap FIR compensation filters is shown.

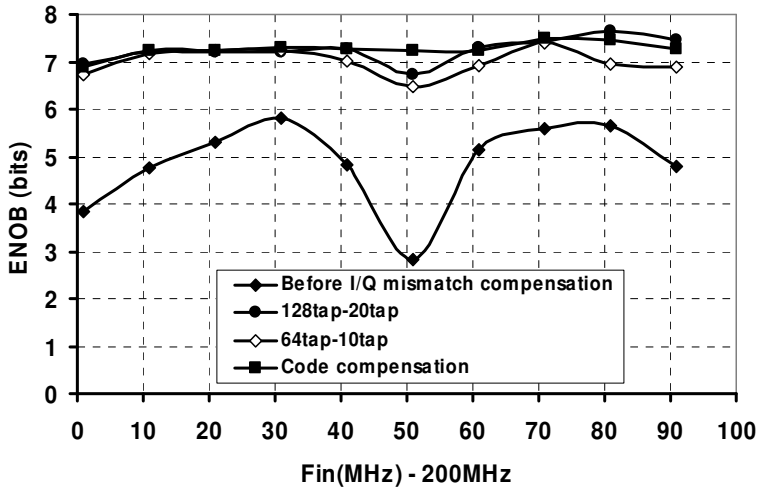


Figure 4.14: Measurement results for the total system ENOB before and after I/Q mismatch compensation.

Figure 4.14 depicts the ENOB values before and after compensating for the I/Q mismatches. In this figure, ENOB values are reported for a) before compensating for I/Q mismatches (all other mismatches are compensated), b) after software compensation, c) after applying 128-tap reconstruction filters and 20-tap compensation filters, d) after applying 64-tap reconstruction filters and 10-tap compensation filters. Note that 64-tap reconstruction filters are used for all the cases, except for the case c.

Figure 4.14 confirms that the 128/20 tap filters (128-tap reconstruction filters and 20-tap compensation filters) have only little advantage over the 64/10 tap filters as expected and discussed in Section 4.1.7. Therefore, to reduce the system complexity, 64/10 tap filters are chosen. As shown in Figure 4.14, an ENOB of more than 7 bits is achieved across the entire input band for the total system, using subband ADCs with path resolution of 8.3 bits.

In this 2-channel system, a total of six FIR filters (four 10-tap compensation filters and two 64-tap reconstruction filters) are used. To reduce the complexity and power consumption of the system, filter length and coefficient resolution of the digital filters are adjusted for the required resolution of the overall ADC system.

5 CIRCUIT-LEVEL IMPLEMENTATION OF THE FTH-ADC: A 4-BIT 4-GHz 52 mW MIXER-FILTER-ADC STAGE IN 90 nm CMOS.

Frequency-translating hybrid analog-to-digital converters (FTH-ADCs) were presented at system- and board-levels in Chapters 3 and 4, respectively. This chapter is devoted to the circuit-level implementation of the FTH-ADC in CMOS.

At the circuit-level, the linearity of the analog blocks should be sufficient to maintain the required signal-to-noise ratio (SNR) for the desired resolution of the overall ADC system. Besides, if used for wireless applications, circuits should be low-power. This calls for low-power, highly-linear, analog, mixer-filter blocks operating at multi-GHz speeds as well as subband ADC blocks with medium-to-high resolution operating at a fraction of the targeted system speed.

In this chapter, one path of a 2-channel, 4-bit, 8-GHz FTH-ADC system, with an analog bandwidth of 4 GHz, is designed and implemented in a 90 nm CMOS technology. This path consists of a highly-linear mixer-filter-ADC block that can operate at sampling rates of up to 4 GHz with an SNDR of at least 26 dB.

The block consists of a fully-differential, 5^{th}-order Butterworth G_m-C filter, with a cutoff frequency of 1 GHz, and a passive, highly-linear, double-balanced mixer operating at 4 GHz with at least 26 dB of linearity (to provide for the SNR required for 4-bit resolution

as shown in (2.1)). The filter design can be extended for externally tunable gain and cutoff frequency.

A fully-differential, flash ADC architecture with 4 bits of resolution operating at 4 GS/s is adopted for this path [57]. This ADC is implemented using current-mode logic (CML) blocks. Both digital and analog parts of the ADC circuit are fully-pipelined to enhance the speed. Therefore, the mixer-filter has a THD $\leq$ 5% (26 dB) over its full 1 GHz bandwidth and provides a signal with a voltage swing of 350 mV_{pp} for the subsequent ADC stage. It should be noted that a higher THD is in fact attainable for the mixer-filter stage as will be explained in the following sections. In fact, due to the limited resolution of the available ADC, the targeted system resolution is set to 4 bits.

The complete mixer-filter-ADC block (a single path of the FTH-ADC), is implemented in a CMOS 90 nm technology and consumes a total measured power of 52 mW from a 1.2 V supply and occupies an active area of 0.05 mm^2 (mixer: 11×13 μm^2, filter: 80×260 μm^2, ADC: 300×100 μm^2).

Note that the analog part of the 4-bit, 8-GHz FTH-ADC system would consist of four mixer-filter-ADC paths, together with a frequency synthesizer (The LO frequencies are multiples of each other). To put this into perspective, a reported 8-bit, 4-GHz, fully-CMOS time-interleaved ADC consumes a power of 4.6 W from a 3.3 V supply. This ADC is implemented in CMOS 0.35 μm technology and attains a minimum ENOB of more than 6 bits for input bandwidths around 1 GHz and around 5 bits for input bandwidths around 2 GHz [28].

5.1 The Mixer Block

Depending on the performance requirements, various mixer circuits can be chosen. Passive mixers typically achieve better speed and linearity as compared to the active mixers, however, the conversion gain of passive mixers is less than unity. By virtue of their gain, active mixers perform better in terms of noise [58].

Also, mixers can be implemented as single-balanced or double-balanced. Double-balanced structures are fully-differential both in LO and RF inputs and therefore generate less even-order distortions. Besides, these structures are less susceptible to LO noise [58].

5.1.1 The Structure

Since a highly-linear mixer is desired, a double-balanced passive mixer structure is chosen and the overall conversion gain (which is less than one for the passive mixer) will be compensated by the filter gain. Implementing a linear mixer in 90 nm CMOS technology is challenging since a supply of 1 V is available and therefore the maximum allowed swing on the input signals is small. This will be further discussed in the following subsection.

The passive mixer, as shown in Figure 5.1, includes four cross-coupled PMOS transistors, M'_1-M'_4, operating in the triode region [49], [59]. The cross-coupled double-balanced structure ensures that the even-order non-linear components in the transistor voltage-to-current characteristics almost cancel out through symmetry and the output voltage is the multiplication of the two input signals, V_{RF} and V_{LO} [49], [59], given as:

$$V_{out}^{+} - V_{out}^{-} = K(V_{RF}^{+} - V_{RF}^{-})(V_{LO}^{+} - V_{LO}^{-}) \tag{5.1}$$

where $K = \mu_n C_{ox} \frac{W}{L}(R_{in})$ and R_{in} is the input impedance of the following filter stage. In case of mismatch between the input transistors, an extra quadratic term will appear in the output as [59]:

$$V_{out}^{+} - V_{out}^{-} = K(V_{RF}^{+} - V_{RF}^{-})(V_{LO}^{+} - V_{LO}^{-}) + \Delta K(V_{LO}^{+} - V_{LO}^{-})^2. \quad (5.2)$$

This extra term of V_{LO} is composed of a high-frequency component and a baseband component that can be removed by the following digital stages of the ADC structure. This explains why an RF signal applied to the gates is preferred, in contrast to [49]. Note that if the RF signal is applied to the drain, removing the resulting signal-dependent high-frequency component is much harder at the digital stage.

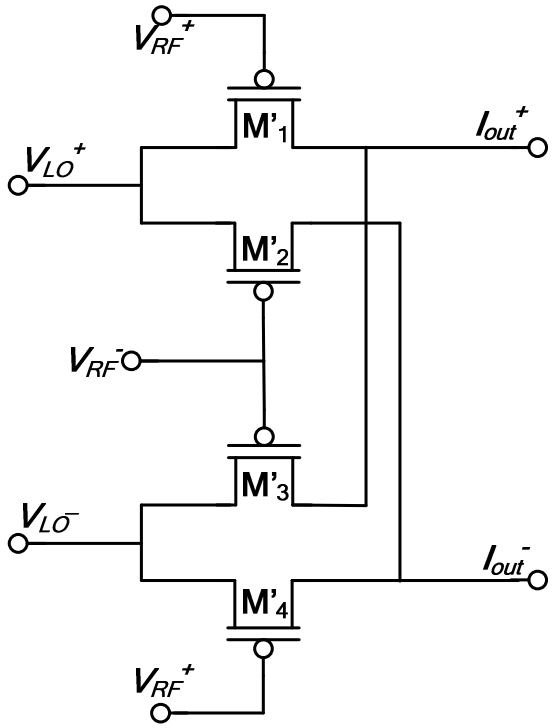


Figure 5.1: The cross-coupled double balanced mixer stage.

In fact, removing a known frequency component (multiples of the LO frequencies), is possible through notch filtering stages. This is while removing unknown, input-dependent multiple RF frequency components is harder and costly.

5.1.2 DC-Biasing and Maximum Swings

To avoid distortion, the dc-biasing and maximum allowed signal swings should be chosen such that all four transistors are kept in triode region at all times [59]. This means that the minimum drain voltage $(V_{LO,DC} - V_{LO,AC}/2)$ should be larger than the maximum gate voltage $(V_{RF,AC}/2 + V_{RF,DC})$ by at least one transistor threshold voltage (V_T). Therefore, the biasing points are chosen as: $V_{LO,DC}$ = 850 mV, and $V_{RF,DC}$ = 150 mV. The signal swings of $V_{LO,AC}$ = 300 mV_{pp}, and $V_{RF,AC}$ = 300 mV_{pp} can therefore be used. This results in a mixer output swing of 70 mV_{pp}. Note that in this chapter, all reported voltage values are single-ended peak-to-peak values.

5.1.2.1 Mixer linearity

The IIP3 or the third intercept point is a measure of linearity. It is defined as the input signal level for which the power of the third-order intermodulation products becomes equal to the desired input signal power [58]. The 1-dB compression point is the input signal level for which the output level drops by 1 dB below the ideal output level as predicted by the small signal gain.

Simulations are performed on the mixer for linearity tests around 2.4 GHz. An IIP3 of 17.5 dBm and a 1-dB compression point of 10.7 dBm are achieved as shown in Figure 5.2 and Figure 5.3, respectively. Note that for 4-bit resolution, the intermodulation terms should always be at least 26 dB below the output signal level.

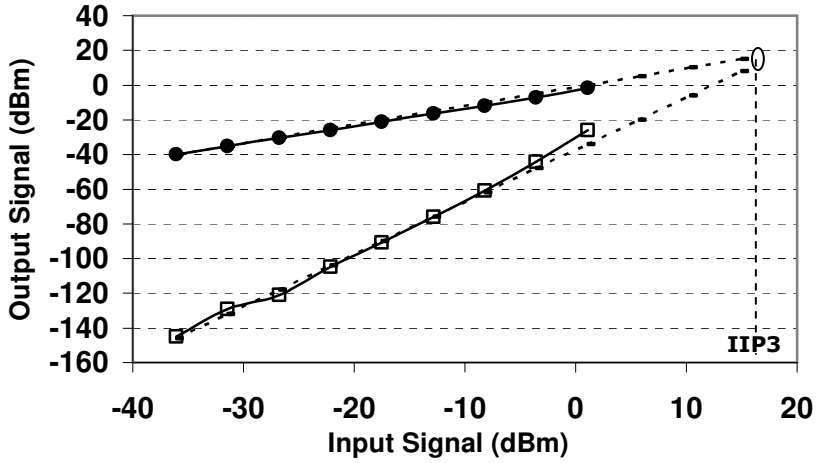


Figure 5.2: Mixer IIP3.

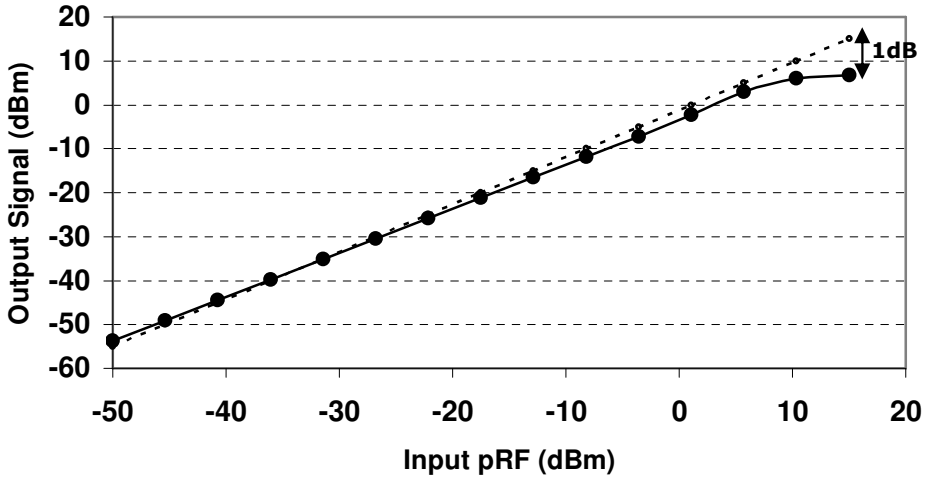


Figure 5.3: Mixer 1-dB compression point.

5.2 The Filter Block

There are various ways to implement an integrated high-frequency continuous-time analog filter. In one approach, the transfer function of the filter can be implemented as a

cascade of first-order and second-order (biquad) stages. Each stage implements a pole or a pair of poles (and a pair of zeros, if desired).

The second approach is to use a passive or active implementation of the LC-ladder structure, e.g., by replacing inductors with equivalent "gyrators" or other active inductor elements [60]-[62]. While the second method can result in less sensitivity of the filter frequency response to individual element values, the first method is chosen in here for its simplicity and flexibility [60].

In terms of circuit design, several techniques can also be used to implement an active continuous-time filter. Two most recently used approaches include the transconductor-based and the op-amp-based implementation [60], [63]. Since the filter is supposed to be highly-linear and operate at high frequencies, an active transconductor-based G_m-C filter is chosen. G_m-C filters are preferred to op-amp-based filters because of the limited bandwidth of op-amps. To control finite-gain transfer function deviations, op-amps with sufficient loop gain at multi-GHz frequency range are required, which are very challenging to design [63].

In the design of the transconductor-based filters, care should be taken to linearize the transconductor over the expected input signal swing to avoid detuning and distortion in filter's frequency response [22], [60], [64] and to provide for the desired linearity of the filter.

5.2.1 The Transconductor

5.2.1.1 The structure

The basic transconductor block used in this filter is shown in Figure 5.4. As can be seen in this figure, the transconductor includes a main differential pair, M_1-M_2, together with

two sets of current-source loads. The first set include M_5-M_6, controlled by dc biasing and the second set include M_7-M_8, controlled by the common-mode feedback circuit (CMFB). The latter transistor pair is much smaller in size and is used as a slight control tap for CMFB circuit and avoids abrupt changes caused by the CMFB.

The CMFB circuit used for this filter is a single-ended op-amp as shown in Figure 5.4. This circuitry includes M_{11}-M_{15} and the resistive sensing network. The output of the transconductor is sampled by resistive sensing through resistors R_1=R_2=R, and is compared with a common-mode reference voltage, V_{ref}, that is set to be 700 mV. The resulting feedback will then adjust the CMFB bias voltage of M_7-M_8 that adjusts the bias current of the transconductor. As a result, the DC voltage of the output is adjusted around V_{ref}.

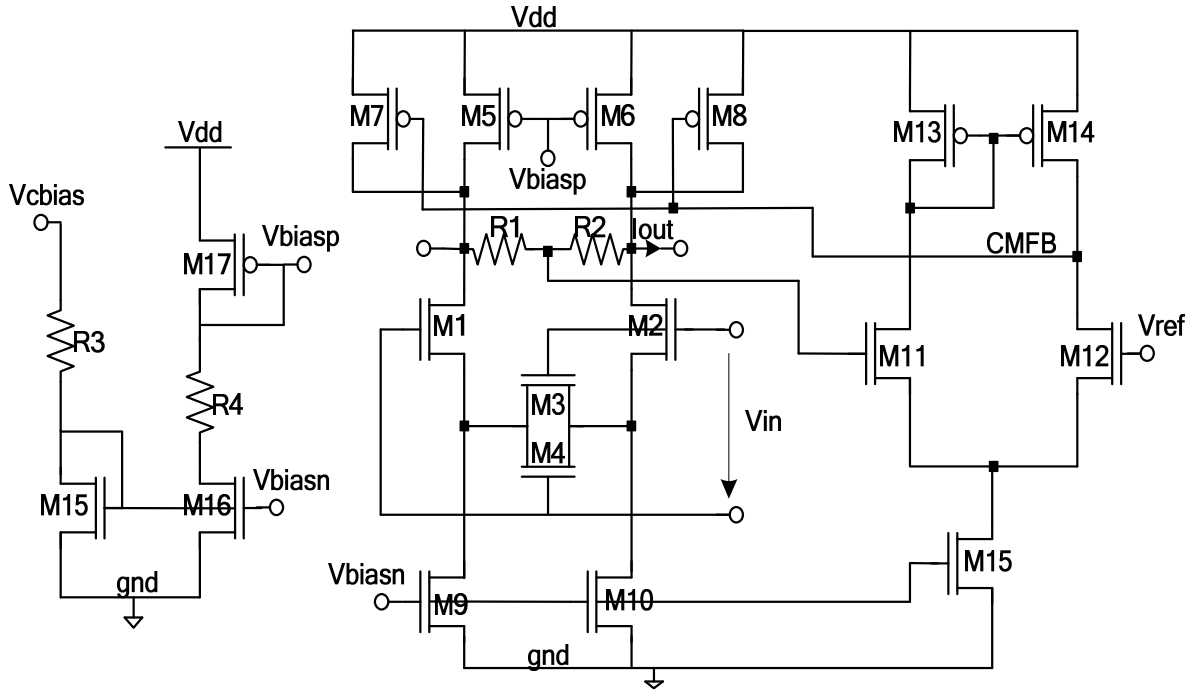


Figure 5.4: The basic transconductor block including the common-mode feedback (CMFB), and the biasing circuitry, including the external bias control voltage, *Vcbias*.

The bias current of the transconductor and therefore the value of its output current, i_{out} and transconductance, g_m, can be adjusted by changing the source bias current of the transconductor block through M_5-M_6 (*Vbiasp*) and M_9-M_{10} (*Vbiasn*). These two biasing voltages are both adjusted by an external bias control voltage (*Vcbias*) as shown in Figure 5.4. This will be further discussed in Section 5.2.1.3.

5.2.1.2 Transconductor Linearity

In order to increase the linearity of g_m over the input voltage swing, a pair of transistors, M_3-M_4, is used in the triode region across the differential input such that the gates of M_3 and M_4 are connected to the gates of the input transistors M_1 and M_2, respectively [64]. This transistor pair is also shown in Figure 5.4.

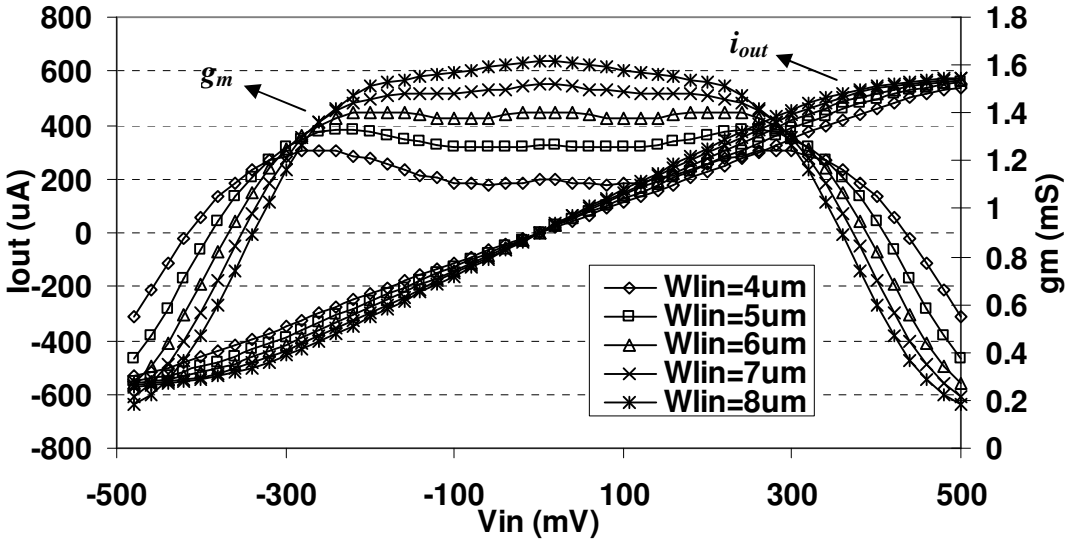


Figure 5.5: The output current and the transconductance versus the input signal swing for various *Wlin* values (*Llin* = 0.2 μm).

As explained in [22], the linearity of this transconductor is proportional to the biasing current and can be tuned by changing it. In fact, the transistor pair M_3-M_4 act like two source degeneration resistors for the differential pair M_1-M_2. Therefore, the linearity is improved.

Hence, by changing the sizing of M_3-M_4, the linearity can be adjusted. Figure 5.5 illustrates the variations of the output current, i_{out}, and the transconductance, $g_m = \partial i_{out} / \partial V_{in}$, as a function of the input voltage V_{in}, for various widths of the M_3-M_4 transistors (*Wlin*). (*Llin* = 0.2 μm). Based on this figure, the best linear case is for $W_{lin} = 6\ \mu m$ where an almost horizontal line is achieved for g_m over an input swing of about 350 mV_{pp}.

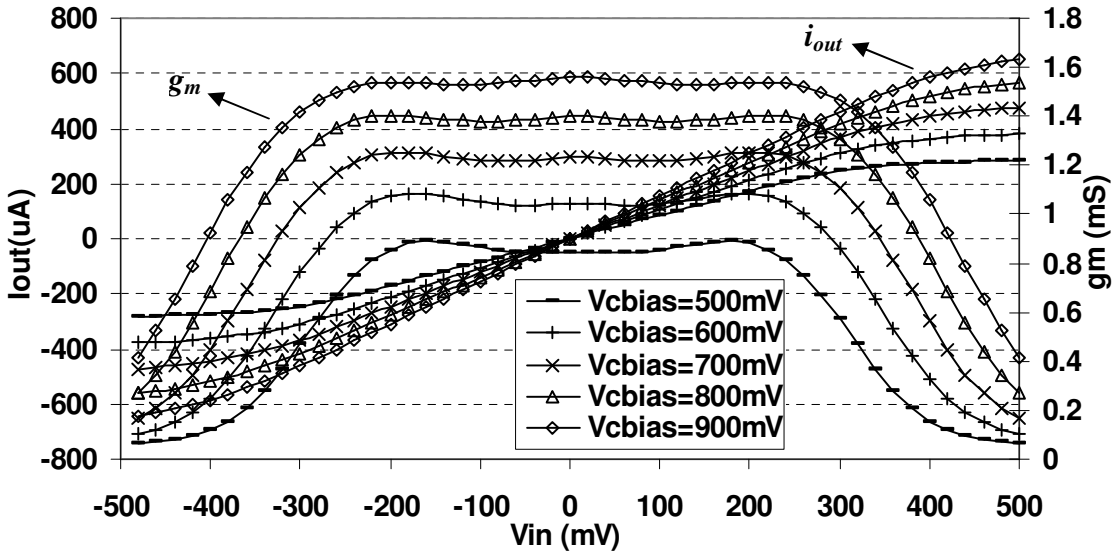


Figure 5.6: The output current and the transconductance versus the input signal swing for various dc biasing voltages of a single transconductor stage.

5.2.1.3 Tuning the Transconductance

As explained before, an external bias control voltage (*Vcbias*), can adjust the bias currents of the transconductor and therefore the value of its transconductance. Figure 5.6 shows how g_m and i_{out} of a single transconductor can be adjusted by changing the DC bias control voltage (*Vcbias*).

5.2.2 The Filter

5.2.2.1 The structure

The normalized 5th-order Butterworth low-pass filter transfer function can be written as [65]:

$$H(s) = \frac{1}{(s+1)(s^2+0.61s+1)(s^2+1.61s+1)} \tag{5.3}$$

This transfer function can be implemented as a cascade of one first-order stage and two second-order stages (biquads), respectively, as shown in Figure 5.7. Each row in this figure represents one stage of the filter. Note that each stage is composed of differential transconductor blocks that were discussed earlier. For this section, ignore the parallel blocks denoted as <1:n> and consider all transconductors as single stage.

The transfer function for the first-order system, (the first row in Figure 5.7), can be written as:

$$H_1(s) = \frac{g'_{m1}}{\frac{C'_1 s}{2} + g'_{m2}} \tag{5.4}$$

The cutoff frequency of this filter is:

$$\omega_{c1} = \frac{2g'_{m2}}{C'_1} \tag{5.5}$$

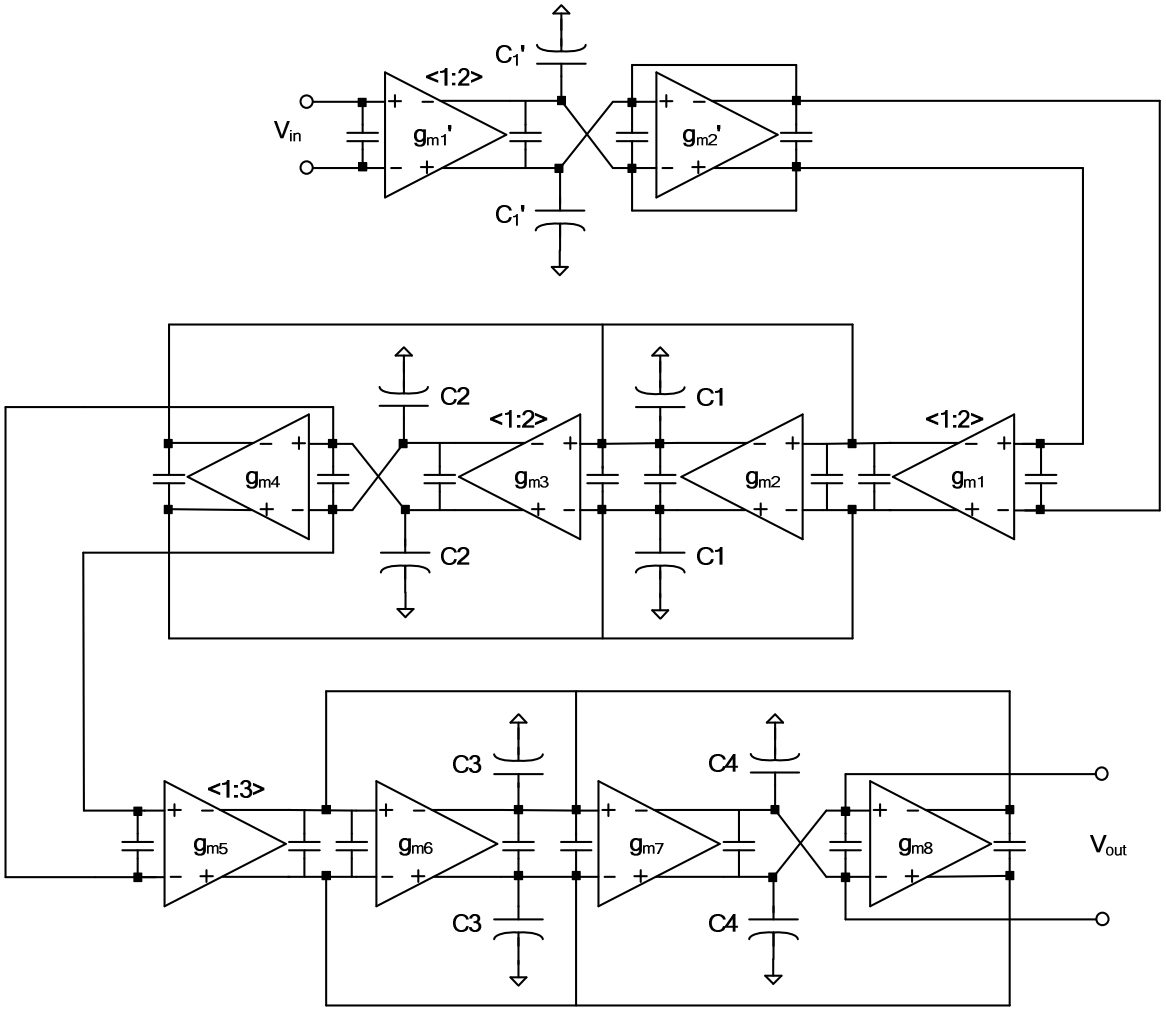


Figure 5.7: The overall 5th-order Butterworth filter structure, including one first-order and two second-order stages

Each second-order filter (the second and third rows in Figure 5.7) has a transfer function of the form:

$$H_2(s) = \frac{g_{m1} \cdot g_{m3}}{\frac{C_1 C_2}{4} s^2 + \frac{g_{m2} C_2}{2} s + g_{m4} \cdot g_{m3}} \tag{5.6}$$

The cutoff frequency of such second-order (biquad) filter is:

$$\omega_{c2} = \sqrt{\frac{4 g_{m3} g_{m4}}{C_1 C_2}} \tag{5.7}$$

To implement the 5th-order Butterworth transfer function using the above-mentioned transconductor stages, the transconductance of each stage, g_m, should be chosen carefully. If g_m is selected too high, then it will be more difficult to design the stage and it will consume more power. If g_m is chosen too low, then the capacitances will have to be small as the cutoff frequency is a function of g_m/C. This will make the capacitor sizes comparable to the parasitic capacitances and therefore the effects of the process variations will be more pronounced.

Note that the equivalent capacitances include the input/output capacitances of the transconductors as well as the other parasitic capacitors (parasitic capacitances are shown in Figure 5.7 with no labels) and therefore have a minimum non-zero value. Hence, these capacitors should be accounted for in calculating the targeted frequency response [66].

5.2.2.2 The Design

Assuming a constant $g_m = 0.5\ m\Omega^{-1}$ for all of the transconductances, the required capacitors to realize the transfer function in (5.3), with a cutoff frequency of 1 GHz are calculated to be as follows: C'_1 = 160 fF, C_1 = 101 fF, C_2 = 256 fF, C_3 = 265.3 fF and C_4 = 95.5 fF.

A major goal in this design is to provide the desired linearity to provide the sufficient SNDR for a 4-bit, 4-GS/s subchannel ADC with an input swing of 350 mV_{pp}. Since a passive linear structure is used at the mixer stage, the filter stage is designed to have a gain of 5. This means that while the maximum input signal swing of the filter is only 70 mV_{pp} (the maximum output signal swing of the mixer), the output stage of the filter should be able to accommodate for the required 350 mV_{pp} output swing and therefore the last transconductance stages of the filter should operate linearly for this range of input swing as shown in Figure 5.5.

5.2.2.3 Gain and Bandwidth Adjustability

As can be seen from equations (5.4) to (5.7), the first transconductance of each first- and second-order stage, i.e., g'_{m1}, g_{m1} and g_{m5}, can be used to adjust the DC gain without changing the cutoff frequency. In a similar way, the third transconductance of each second-order stage, i.e., g_{m3}, g'_{m2} and g_{m7}, can be used to adjust the cut-off frequency without changing the DC gain.

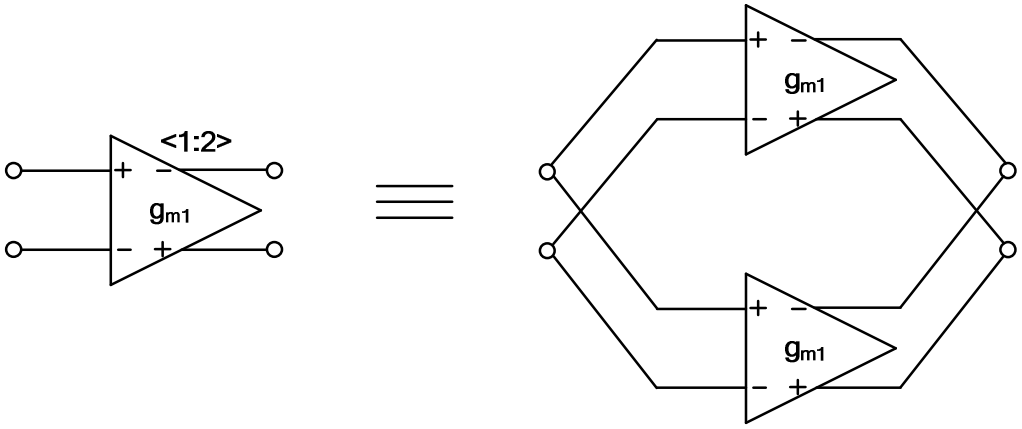


Figure 5.8: Parallel connection of two unit transconductors.

For simplicity and symmetry of the design and layout and to avoid redesign of the transconductor block, multiple stages of g_m are used in parallel for the first transconductance of each first- and second-order stage and the third transconductance of the first biquad stage in order to increase their equivalent transconductance.

Parallel transconductors are also used in [66] and it is shown that the transconductance is increased linearly by increasing the number of the parallel transconductors. Figure 5.8 shows the parallel connection of two identical transconductors and its equivalent notation. Note that in <1:n>, n shows the number of parallel transconductors in the block.

The number of parallel transconductors for each stage is also shown in Figure 5.7. The bias currents of the first transconductor of each stage (gain tuning transconductor) are different from the bias currents of the rest of the transconductors to provide independent tunability for the gain stage without affecting the bandwidth of the filter. For this purpose, the control DC bias voltage of the gain tuning transconductors, *Vcbias* is connected to an external voltage source, *Vg,* whereas the control DC bias voltage of the rest of the transconductors of the filter are connected to another external voltage source, *Vgb*.

The external DC sources, *Vg* and *Vgb,* can therefore be used to adjust the gain and cutoff frequency of the filter. Figure 5.9 depicts the frequency response of the filter for different values of *Vg*. Note that the cutoff frequency is kept constant while the DC gain is adjusted by changing *Vg*. Figure 5.10 illustrates the tunability of the filter cutoff frequency and gain for different values of *Vgb*.

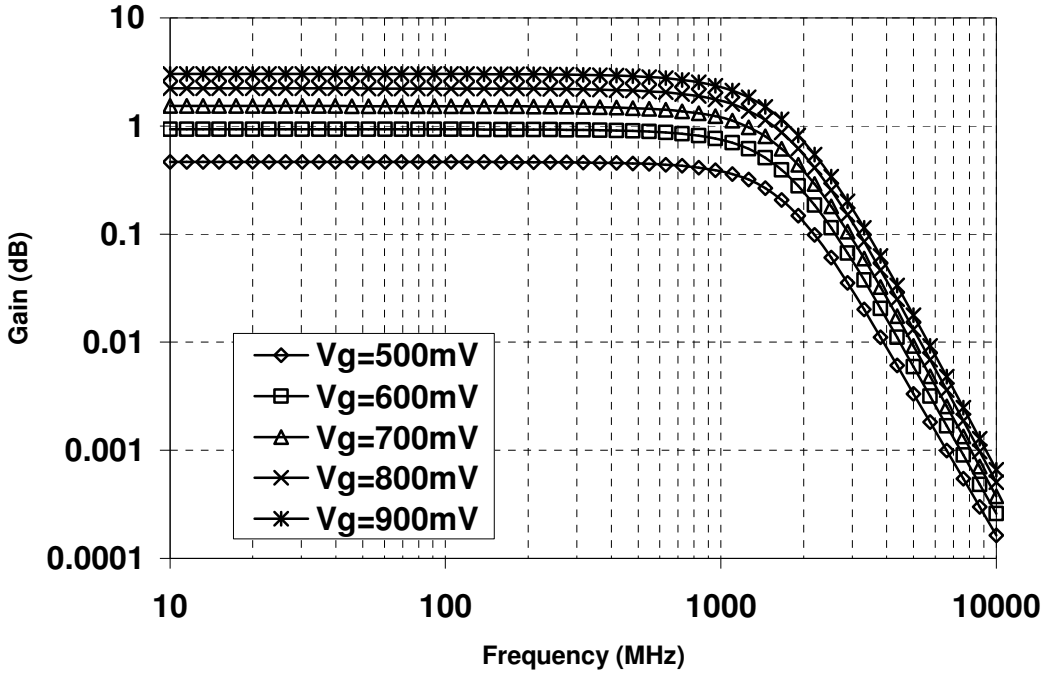


Figure 5.9: Frequency response of the filter with varying bias voltage (*Vg*) to adjust dc-gain without affecting the cut-off frequency (*Vgb* = 800 mV).

This design can further be extended for gain and cutoff frequency programmability, similar to [66]. For this purpose, a digitally programmable DC biasing source can be used to control the external voltages as well as to turn various parallel transconductor cells on/off.

Note that a separate DC bias could also be used for changing the third transconductance of each second-order stage, i.e., g_{m3}, g'_{m2} and g_{m7}, in order to adjust the bandwidth while keeping a constant gain. However, due to the limited number of pins of the on-chip test probe station, this option is not pursued in this design.

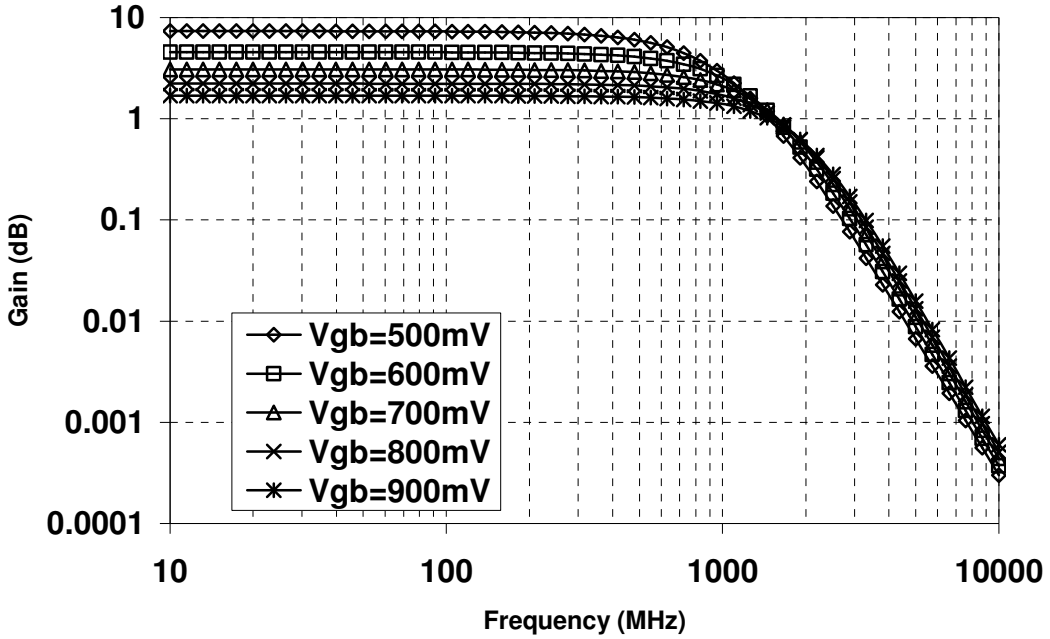


Figure 5.10: Frequency response of the filter with varying bias voltages (*Vgb*) to adjust dc gain and cut-off frequency (*Vg* = 800 mV).

5.3 The Mixer-Filter Block

The mixer-filter block should provide the dynamic range and output swing required for the following ADC stage, i.e., at least 5% (26 dB) of total harmonic distortion (THD) and 350 mV_{pp} over the entire 1 GHz sub-channel bandwidth for a 4-bit ADC. Simulation results for the THD versus the output voltage swing of the mixer-filter block for an IF typical test frequency of 333 MHz and *Vg* = 800 mV and *Vgb* = 800 mV (DC gain of 5), is plotted in Figure 5.11.

As can be seen from this figure, a THD of less than 3% is achieved for an output swing of more than 450 mVpp, which are better than the required performance. A margin is

considered to accommodate for the unaccounted device noise and distortion components that are not considered in the THD calculations.

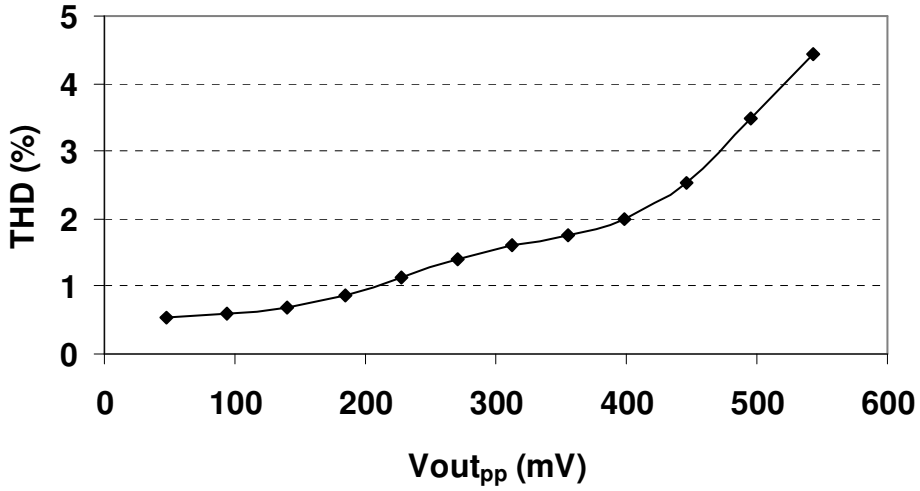


Figure 5.11: The total harmonic distortion of the output spectrum versus the output signal swing for a typical point, f_{IF} = 333 MHz and $Vg = Vgb$ = 800 mV (dc-gain of 5).

5.4 Measurement Results

5.4.1 The Layout

The chip micrograph is shown in Figure 5.12. The layout includes the mixer-filter-ADC stage, a mixer-filter stage and some other test circuits. The filter is composed of an array of 15 transconductors and 10 capacitors; and the mixer is composed of a symmetric structure of four cross-coupled transistors. The capacitors are chosen as metal-insulator-metal (MIM) type for their moderate density (capacitance per area) and high Q-factors [67]. Note that the value of these capacitors have a direct effect on the transfer function of the filter.

In the flash ADC design, a common-centroid layout is used for all transistors and resistors in pair and the resistor ladder. Using the common-centroid layout technique as well as a two-stage resistor averaging network in the ADC, the effect of mismatches are reduced and the need for digital calibration is obviated [57].

High-speed input signals, including the RF and LO and ADC clock signals are terminated with on-chip 50 Ω resistors. All high-speed I/O signals are routed such that the lengths of the differential paths match. The body of all NMOS and PMOS transistors are connected to ground and DC power-supply, respectively. Voltage-to-current converter buffers are used at the outputs of the ADC to drive the 50 Ω input resistance of the high-speed measurement device.

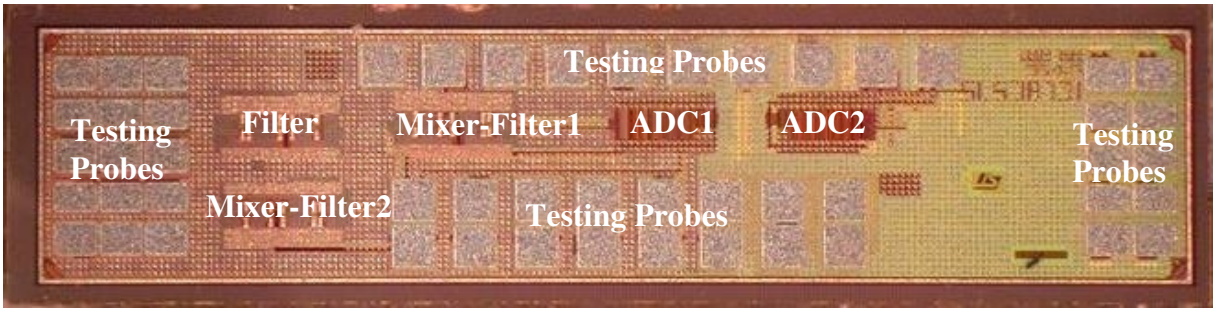


Figure 5.12: The chip micrograph.

The complete mixer-filter-ADC block (a single path of the FTH-ADC), is implemented in a 90 nm CMOS technology and consumes a total measured power of 52 mW from a 1.2 V supply with an active area of 0.05 mm^2 (mixer: 11×13 μm^2, filter: 80×260 μm^2, ADC: 300×100 μm^2).

The reason for choosing the high power supply of 1.2 V in 90 nm CMOS technology is to increase the signal swing and therefore enhance the linearity and noise performance of

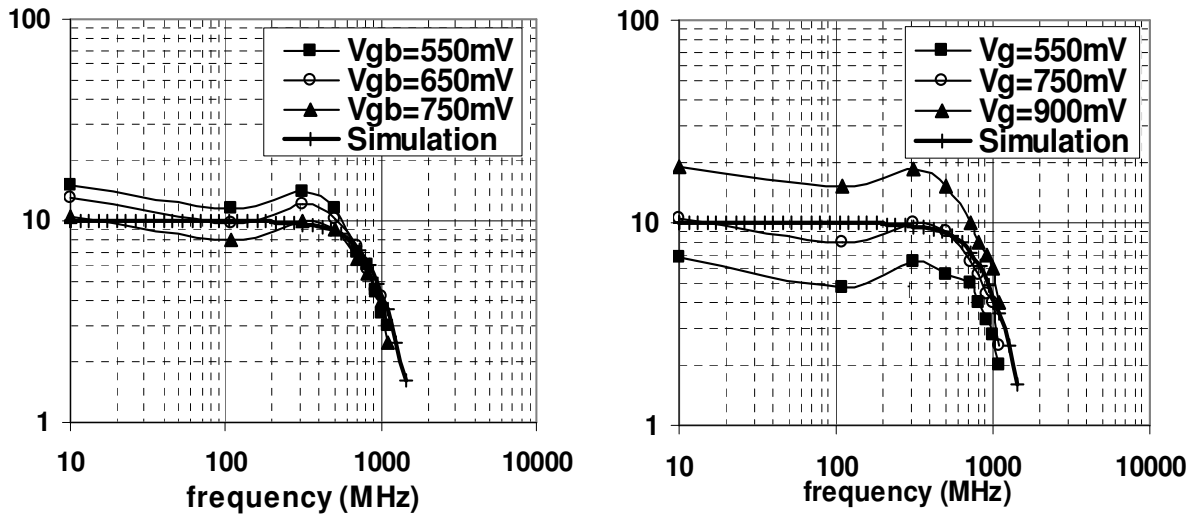
the circuits. The chip is laid out for on-chip testing and different configurations of on-chip probes are used for various test scenarios, as can be seen in the figure. The total area of the chip including the pads is 1.5 mm^2.

5.4.2 Mixer-Filter Measurements

In addition to the complete mixer-filter-ADC stage, a separate mixer-filter block is also implemented on the same chip for characterization of the analog part. At the output stage of the mixer-filter circuit, an extra transconductor is used to act as a buffer in order to drive the 50 Ω input resistance of the oscilloscope. However, the 50 Ω loading at the output still reduces the output signal amplitude and therefore measurements on these pins are limited.

The mixer-filter circuit was tested using two 180° splitters to provide for the differential RF and LO inputs of the double-balanced mixer and four bias-Tees to provide the common mode of the input RF and LO signals. Due to the splitter bandwidth limitations, a test frequency of f_{LO} = 1.3 GHz was chosen. As for the differential outputs measurement, a 180° power combiner can be used or one output can be terminated by a 50 Ω termination while the other one is measured.

Figure 5.13 depicts the tunability of the gain and cutoff frequency of the mixer-filter with the dc-bias controls. As shown in Figure 5.13 (a), the gain and bandwidth of the mixer-filter can be tuned by tuning the external biasing control voltage, *Vgb* and as shown in Figure 5.13 (b), the gain of the mixer-filter can be adjusted while keeping the cutoff frequency constant by tuning the external biasing control voltage, *Vg*.



(a) (b)

Figure 5.13: Frequency response tunability measurement results of the mixer-filter with (a) Vg = 750 mV and (b) Vgb = 650 mV, with f_{LO} = 1.3 GHz.

As explained before, due to lack of 50 Ω matching at the output of the mixer-filter stage, the amplitude of the output is measured smaller than its actual value. Therefore, these plots should not be compared numerically to the simulation results.

To test for the linearity of the mixer-filter, THD calculations were done on the output spectrum measurements of the mixer-filter for f_{LO} = 1.3 GHz with inputs of f_{IF} = 10 MHz and f_{IF} = 333 MHz ($f_{IF} = \left| f_{RF} - f_{LO} \right|$). For this purpose, a real-time oscilloscope with a sampling frequency of 20 GS/s was used to capture the output measured data. The THD was then calculated on the FFT of this captured data. In this test, the dc-bias control voltages for the filter stage were chosen as: Vg = 750 mV, Vgb = 650 mV.

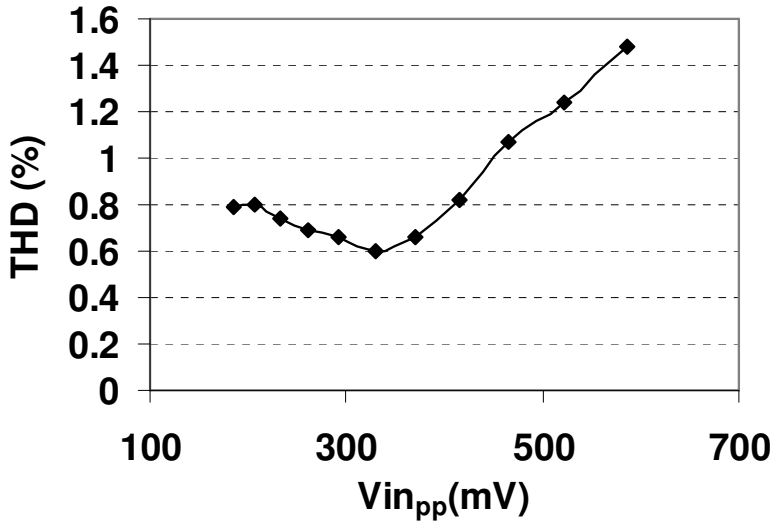


Figure 5.14: The mixer-filter output THD vs. input signal swing measurement results for f_{LO} = 1.3 GHz, *Vg* = 750 mV, *Vgb* = 650 mV and f_{IF} = 10 MHz.

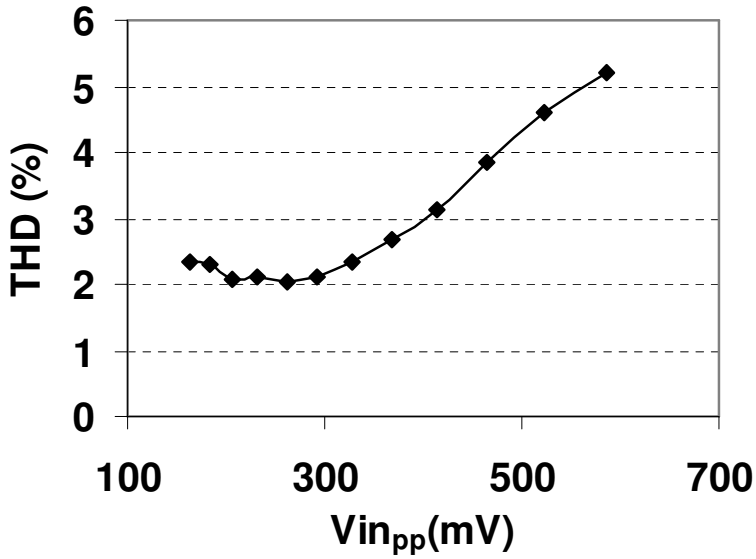


Figure 5.15: The mixer-filter output THD vs. input signal swing measurement results for f_{LO} = 1.3 GHz, *Vg* = 750 mV, *Vgb* = 650 mV, f_{IF} = 333 MHz.

Figure 5.14 and Figure 5.15 depict the output THD (%) versus the input signal swing for IF output frequencies of f_{IF} = 10 MHz and f_{IF} = 333 MHz, respectively. As can be seen in these figures, an output spectrum with less than 1.5% of THD is attainable in the low-frequency range with an input swing of up to 580 mV_{pp} and an output spectrum with less than 3% of THD is attainable in the higher frequency range with an input swing of up to 420 mV_{pp}.

These measurement results confirm the performance requirements on the mixer-filter stage for at least 4-bit operation. It should be noted that for low input voltages, the measured output is very small (since it is not matched) and therefore the measured THD is not linearly increased.

5.4.3 Mixer-Filter-ADC Measurements

A similar test set-up to the one used for the mixer-filter measurements was used to measure the performance of the mixer-filter-ADC path. The ENOB and spurious-free dynamic-range (SFDR) of the mixer-filter-ADC output were measured over the 1 GHz IF bandwidth using f_{LO} = 1.3 GHz. A digital square clock frequency of f_{clk} = 4 GHz with 1 V_{pp} voltage swing was applied to the ADC. The SFDR indicates a measure of the largest unwanted signal component present in the output spectrum.

The measurement results for ENOB and SFDR of the mixer-filter-ADC path are shown in Figure 5.17. Due to an offset error at the output of the mixer-filter block, achieving a full dynamic-range swing at the input of the ADC was not possible for higher frequencies and even increasing the mixer-filter-ADC path gain would lead to signal clipping on one side that was evident as saturation to the lowest code at the output of the ADC.

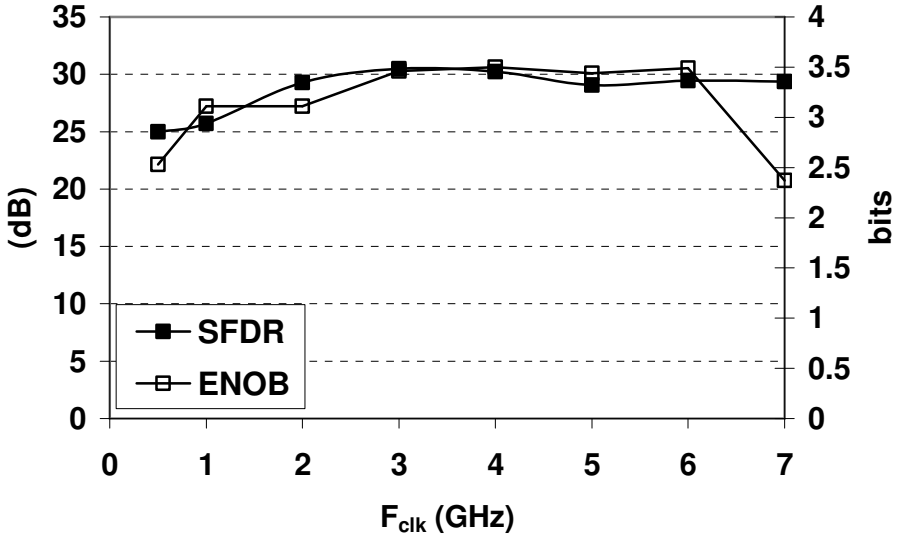


Figure 5.16: ENOB and SFDR for constant input frequency of f_{IF} = 10 MHz versus the ADC clock frequency (f_{RF} = 1.31 GHz, f_{LO} = 1.3 GHz).

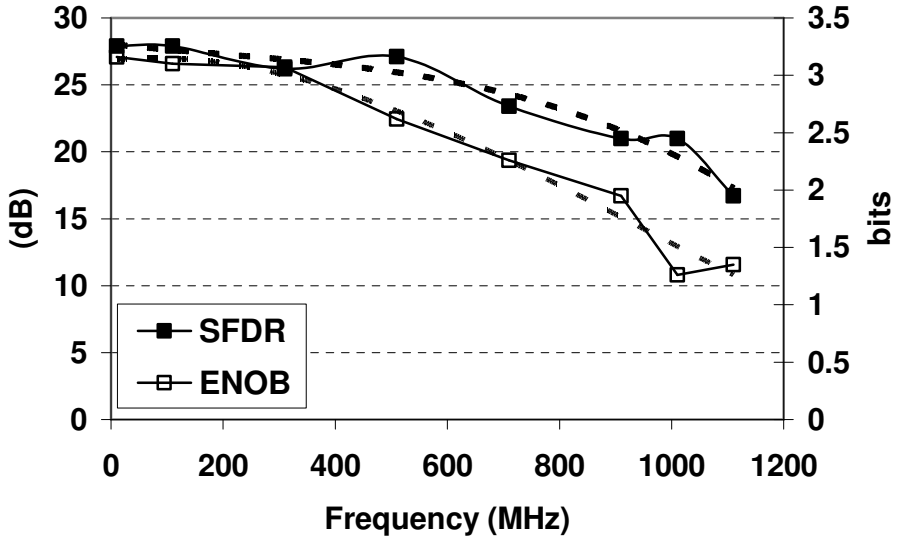


Figure 5.17: ENOB and SFDR for ADC clock frequency of f_{cl} = 4 GHz versus the f_{IF} across the 1 GHz bandwidth.

Therefore, the total measured ENOB for these frequencies drops faster than expected. Note that the ENOB and SFDR are expected to drop corresponding to the 5^{th}-order Butterworth filter frequency characteristic around 1 GHz.

The offset error at the output of the mixer-filter is partly due to generating the reference voltages of the flash ADC on-chip. If external pins could be used to tune these reference voltages, better resolution and less offset would be achieved. However, this was not an option in this case due to lack of extra external pins. A buffer could also be used to drive the input capacitance of the ADC and DC level-shifting.

The ENOB and SFDR at fIF = 10 MHz were also tested for higher ADC clock frequencies for the mixer-filter-ADC path as shown in Figure 5.16. It can be seen that the mixer-filter-ADC can operate with an ENOB of about 4 bits at clock speeds of up to 6 GHz.

6 SUMMARY, CONCLUSION, AND FUTURE WORK

6.1 Summary and Conclusion

Many emerging applications call for wideband ADCs operating at GHz speeds with low power and cost. Realizing such ADCs with single-stage architectures such as flash and sigma-delta architectures is very challenging with the existing CMOS technologies, in particular if medium-to-high resolution is desired. Therefore, parallel architectures are preferred.

Various parallel architectures are reviewed, such as the time-interleaved (TI) structures, quadrature mirror filter bank frequency-band decomposition (QMF-FBD) ADCs, Hadamard-modulated ADCs, and hybrid FBD (HFB) structures. These structures, are generally composed of an analysis filter bank, arrays of downsamplers and subband ADCs, upsamplers, and finally a synthesis filter bank. The analysis filter bank is an array of filters that decompose the signal into narrower subbands. Similarly, the synthesis filter bank is a group of filters that reconstruct the original wideband signal. In the case of the time-interleaved architecture, these filters are simple delays, and the signal is split in the time domain (time-multiplexed), whereas in the QMF-based structure, a low-pass filter and several contiguous discrete-time bandpass filters are used to split the signal in the frequency domain.

The hybrid architecture is similar to that of the QMF-FBD except for the analysis filter bank, which is an array of continuous-time filters instead of discrete-time analog filters. In the Hadamard-modulated architecture, analysis filters are not explicitly defined.

Instead, some analog preprocessing and some digital post-processing and filtering is used to decouple the signal from the quantization noise.

The TI systems are one of the popular structures. These systems, however, are sensitive to jitter and need a wideband, high-precision S/H stage. To solve this problem, a two-stage S/H can be used, with the first stage implemented as a wideband precise S/H in a suitable technology such as GaAs. Speed and precision requirements are therefore relaxed in the following subband S/H stages. In practice, the required speed in the first-rank S/H limits the number of channels that can be interleaved. Instead, many calibration techniques have been proposed to compensate for timing errors. The TI structures are also sensitive to component mismatch between the channels and these errors should also be compensated in the calibration stage and/or digital domain.

In the QMF-FBD, this problem is solved to some extent, since the input is discrete and subband downsamplers act similar to a second sampling stage. However, the problem of implementing a wideband high-precision S/H circuit is still a major challenge, particularly in CMOS technology. Hadamard-modulated ADCs channelize already sampled, discrete data. The S/H stage is therefore a bottleneck for these systems in achieving a high bandwidth. In the HFB, signal sampling is performed after filtering the wideband input signal into narrower subbands. However, since this architecture does not frequency-translate high-frequency bands down to baseband, the HFB still requires high-frequency S/H circuitry that needs to operate over the corresponding frequency-band of each channel.

In this thesis, a new parallel ADC architecture is proposed to increase the conversion speed of ADCs while maintaining a medium-to-high resolution. This architecture addresses the sampling problem by performing all of the sampling in the narrowband baseband. In this

structure, sampling is accomplished after splitting the input wideband signals into narrower subbands and frequency-translating them into baseband where identical narrowband baseband S/H blocks can be used. Therefore, lower-speed, lower-precision S/H stages are required and single-chip fully-CMOS implementation of the entire ADC is feasible.

In Chapter 3, the proposed parallel ADC architecture, namely, the frequency-translating hybrid ADC (FTH-ADC) is introduced and analyzed. Also, it is shown how the digital reconstruction part, including the digital FIR reconstruction filters are designed and optimized for such architectures based on the measurements on the analog path.

In Chapter 4, a proof of concept board-level implementation of an FTH-ADC is used to analyze the effects of major analog non-idealities and errors. Also, error measurement and compensation methods are presented for this architecture. Some design trade-offs and sources of complexity in the FTH-ADC systems are also discussed in this chapter. Finally, it is shown that using four 8-bit, 100 MHz subband ADCs, four 25 MHz Butterworth filters, two 64-tap, FIR reconstruction filters, and four 10-tap FIR imbalance compensation filters (α, β factors), a total FTH-ADC system with an input bandwidth of 100 MHz and an effective sample rate of 200 MHz is achieved with an ENOB of more than 7 bits over the entire bandwidth.

Chapter 5 is devoted to circuit-level implementation and CMOS 90 nm integration and measurement of one channel of an 8-GHz, 4-bit, FTH-ADC system; including a highly-linear mixer (at least 26 dB of linearity) and a 5^{th}-order, 1 GHz, Butterworth G_m-C active filter. These blocks, together with a 4-bit, 4-GHz subband ADC consume a total power of 52 mW out of a 1.2 V power supply, with an active area of 0.05 mm^2 (mixer: 11×13 μm^2, filter: 80×260 μm^2, ADC: 300×100 μm^2).

The one channel implementation consists of a fully-differential 5^{th}-order Butterworth G_m-C filter and a double-balanced passive mixer and is designed to have a THD ≤ 5% (26 dB) over its full 1 GHz bandwidth and to provide an output voltage swing of 350 mV_{pp} for the subsequent subband 4-bit, 4 GS/s ADC stage.

It should be mentioned that although the focus of this thesis is on CMOS implementation, the idea of FTH-ADC structure is not limited to any particular technology or type of subband ADC structure. In fact, this structure can be used to push the performance limits of any available ADC to increase the bandwidth and sampling rate while maintaining its resolution. Therefore, the FTH-ADC system can be used to achieve performance metrics in terms of resolution and conversion rate that is not attainable with conventional ADCs.

Major challenges and limitations in this architecture include linearity of the analog mixers and the overall system power. Also, increasing the number of parallel channels may have adverse effects on the overall power and cost. Therefore, as with other architectures, benefits of the FTH-ADC depend on the specifications of the target application. For example, this structure suits applications that require medium resolution ADCs (6-8 bits) with giga-hertz conversion rates.

6.2 Future Work

One of the key challenging parts in the design of the FTH-ADC is providing sufficient linearity in the mixers. Designing quadrature mixers with output SNRs of more than 40 dB (about 6 bits) is challenging with the current CMOS technology [59]. As an alternative to solve this problem, the idea of digitally-assisted analog circuits can be used

[68]. In these systems, the analog circuits are simplified and their errors are compensated in the digital domain. This may be used to compensate for mixer unwanted harmonics or centre-frequency offsets.

Although jitter is somewhat tolerable in these systems (as discussed in Chapter 4), care should be taken to minimize the jitter and phase imbalance in the mixer LOs and ADC clock signals. One solution to this problem is to use a single source for all these signals and to use a frequency multiplier to produce the various frequencies needed. Note that the LO signals of each channel are multiples of the LO signal of the first channel and the ADC clock frequency is four times the frequency of the LO signal of the first channel.

Similar to [44], standard analog analysis filters in the FTH-ADC can be replaced by optimized ones such that better resolutions are attainable. In this case, the analog and digital filters of the filter bank should be optimized together. Also, infinite impulse response (IIR) digital synthesis filters can be optimized to reconstruct the digital representation of the analog wideband signals. These filters may be harder to design due to their stability and phase distortion problems.

As another approach, similar to the one used in [69] for HFB structures, two levels of filtering can be used so that the optimization for the distortion term and the aliasing terms can be performed independently. This leaves more parameters to be optimized and provides for better degrees of freedom and therefore better optimization.

Sigma-delta modulators with oversampling ratios more than 2 can be used as the subband ADCs to provide for higher resolution ADCs. In this case, noise-shaping filters may be added in the digital reconstruction part. These filters may also be merged to the reconstruction and/or compensation filters. As explained before, the OSR = 2 can be

replaced by Nyquist sample rates in the subband ADCs, i.e., subband ADCs with a sample rate of Ω_B/M can be used; together with an upsampler and a digital low-pass filter to remove the extra components due to quadrature sampling. These components should be attenuated to avoid deteriorating the SNR of the overall system.

Similar to [49], time-interleaved ADCs can be used in each channel to achieve higher speeds for subband ADCs and therefore higher speeds for the total system. This will allow for the use of higher-resolution, lower-speed subband ADCs and therefore a higher overall resolution for the total ADC system (Recall the trade-off between resolution and speed in single-stage ADCs). Also, other structures, such as the tree-structured [30], or any other parallel or single-stage ADCs can be used as the subband ADCs.

The idea of shifting the signal into baseband can also be implemented with other structures, such as complex filters [70]-[71] or quadrature bandpass sampling [72]-[73].

If the FTH-ADC is used in a receiver architecture, the receiver downconversion mixers and the ADC mixers can be merged and the digital reconstruction structure may also be used to compensate for the channel characteristics.

The frequency transition region where the channels of the FTH-ADC overlap can also be optimized to enhance performance results, depending on the type of the analog analysis filters used.

The local oscillators (LOs) for this system are not implemented in this thesis. Various techniques such as polyphase filters [74], multi-phase LC oscillators [75], or Microstrip transmission lines [76], can be used to implement the 90° phase shifts for the quadrature mixers.

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