A Low-Jitter Spread Spectrum Clock Generator Using FDMP

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***Abstract*—A 1.5 GHz spread spectrum clock generator (SSCG) is realized by a fractional N frequency synthesizer with a third-order delta-sigma modulator and a fractional dual-modulus prescaler (FDMP). This FDMP utilizes a fractional division ratio to have a small phase step to improve the jitter performance. This SSCG has been fabricated in a 0.18 um CMOS process, and it consumes 34.2 mW from a supply of 1.8 V. The measured rms jitter is 5.55 ps and the measured electromagnetic interference reduction amount is 14.77 dB. The measured phase noise is -97.18 dBc/Hz at 1 MHz offset.**

***Index Terms*—Delta-sigma modulator (DSM), low jitter, prescaler, spread spectrum clock generator (SSCG).**

I. Introduction

THE serial advanced technology attachment (SATA) is becoming an important technique for the next- generation internal storage interconnection. As the clock becomes faster, the electromagnetic interference (EMI) issue is harmful. Several techniques [1]–[6] have been presented to improve this effect, such as frequency modulation [1], pulse swallow [2], phase interpolation [3], and delta-sigma (DSM) modulation [4]–[6]. For these techniques, the fractional-N frequency synthesizer using a delta-sigma modulator (DSM) is popular, because it is realized mostly by digital circuits and has a better EMI reduction.

Since a higher-order DSM may have multilevel outputs, a multi-modulus prescaler is needed in a fractional-N frequency synthesizer. However, the phase shift of the voltage-controlled oscillator (VCO) is large. In [4], a DSM with a level shifter is proposed to realize the fractional outputs of ± 0.5, ± 1.5, and so on. It reduces the phase shift generated by the DSM and achieves a low jitter performance [4]. However, the minimum division step of the prescaler is still unity. In this paper, a spread spectrum clock generator (SSCG) with an eight-phase VCO [7] and a fractional dual- modulus prescaler (FDMP) is presented to reduce the minimum division step to 0.375. It not only improves the phase resolution, but also decreases the jitter [8]. The resulting EMI reduction is also improved.

II. Circuit Description

The proposed SSCG is shown in Fig. 1. Basically, it is realized by a fractional-N frequency synthesizer with an eight-phase VCO and a divide-by-$(N-1/8)/(N+2/8)$ FDMP. To meet the SATA requirements [4], [5], the modulation controller realizes a down-spreading frequency deviation of 5000 ppm (1.4925–1.5 GHz).

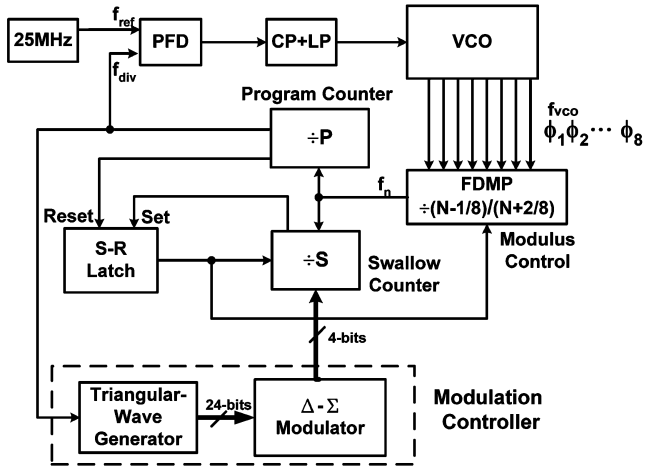

Fig. 1. Proposed SSCG.

This modulation controller is composed of a triangular wave generator and a third-order DSM, which has an input control word of 24-bits. The frequency of the triangular wave is 31 kHz and the reference clock is 25 MHz. The swallow counter in this SSCG is modulated by a third-order DSM. A programmed counter of $P = 15$ and a swallow counter of $S = 1 - 8$ are adopted. All the circuits will be described as follows.

A. Fractional Dual-Modulus Prescaler (FDMP)

Fig. 2(a) shows the proposed FDMP. It is composed of a divide-by-N divider, an $8 - 1$ multiplexer, and a 3-bits adder with three D flip-flops (DFFs). Assume there is a VCO with eight-phase outputs, $\phi_1 - \phi_8$. Three bits (M0, M1, and M2) serve as the inputs of the adder and they are accumulated under the clock signal $\mathrm{f_n}$, which is realized by the divide-by-N output of the selected VCO phase. Three output bits (S0, S1, and S2) of the DFFs will choose one among the eight VCO outputs by the 8-1 multiplexer. Table I gives the selected VCO output with respect to the controlling bits, (S0, S1, and S2).

From the 2's complement point of view, when $\mathrm{M2} = 0$, the adder will accumulate a positive value and the selected phase will increase in a forward direction. When $\mathrm{M2} = 1$, the adder will accumulate a negative value and the selected phase will decrease in a backward direction. If $(\mathrm{M2}, \mathrm{M1}, \mathrm{M0}) = (1, 0, 0)$, the outputs of the VCO, for example, ϕ_4 and ϕ_8, will be selected alternatively. The phase is decreased by half the period of the VCO, i.e., divided by $(N - 4/8)$. The output frequency fvco, of the VCO is equivalently divided by $(N - 4/8)$ to generate the output frequency fn of the FDMP. If $(\mathrm{M2}, \mathrm{M1}, \mathrm{M0}) = (0, 1, 0)$,

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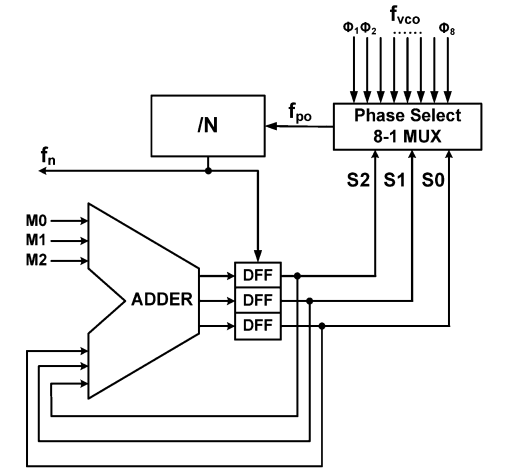
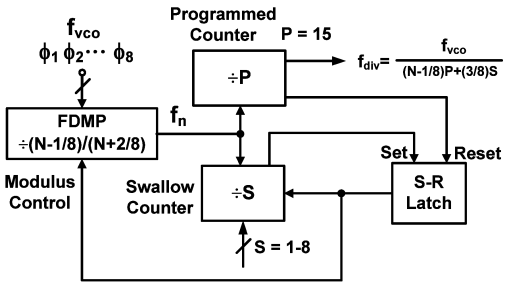


(a)



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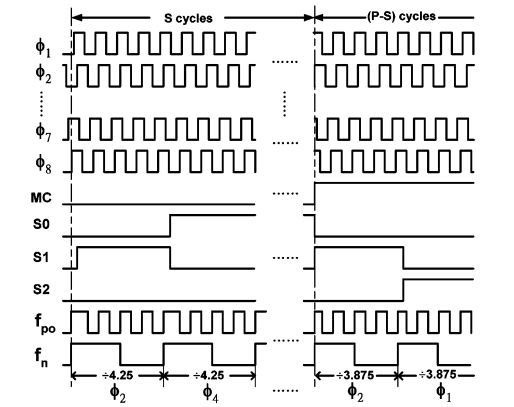
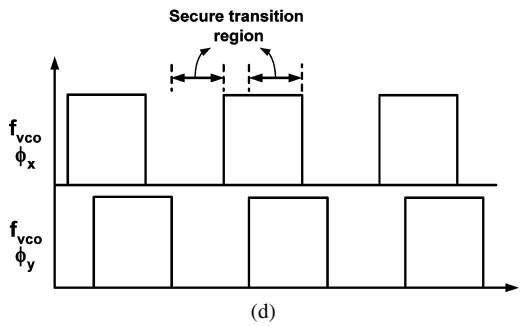


(c)



(d)

Fig. 2. (a) Fractional dual-modulus prescaler, (b) multimodulus programmable divider, (c) timing diagram for Fig. 2(b) with $N = 4$, (d) secure transition region for the controlling signals, S0, S1, and S2.

the outputs of the VCO, for example, ϕ_2, ϕ_4, ϕ_6 and ϕ_8, will be selected sequentially. The phase is increased by $1/4$ times

TABLE I
PHASE SELECTION CIRCUIT

S0 S1 S2	Selected Output	Phase
0 0 0	ϕ_8	315°
0 0 1	ϕ_1	0°
0 1 0	ϕ_2	45°
0 1 1	ϕ_3	90°
1 0 0	ϕ_4	135°
1 0 1	ϕ_5	180°
1 1 0	ϕ_6	225°
1 1 1	ϕ_7	270°

the period of the VCO, i.e., divided by $(N + 2/8)$. Hence, according to different combinations of (M2, M1, M0), this FDMP can generate the division ratios of $N - 4/8, N - 3/8$, $N - 2/8$, $N - 1/8$, $N, N + 1/8$, $N + 2/8$, and $N + 3/8$, respectively. To realize a dual-modulus prescaler, one can select two from the above eight division ratios. There are 56 kinds of different combinations. Since we would like to realize a divide-by-$(N - 1/8)/(N + 2/8)$ FDMP, the following relation is implemented as $(\mathrm{M2}, \mathrm{M1}, \mathrm{M0}) = (\mathrm{MC}, 1, \mathrm{MC})$ where MC represents the modulus control. When $\mathrm{MC} = 1$, i.e., $(\mathrm{M2}, \mathrm{M1}, \mathrm{M0}) = (1, 1, 1)$, the division ratio is N$-1/8$. When $\mathrm{MC} = 0$, i.e., $(\mathrm{M2}, \mathrm{M1}, \mathrm{M0}) = (0, 1, 0)$, the division ratio is $N + 2/8$. Thus, a divide-by-$(N - 1/8)/(N + 2/8)$ FDMP is realized.

The multimodulus programmable divider using a FDMP is shown in Fig. 2(b). Different from the conventional structure in [9], the divide-by-$N/N + 1$ dual-modulus prescaler is replaced by the proposed divide-by-$(N-1/8)/(N+2/8)$ FDMP. A programmed counter $(P = 15)$, a programmable swallow counter $(S = 1$–$8)$, and an SR latch are needed. The output clock from the programmed counter serves as the clock for the modulation controller and the phase-frequency detector (PFD). The operation of this multimodulus programmable divider is described as follows. When a new division cycle starts, MC is reset to 0 and the FDMP divides by $(N+2/8)$ for S cycles. Next, MC is set to 1 and the FDMP divides by $(N - 1/8)$ for the remaining $P - S$ cycles. Fig. 2(c) shows the timing diagram of the multimodulus programmable divider with $N = 4$. In Fig. 2(c), the signal $\mathrm{f_{po}}$, is divided by 4.25 for S cycles and divided by 3.875 for the remaining $P - S$ cycles. Note that the timing for the three control signals S0, S1, and S2, from the three DFFs is important. To consider a case that one has to jump between two VCO outputs, ϕ_x and ϕ_y where $x \neq y$ and $x, y = 1-8$, as shown in Fig. 2(d). The secure transition regions are defined when both ϕ_x and ϕ_y are high or low. If the controlling signals, S0, S1, and S2, do not fall into these regions, an undesired glitch may occur and it will cause errors in case that its magnitude is enough large. Finally, the division ratio of the multimodulus programmable divider is calculated as

$$(N + 2/8) \times S + (N - 1/8) \times (P - S) = (N - 1/8) \times P + 3/8 \times S. \quad (1)$$

Since the swallow counter is modulated by the DSM, the value of S changes from 1 to 8. Compared to the conventional approach, the division ratio of the swallow counter is multiplied

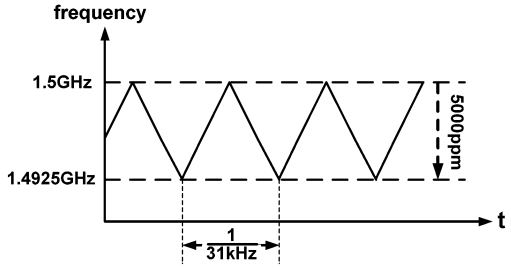


Fig. 3. Triangular wave modulation profile.

by a fractional factor of $3/8$ in this proposed multimodulus programmable divider. Thus, a smaller division step is realized and the corresponding jitter is reduced.

B. SSCG Design

For an SSCG in the SATA application, a 31 kHz triangular wave generator, a divide-by$-3.875/4.25$ FDMP and a DSM are used to realize the down spreading of 5000 ppm at 1.5 GHz. The frequency modulation profile is shown in Fig. 3. In the SATA application, the down spreading of 5000 ppm implies that the output of this SSCG lies within 1.4925 and 1.5 GHz. For a reference clock of 25 MHz, the average division ratio of the divider should be within 59.7 and 60. Assume the fractional division ratio is expressed as

$$\bar{n} + \frac{K}{2^M} \cdot \frac{\phi_{\text{step}}}{2} \tag{2}$$

where $\bar{n}$ is the average value of all division ratios, K is a modulator input control word, M is the number of bits of the DSM, ϕ_{step} is the jumped phase step, which corresponds to the minimal division step of the divider. Assume M is known and there are three parameters, $\phi_{\text{step}}, \bar{n}$, and K, to be determined.

First, the required jumped phase step must be calculated. According to (2), to have the maximal and minimal output frequencies with the corresponding modulator input control word, two following equations are derived from (2)

$$\bar{n} + \frac{K_1}{2^M} \cdot \frac{\phi_{\text{step}}}{2} = 60 \tag{3a}$$

And

$$\bar{n} + \frac{K_2}{2^M} \cdot \frac{\phi_{\text{step}}}{2} = 59.7 \tag{3b}$$

where K_1 and K_2 are the maximal and minimal modulator input control words, respectively. By subtracting (3a) from (3b), the following equation is obtained:

$$\left(\frac{K_1}{2^M} - \frac{K_2}{2^M}\right) \cdot \phi_{\text{step}} = 0.6. \tag{4}$$

Since $-1 \leq (K_1/2^M, K_2/2^M) \leq 1$, i.e., $|K_1/2^M - K_2/2^M| \leq 2$, the required jumped phase step $\phi_{\text{step}} \geq 0.3$ can be calculated according to (4). However, if $\phi_{\text{step}} = 0.3$ is chosen, integrators in the DSM may enter into saturation mode and distortion will occur. Therefore, the desired phase step should be $\phi_{\text{step}} > 0.3$. For example, if an eight-phase VCO is adopted, the closest solution is $\phi_{\text{step}} = 0.375$, i.e., to jump three phases within eight phases.

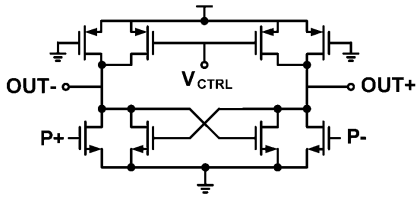


Fig. 4. VCO delay cell.

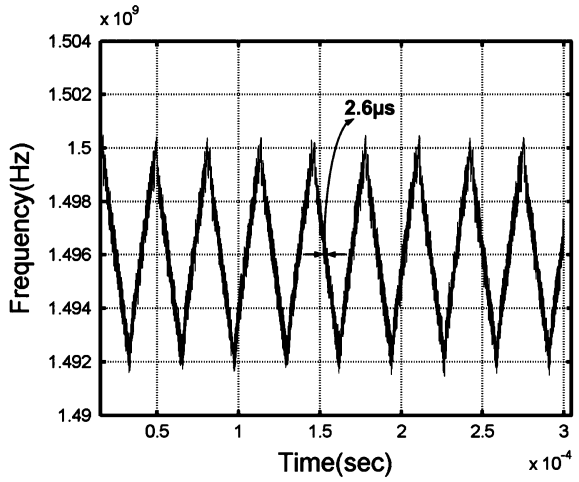
Second, the average division ratio of $\bar{n}$ must be calculated. Based on (3a) and (3b) and $\phi_{\text{step}} = 0.375$, since $-1 \leq (K_1/2^M, K_2/2^M) \leq 1$, $\bar{n}$ must range from 59.8125 to 59.8875. There are several dual-modulus division combinations, such as $\text{N}/(\text{N}+3/8), (N-1/8)/(N+2/8), (N-2/8)/(N+1/8), (N-3/8)/N$, and $(N-4/8)/(N-1/8)$ that can be chosen to meet $\phi_{\text{step}} = 0.375$. To choose the required $\bar{n}$, one has to consider the multimodulus programmable divider in Fig. 2(b). In this programmable divider, two integer programmable counters P and S, are needed to realize required $\bar{n}$ within 59.8125 and 59.8875. One possible set of the solutions is 59.8125, by using two programmable dividers, $P = 15$ and $S = 1-8$, and a divide-by-$(N-1/8)/(N+2/8)$ FDMP with $N = 4$. The programmable counter S, is modulated by a DSM. The division ratio is calculated as $(N-1/8) \times P + (3/8) \times S$, and the corresponding eight division ratios are 58.5, 58.875, 59.25, 59.625, 60, 60.375, 60.75, and 61.125. One can find that the minimal division step is 0.375 instead of 1, compared with a conventional divide-by-$N/(N+1)$ dual-modulus prescaler. Note that when the spread spectrum clocking function is turned ON, the divider is changing among these eight division ratios to realize the required frequency deviation. However, when the spread spectrum clocking function is turned OFF, the normal division ratio of 60 is selected to generate the output frequency of 1.5 GHz with a reference clock of 25 MHz. When ϕ_{step} and $\bar{n}$ are determined, two parameters can be calculated as $K_1 = 2^M$ and $K_2 = -0.6 \cdot 2^M$.

C. Eight-Phase VCO

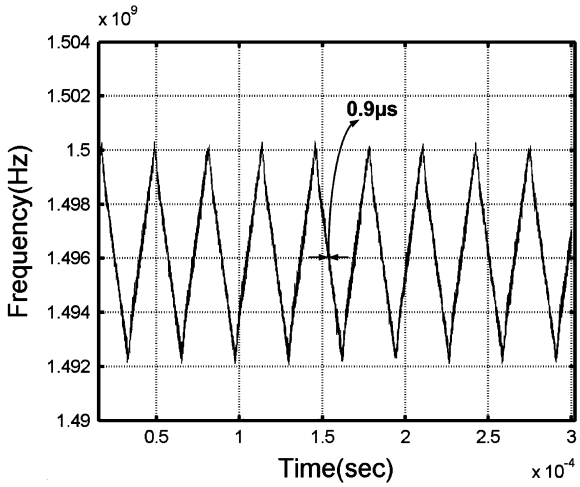
To realize an eight-phase VCO, a fully-differential four-stage voltage-controlled ring oscillator is adopted. Fig. 4 shows the delay cell for every stage. The input NMOS transistors are adopted to have a higher speed. The NMOS cross-coupled pair is used to increase the gain and speed of the delay cell. It also prevents oscillator from latching into a stable common-mode state. Two normally-ON PMOS transistors act as the loads and the other two PMOS ones act as the voltage-controlled resistors to adjust the oscillation frequency. The VCO needs a careful layout to make it symmetrical and reduce the phase mismatch. This voltage-controlled ring oscillator provides the eight phase outputs, low power and small area.

D. DSM and Triangular Wave Generator

A digital third-order multistage noise-shaping (MASH) $1-1-1$ DSM [10], [11] is adopted, which has a modulator input control word of 24-bits for the SSCG. Conventionally, a higher-order single-loop DSM has stability issues, which may reduce the available input dynamic range. Hence, the MASH architecture is adopted to solve this problem [12]. Since this DSM is



(a)



(b)

Fig. 5. Simulated frequency modulation profile for a conventional SSCG using an (a) divide-by-$N/N+1$ prescaler and (b) divide-by-$(N-1/8)/(N+2/8)$ prescaler.

third-order, this SSCG uses a fourth-order loop to suppress the quantization noise at high frequencies.

A finite state machine is used to realize a 31 KHz triangular waveform in our design. Since a triangular wave can be viewed as the ramp function with positive and negative slopes, two states are used: one state represents the ramp function with a positive slope and the other represents the ramp function with a negative slope. The triangular-wave generator and the third-order 24-bits DSM are realized by automatic synthesis tools. The realized area is only 0.25 mm $\times$ 0.1 mm.

III. Simulation Results

The loop was simulated with a VCO gain $(\mathrm{K_{vco}})$ of 900 MHz/V, CP current $(\mathrm{I_{cp}})$ of 200 μA, and a reference clock of 25 MHz. The fractional-N frequency synthesizer has a resulting loop bandwidth of 500 kHz and a phase margin of 59°. Fig. 5(a) shows the simulated frequency modulation profile for a conventional SSCG using a divide-by-$N/N+1$ dual-modulus prescaler, which has eight division ratios of 56$\sim$63 in a step of unity. Fig. 5(b) shows the simulated frequency modulation profile for the proposed SSCG using the proposed divide-by-$(N-1/8)/(N+2/8)$ FDMP, which has eight division ratios of 58.5–61.125 in a step of 0.375. For the modulated triangular waveform of 31 kHz, the simulated time deviation in Fig. 5(a) is 2.6 μs and is 0.9 μs in Fig. 5(b). The case with a smaller time deviation will introduce a less jitter. The simulation result indicates that the proposed SSCG

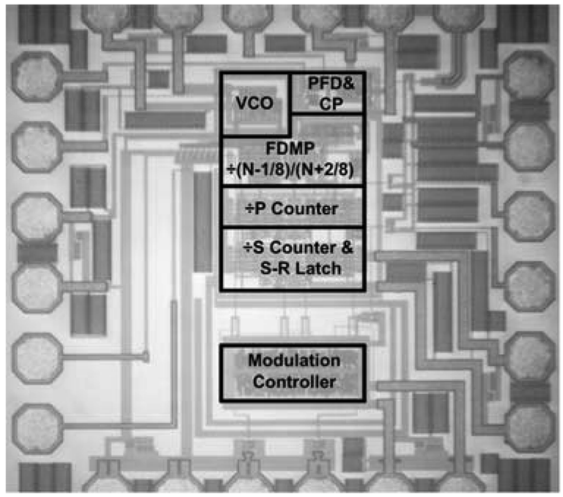
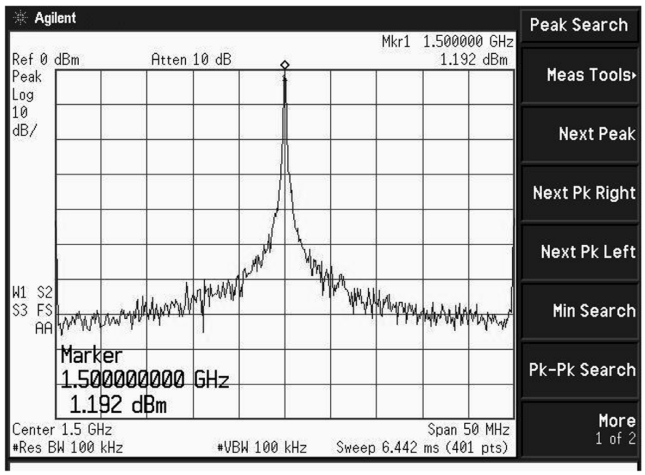


Fig. 6. Die photo.



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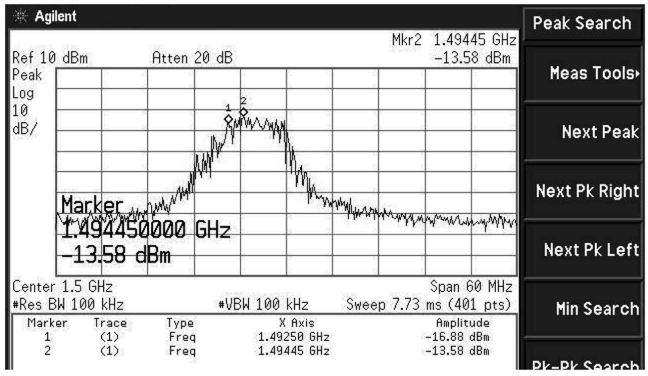

(b)

Fig. 7. Measured frequency spectrum with SSC function: (a) turned OFF and (b) turned ON

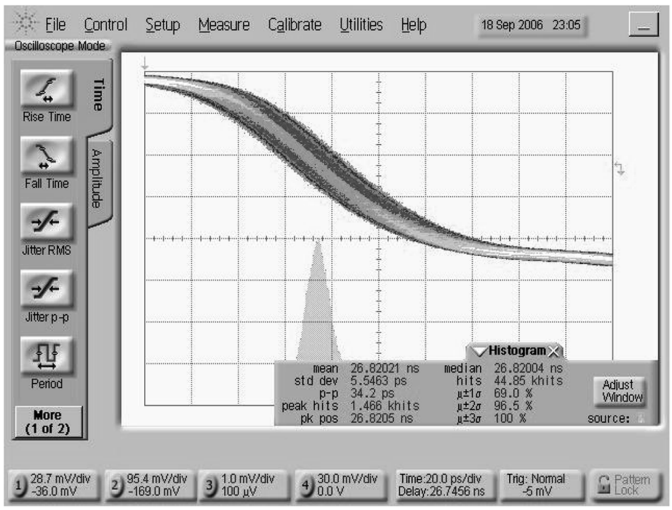

Fig. 8. Measured jitter with SSC turned ON.

TABLE II
COMPARISONS WITH OTHER WORKS

	[2]	[3]	[4]	[5]	Our
Modulation method	Pulse Swallow	Phase Interpolated	Delta-Sigma Modulation		
EMI reduction(dB)	7	5.4	10.3	9.8	14.77
RMS jitter(ps)	9.3*	-	8.1	3.24	5.55
Pk-Pk jitter(ps)	57.2*	-	-	58.3	34.2
Power (mW)	-	-	54	77	34.2
Core Area (mm^2)	-	-	0.42	0.31	0.17
Technology (um)	0.13	0.15	0.15	0.18	0.18
Application	SATA 1.5GHz Clock				

* Measured with SSC off

has an improvement factor of $8/3$ when compared with the conventional SSCG. It is consistent with the minimal division step of $3/8$ in the proposed SSCG.

IV. EXPERIMENTAL RESULTS

This SSCG has been fabricated in a 0.18 μm CMOS process. The power dissipation is 34.2 mW from a supply of 1.8 V. The die photo is shown in Fig. 6 and the core area is 0.56 mm $\times$ 0.31 mm. To reduce the noise coupling from the modulation controller to the frequency synthesizer, double guard rings are used to isolate the noise.

Fig. 7(a) shows the measured frequency spectrum at 1.5 GHz when spread spectrum clocking (SSC) function turns OFF. The measured peak carrier is 1.19 dB. Fig. 7(b) shows the measured frequency spectrum when the SSC function turns ON, and it spreads from 1.4925 to 1.5 GHz, i.e., a frequency deviation of 5000 ppm ($\sim$7.5 MHz). The measured peak carrier is -13.58 dB at 1.49445 GHz for the resolution bandwidth of 100 kHz.

Thus, the measured EMI reduction amount is 14.77 dB. The measured phase noise is -97.18 dBc/Hz at the offset frequency of 1 MHz. In Fig. 8, the measured PLL rms jitter with SSC turned ON is 5.55 ps and the measured peak-to-peak jitter is 34.2 ps. The jitter is measured by using a self-triggered signal.

The performance summary and comparisons are provided in Table II. In Table II, the EMI reduction amounts are compared for the resolution bandwidth of 100 kHz. The rms and pk-pk jitter are listed for a clear comparison. Note that all jitter values are compared with SSC turned ON except [2]. Because 10 phases are used in [5], the measured rms jitter is better. But it shows a large pk-pk jitter which may come from a lower order DSM. Since a lower order DSM can not properly scramble the relationship between input and quantization noise, the resulted noise is contributed to the deterministic jitter.

V. CONCLUSION

A 1.5 GHz SSCG for the SATA application is presented. By using the proposed FDMP, the minimum division step is reduced to 0.375. It results in lower jitter than conventional dual-modulus architectures. A compact triangular-wave generator is also presented. The design issues for the proposed SSCG have been discussed and analyzed. This SSCG has been fabricated in 0.18 μm CMOS process. The measurement results confirm the theoretical analysis.

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