Hardware Architecture for List Successive Cancellation Decoding of Polar Codes

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Abstract—We present a hardware architecture and algorithmic improvements for list SC decoding of polar codes. More specifically, we show how to completely avoid copying of the likelihoods, which is algorithmically the most cumbersome part of list SC decoding. The hardware architecture was synthesized for a blocklength of N = 1024 bits and list sizes L = 2, 4 using a UMC 90nm VLSI technology. The resulting decoder can achieve a coded throughput of 181 Mbps at a frequency of 459 MHz.

Index Terms-Polar codes, list SC decoding, VLSI.

I. INTRODUCTION

► HANNEL polarization gives rise to an elegant and provably good class of channel codes, called *polar* codes [1]. Decoding of polar codes is usually performed using a successive cancellation (SC) decoder [1]. Some hardware architectures for SC decoding of polar codes were discussed in [2], [3], [4], and [5], while the first ASIC of such a decoder was presented in [6]. Moreover, an FPGA implementation of a belief propagation decoder for polar codes was presented in [7]. Recently, more sophisticated decoding algorithms, such as the list SC decoder [8], [9], and the stack SC decoder [9], were introduced. These algorithms provide improved error correcting performance at the cost of increased complexity. Stack SC decoding suffers from high memory requirements, costly metric normalization, and non-deterministic decoding latency, making list SC decoding more attractive from a practical perspective. Unfortunately, the list SC decoder is burdened by a likelihood copying step and no architecture of such a decoder exists yet in the literature.

Contribution and Outline: This brief presents an architecture for list SC decoding of polar codes. To this end, we also describe how the copying of the intermediate likelihoods in the list SC decoding algorithm can be avoided. In Section II, we briefly review the construction and decoding of polar codes. Section III discusses algorithmic improvements to list SC decoding, while in Section IV the proposed list SC decoder architecture is described. Section V summarizes VLSI implementation results and concludes this letter.

II. POLAR CODES

We use a_1^N to denote a row vector (a_1, \ldots, a_N) and a_i^j to denote the subvector (a_i, \ldots, a_j) . We use the operators log and ln for the binary and natural logarithm, respectively.

A polar code is constructed by recursively applying a polarizing transform n times to the binary input symmetric and memoryless channel W. This transform is linear and it can be expressed as a 2×2 matrix, denoted by **F**. The n-fold

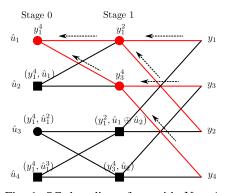


Fig. 1: SC decoding of u_1 with N = 4.

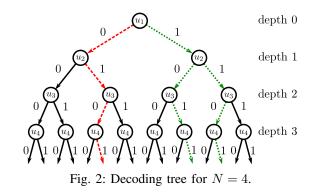
application of this transform can be expressed as an $N \times N$ matrix **G**, with $\mathbf{G} = \mathbf{F}^{\otimes n}$, where $^{\otimes n}$ denotes the *n*-fold application of the Kronecker product. Encoding is performed by choosing a sequence $u_1^N \in \{0,1\}^N$ and calculating the codeword $x_1^N = u_1^N \mathbf{G}$. This codeword is transmitted over N uses of W and a noisy codeword y_1^N is received.

A. Successive Cancellation Decoding

The decoding method proposed by Arikan is based on successive cancellation. First, an estimate for u_1 , denoted by \hat{u}_1 , is calculated based on y_1^N . Then, u_2 is decoded, based on y_1^N and the knowledge of \hat{u}_1 , etc. In principle, it is possible to calculate the mutual information between (y_1^N, u_1^{i-1}) and u_i for every *i*. A polar code of rate R is constructed by letting only the $NR u_i$'s with the highest mutual information convey information, while freezing the remaining u_i 's to 0. The sets of non-frozen and frozen bit indices are denoted by \mathcal{A} and \mathcal{A}^c , respectively. The exact decoding procedure is dictated by the recursive structure of the code. In Fig. 1, the decoding process is visualized for N = 4. On the right-hand side of the graph, the likelihoods $W(y_i|x_i), i = 1, \dots, N, x_i \in \{0, 1\}$ are available. These likelihoods are combined pair-wise by going through a data dependency graph (DDG) with $N \log N$ nodes, which are grouped into $\log N$ stages. The output on the left side of the graph is $P(y_1^N, \hat{u}_1^{i-1}|u_i), u_i \in \{0, 1\}, i = 1, ..., N$. Hard decisions are taken according to

$$\hat{u}_{i} = \begin{cases} \arg \max_{u_{i} \in \{0,1\}} P(y_{1}^{N}, \hat{u}_{1}^{i-1} | u_{i}), & i \in \mathcal{A}, \\ 0, & i \in \mathcal{A}^{c}. \end{cases}$$
(1)

The two pairs of incoming likelihoods at each node, denoted by a_1^2 and b_1^2 , are combined in order to produce the *intermediate likelihoods*, according to either $f : [0,1]^4 \rightarrow [0,1]^2$ or



 $g: [0,1]^4 \times \{0,1\} \to [0,1]^2$ with

$$f(a_1^2, b_1^2) = \left(\frac{1}{2} \left(a_1 b_1 + a_2 b_2\right), \frac{1}{2} \left(a_2 b_1 + a_1 b_2\right)\right), \quad (2)$$

$$g(a_1^2, b_1^2, \hat{u}_s) = \left(\frac{1}{2}a_{1+\hat{u}_s}b_1, \frac{1}{2}a_{2-\hat{u}_s}b_2\right),\tag{3}$$

where \hat{u}_s is called a *partial sum*. Each partial sum is a linear combination of some of the previously decoded codeword bits [1]. The circle and square nodes of the DDG in Fig. 1 represent application of f and g, respectively. If intermediate likelihoods are stored, then the computational complexity of SC decoding is $O(N \log N)$ [1].

B. List SC Decoding

Successive decoding can be described as a search procedure on a full binary tree. The $2^{(i-1)}$ nodes at depth (i-1) represent u_i given all possible choices for \hat{u}_1^{i-1} . The two outgoing edges of each node in the tree are labeled with the two possible choices for \hat{u}_i . A decoder explores one or more paths in the tree by deciding which edge to follow at each step based on some metric. The SC decoder explores a single path from the root to the leaves of the tree. It uses the likelihood in (1) as a metric for edges corresponding to non-frozen bits and it always follows the edge corresponding to 0 for frozen bits. The SC decoder has the drawback that erroneous decisions at some point can never be recovered in the future. The list SC decoder, on the other hand, performs a breadth-first search on the tree under a complexity constraint. This constraint is enforced by discarding some of the paths at each step. Specifically, the list SC decoder with list size L keeps track of L paths simultaneously and also uses the likelihood in (1) as a path metric when encountering non-frozen bits. More formally, let $(\hat{u}_1^{i-1}(1),\ldots,\hat{u}_1^{i-1}(L))$ denote the L distinct decoding paths after the (i - 1)-th bit has been decoded. For every path $l \in \{1, \ldots, L\}$, there are two choices for $\hat{u}_i(l)$. Out of the resulting 2L paths, the L paths with the highest metric are preserved. When bit N is reached, the path with the highest metric is set as the decoded codeword. Decoding paths for an SC and a list SC decoder with L = 2 are shown by the red dashed and green dotted lines in Fig. 2, respectively.

All results in this paper are illustrated for N = 1024 and R = 0.5. The performance of list SC decoding over an AWGN channel for some practical list sizes is compared with the performance of SC decoding in Fig. 3. We performed 10^7

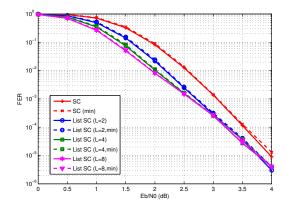


Fig. 3: Frame error rate (FER) performance of a (1024, 512) polar code under SC and list SC decoding with various L.

Monte-Carlo simulations for each data point. We observe that the returns of increased list size are small for L > 4 and that at high SNR using L > 2 provides almost no gain. However, at a FER of 10^{-2} , which is a sensible target FER for many communications standards, e.g., [10], the gain of list SC decoding is not negligible.

III. ALGORITHMIC CONSIDERATIONS

For each path, the intermediate likelihoods, the partial sums, and the path itself are stored in memories. We call these three memories collectively the *state-memories*. The content of each memory forms the *state* of each path. After the path selection step, each of the initial L paths is either discarded, kept, or duplicated, depending on whether it has zero, one, or two child nodes in the set of L out of 2L largest metrics, respectively. In order to duplicate a path, in a straightforward implementation its state is copied from one state-memory to another statememory, with some differences between the two copies that correspond to the two different choices for \hat{u}_i . It was shown in [8] that list SC decoding can be performed with complexity $O(LN \log N)$ when using a *lazy copy* technique. Our approach is to introduce an auxiliary *pointer memory* in order to avoid the high complexity of likelihood copying.

The algorithm in Fig. 4 describes list SC decoding. LI, \hat{U}_s , \hat{u} , and p denote the likelihood, partial sum, path, and pointer memories, respectively. For simplicity we think of LI as a three-dimensional memory which is indexed by the path index, the current stage index, and the bit index. Each element of LI stores a likelihood pair. The channel likelihood pairs are assumed to be stored in $LI(:, \log N, i), i = 1, \dots, N$, before LISTSC is called. \hat{U}_s , \hat{u} , and p are two-dimensional memories. Their first dimension is indexed by the path index and their second dimension is indexed by a combination of the partial sum, bit, and stage indices. The operation and structure of the pointer memory are described in the following section. The 2L path metrics are stored in the $L \times 2$ memory M. PATHSELECTION takes 2L path metrics as input and outputs the indices of the parent paths corresponding to the paths with the L best metrics, denoted by $l_p(l)$, l = 1, ..., L, and the corresponding values for $\hat{u}(l, i)$. The straightforward copying approach is chosen for the partial sums and the paths because

1: function LISTSC(L)2: for $i \leftarrow 1$ to N do $stage \leftarrow$ index of first '1' in $\log N$ -bit MSB-0 binary 3: representation of (i-1) (if i = 1, then $stage \leftarrow \log N$) 4: for $l \leftarrow 1$ to L do 5: for $s \leftarrow stage - 1$ to 0 do 6: $LI(l, s, :) \leftarrow UPDATESTAGE(LI(p(l, s+1), s+1, :))$ 7: $p(l,s) \leftarrow l$ 8: end for $M(l,:) \leftarrow LI(l,0,i)$ Q٠ 10: end for 11: if $i \in \mathcal{A}^c$ and i < N then 12: $\hat{u}(l,i) \leftarrow 0, \ l = 1,\ldots,L$ 13: else $(l_p(:), \hat{u}(:, i)) \leftarrow \text{PathSelection}(M)$ 14: 15: $p(l,:) \leftarrow p(l_p(l),:), \ l = 1, \dots, L$ 16: $\hat{U}_s(l,:) \leftarrow \hat{U}_s(l_p(l),:), \ l = 1, \dots, L$ $\hat{u}(l,:) \leftarrow \hat{u}(l_p(l),:), \ l = 1, \dots, L$ 17: 18: end if 19: end for 20: return $\hat{u}(1,:)$

Fig. 4: LISTSC: List SC decoding with list size L.

it can be carried out in a single clock cycle in hardware with small overhead due to the small size of the involved memories. Lines 4–10 of ListSC can be performed in parallel, since there are no data dependencies between the loop iterations. UPDATESTAGE, which performs the likelihood updates for the given decoding stage using the update rules described in [1], can also be executed in parallel for the 2^s nodes of the DDG that require updating at stage *s* [3].

A. Low-Complexity State Copying

In this section, we describe the function of the pointer memory p. Assume that, for the code in Fig. 1, we have L = 2, and u_1, u_2 are non-frozen while u_3, u_4 are frozen. Decoding starts with one (empty) path. The path metrics for $\hat{u}_1 = 0, 1$, are calculated using the SC procedure based on the contents of the first state-memory. The intermediate likelihoods which are produced are written to the first state-memory. In general, the intermediate likelihoods which are produced for path $l \in \{1, \ldots, L\}$, are written to the *l*-th state-memory. Instead of taking a hard decision on \hat{u}_1 as the SC decoder would, the list SC decoder duplicates the (empty) parent path and extends the first copy with $\hat{u}_1 = 0$ and the second copy with $\hat{u}_1 = 1$. The SC procedure for the two new paths requires the intermediate likelihoods produced by their parent path in order to calculate the path metrics for $\hat{u}_2 = 0, 1$. These likelihoods are located in the first state-memory, since they were produced by the first path in the previous decoding step. The intermediate likelihoods produced by the SC procedure for $\hat{u}_2 = 0, 1$, for the first and second paths are written to the first and second state-memory, respectively. From lines 5-8 of the list SC algorithm in Fig. 4, we see that the SC procedure does not process all stages of the decoding graph for each u_i . So, if after \hat{u}_2 has been processed the list SC decoder follows a new path whose parent is the second path, it has to read the intermediate likelihoods for the stages which were not processed when decoding \hat{u}_2 from the first state-memory, and the intermediate likelihoods for the stages which were processed when decoding \hat{u}_2 from the second state-memory. The auxiliary pointer memory p of dimension $L \times (\log N - 1)$ keeps track of which memory stores each path's likelihood for each stage. When a decision for \hat{u}_2 needs to be made, there are four candidate paths, out of which the two paths with the best metrics are kept, while the remaining two are discarded. Now, instead of copying the intermediate likelihoods of the paths that we want to keep, it suffices to copy the references to the state-memories contained in the pointer memory. Since u_3 and u_4 are frozen, both paths are extended with $\hat{u}_3 = 0$ and $\hat{u}_4 = 0$ and the best path is declared as the decoded codeword.

B. Likelihood Representation

SC decoding can be carried out in the log-likelihood ratio (LLR) domain by modifying (2)-(3) [2]. LLRs provide reduced storage requirements, increased numerical stability, as well as simplified computations with respect to a likelihood based implementation. The list SC decoding algorithm is described using likelihoods and log-likelihoods (LLs) in [8] and [9], respectively. LLRs can be converted to LLs by using $LL(x_i) = \ln \frac{\exp(LLR)^{1-x_i}}{1+\exp(LLR)}$. However, this conversion assumes that $L(x_i) = \ln \frac{\exp(LLR)^{1-x_i}}{1+\exp(LLR)}$. that LL(0) + LL(1) = 1, which is not true in general. Thus, each LL is normalized by a different factor, so the ordering of the path metrics will be affected and they can no longer be used to choose the L best paths. For this reason, in our decoder the likelihoods are represented in LL form, which also simplifies the computations in (2)–(3) and provides numerical stability, but requires more storage. We use negative LLs, which are always positive numbers and do not require a sign bit, to make the binary representation more compact. Assuming transmission over an AWGN channel with noise variance σ^2 , the negative LLs are

$$LL(x_i) = -\ln W(y_i|x_i) = \frac{(y_i - \mu(x_i))^2}{2\sigma^2} + \ln \sqrt{2\pi\sigma^2}, \quad (4)$$

where $\mu(x_i) = 1 - 2x_i$, $x_i \in \{0, 1\}$, is the modulated version of codeword bit x_i . Using negative LLs, (2) and (3) become

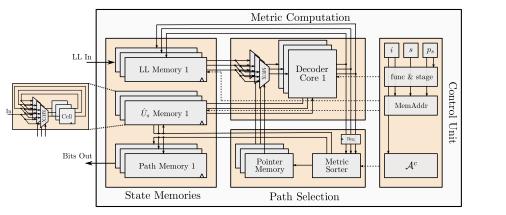
$$f(a_1^2, b_1^2) = (\min^*(a_1 + b_1, a_2 + b_2), \\ \min^*(a_2 + b_1, a_1 + b_2)), \quad (5)$$

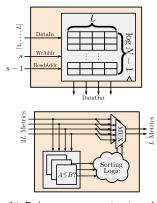
$$g(a_1^2, b_1^2, \hat{u}_s) = (a_{1+\hat{u}_s} + b_1, a_{2-\hat{u}_s} + b_2), \qquad (6)$$

where $\min^*(a, b) = \min(a, b) + \ln(1 + e^{-|a-b|})$. The f function is simplified by using an approximation that ignores the $\ln(\cdot)$ term. In Fig. 3, the performance of SC and list SC decoding with this approximation are plotted using dashed lines. There is practically no difference in performance with respect to the exact implementation for the used blocklength and list sizes. Our simulations show that the loss becomes slightly larger as the blocklength is increased. For example, for $N = 2^{15}$ the loss is approximately 0.1 dB. Moreover, let c, d > 0 be constants. Then, for any $a, b \ge 0$, we have

$$\min(ca + d, cb + d) = c\min(a, b) + d,$$
 (7)

$$(ca + d) + (cb + d) = c(a + b) + 2d.$$
 (8)





(b) Pointer memory (top) and metric sorter (bottom).

(a) List SC decoder architecture with details of the structure of the memory cells.

Fig. 5: Block diagram of the proposed list SC decoder architecture.

At each stage of SC decoding only one type of function is used, so the constant terms are common for all involved calculations. Thus, they can be recursively factored out and removed without affecting the ordering of the path metrics. So, we can use $LL(x_i) = (y_i - \mu(x_i))^2$, which is easier to handle by the quantization step.

IV. LIST SC DECODER ARCHITECTURE

The list SC decoder is a combination of three components. The first component is the metric computation unit (MCU), which calculates the metrics for each path using the sequential SC procedure. The second component, called the statememories component, consists of L state-memories, which the MCU uses to compute the 2L path metrics. Moreover, a third component manages the tree search by performing path selection based on the metrics that are calculated by the MCU. An overview of the proposed list SC decoder architecture is presented in Fig. 5(a). The MCU contains L SC decoder cores, which perform the metric calculation based on the state that they are supplied with. Multiplexers are responsible for redirecting the correct LLs to each decoder core, according to the entries of the pointer memory. The path selection unit contains a sorter which finds the L best metrics out of 2Loptions, along with the path index and the value of $\hat{u}_i(l)$ from which they resulted, and the pointer memory, which manages the memory read access of the SC decoder cores.

A. LL Quantization

Since the LLs are positive numbers, as SC decoding moves towards stage 0, their dynamic range increases. When an LL pair saturates, it is useless for making a decision. Thus, when using LLs, it is crucial to avoid saturation. In (5) and (6), two numbers with the same dynamic range are added. The simplest way to avoid all saturations is to increase the number of bits used to store the LLs by one bit per stage. This way, the only performance degradation with respect to the floating point implementation comes from the quantization of the channel LLs. Let Q_{ch} denote the number of bits used for the quantization of the channel LLs. The performance of the list SC decoder under various quantization bit-widths using a

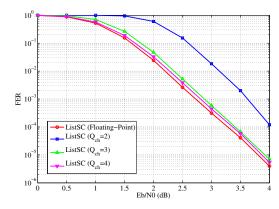


Fig. 6: FER performance of a (1024, 512) polar code under floating-point and fixed-point list SC decoding for L = 2.

uniform quantizer with quantization step $\Delta = 1$ is presented in Fig. 6. For the remainder of this paper, we choose $Q_{ch} = 3$, since the degradation with respect to the floating point and to the $Q_{ch} = 4$ implementations is very small.

B. Metric Computation Unit

The architecture of the SC decoder cores contained in the MCU is derived from the log-likelihood ratio (LLR) based architecture of [3], which was modified to implement LL based SC decoding. Each decoder core consists of P processing elements (PEs) that operate on up to P nodes of each stage of the DDG in parallel. For fair comparison, we chose P = 64as in [6]. Three counters track the index i of the bit that is currently being decoded, the current stage s within the decoding graph, and the current part within the stage p_s for the stages that require more than one cycle to be processed. All control signals and memory addresses are generated based on (i, s, p_s) . The maximum LL bit-width, denoted by Q_{max} , determines the width of the PEs. Using the LL quantization scheme described previously, we have $Q_{\text{max}} = Q_{ch} + \log N$. The PEs implement both (5) and (6). An additional input is used to choose between the f and g outputs. Due to the choice of quantization scheme, no overflow checks are needed. The MCU contains L L-to-1 multiplexers, which are controlled by

C. State-Memory

SC decoding can be implemented by storing 2N LL pairs [3], requiring a total of 4N data words. The N first pairs that correspond to the channel LLs are never overwritten during SC decoding. Thus, only one copy of the channel LL memory is needed, from which all decoder cores can read. The remaining N memory position pairs have to be distinct for each path. The number of required memory position pairs is (L + 1)N and the total number of bits used for LL storage is

$$B_{\rm LL} = 2\left(NQ_{ch} + L\sum_{i=0}^{\log N-1} 2^i \left(Q_{ch} + \log N - i\right)\right)$$
(9)

$$= (2L+2)NQ_{ch} + 2L(2N - \log N - Q_{ch} - 2).$$
(10)

There are L partial sum and L path memories, with N memory positions of 1 bit each, resulting in a total of 2LN bits. The architecture of the partial sum memories is identical to the one used in [3]. In order to complete the state copying step in a single cycle, all the contents of each of the L partial sum memories can be copied to and from one another by means of crossbars, as illustrated in Fig. 5. The same holds for the path memories. So, the number of bits per MCU state is

$$B_{\text{tot}} = (2L+2)NQ_{ch} + 2L(3N - \log N - Q_{ch} - 2).$$
(11)

D. Path Selection

1) Metric Sorter: For the path selection step, the 2L metrics are sorted in a single cycle. To minimize the delay, a radix-2L sorter was implemented by extending the architecture presented in [11] to support finding of the L smallest values, instead of only the 2 smallest values. This sorter requires 2L(2L-1)/2 comparators of Q_{max} -bit quantities. Since a single sorter is needed, minimizing its size is not critical. In fact, the metric sorter occupies only 0.1% and 0.8% of the total decoder area for L = 2 and L = 4, respectively. A register is added between the output of the MCU and the metric sorter in order to reduce the length of the critical path. Unfortunately, decoding can not proceed before the choice of paths is made, so an idle cycle is introduced every time the output of the metric sorter is needed. This happens RN times per codeword. Thus, by modifying the expression found in [6], the number of cycles required to decode one codeword is

$$C_{\text{list}} = (2+R)N + \frac{N}{P}\log\frac{N}{4P}.$$
 (12)

If we ignore the second term, which is small, then the overhead with respect to the case where we do not add a register is approximately RN cycles, or $\frac{RN}{2N} = 50R$ percent. Nevertheless, adding the register leads to a higher throughput due to a higher clock frequency. The architecture of the metric sorter is presented in Fig. 5(b).

TABLE I: Synthesis results and comparison.

	Proposed Architecture		[3]	[6]
Algorithm	List SC		SC	SC
Code Length	N = 1024		N = 1024	N = 1024
List Size	L = 2	L = 4	n/a	n/a
Cell Area	1.60 mm^2	3.53 mm^2	0.31 mm^2	$1.71 { m mm}^2$
Scaled to 65 nm	0.84 mm^2	1.85 mm^2	0.31 mm^2	0.22 mm^2
Clock Freq.	459 MHz^1	314 MHz ¹	500 MHz	150 MHz
Throughput	181 Mbps	124 Mbps	246 Mbps	49 Mbps
Technology	UMC 90 nm		TSMC 65 nm	180 nm

¹ We used the typical timing model at 25°C and 1V supply voltage.

2) Pointer Memory: The pointer memory contains $L \times (\log N - 1)$ elements. Each element can take on L distinct values, so we need $\lceil \log L \rceil$ bits for the representation. In total, the pointer memory contains $L \lceil \log L \rceil (\log N - 1)$ bits. For example, for L = 2, 4 and N = 1024, this translates to 18 and 72 bits, respectively, which is negligible. This memory also has the copying functionality that the partial sum and path memories provide. The architecture of the pointer memory is presented in Fig. 5(b).

V. SYNTHESIS RESULTS & CONCLUSION

Synthesis results for N = 1024 and L = 2, 4 using a UMC 90nm CMOS technology are shown in Table I. Since there exist no other list SC decoder architectures in the literature, we try to quantify the additional hardware complexity that is required to reap the decoding gain benefits of list SC decoder synthesis results of [3] and the chip results of [6].

In this work, the first list SC decoder architecture in the literature was presented. It was also described how to avoid copying of the intermediate likelihoods by copying between pointers instead of the actual values.

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