## A Memcomputing Pascaline

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The original Pascaline was a mechanical calculator able to sum and subtract integers. It encodes information in the angles of mechanical wheels and through a set of gears, and aided by gravity, could perform the calculations. Here, we show that such a concept can be realized in electronics using memory elements such as memristive systems. By using memristive emulators we have demonstrated experimentally the memcomputing version of the mechanical Pascaline, capable of processing and storing the numerical results in the multiple levels of each memristive element. Our result is the first experimental demonstration of multidigit arithmetics with multi-level memory devices that further emphasizes the versatility and potential of memristive systems for future massively-parallel high-density computing architectures.

The Pascaline, built by the mathematician Blaise Pascal, is one of the first known mechanical

calculators to perform the basic arithmetic operations  $*^{1}$  that has been produced on a "large scale" for its times. The machine, whose picture is shown in Fig. 1a, uses gears and wheels and is aided by gravity to transfer the carry of the addition <sup>2</sup>. It encodes ten digits in certain positions (rotation angles) of the wheels (one wheel for each power of the base-ten system), so we could call it a *multi-state machine* in the sense that each of the memory elements (wheels) encodes more than two values of information. In addition, the results of the computation are stored directly in the states (angles) of the wheels themselves, enabling the user to read out the result of the computation without any additional device. Although the commercial success of the Pascaline was limited, it is considered an important step in the development of computing machines.

The Pascaline is of course far less powerful than our present digital computers. However, these latter ones typically store one bit of information per memory cell, namely our present digital machines are *two-state* (binary) machines. In addition, our present computers employ a different unit, other than the memory, to actually perform the computation, thus requiring constant communication between the memory and this computing unit. It is thus tempting to employ the multi-state and computing-in-memory features of the Pascaline in future computing architectures. Indeed, multi-state memory would allow an increased information storage on a single element, and if the results of arithmetic operations on these multiple states could be stored directly in the memory itself (like for the Pascaline), there would be no need to transfer information from the physical location where it is computed to where it is stored (at present, this represents an important

<sup>\*</sup>Practically only addition, since subtraction was performed using the method of nine's complements, multiplication as repeated subtraction.

bottleneck in our digital computers <sup>3</sup>).

For the above reasons, the concept of using memory to process information (*memcomputing*<sup>4</sup>) is now receiving increased attention. Its foundations are supported by the mathematical notion of a Universal Memcomputing Machine<sup>5</sup> – an alternative computing paradigm to the Turing Machine – which shows substantial advantages when realized in hardware. Memory elements that store multiple levels of information can be fabricated either using active devices (e.g., transistors) or passive ones. The passive ones, in particular, hold the advantage that they require much less power to perform computation than active elements <sup>6–9</sup> and can be realized with a variety of materials and systems down to nanoscale dimensions <sup>7,10</sup>.

In this paper, we will demonstrate experimentally a memcomputing machine that works like the Pascaline. We will use emulators of memristive elements (resistors with memory) we have introduced previously<sup>11,12</sup> to build such a device. We will show that it is capable of addition and subtraction directly in memory. We choose to work in base-10 but our machine can easily work in any base.

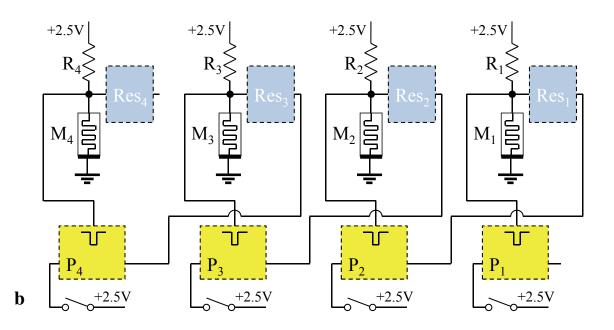
We should note that multi-bit information processing and storage with memristive devices has been demonstrated in several experiments <sup>9,13–17</sup>, and indeed multi-bit arithmetics with memristive devices has already been considered in the literature, but in a considerably simpler architecture than what we show in this work. For instance, in Ref. 15 Wright *et. al.* demonstrated a single digit base-10 arithmetics with phase-change materials. The authors of Ref. 17 reported a "memristive abacus" based on synaptic Ag-Ge-Se devices that can calculate decimal fractions. All this previous

work is limited to single-digit operations that are certainly not enough for any practical purpose.

The experimentally built memristive Pascaline (see Fig. 1b) consists of four identical blocks responsible for four different digits of a number. The blocks are coupled to each other in series so as to carry over. Each block consists of a memristor  $M_i$  connected in series with a resistor  $R_i$  to +2.5 V, a reset circuit Res<sub>i</sub>, displayed in detail in Fig. 2a, and a pulse generator  $P_i$  (here, i = 1, 2, 3, 4). The digit value is stored in the state of the memristor and represented by the voltage across the memristor in the absence of programming and reset pulses. The memristors are connected in such a way that negative programming pulses from  $P_i$  increase their memristors implemented with memristor emulators <sup>11,18</sup> (see Fig. 2b). The memristor model <sup>11</sup> parameters are  $\alpha = 0$ ,  $\beta = 62$  k $\Omega/V$ ·s,  $V_T = 1.2$  V,  $R_{min} = 1$  k $\Omega$ ,  $R_{max} = 10$  k $\Omega$ . Figure 2c presents experimentally measured pinched hysteresis loops of a single memristor connected to an AC voltage source. The frequency behavior of these loops is typical for memristive devices <sup>19</sup>. The memristive Pascaline is powered by a 5V voltage source and employs 2.5V as a virtual ground. The outputs of pulse generators  $P_i$  in Fig. 1c take -2.5 V during the pulse, and are otherwise in a non-connected state.

The reset circuit Res (Fig. 2a) compares the voltage across the memristor  $V_M$  with a threshold voltage  $V_t$  (applied to the 'minus' terminal of A<sub>1</sub>) and generates a positive (+2.5 V) reset pulse as soon as the voltage on the memristor exceeds  $V_t$ . The reset pulse width is defined by  $R_{R,2}C_1$ time constant (see Fig. 2a) that needs to be sufficiently long to set the memristor into its  $R_{min}$ state. This pulse is also used for carry over: as it can be seen from Figure 1b, the output of Res<sub>i</sub> is



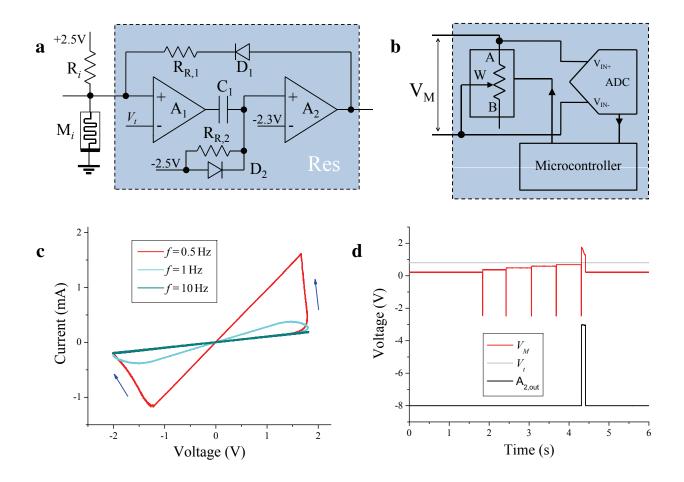


**Figure** 1: **Pascaline machines: from past to present. a.** Mechanical Pascaline (machine de la Reine Christine de Suède, 1652) exhibited in the Musée des Arts et Métiers (Paris). **b.** Memcomputing Pascaline. Pulse generators  $P_1$ - $P_4$  (at the bottom) are triggered by push in buttons or carry pulses from Res circuits. The outputs of  $P_1$ - $P_4$  (top terminals) provide negative voltage pulses increasing memristances of  $M_1$ - $M_4$  in steps. Reset circuits Res<sub>1</sub>-Res<sub>4</sub> are used to reset memristors when their memristances exceed a threshold (at the same time generating the carry pulse).

connected to the input of  $P_{i+1}$ .

The present Pascaline architecture supports different number bases, which are defined by the length of the memristor programming pulses (from pulse generators  $P_i$ ) and thresholds of reset circuits  $V_t$ . For example, using 10 ms programming pulse width, we have obtained a base-5 operation, as demonstrated in Figure 2**d**. The size of the base can be programmed by tuning the pulse width. For instance, the memristor device emulated here, allows a maximum base size determined by  $\lceil (R_{max} - R_{min})/(\beta\Delta\tau\Delta V) \rceil$ ,  $\Delta\tau$  being the pulse width,  $\Delta V$  the difference between the pulse amplitude and the threshold voltage,  $V_T$ , and  $\lceil \rceil$  denotes the ceiling value. A memristive analog of a French monetary (nondecimal) Pascaline could be realized by programming pulse widths for each digit or selecting different values of  $V_t$ , that, according to the reset circuit configuration in Figure 2**a**, introduces additional constraints to the size of the base.

Finally, addition and subtraction with the memcomputing Pascaline is presented in Figure 3. The decimal operation regime has been obtained using 6 ms wide programming pulses. The voltage thresholds, indicated by the digital readouts in Figs. 3 (a) and 3 (b), are determined by the internal parameters of memristors. In the case of the selected device used for emulating the Pascaline, the resistance levels linearly depend on time and pulse amplitude. As an example of addition, we show that 1642 (the year when the first mechanical calculator was built) plus 373 equals 2015. The subtraction is implemented using nine's complements (the same method is used with the mechanical Pascaline). So, in order to subtract 373 from 2015, we add 373 to the nine's complement of 2015 - 7984 – and find the nine's complement of the addition result (8357) – 1642



**Figure** 2: **Building blocks of the memristive Pascaline. a.** Schematics of the reset circuit Res<sub>i</sub> connected to a memristor.  $R_i = R_{R,2} = 10 \text{ k}\Omega$ ,  $R_{R,1} = 470 \Omega$ ,  $C_1 = 10 \mu$ F,  $A_{1(2)}$  are MCP6542 comparators (Microchip), D<sub>1</sub> is a common silicon diode, D<sub>2</sub> is a low forward voltage germanium diode, and  $V_t$  is approximately 0.8 V. **b.** Schematics of the memristor emulator. The microcontroller continuously updates the resistance of digital potentiometer according to a preprogrammed equation. The applied voltage is measured by the analog-to-digital converter (ADC). **c.** Measured I - V curves of memristor driven by an AC voltage source. **d.** Response of the circuit shown in **a** to a train of -2.5 V amplitude, 10 ms width pulses applied to the top terminal of M<sub>1</sub>. Under these conditions, the circuit implements base-5 arithmetics (note that the memristor resets by the fifth pulse).  $V_M$  is the voltage on the memristor,  $V_t$  is the threshold voltage,  $A_{2,out}$  is the 7 output voltage of the op-amp 2 in **a**.

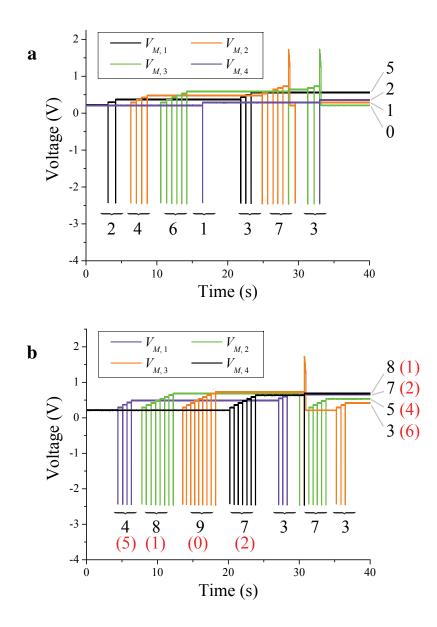


Figure 3: Base-10 addition and subtraction with the memcomputing Pascaline. a. Addition: 1642+373 = 2015. b. Subtraction (implemented using nine's complements): 2015-373 = 1642. The complements of the first input number and output number are shown in parentheses.  $V_{M,i}$  are the voltages on each of the four memristors.

-, which is the answer to the subtraction problem.

In summary, we have demonstrated a memcomputing Pascaline that is able to add and subtract using the multiple levels of memory elements (memristors in the present case). Even though we have used emulators of memristors, this machine can be fabricated with actual nano-scale devices and operate also with memcapacitors or meminductors <sup>6</sup>, albeit in a slightly different architecture, potentially offering lower energy consumption. The machine can support any type of numerical base, and is the first experimental demonstration of multi-digit arithmetics with multilevel memory devices, an important step forward for future massively-parallel and high-density computing architectures.

- Pascal, B. Lettre dédicatoire à Monseigneur le Chancelier sur le sujet de la Machine nouvellement inventée par le sieur B. P. pour faire toutes sortes d'opérations d'arithmétique par un mouvement réglé sans plume ni jetons, Avec un avis nécessaire à ceux qui auront curiosité de voir ladite Machine et s'en servir. Suivi du Privilège du Roy. (1645).
- 2. Œuvres de Pascal (La Haye, 1779).
- 3. Backus, J. Can programming be liberated from the von neumann style? a functional style and its algebra of programs. *Comm. Assoc. Comp. Machin.* **21**, 613–641 (1978).
- 4. Di Ventra, M. & Pershin, Y. V. The parallel approach. Nature Physics 9, 200 (2013).
- 5. Traversa, F. & Di Ventra, M. Universal memcomputing machines. *IEEE Trans. Neur. Netw. Learn. Syst. (in press)* (2015).

- Di Ventra, M., Pershin, Y. V. & Chua, L. O. Circuit elements with memory: Memristors, memcapacitors, and meminductors. *Proc. IEEE* 97, 1717–1724 (2009).
- Pershin, Y. V. & Di Ventra, M. Memory effects in complex materials and nanoscale systems. *Advances in Physics* 60, 145–227 (2011).
- Chu, H.-L. *et al.* Programmable redox state of the nickel ion chain in dna. *Nano Letters* 14, 1026–1031 (2014).
- OKelly, C., Fairfield, J. A. & Boland, J. J. A single nanoscale junction with programmable multilevel memory. ACS Nano 8, 11724–11729 (2014).
- Di Ventra, M. & Pershin, Y. V. Memory materials: a unifying description. *Materials Today* 14, 584 (2011).
- 11. Pershin, Y. V. & Di Ventra, M. Practical approach to programmable analog circuits with memristors. *IEEE Trans. Circ. Syst. I* 57, 1857 (2010).
- 12. Pershin, Y. V. & Di Ventra, M. Experimental demonstration of associative memory with memristive neural networks. *Neural Networks* **23**, 881 (2010).
- Nian, Y. B., Strozier, J., Wu, N. J., Chen, X. & Ignatiev, A. Evidence for an oxygen diffusion model for the electric pulse induced resistance change effect in transition-metal oxides. *Phys. Rev. Lett.* 98, 146403 (2007).
- Driscoll, T., Kim, H.-T., Chae, B. G., Di Ventra, M. & Basov, D. N. Phase-transition driven memristive system. *Appl. Phys. Lett.* 95, 043503–1–043503–3 (2009).

- 15. Wright, C. D., Liu, Y., Kohary, K. I., Aziz, M. M. & Hicken, R. J. Arithmetic and biologicallyinspired computing using phase-change materials. *Adv. Mater.* **23**, 3408 (2011).
- 16. Kim, K.-H. *et al.* A functional hybrid memristor crossbar-array/cmos system for data storage and neuromorphic applications. *Nano Letters* **12**, 389–395 (2012).
- 17. Xu, H. *et al.* The chemically driven phase transformation in a memristive abacus capable of calculating decimal fractions. *Sci. Rep.* **3**, 1230 (2013).
- Driscoll, T., Pershin, Y. V., Basov, D. N. & Di Ventra, M. Chaotic memristor. *Applied Physics A (in press)* (2010).
- Chua, L. O. & Kang, S. M. Memristive devices and systems. *Proceedings of IEEE* 64, 209–223 (1976).

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**Competing Interests** The authors declare that they have no competing financial interests.

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