# A Demonstration of Implication Logic Based on Volatile (Diffusive) Memristors

Yuriy V. Pershin, Senior Member, IEEE

Abstract—Implication logic gates that are based on volatile memristors are demonstrated experimentally with the use of relay-based volatile memristor emulators of an original design. The fabricated logic circuit involves two volatile memristors and it is capable of performing four fundamental logic functions (two types of material implication and the negations thereof). Moreover, current-voltage characteristics of individual emulators are recorded and self-sustained oscillations in a resistor-volatile memristor circuit are found. The developed emulator offers a great potential for memristive circuit experiments because of its simplicity, similarity of response with volatile memristors, and low cost. Our findings, which are based on emulators, can easily be reproduced with physical volatile memristors and, thus, open up possibilities for emerging in-memory computing architectures.

Index Terms—memristors, logic gates, threshold voltage, inmemory computing

#### I. INTRODUCTION

**D** URING the past decade, memristor technology has experienced an explosive growth, which has the potential to revolutionise information processing and storage. The key advantage of memristors [1], [2] (as well as memcapacitors and meminductors [3]) over the traditional electronic components is the possibility to store and process information on the same physical location. Memristive behavior has been observed in many systems and devices [4]. Up to now, however, most attention has been focused on devices with non-volatile storage capability [5]. The future applications of non-traditional memristors are still not fully understood, and their theoretical and circuit-level models are still at an early stage of development.

The present paper explores an in-memory computing application of volatile memristors, namely, memristors capable of storing information only when connected to a power source. Specifically, we will limit ourselves to devices exhibiting two possible resistance states (ON and OFF states) in a finite range of voltages and switching to the OFF state when a smaller voltage is applied. Several physical systems satisfy these requirements, including NEMS switches [6], [7], Mott memristors [8], graphene field emitters [9], and diffusive memristors [10]. The last system has recently attracted attention because of its promising characteristics for the use in artificial neural networks [10], random signal generators [11], and sensing applications [12]. Physically, in such diffusive memristors Ag atoms spread under electrical bias and regroup spontaneously under zero/small bias because of interfacial energy minimization [10], [11]. Moreover, it was shown that two Mott memristors can be used to build a neuristor [13], which is an electronic analog of the Hodgkin-Huxley axon. In what follows we will keep our discussion general, without referring to any particular physical realisation of volatile memristors. In our electronic circuit experiments, the volatile memristors are represented by emulators built out of conventional electronics components (resistors and relays). The volatile memristor emulator is developed as a part of the present work.

This paper experimentally demonstrates the implication logic [14] gates based on volatile memristors. Previously, in-memory logic gates were realised experimentally by employing bipolar non-volatile memristors [14], and explored theoretically based on bipolar non-volatile memristors (see, e.g., [15], [16], [17], [18], [19]), unipolar non-volatile memristors [20], [21], memcapacitors [22], [23], and volatile memristors (graphene field emitters [24]). The advantage of using memory devices in logic circuits is that they can serve simultaneously as a gate and latch. Here, we employ volatile memristors to create a polymorphic implication logic circuit and we demonstrate four kinds of fundamental logic gates using the same circuit. To the best of our knowledge, this is the first experimental realisation of implication logic gates based on volatile memristors. Moreover, the response of individual emulators is explored. It is found that a simple resistor-volatile memristor circuit can exhibit self-sustained oscillations with a pattern involving both regular and random components.

The rest of this paper is organised as follows. Section II-A introduces the relay-based emulator of volatile memristors and provides details on its specific realisation and response. Self-sustained oscillations in the resistor-volatile memristor circuit are briefly considered in Section II-B. Section III presents the implication logic gates based on volatile memristors. One of our main results is the experimental demonstration of four fundamental logic functions using the same circuit, which is contained in Section III. Our concluding remarks are given in Section IV.

# II. VOLATILE MEMRISTOR EMULATOR

## A. Emulator

Memristor emulators [25] are valuable tools for circuit prototyping when physical memristors are not accessible. A number of emulator designs are available in the literature based either on analog [26], [27], [28] or digital [29], [30] techniques. With rare exceptions [31], [32], a common feature of memristor emulators is the need for an external power

Y. V. Pershin is with the Department of Physics and Astronomy, University of South Carolina, Columbia, SC 29208 USA (e-mail: pershin@physics.sc.edu).

Manuscript received June ..., 2018; revised ....

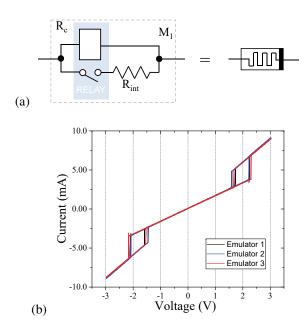


Fig. 1. (a) Schematics of volatile memristor emulator. An effective twoterminal volatile memristive system is formed by connecting the relay coil in parallel with series-connected resistor and reed switch. (b) Current-voltage characteristics of three physically different emulators with  $R_{int} = 680 \ \Omega$ .

source. Here, we show that the volatile memristors can be emulated in a very simple way and at low cost. The proposed emulator operates without an external power source and it demonstrates a high similarity to the response of volatile memristors.

Fig. 1(a) shows the emulator schematics. The volatile memristor emulator consists of a reed relay and resistor, forming an effective two-terminal memristive system. At lower applied voltages, the reed switch is open. In this case, the emulator resistance equals the coil resistance  $R_{OFF} = R_c$ . Meanwhile, at higher applied voltages, the switch is closed and the total resistance is  $R_{ON} = R_c R_{int}/(R_c + R_{int})$ . The interval between the pull-in and drop-out voltages of relay is the bistability (memory) region.

Three identical volatile memristor emulators were created and their current-voltage characteristics were measured. In the present experiments, reed relays with the coil resistance of  $R_c = 600 \ \Omega$  and nominal operating voltage of 5 V are employed (part number HI05-1A66, Standex-Meder Electronics). Fig. 1(b) shows that the current-voltage characteristics of different emulators are very close to each other. According to Fig. 1(b), at positive voltages, the OFF to ON transition occurs at  $V_{th} \approx 2.2$  V, while the ON to OFF transition takes place at  $V_{hold} \approx 1.6$  V. Moreover, the hysteresis region in the negative domain is slightly shifted to lower voltage amplitudes, which is likely due to an asymmetry in the reed switch response with respect to the magnetic field direction.

In addition, mention should be made of the inductive effects originating from the relay coil. The relay coil can be represented by a resistor and inductor connected in series and described by the impedance of the form  $Z = \sqrt{R_{int}^2 + (\omega L)^2}$ , where  $\omega$  is the angular frequency of input and L is the coil inductance. It follows from this expression that the resistive

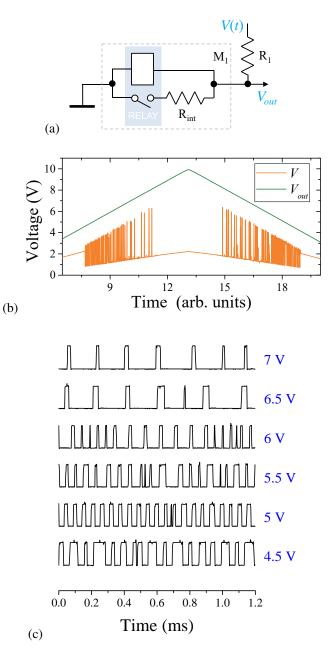


Fig. 2. (a) Resistor-volatile memristor circuit. (b) Applied and output voltages as functions of time in the resistor-volatile memristor circuit with  $R_{int} = 220 \ \Omega$  and  $R_1 = 680 \ \Omega$ . (c) Digitised  $V_{out}$  measured at the output of a comparator at several constant values of the applied voltage V (indicated on the plot). The curves are shifted for clarity.

response is dominant at lower frequencies and transforms into an inductive response at higher frequencies. The transition frequency  $\nu_t$  can be estimated from the condition of equal contributions of the resistive and inductive components to the impedance, namely:  $R_{int} = 2\pi\nu_t L$ . In the present realisation of the emulator, the coil inductance L = 0.17 H leads to  $\nu_t = 560$  Hz. The inductive effects should be considered when designing circuits with relay-based emulators operating at higher frequencies.

# B. Resistor-volatile Memristor Circuit

To better understand the emulator behavior in electronic circuits, consider a circuit of series-connected resistor and memristor subjected to an applied voltage V(t) (see Fig. 2(a)). An interesting (and potentially useful) feature of this circuit is the possibility of self-sustained memristance (memory resistance [2]) oscillations. These oscillations are clearly seen in Fig. 2(b) showing the response of resistor-volatile memristor circuit to the applied voltage of sawtooth wave form. Technically speaking, the oscillations occur at such applied voltages when in the  $R_{ON}$  state of memristor  $V_M > V_{th}$  and in the  $R_{OFF}$  state  $V_M < V_{hold}$ . Under these conditions, the memristor will continuously switch back and forth between its low- and high-resistance states. In fact, the same oscillation mechanism works in systems with negative differential resistance.

To derive the necessary condition for the oscillations, consider the resistor-volatile memristor circuit at the onset of switching, namely: assuming that the voltage across  $M_1$  is  $V_M = V_{th}$  and  $R_M = R_{OFF}$ . In this case, the applied voltage  $\tilde{V}$  is given by

$$\tilde{V} = \frac{R_1 + R_{OFF}}{R_{OFF}} V_{th}.$$
(1)

The switching into  $R_{ON}$  drops  $V_M$  to

$$V'_M = \frac{R_{ON}}{R_1 + R_{ON}} \tilde{V}.$$
 (2)

If, after this switching,  $V'_M < V_{hold}$  then the memristor will switch back into the  $R_{OFF}$  state, and so on. In other words, the resistor-volatile memristor circuit will exhibit self-sustained oscillations. By combining the inequality  $V'_M < V_{hold}$  with Eqs. (1), (2) one finds

$$\frac{R_{ON}(R_1 + R_{OFF})}{R_{OFF}(R_1 + R_{ON})} V_{th} < V_{hold},$$
(3)

which is the necessary condition for the existence of circuit instability. Clearly, the circuit is stable in the limit of  $R_{ON} \rightarrow R_{OFF}$  (note that  $V_{th} > V_{hold}$ ) and unstable at some smaller values of  $R_{ON}$ .

In the measurements, the signal from the resistor-volatile memristor circuit was transformed to the standard 0 V-(+5 V) logic levels using a comparator with the threshold voltage set at about 2.5 V. Fig. 2(c) presents examples of comparator output for several constant values of the applied voltage V. This plot demonstrates that both the frequency and probability of logic "1" in the output signal depend on V. The output signal contains the regular (most clearly seen at V = 5 V curve) and random components, as well as a combination of frequencies (V = 6 V curve). From the physics point of view, the random component can be associated with probabilistic sticking/unsticking of relay reeds and/or their complex dynamics under Fig. 2(a) circuit conditions.

# **III. IMPLICATION LOGIC GATES**

The implication logic circuit that is considered in this work is slightly different from the circuit based on non-volatile memristors [14]. Modifications are needed to ensure that the

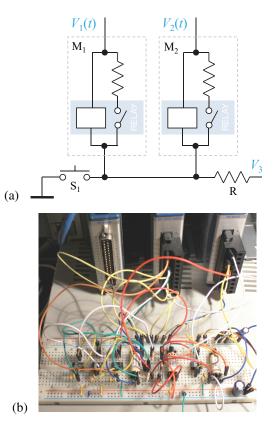


Fig. 3. (a) Implication logic circuit. In the present measurements, the switch  $S_1$  is implemented by a relay. (b) Photograph of experimental setup. Two memristor emulators are located in the center, while the switch  $S_1$  is to the right. Operational amplifiers are used as buffers.

volatile memristors stay in their bistable (hysteresis) regions between the operations. The selected circuit design and its experimental realization are presented in Fig. 3. In particular, Fig. 3(a) shows a circuit comprising two volatile memristors, resistor, and switch. Three voltage sources are used to drive the circuit. It is convenient to split the calculation sequence into three phases: initialisation, hold, and calculation. The switch is closed in the initialisation and hold phases, and it is opened within the calculation phase to induce a gate operation.

To store the information,  $S_1$  is kept closed and  $V_0 = 1.9$  V is applied to  $M_1$  and  $M_2$  ( $V_1 = V_2 = V_0$ ). To initialise the memristor state, 0 V or 5 V is applied to a given memristor. The calculation is performed from the hold phase by changing  $V_1$  and  $V_2$  to desired values, setting  $V_3$ , opening and closing the switch (the calculation phase). The entire calculation sequence consists of the following steps: initialisation, hold, calculation, hold. Note that the calculation results are stored in the final states of memristors. The final states of the memristors were monitored using small resistors connected in series with memristors and measuring the voltage drops across these resistors. To eliminate the effect of self-sustained oscillations discussed in Sec. II-B (or at least to reduce it to some insignificant areas in the parameters space), emulators with relatively large  $R_{int} = 680 \ \Omega$  were used in combination with a smaller common resistor ( $R = 220 \ \Omega$ ).

Diagrams of logic operations are obtained following the approach introduced in Ref. [23]. For each pair of input

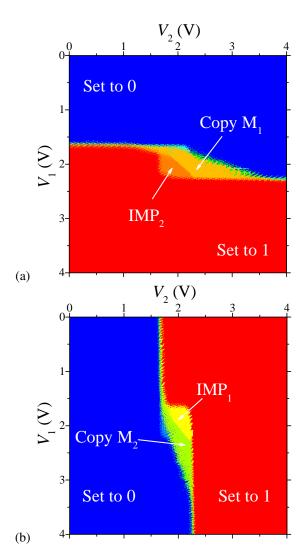


Fig. 4. Logic gate type as a function of voltage amplitudes  $V_1$  and  $V_2$  (in the calculation phase). Plot (a) shows the gate type related to the final state of M<sub>1</sub>. Plot (b) presents the gate type related to the final state of M<sub>2</sub>. The measurements were performed at  $V_3 = -1.9$  V. Here, IMP<sub>1</sub> denotes M<sub>1</sub>  $\rightarrow$ M<sub>2</sub>, and IMP<sub>2</sub> denotes M<sub>2</sub>  $\rightarrow$ M<sub>1</sub>.

combinations ((0,0), (0,1) (1,0), (1,1)), the final states of memristors are measured after applying the entire calculation sequence. The type of logic operation is identified using a code [23], [24] calculated based on the final states of memristors. The code is an integer number (from 0 to 15) that encodes the logic operation type and it is calculated as described in Ref. [23]. The code is translated to the logic operation type with the help of the table from Ref. [23]. Overall, our measurements confirm the possibility of logic operations previously predicted theoretically for the case of graphene autoemission memristors [24].

Fig. 4 presents measurement results based on Fig. 3 circuit taken at  $V_3 = -1.9$  V. The logic operation type is plotted as a function of  $V_1$  and  $V_2$  applied in the calculation phase. Fig. 4 indicates that two types of material implication,  $M_1 \rightarrow M_2$  and  $M_2 \rightarrow M_1$ , can be realised by Fig. 3 circuit at  $V_3 = -1.9$  V. Moreover, note that Fig. 4(a) and Fig. 4(b) can be transformed to each other under the flip across the  $V_1 = V_2$  diagonal and

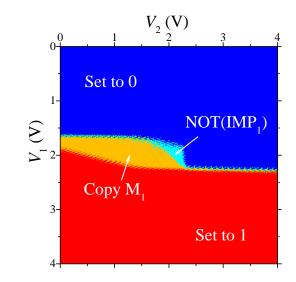


Fig. 5. Logic gate type as a function of voltage amplitudes  $V_1$  and  $V_2$ . This plot is generated based on the final result stored in M<sub>1</sub>. The measurements were performed at  $V_3 = -1.2$  V. Here, NOT(IMP) is the negation of implication.

interchange of indices 1 and 2 in the operation type (this property stems from the symmetric connections of  $M_1$  and  $M_2$  in the circuit).

The circuit functionality is changed when  $V_3$  is shifted to -1.2 V. The map of logic functions for this case is presented in Fig. 5 for the result stored in M<sub>1</sub>. Fig. 5 shows that there is a region of voltages in which the negation of implication NOT(IMP<sub>1</sub>) is realised. Symmetrically, under appropriate conditions, the final state of M<sub>2</sub> stores the result of another type of the negation of implication (NOT(IMP<sub>2</sub>)).

### IV. DISCUSSION AND CONCLUSION

In conclusion, the possibility of in-memory computing based on volatile (diffusive) memristors has been demonstrated. Using two volatile memristor emulators, the implication logic circuit was created and four kinds of fundamental logic gates were shown experimentally. This type of operation is fundamentally different from the case of traditional logic gates having a predetermined functionality. Specifically, in addition to the trivial operations (set to 1, set to 0 and copy the initial states), the following fundamental [33] logic gates have been demonstrated: IMP<sub>1</sub>, IMP<sub>2</sub>, NOT(IMP<sub>1</sub>), and NOT(IMP<sub>2</sub>). Moreover, self-sustained oscillations were measured in the resistor-volatile memristor circuit. It has been found that the voltage oscillations involve both regular and random components, which shows the potential application of the resistor-volatile memristor circuit in the area of random number generation.

The present work broadens the opportunities for exploiting volatile memristors for information processing and storage. Compared to the traditional implication logic circuits that are based on non-volatile memristors [14], volatile memristive circuits are slightly more complex because volatile devices require a power source to store information. We note that several non-idealities of real memristors such as the stochastic component in their dynamics [11] and variability of device parameters were not captured by our emulators. Such nonidealities (which do also exist in non-volatile memristors) must be considered when designing future in-memory computing circuits/systems.

The volatile memristor emulator that was introduced in this work offers a low cost and simple design alternative to physical memristors for the use in rapid memristive circuit prototyping. Conceptually, its operation principles can help to explain the operation of volatile memristors, as well as of circuits based thereof. It is anticipated that the volatile memristor emulators may also find use in undergraduate teaching laboratories to teach memristor technology and provide relevant hands-on experience.

#### ACKNOWLEDGEMENT

The author would like to thank V. A. Slipko for our useful discussions.

#### REFERENCES

- L. O. Chua, "Memristor the missing circuit element," *IEEE Transac*tions on Circuit Theory, vol. 18, pp. 507–519, 1971.
- [2] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proceedings of IEEE*, vol. 64, pp. 209–223, 1976.
- [3] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: Memristors, memcapacitors, and meminductors," *Proc. IEEE*, vol. 97, no. 10, pp. 1717–1724, 2009.
- [4] Y. V. Pershin and M. Di Ventra, "Memory effects in complex materials and nanoscale systems," *Advances in Physics*, vol. 60, pp. 145–227, 2011.
- [5] F. Pan, S. Gao, C. Chen, C. Song, and F. Zeng, "Recent progress in resistive random access memories: Materials, switching mechanisms, and performance," *Materials Science and Engineering: R: Reports*, vol. 83, pp. 1 – 59, 2014.
- [6] H. Nieminen, V. Ermolov, K. Nybergh, S. Silanto, and T. Ryhanen, "Microelectromechanical capacitors for rf applications," *J. Micromech. Microeng.*, vol. 12, p. 177, 2002.
- [7] J. Sun, M. E. Schmidt, M. Muruganathan, H. M. H. Chong, and H. Mizuta, "Large-scale nanoelectromechanical switches based on directly deposited nanocrystalline graphene on insulating substrates," *Nanoscale*, vol. 8, p. 6659, 2016.
- [8] M. D. Pickett, G. Medeiros-Ribeiro, and R. S. Williams, "A scalable neuristor built with Mott memristors," *Nature materials*, vol. 12, p. 114, 2013.
- [9] V. I. Kleshch, D. A. Bandurin, A. S. Orekhov, S. T. Purcell, and A. N. Obraztsov, "Edge field emission of large-area single layer graphene," *Appl. Surf. Sci.*, vol. 357, Part B, p. 1967, 2015.
- [10] Z. Wang, S. Joshi, S. E. Savelev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li *et al.*, "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," *Nature materials*, vol. 16, p. 101, 2017.
- [11] H. Jiang, D. Belkin, S. E. Savelev, S. Lin, Z. Wang, Y. Li, S. Joshi, R. Midya, C. Li, M. Rao *et al.*, "A novel true random number generator based on a stochastic diffusive memristor," *Nature communications*, vol. 8, p. 882, 2017.
- [12] J. H. Yoon, Z. Wang, K. M. Kim, H. Wu, V. Ravichandran, Q. Xia, C. S. Hwang, and J. J. Yang, "An artificial nociceptor based on a diffusive memristor," *Nature communications*, vol. 9, p. 417, 2018.
- [13] H. D. Crane, "The neuristor," *IRE Transactions On Electronic Computers*, vol. 9, p. 370, 1960.
- [14] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'Memristive' switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, pp. 873–876, 2010.
- [15] S. Shin, K. Kim, and S. M. Kang, "Memristive XOR for resistive multiplier," *Electronics Letters*, vol. 48, pp. 78–80, 2012.
- [16] S. Kvatinsky, D. Belousov, S. Liman, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MAGIC–memristor-aided logic," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 11, pp. 895–899, 2014.

- [17] G. Papandroulidakis, I. Vourkas, N. Vasileiadis, and G. C. Sirakoulis, "Boolean logic operations and computing circuits based on memristors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, pp. 972–976, 2014.
- [18] Y. Zhang, Y. Shen, X. Wang, and L. Cao, "A novel design for memristorbased logic switch and crossbar circuits," *IEEE Transactions on Circuits* and Systems I: Regular Papers, vol. 62, pp. 1402–1411, 2015.
- [19] L. Guckert and E. E. Swartzlander, "MAD gates-memristor logic design using driver circuitry," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, pp. 171–175, 2017.
- [20] X. Sun, G. Li, L. Ding, N. Yang, and W. Zhang, "Unipolar memristors enable stateful logic operations via material implication," *Appl. Phys. Letr.*, vol. 99, p. 072101, 2011.
- [21] E. Amrani, A. Drori, and S. Kvatinsky, "Logic design with unipolar memristors," in Very Large Scale Integration (VLSI-SoC), 2016 IFIP/IEEE International Conference on, 2016, pp. 1–5.
- [22] F. L. Traversa, F. Bonani, Y. V. Pershin, and M. D. Ventra, "Dynamic computing random access memory," *Nanotechnology*, vol. 25, p. 285201, 2014.
- [23] Y. V. Pershin, F. L. Traversa, and M. D. Ventra, "Memcomputing with membrane memcapacitive systems," *Nanotechnology*, vol. 26, p. 225201, 2015.
- [24] Y. V. Pershin and S. N. Shevchenko, "Computing with volatile memristors: an application of non-pinched hysteresis," *Nanotechnology*, vol. 28, p. 075204, 2017.
- [25] D. Biolek, "Memristor emulators," in *Memristor Networks*. Springer, 2014, pp. 487–503.
- [26] B. Muthuswamy, "Implementing memristor based chaotic circuits," Int. J. Bif. Chaos, vol. 20, pp. 1335–1350, 2010.
- [27] H. Kim, M. P. Sah, C. Yang, S. Cho, and L. O. Chua, "Memristor emulator for memristor circuit applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, no. 10, pp. 2422–2431, 2012.
- [28] D. Yu, H. H.-C. Iu, A. L. Fitch, and Y. Liang, "A Floating Memristor Emulator Based Relaxation Oscillator," *IEEE Trans. Circ. Sys. I*, vol. 61, no. 10, pp. 2888–2896, OCT 2014.
- [29] Y. V. Pershin and M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Networks*, vol. 23, p. 881, 2010.
- [30] Z. Kolka, D. Biolek, and V. Biolková, "Hybrid modelling and emulation of mem-systems," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 25, no. 3, pp. 216–225, 2012.
- [31] S. Asapu and Y. V. Pershin, "Electromechanical emulator of memristive systems and devices," *IEEE Transactions on Electron Devices*, vol. 62, p. 3678, 2015.
- [32] A. Ascoli, F. Corinto, and R. Tetzlaff, "A class of versatile circuits, made up of standard electrical components, are memristors," *International Journal of Circuit Theory and Applications*, vol. 44, pp. 127–146, 2016.
- [33] A. N. Whitehead and B. Russell, *Principia mathematica*. University Press, 1912, vol. 2.