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Systematic Synthesis of Step-Down Switched-Capacitor Power Converter Topologies

Dennis Øland Larsen, *Member, IEEE*, Martin Vinter, and Ivan Jørgensen, *Member, IEEE*,

Abstract—In this paper an algorithm for finding two-phase step-down switched-capacitor converter topologies is presented. The output stage is considered as a number of nodes, namely ground, input, output, and the top and bottom plates of the capacitors. Finding all switch placements between these nodes yields a complete database of possible topology implementations. The algorithm is applied for the case of one to four flying capacitors. This result is useful in the design of multi-topology gearbox output stages where several topologies are implemented. Having a database of all possible implementations allows for designing optimal output stages based on a number of possible performance metrics. All parts of the synthesis method is automated. In the case of four flying capacitors a total of 8.40 billion topologies are found.

Index Terms—dc-dc converter, switched capacitor converter, switched-mode power supply, topology synthesis

I. INTRODUCTION

SWITCHED-CAPACITOR converters (SCCs) rely on charging and discharging capacitors by periodically switching between a number of operating phases. The specific capacitor interconnection in the different phases, called a topology, gives rise to a certain ideal voltage conversion ratio M . The attainable values of M depend on the number of flying capacitors N_{cfly} . In [1] it was shown that given $k = N_{cfly} + 1$, M has the following bounds for two-phase converters (here disregarding negative conversion ratios):

$$M = \frac{1 \leq P \leq F_k}{1 \leq Q \leq F_k}, \quad (1)$$

where P and Q are integers and F_k is the k 'th Fibonacci number. This fraction limits both the voltage conversion ratio $VCR = V_{out}/V_{in} < M$ and the efficiency $\eta < VCR/M$. These two limitations call for using multi-topology output stages, also called gearboxes, in applications where the VCR varies across a wide range such as battery-powered applications [2]–[9], energy harvesting [10], and dynamic voltage scaling for multi-core processors [11]. Each gear, with an ideal voltage conversion ratio M , requires switches to implement a certain interconnection of the capacitors, and the combined multi-topology output stage consists of the union of the switches required for each topology. An unconnected output stages is depicted in Fig. 1.

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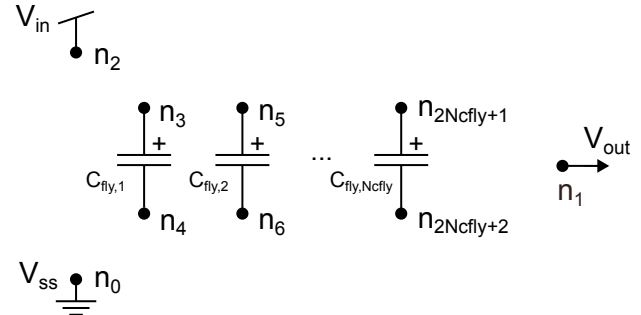


Fig. 1. An unconnected SCC output stage with each node named $n_0, n_1, \dots, n_m$. The objective of this work is to find all possible topology implementations by generating all valid switch combinations. An output filtering capacitor is connected to V_{out} but not shown.

The problem of synthesizing topologies with any M has been addressed in [12]–[16]. The prior art methods can be grouped in two. One is the synthesis based on canonical forms where a predefined switch structure is repeated for each flying capacitors [12], [13], [15], [16]. The other approach is the iterative algorithm in [14]. The first method, based on canonical forms, has the advantage of a fixed structure that is easily extended to a large number of flying capacitors. The second approach, the iterative algorithm, is more general as it does not assume a pre-defined switch placement. However, the rules for iteratively adding capacitors either in series with a terminal or parallel to the entire previous capacitor configuration excludes some topologies, such as the ladder converter, from being synthesized with this approach. An automated approach for synthesizing topologies that does not rely on a pre-defined interconnection structure or designer-input, such as assigning capacitor polarity by inspection [14], would allow for systematic design of both single-topology and gearbox output stages.

In this work we propose an algorithm for systematically finding all possible step-down topologies. The algorithm is applied to the cases of one to four flying capacitors. In the following, an overview of the method is given, followed by a description of each of its parts using a 1/3 with two flying capacitors as a vehicle for the method development. Finally, an example case of synthesizing a 1/8 converter is given and compared with prior art.

II. OVERVIEW OF PROPOSED SYNTHESIS METHOD

The presented method has three parts as described in the following:

- **Part A:** Capacitor interconnection generation

- A list of all possible switch placements is build
- **Part B:** Invalid interconnection removal
 - Invalid interconnections are removed based on a set of constraints using adjacency matrices
- **Part C:** Capacitor interconnection combination
 - All combinations of two capacitor interconnections from the list generated in Part A-B are tested
 - The combination of two capacitor interconnections is denoted a candidate topology
 - Each candidate topology is stored in the database if it implements a valid SCC circuit.

The following constraints are imposed in Part B to reduce the number of capacitor interconnections combinations to be tested in Part C: (i)

- 1) Capacitor voltages are positive: $V_{cfly,i} > 0$
- 2) Capacitor positive terminals are not connected to V_{ss}
- 3) Capacitor negative terminals are not connected to V_{in}
- 4) Only a single switch can connect two nodes

The solutions with $V_{cfly,i} < 0$ can be generated by reversing the capacitor terminals but in this study such solutions are considered redundant. Constraints (ii) and (iii) were imposed to avoid having nodes in the output stage with a voltage below V_{ss} or above V_{in} . For bulk CMOS implementations having a node $V_{n,i} < V_{ss}$ would forward-bias the body diode of any transistor connected to node n_i . Constraint (iv) were imposed to avoid parallel switches.

III. TOPOLOGY SYNTHESIS

A. Capacitor Interconnection Generation

A two-phase SCC topology is defined as two distinct interconnections of the flying capacitors and the three external terminals: V_{ss} , V_{out} , and V_{in} (see Fig. 1). In this section, all the capacitor interconnections that could potentially be part of a two-phase topology are found. A compact switch terminal assignment notation is adopted, which alleviates the algorithmic generation of all possible interconnections.

Each flying capacitor is considered to have a switch connected to its top and bottom node. The other terminal of each of these switches is connected to another node in the output stage. The case for $N_{cfly} = 2$ is shown in Fig. 2a. The next step is to choose where to connect the other terminal of each of the switches connected to the capacitor terminals. The valid nodes a switch can be connected to are listed in curly-braces next to each unconnected switch terminal in Fig. 2a. In the following we denote the switches as “the n_x switch” for the switch connected to the capacitor terminal node n_x (i.e. n_3 , n_4 , n_5 , or n_6). The n_3 switch (top left in Fig. 2a) can be connected to any of the nodes $\{n_1, n_2, n_5, n_6\}$. It cannot be connected to n_0 as this would make $V_{n4} < V_{ss}$ as $V_{cfly,1} > 0$, and n_3 and n_4 are excluded as this would either short $C_{fly,1}$, resulting in $V_{cfly,1} = 0$, or having both terminals of the switch connected to the same node.

The two capacitor interconnections used in a 1/3 topology are shown in Fig. 2b-c as an example. Under each capacitor interconnection is listed the interconnection list S_{ph} . The entries in this list are the node numbers of the nodes that

each of the switches are connected to. The first entry is the n_3 switch connection, followed by the n_4 switch connection and so forth. In summary, the list S_{ph} has the following entries for the case of $N_{cfly} = 2$:

$$S_{ph} = [X_{n3}, X_{n4}, X_{n5}, X_{n6}] \quad (2)$$

$$X_{n3} \in \{1, 2, 5, 6\}, \quad X_{n4} \in \{0, 1, 5, 6\}$$

$$X_{n5} \in \{1, 2, 3, 4\}, \quad X_{n6} \in \{0, 1, 3, 4\}$$

All capacitor interconnections can then be generated by choosing all combinations of these entries. The number of switch connections to make is equal to the number of capacitor terminals $2N_{cfly}$. Each switch can be connected to two of the three external nodes (V_{ss} , V_{out} , V_{in}), along with any of the capacitor terminals except the terminals of the capacitor that the switch is already connected to $2(N_{cfly} - 1) + 2 = 2N_{cfly}$. The total number of capacitor interconnections is therefore:

$$N_{ph} = (2N_{cfly})^{2N_{cfly}} \quad (3)$$

Any overlapping switches in the generated S_{ph} lists are removed. The case in Fig. 2b was e.g. generated as $S_{ph} = [2, 5, 4, 1]$ but as both the second and third entry represents a switch from n_4 to n_5 , the last entry is replaced with -1 representing “no switch” (see the switch crossed out in Fig. 2b).

B. Invalid Interconnection Removal

The outcome of this part is a number of capacitor interconnections lists N_{ph} . In Part C of the method, the total number of combinations to test is given by the binomial coefficient, i.e. every possible way of choosing two capacitor interconnections from the list of N_{ph} possibilities:

$$N_{\text{candidates}} = \binom{N_{ph}}{2} = \frac{N_{ph}!}{2!(N_{ph} - 2)!} = \frac{N_{ph}^2 - N_{ph}}{2} \quad (4)$$

This is potentially a very large number of combinations and it is therefore desirable to rule out as many capacitor interconnections as possible in Part B.

To systematically remove invalid capacitor interconnections, the output stage is considering as an undirected graph G having nodes $n_0, n_1, \dots, n_m$, where $m = 2N_{cfly} + 2$, and each switch representing an edge in G . The adjacency matrix is then a symmetric $(m+1) \times (m+1)$ matrix $\mathbf{A}_{adj}$ where each entry $a_{ij} = a_{ji} = 1$ if node n_i is connected to node n_j by a switch. All other entries are zero. For the capacitor interconnection in Fig. 2c, the adjacency matrix is:

$$\mathbf{A}_{adj,p2} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (5)$$

The first row of and column of $\mathbf{A}_{adj}$ represents the connections to and from n_0 (as it is an undirected graph). Similarly, the second row is connections to n_1 and so forth. From the

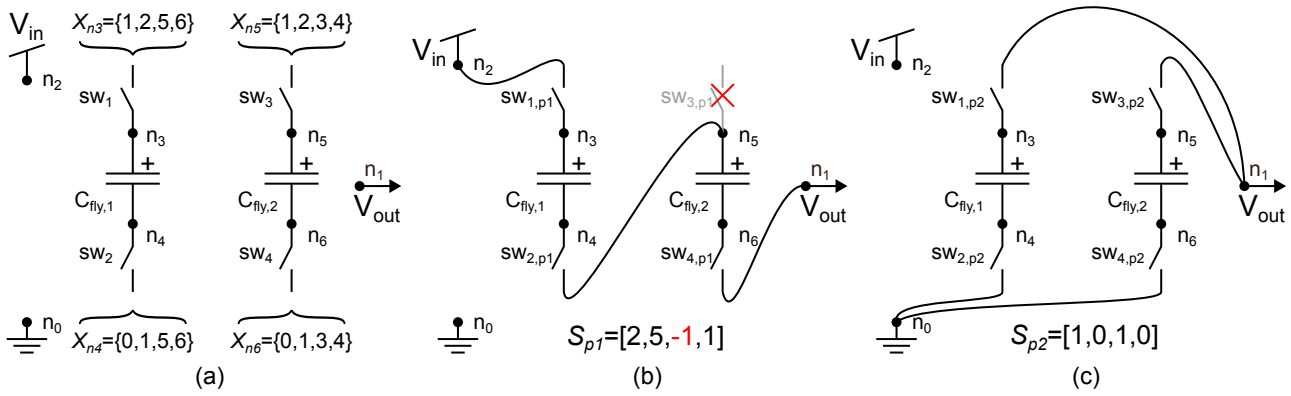


Fig. 2. Output stage with $N_{cfly} = 2$ with (a) a switch for each capacitor terminal showing the list of valid connections of each. An example capacitor interconnection for a 1/3 topology in (b) for phase 1 and in (c) for phase 2. Below each capacitor interconnection in (b) and (c) are the switch terminal assignment lists S_{p1} and S_{p2} .

first row and column in (5) we e.g. see that n_0 is connected to n_4 and n_6 , which agrees with Fig. 2c.

The powers of the adjacency matrix can be used to find walks between any nodes in the graph. It can be shown that the $(i, k)^{th}$ entry a_{ij}^k of $\mathbf{A}_{adj}^k$ represents the number of walks of length k starting and ending in n_i and n_j , respectively. Using this property, and the fact that only the switches and not capacitors are included as vertices in the graph, allows for detecting if there is any path through the capacitor interconnection that would short-circuit a capacitor, or e.g. connect a top plate to V_{ss} . A total of four checks are performed using adjacency matrices:

- Capacitor top plate to V_{ss} or bottom plate to V_{in}
- Anti-parallel capacitor connections (not allowed as $V_{cfly,i} > 0$)
- Both ends of a series connection of several capacitor being connected to the same node
- Loops containing only switches

In the case of $N_{cfly} = 4$, the above techniques reduce the number of capacitor interconnections from $N_{ph} = (2N_{cfly})^{2N_{cfly}} = 16777216$ to only $N_{ph} = 327436$. Using (4) this amounts to a reduction by a factor 2625 in the number of candidate topologies to check in the next step.

C. Phase combination

A candidate topology is valid if we can find a set of $N_{cfly} + 1$ independent Kirchhoff's voltage law (KVL) equations. This allows for solving for the flying capacitor voltages $V_{cfly,i}$, $i \in \{1, 2, \dots, N_{cfly}\}$ and output capacitor voltage V_{out} as a function of V_{in} . To obtain the KVL equations the approach from [17], [18] using node incidence matrices is employed.

The rows of the node incidence matrix $\mathbf{A}_{inc}$ represent the circuit nodes except V_{ss} (n_0), and each column constitutes the connection of each element in the circuit. The first column is the input, followed by the flying capacitors, the output, and the switches. We set $a_{ij} = 1$ of $\mathbf{A}_{inc}$ if the j^{th} element has its positive terminal connected to the i^{th} node. Conversely, $a_{ij} = -1$ if the negative terminal of the j^{th} element is connected to the i^{th} node. Finally, $a_{ij} = 0$ if the j^{th} element is not connected to the i^{th} node. The switches are chosen to

have the positive terminal connected to the capacitor terminal. We partition $\mathbf{A}_{inc}$ in a sub-matrix consisting of the input, capacitors and output, $\mathbf{A}_{inc,c}$, and another containing the switches $\mathbf{A}_{inc,r}$

$$\mathbf{A}_{inc} = [\mathbf{A}_{inc,c} \quad \mathbf{A}_{inc,r}]. \quad (6)$$

The capacitors are connected to the same nodes in each phase, i.e. the $\mathbf{A}_{inc,c}$ is equal for both phases. A different set of switches are active on each phase resulting in an $\mathbf{A}_{inc,r}$ matrix for each phase. For the capacitor interconnection in Fig. 2b, the following node incidence matrix is obtained:

$$\mathbf{A}_{inc,p1} = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 1 \end{bmatrix}, \quad (7)$$

where the first four columns are $\mathbf{A}_{inc,c}$ and the last three are $\mathbf{A}_{inc,r1}$ (one column for each switch). Referring to Fig. 2b we see that the first column shows that the input is connected to n_2 , the second column shows that $C_{fly,1}$ is connected to n_3 and n_4 , the third column that $C_{fly,2}$ is connected to n_5 and n_6 , and fourth column that the output is connected to n_1 .

For phase 2 of the example 1/3 topology (Fig. 2c) we have:

$$\mathbf{A}_{inc,p2} = \begin{bmatrix} 0 & 0 & 0 & 1 & -1 & 0 & -1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \quad (8)$$

Next, the KVL equations are found by obtaining a basis for the null space (kernel) of $\mathbf{A}_{inc,p1}$ and $\mathbf{A}_{inc,p2}$ [17], [18]. Practically, this is done by Gauss-Jordan elimination and possible columns re-ordering. The resulting KVL equations on matrix-form for the two phases are:

$$\text{KVL}_{ph1} = [-1 \quad 1 \quad 1 \quad 1 \quad -1 \quad 1 \quad 1] \mathbf{V}_{comp} = 0, \quad (9)$$

$$\text{KVL}_{ph2} = \begin{bmatrix} 0 & 1 & 0 & -1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & -1 & 1 \end{bmatrix} \mathbf{V}_{comp} = 0, \quad (10)$$

TABLE I
NUMBER OF VALID TOPOLOGIES

N_{cfly}	1	2	3	4
N_{topol}	2	542	1.12×10^6	8.40×10^9

where $\mathbf{V}_{comp}$ is the component voltage vector:

$$\mathbf{V}_{comp} = [V_{in} \ V_{cfly,1} \ V_{cfly,2} \ V_{out} \ V_{sw1,p1} \ \dots \ V_{swN,pN}]^T, \quad (11)$$

Writing e.g. (9) as an equation yields:

$$-V_{in} + V_{cfly,1} + V_{cfly,2} + V_{out} - V_{sw1,p1} + V_{sw2,p1} + V_{sw4,p1} = 0 \quad (12)$$

A valid SCC topology will have zero voltage-drop across the switches in the unloaded steady-state case. Furthermore, the capacitor voltages should be equal in each phase. A set of three KVL equations in four variables $[V_{in}, V_{cfly,1}, V_{cfly,2}, V_{out}]$ from the first four columns of (9) and (10) are then found:

$$\text{KVL}_c = \begin{bmatrix} -1 & 1 & 1 & 1 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & -1 \end{bmatrix} \quad (13)$$

The system of equations can be solved as a function of V_{in} by setting $V_{in} = 1$. The resulting system to solve is:

$$\begin{bmatrix} 0 & 0 & -3 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \end{bmatrix} \mathbf{V}_x + \begin{bmatrix} -1 \\ 0 \\ 0 \end{bmatrix} V_{in} = 0 \quad (14)$$

The solution to this is:

$$\mathbf{V}_x = [V_{cfly,1} \ V_{cfly,2} \ V_{out}]^T = [1/3 \ 1/3 \ 1/3]^T, \quad (15)$$

i.e. the capacitor voltages and V_{out} are all equal to a third of V_{in} as expected for the 1/3 topology in Fig. 2b-c. The above process of generating node incidence matrices, finding KVL equations from the null space, and solving the KVL equations as a function of V_{in} , is performed for all combinations of capacitor interconnections that were generated in Part A and B of the algorithm.

The number of entries in the result databases for one to four flying capacitors are listed in Table I.

IV. EXAMPLE: SYNTHESIS OF 1/8 TOPOLOGY

To show an example usage of the obtained database, a 1/8 topology is synthesized using four C_{fly} , and the results compared to the Fibonacci canonical form in [12]. To compare, we consider the sum of square charge flow vectors

$$K_{SSL} = \sum_{i=1}^{N_{cfly}} a_{c,i}^2, \quad K_{FSL} = 2 \sum_{i=1}^{N_{sw}} a_{r,i}^2, \quad (16)$$

and the maximum capacitor steady-state voltages. Using the canonical form, three possible implementations of the 1/8 topology is found. All three have the same charge flow vector sums:

$$K_{SSL,canon} = 0.234, \quad K_{FSL,canon} = 2.19 \quad (17)$$

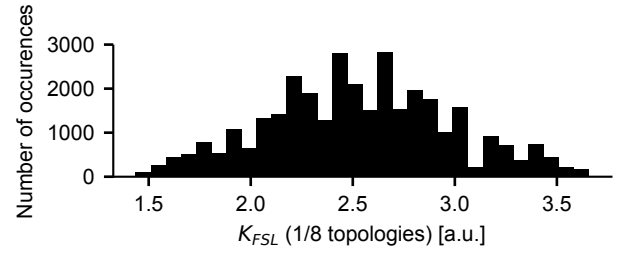


Fig. 3. Histogram of the sum of squared switch charge flow elements for 33 489 topologies having $M = 1/8$.

Of the three solutions, one has a maximum absolute capacitor voltage of $(5/8)V_{in}$, and the other two $(3/8)V_{in}$.

Next, the 33 489 topologies having $M = 1/8$ from the generated database are compared. They all have $K_{SSL} = 0.234$, i.e. that same as the canonical result. A histogram of the K_{FSL} values are shown in Fig. 3. A total of 108 topologies have the lowest $K_{FSL} = 1.44$, of which 52 have a maximum capacitor voltage of $(3/8)V_{in}$. An example of this has the following switch terminal assignments:

$$S_{p1} = [2, 9, 7, 0, 10, 1, -1, -1], \quad S_{p2} = [5, 0, 9, 1, 1, 0, -1, 0] \quad (18)$$

A steady state capacitor voltages $[3/8, 2/8, 1/8, 3/8] V_{in}$.

V. TOPOLOGY ANALYSIS

The previous section shows an example of how the automated synthesis of topologies can be used for designing a specific switched capacitor topology. The fast switching limit and slow switching limit metrics are based on the charge flow analysis and ideal transformer model from [19]. More detailed modeling of switched capacitor topologies using state space methods have also been presented. State space modeling is used in [20] for performance analysis, for controller design in [21], for a fully-integrated converter using deep trench capacitors in [3], in [22] a model was developed for complex topologies and verified experimentally, and in [18] and automated state model generator was presented. Finally, in the book chapter [23, Ch. 13] a comprehensive list of converter parameters for comparing topologies is given.

The presented method presented in this paper for synthesizing switched capacitor topologies and the corresponding database of topologies serves as the input for these analysis methods for comparing the performance of each topology based on the specific parameters of the devices available in the specific design case.

VI. CONCLUSION

An algorithm for finding all possible step-down converter topologies was developed. A total of 2, 542, 1.12 million, and 8.40 billion topologies was found for one to four flying capacitors. Knowing all ways an ideal voltage conversion ratio M can be implemented, allows for finding optimal designs by considering e.g. the maximum operating voltages of the switches and capacitors used in a design. As an example, a

1/8 topology was synthesized using four flying capacitors and compared with the Fibonacci canonical synthesis. A total of 33 489 implementations of the 1/8 topology was found, of which 52 had 34.2% lower sum of squared switch charge flow vector elements while other performance metrics were equal to the result of using the prior art synthesis method. The algorithm is best suited for a low number of flying capacitors due to the rapidly growing solution space.

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