An Adaptive-Resolution Quasi-Level-Crossing Delta Modulator With VCO-Based Residue Quantizer

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***Abstract*—This brief introduces an adaptive-resolution (AR) quasi-level-crossing delta modulator ADC with a voltage-controlled oscillator (VCO)-based residue quantizer for Internet-of-Things (IoT) wireless sensor nodes. The residue voltage signal is digitized by a VCO-based residue quantizer, thus leading to a straightforward implementation of level-crossing (LC) and AR algorithms in digital domain. The inherent and mismatch-induced dithering provided by the VCO-based residue quantizer increases the proposed modulator's dynamic range and average sampling rate for slowly-varying input signals, enabling accurate sampling and conversion. For fast-varying signals, the AR algorithm is adopted to reduce the average sampling rate by a factor of three compared to the straightforward LC algorithm at the edge of the modulator's signal bandwidth. Fabricated in 28-nm CMOS, the proposed modulator achieves a peak SNDR of 53 dB over a signal bandwidth of 1.78 MHz.**

***Index Terms*—Adaptive resolution (AR), ADC, compressed sensing, delta modulator, event-based signal processing, Internet-of-Things (IoT), level-crossing (LC), VCO-based quantizer.**

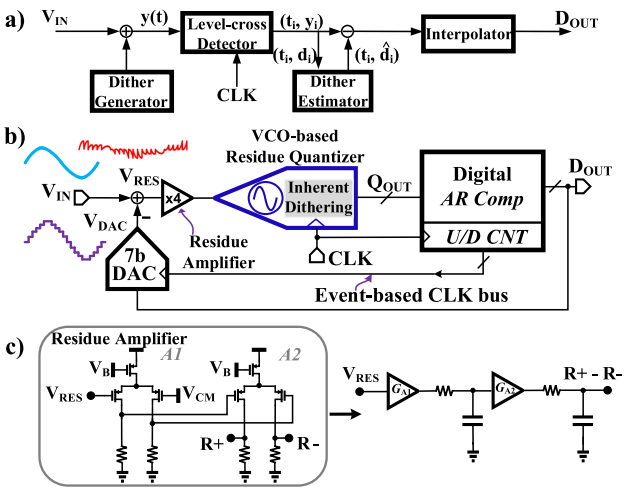

Fig. 1. (a) Dither applied to LC-ADC in [8]. (b) Proposed LC delta modulator topology as an improvement to [7], [10] and introducing a VCO-based residue quantizer. (c) Simplified schematic of residue amplifier and its corresponding linear model.

I. Introduction

IN IOT systems, the ever-increasing need for real-time environment monitoring leads to transmission, processing and storage of large volumes of data, entailing significant power consumption and hardware resources. Considering that most information in the physical environment exhibits sparsity in the time domain, compressed sensing can be applied to the sensors to reduce the average sampling rate [1].

Level-crossing sampling (LCS) is an attractive technique which can be employed in ADCs for compressed sensing applications—it samples and converts the input signal only when it crosses specific threshold levels [2]. Therefore, LC ADCs feature input-dependent sampling rate and power consumption. The two main topologies of LC ADCs, the delta-modulator-based [3], [4] and the flash-based [5], [6], commonly adopt continuous-time (CT) comparators as the threshold detectors, where large gain and bandwidth requirements must be imposed to reduce the variation in propagation delay [6]. However, it is difficult to implement high-gain and high-bandwidth CT comparators in low-voltage deep-nanoscale technology due to the low intrinsic gain of transistors, thus limiting the conventional LC ADCs' accuracy. Adaptive resolution (AR) LCS adjusts the threshold levels based on the slew rate of input signal, thus further reducing the average sampling rate. In [3], the AR algorithm is achieved through a time-varying comparison window, which results in a rather complex implementation.

In response, a *quasi*-level-crossing topology was proposed in [7] to digitize the residue voltage of the delta modulator with a 4-bit SAR sub-ADC, moving the LC and AR processing into the sampled digital domain, thus fully benefiting from the CMOS technology scaling. Moreover, the output of this quasi-evel-crossing ADC can directly interface to the discrete-time (DT) DSPs. Nonetheless, LC and quasi-level-crossing ADCs generally have limited dynamic range (DR) as signals with small amplitude variations do not cross any threshold levels and remain undetected [10]. Furthermore, sampling of slowly varying components of the input signal might not satisfy the Nyquist criterion. Such signals cannot be recovered by the downstream DSP due to the sub-Nyquist

Manuscript received November 12, 2019; revised February 10, 2020; accepted March 2, 2020. Date of publication March 6, 2020; date of current version November 24, 2020. This work was supported in part by the Science Foundation Ireland under Grant 14/RP/I2921, and in part by the Marie Sklodowska-Curie Actions under Grant 747585. This brief was recommended by Associate Editor L. A. B. G. Oliveira. *(Corresponding author: Hongying Wang.)*

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Digital Object Identifier 10.1109/TCSII.2020.2979078

sampling. In Fig. 1a, $y(t)$, consisting of the input signal $V_{\rm IN}$ and dithering, is injected into the flash-based LC ADCs to trigger the level-crossing events (t_i, y_i), and then the digitized dithering $(t_i,\ \hat{d}_i)$ is subtracted from the level-crossing events with only the input signal and dithering quantization error left. As a result, enough digitized samples of the input signal $V_{\rm IN}$ are obtained at the output, which ensures correct recovery of the input signal [8]. *Implicit* dithering is introduced in [9] using VCOs. LCS processing is shifted into the phase domain to provide noise-shaping capabilities. The highly nonlinear VCO, however, needs to be linearized through a digital calibration.

In this brief, we replace the SAR-based residue quantizer in [7], [10] with a VCO-based residue quantizer, as depicted in Fig. 1b. We demonstrate that performance requirements for this VCO-based quantizer (generally considered as the main nonlinearity contributor in a standalone VCO-based ADC) can be significantly relaxed, since its distortion and mismatch are well tolerated within the delta-modulator-based quasi-level-crossing ADC loop. Indeed, the inherent and mismatch-induced dithering in the VCO-based residue quantizer, whose effects can be filtered out, not only mitigates the leakage effects of the switched-capacitor (sw-cap) subtractor on the system performance [10], but also increases the DR of the system and its average sampling rate for low-amplitude and slowly varying input signals. Section II introduces the proposed topology, and presents system-level analysis. Section III discusses the circuit implementation. Section IV discloses the measurement results.

II. System Analysis

The proposed AR delta modulator is shown in Fig. 1b. The residue voltage $\rm V_{RES}$ is amplified and low-pass filtered by the residue amplifier (details shown in Fig. 1c) and then digitized with the VCO-based residue quantizer. The residue quantizer consists of a ring-VCO (RVCO) which converts the voltage into an intermediate information, i.e., the generated carrier phase. The latter is then quantized and differentiated in a frequency-to-digital converter (FDC). The digitized $\rm V_{RES}$, bus $\rm Q_{OUT}$, is compared to ten different digital levels (ten threshold levels are chosen for the sake of demonstration of the AR algorithm), and if at least one among the ten digital levels is crossed, the up/down counter accordingly updates the 7-bit binary output $\rm D_{OUT}$ for the feedback DAC and the event-based CLK (CLK_event) will be enabled to trigger the update of the feedback DAC.

The two cascaded low-gain amplifiers in the residue amplifier function as a 2nd-order RC low-pass filter (LPF), see Fig. 1c, whose z-domain transfer function can be expressed as:

$$H_{\rm LPF}(z) = \frac{G_{\rm A}\cdot(1-p_1)\cdot(1-p_2)}{(1-p_1z^{-1})\cdot(1-p_2z^{-1})} \tag{1}$$

where $G_{\rm A}$ is the overall dc gain of the residue amplifier (equal to 4), while p_1 and p_2 are its poles and located around 10 MHz, which are much higher than the signal bandwidth. We define $\alpha = \rm LSB_{DAC}/LSB_{sub-ADC}$, where $\rm LSB_{DAC}$ and $\rm LSB_{sub-ADC}$ are respectively the LSBs of the sw-cap DAC and of the residue quantizer sub-ADC. The z-domain transfer functions to the system output $D_{\rm OUT}$ from the input (source) noise of VCO residue quantizer E_V ($\rm NTF_V$) and from the input signal $V_{\rm IN}$ (STF) were shown in [10]. The z-domain transfer function to the system output $D_{\rm OUT}$ from the phase quantization noise E_Q of the VCO-based residue quantizer ($\rm NTF_Q$) can be derived in a similar way as in [10]:

$$\rm NTF_Q = \frac{D_{OUT}}{E_Q} = \frac{1-z^{-1}}{1-z^{-1}+z^{-1}\cdot\alpha\cdot G_S\cdot H_{LPF}(z)} \tag{2}$$

where $G_{\rm S}$ is the gain of the subtractor (equal to 1/4). 1st-order noise shaping can be observed in $\rm NTF_Q$ of the phase quantization noise, while the input noise of the VCO-based residue quantizer E_V directly contributes to the in-band modulator noise power.

III. Circuit Implementation

Block diagram of the proposed modulator is shown in Fig. 2a. The sw-cap subtractor and feedback DAC have two operational phases: an update phase asserted by clk1 and a track phase asserted by clk2. As shown in the timing diagram of Fig. 2b, clk1 and clk2 are non-overlapping event-based clocks controlled by *CNG*. During clk1, the sw-cap feedback DAC is updated based on the binary output $\rm D_{OUT}$ while $\rm C_H$ still holds the value of $\rm V_{RES}$ from the last phase. At the rising edge of clk2, the subtraction between $V_{\rm IN}$ and feedback DAC output $V_{\rm DAC}$ is triggered ($V_{\rm RES} = G_S\cdot(V_{IN}-V_{DAC})+V_{CM}$) ($V_{CM}$ is constantly set to half the supply voltage), while s0 and s1 are flipped which will assert the flipping of one among the $C_{\rm H}$'s to remove its memory charge. After the subtraction, the residue amplifier amplifies and low-pass filters $V_{\rm RES}$. The hold capacitor $C_{\rm H}$ maintains the voltage level on $V_{\rm RES}$ during the DAC update phase ($V_{\rm RES}$ is floating then) despite switching perturbations in the circuitry around.[1] The amplified $V_{\rm RES}$ is converted by the 32-level VCO-based residue quantizer (the number of the levels are over-designed and could be reduced to further optimize the power consumption), shown in Fig. 2c, and its output $\rm Q_{OUT}$ is compared versus ten different digital levels, generating the event-based output $\rm EB_{OUT}$. The up/down counter is updated based on $\rm EB_{OUT}$. The trigger *CNG*, which goes high if a level is crossed, decides whether the up/down counter needs to be updated; the *UD* signal, which indicates the sign of the input signal derivative, decides whether the up/down counter needs to be incremented or decremented; $\tilde{\Delta}$ indicates the magnitude of the shift that the up/down counter undertakes during one CLK period.

A. VCO-Based Residue Quantizer

The RVCO in the residue quantizer shown in Fig. 3 consists of 16 pseudo-differential delay stages with 2× passive (resistive) phase interpolation to yield a total of 32 differential phases. Each delay cell is current-starved through a voltage-controlled current source implemented with NMOS transistors, where 24 input transistors are connected in parallel to allow for coarse control of the VCO gain $K_{\rm VCO}$ and free-running frequency $f_{\rm central}$ (about 25 MHz in this implementation). $K_{\rm VCO}$ can further be tuned through the programmable capacitive load of each delay cell (Cap_bank). As the RVCO is continuously oscillating, its supply is set as low as 0.5 V to reduce the dynamic power consumption. The RVCO output phases are sampled using custom sense-amplifier flip-flops, while the downstream hardware for digital differentiation and

[1]Note that $V_{\rm RES}$ is being *constantly* integrated by the VCO so the LPF action by C_H and the residue amplifier helps to suppress the effects of nearby perturbations.

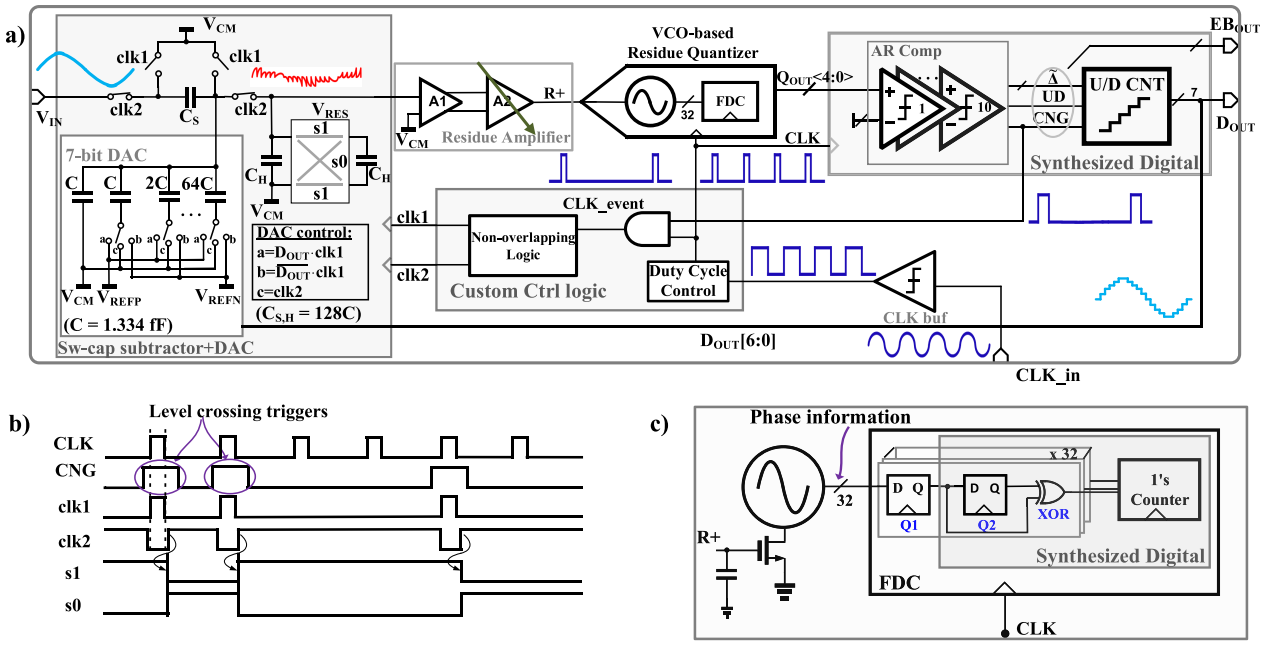

Fig. 2. (a) Block diagram of the proposed adaptive-resolution quasi-level-crossing delta modulator ADC. (b) Event-based clocking timing diagram. (c) VCO-based residue quantizer.

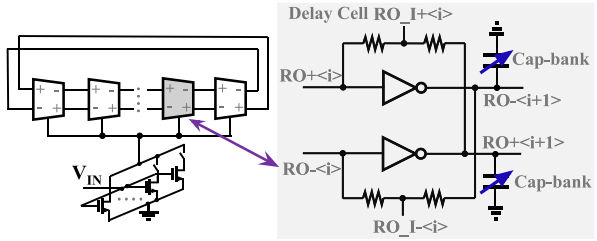

Fig. 3. Schematic of RVCO.

1's counting is implemented using a standard digital synthesis flow, resulting in a simple and straightforward implementation.

The output of the VCO-based residue quantizer $y[n]$ can be expressed as [11]:

$$y[n] = \frac{N_{\text{ph}}}{2\pi}(\Delta\phi_x[n] + \phi_q[n-1] - \phi_q[n]) \tag{3}$$

where N_{ph} is the number of RVCO output phases inside the residue quantizer (32 in this design), $\Delta\phi_{\text{x}}[\text{n}]$ is the VCO phase change in one clock period due to the amplified residue voltage, and ϕ_{q} is phase quantization error. $\phi_{\text{x}}[\text{n}]$ can in turn be expressed as:

$$\Delta\phi_x[n] = 2\pi K_{\text{VCO}}\overline{G_{\text{A}}V_{\text{RES}}}T_{\text{CLK}} \tag{4}$$

in which K_{VCO} is the VCO gain, G_{A} is the dc-gain of the residue amplifier and T_{CLK} is the clock period of the VCO-based quantizer (f_{CLK} is about 100 MHz in this implementation). Therefore, the LSB of the VCO-based residue quantizer is $\text{LSB}_{\text{sub-ADC}} = f_{\text{CLK}}/(K_{\text{VCO}}N_{\text{phase}})$. To obtain $\text{LSB}_{\text{sub-ADC}} = \text{LSB}_{\text{DAC}}$, K_{VCO} needs to be set to $4 \cdot f_{\text{CLK}}$ per volt, and any deviation in this ratio can be treated as a variation in α.

1) Noise: As the phase quantization error in the VCO-based residue quantizer is 1st-order noise-shaped, the dominant in-band noise contributors are the flicker and thermal noise of the RVCO (the NMOS input transistor and the delay cells operate in sub-threshold regime and are relatively of small-width to reduce power consumption), whose input-referred in-band noise is designed to be 0.5 mV_{RMS} to achieve the targeted accuracy of 8.5 bits.

2) Linearity: The VCO-based residue quantizer linearity depends on the global linearity of K_{VCO}. The RVCO input is the amplified residue voltage, which is contained within a small range ($\pm 5\,\text{LSB}_{\text{DAC}}$, which is ± 40 mV) around the output common-mode of the residue amplifier. Consequently, only a small and fairly linear portion of the RVCO voltage-to-frequency tuning curve is exercised. The nonlinearity of K_{VCO} is thus considerably mitigated, and it therefore impacts negligibly on the system THD. Besides, as the RVCO is pseudo-differential, its 2nd harmonic is greatly attenuated. Considering the K_{VCO} nonlinearity, the phase change $\Delta\phi_x[n]$ can be expanded as:

$$\Delta\phi_x[n] = 2\pi T_{\text{CLK}}(\alpha_1\Delta V + \alpha_2\Delta V^2 + \alpha_3\Delta V^3) \tag{5}$$

where ΔV is the average input voltage of the RVCO during the period of T_{CLK}, while α_1, α_2 and α_3 are respectively the first, second and third-order Taylor series coefficients of K_{VCO}. For an amplified residue voltage without triggering the AR algorithm, α_3 at most can lead to some gain error in the signal path. Moreover, it exhibits little overall effect since the RVCO input signal swing is small. Only α_2 can deteriorate the THD of the proposed modulator, although negligibly, as mentioned earlier, given the small swing of the RVCO input signal. For the amplified residue voltage triggering the AR algorithm, the harmonics triggered by the AR are out-of-band, thus they do not affect the ADC in-band linearity.

3) Dithering: In the proposed modulator, the VCO-based residue quantizer inherently features dithering, which is generated during the quantization of the RVCO phase, and it is also caused by the mismatches within the RVCO delay cells and phase-sampling DFFs. This dithering occurs in the digital

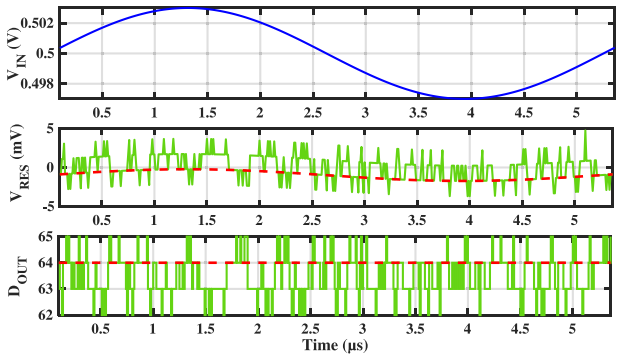

Fig. 4. V_{IN}, V_{RES} and D_{OUT} obtained by behavioral modeling with inherent and mismatch-induced dither generated in the VCO-based residue quantizer (solid line), and without dithering (dashed line).

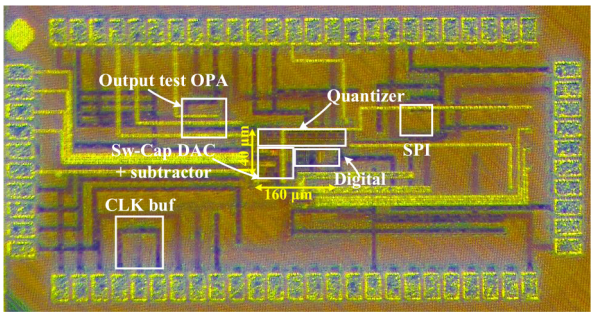

Fig. 5. Chip micrograph.

domain and appears at the VCO-based residue quantizer output Q_{OUT}. Such implicit dithering present within the proposed modulator allows extending the average sampling rate in the case of low-amplitude and slow-varying input signals (see Fig. 4), thus improving the DR of the modulator and guaranteeing that the average sampling rate satisfies the Nyquist criterion of the input signal. The dithering allows the DR of the proposed system to be upperbounded by the peak SNDR of the ADC rather than by the resolution of the feedback DAC. The lowest average sampling rate depends on the dithering frequency. The frequency of the inherent dithering generated by the free-running RVCO is dependent on V_{RES} and f_{CLK}, which is much higher than the signal bandwidth and whose effects are thus filtered out. The dominant spurs of the RVCO caused by the mismatches of delay cells are generated at twice the free-running frequency of the RVCO [11]. The dithering caused by the spurs will be randomized by the FDC due to the barrel-shifting nature of the RVCO phase outputs. Therefore, the implicit dithering is mainly distributed outside of the band and will not lead to the SNR degradation.

IV. Measurement Result

The proposed quasi-level-crossing delta modulator, implemented in TSMC 28-nm LP CMOS, occupies an area of 0.022 mm^2, as shown in Fig. 5. The bandwidth of the proposed ADC can be obtained by considering that the maximum slew rate of the system is constrained by the maximum voltage shift that the feedback DAC can provide during T_{CLK} [10]. Fig. 6 shows the measured output spectrum for a 300.06 kHz full-scale sinusoidal input signal, achieving SNDR and SFDR of 53.07 dB and 63.32 dB, respectively. With the help of an

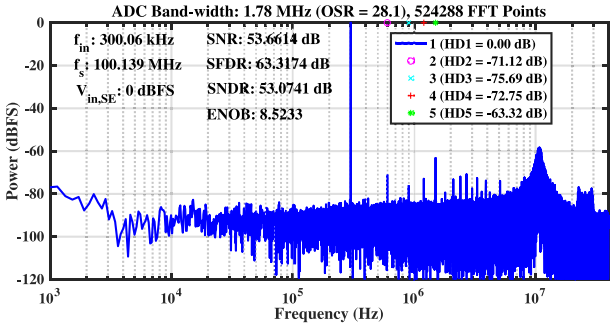

Fig. 6. Measured output spectrum of the modulator with a 300 kHz full-scale sinusoidal input.

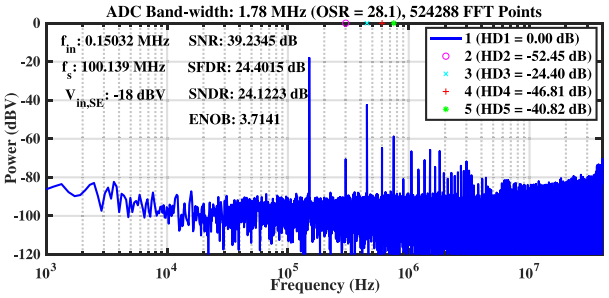

Fig. 7. Measured output spectrum of VCO-based residue quantizer at 100 MS/s and with a differential 176 mV 0.15 MHz input sinewave.

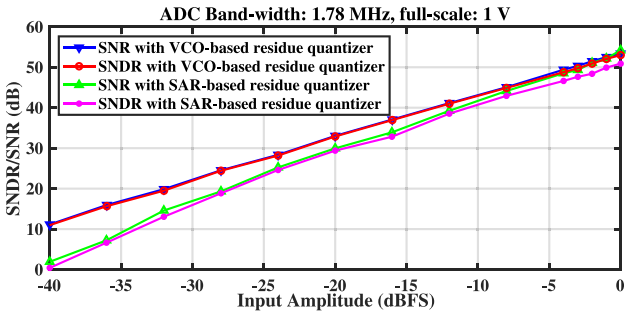

Fig. 8. Measured SNR/SNDR versus amplitude at 300 kHz frequency for a sinusoidal input compared to the dithering-less system with SAR-based residue quantizer of [10].

on-chip design-for-testability circuitry, the output spectrum of the standalone VCO-based residue quantizer with its −18 dBV input signal at 150.32 kHz (which is the amplitude that triggers a full swing at the VCO-based residue quantizer's output) is shown in Fig. 7. Although the HD3 of the standalone VCO-quantizer is rather large (−24.4 dB), the HD3 of the proposed *system* is merely −75.1 dB, indicating that significant harmonic distortion within the VCO-based residue quantizer can be mitigated. The SNDR and SNR of this modulator versus the amplitude of an input 300.06 kHz sinewave is plotted in Fig. 8, suggesting a DR above 50 dB. This is considerably larger than that of the quasi-level-crossing modulator in [10], also plotted in Fig. 8 for comparison, which does not exhibit inherent dithering and whose DR, constrained by the resolution of the 7-bit sw-cap feedback DAC, is limited to ∼ 42 dB.

The output spectrum of a two-tone test shown in Fig. 9 uses two input sinewaves at 110.207 and 100.275 kHz, each at −6 dBFS. Fig. 10 presents the average sampling rate versus the frequency of a −3 dBFS input sinewave. At the edge of

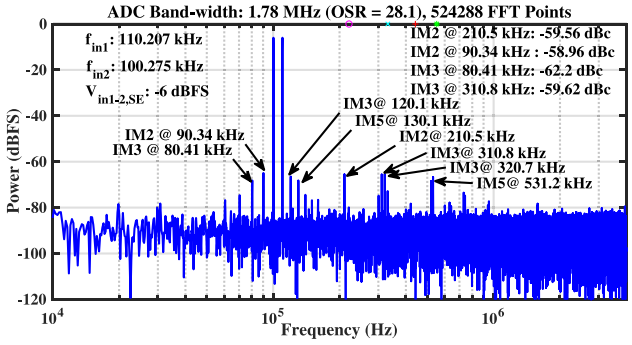

Fig. 9. Two-tone test with input sinewaves at 100.275 and 110.207 kHz.

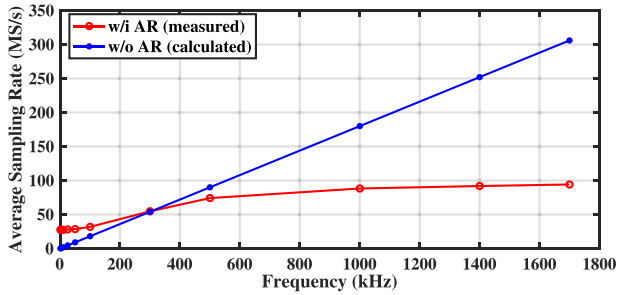

Fig. 10. Measured average sampling rate (w/i AR algorithm) and theoretical average sampling rate (w/o adaptive resolution), versus input sinewave frequency.

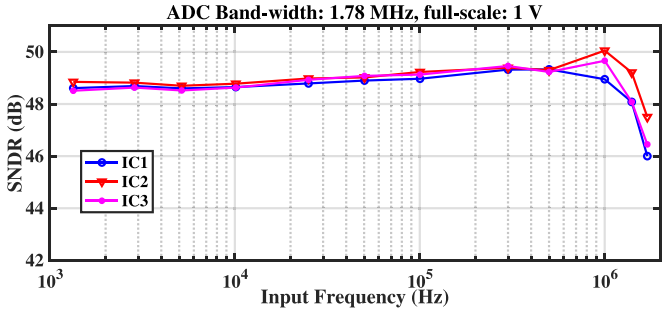

Fig. 11. Measured SNDR versus frequency at −3 dBFS amplitude for a sinusoidal input for three different ICs.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART IN ADCS FOR COMPRESSED SENSING APPLICATIONS

	[3]	[4]	[10]	[6]	**This Work**
Topology	AR LCS	AR LCS	AR LCS	LCS	**AR LCS**
Need CT Comp	Yes	Yes	No	Yes	**No**
Process (nm)	130	180	28	65	**28**
Area (mm^2)	0.3575	0.96	0.0126	0.3	**0.022**
Power	3-9 μW	25 μW	146-205 μW	30 mW	**410 μW**
BW	20 kHz	1 kHz	1.42 MHz	20 MHz	**1.78 MHz**
SNDR (dB)	47-54	52.2	43.1-53.5	59.9	**53.07**
FoM$_W$ (fJ/c-s)	230-888	37,600	186-439	929	**313**

the signal bandwidth (1.78 MHz), the average sampling rate is reduced by a factor of three using the AR algorithm, while for low frequency signals, the average sampling rate is higher than that without AR, due to the inherent and mismatch-induced dithering from the VCO-based residue quantizer. The SNDR of the proposed modulator versus frequency of a sinewave at −3 dBFS amplitude has been measured across three different dies and is presented in Fig. 11. In contrast to [10], this work maintains the SNDR at low input frequencies as the inherent dithering mitigates the effects of the leakage within the sw-cap feedback DAC and subtractor. Finally, Table I compares the presented VCO-based delta modulator with state-of-the-art ADCs for compressed sensing applications. The power consumption of the presented work can be further optimized by reducing the number of phases within the VCO-based residue quantizer.

V. CONCLUSION

An adaptive-resolution (AR) quasi-level-crossing delta modulator equipped with a VCO-based residue quantizer is presented. Such residue quantizer results in a digitally intensive implementation. Large harmonic distortion caused by the nonlinear K_{VCO} can be mitigated, while the phase quantization noise inside the VCO-based residue quantizer is 1st-order noise shaped, with RVCO phase noise dominating the in-band noise floor. With inherent and mismatch-induced dithering inside the VCO-based residue quantizer, the DR of the proposed modulator is increased to >50 dB and the SNDR at low frequencies is not degraded by the leakage within the sw-cap subtractor, while with the AR algorithm, the average sampling rate can be beneficially reduced by a factor of three at the edge of the signal bandwidth.

ACKNOWLEDGMENT

The authors thank TSMC for chip fabrication. They also thank Prof. Marek Miśkowicz, Dr. Pedro Emiliano Paro Filho and Prof. Brian Mulkeen for technical discussions, Paulo Vieira for his lab assistance, and MCCI for technical support.

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