Power packet router with power and signal switches for a single power packet

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Abstract

This brief proposes a power packet router (router) and experimentally verifies its operation. A power packet is a unit of DC power and an information tag. When the tag is attached to the power directly, a power packet ensures their simultaneity during the transmission. The router sends and receives power packets in Time Division Multiplexing scheme. Since the beginning of our research project, the router has generated a power packet with a single switch. The switch ensures the simultaneity of power and information during transmission. On the other hand, the switch limits the capacities of power and information of a power packet. The proposed router ensures the simultaneity by its power packet generation method. It lets the switches operate in sync for power and information to generate a single power packet. The operation is experimentally verified. The results make it confirmed the possibility to combine the individually optimized subunits for packet generation.

1 Introduction

Many vehicles and aircrafts have run partly/fully on electricity. They are equipped with multiple batteries and/or renewable energy sources to operate long time, for redundancy, and other reasons [1, 2]. In conventional direct current (DC) systems, there has been few numbers of power sources, but are increasing. Their cooperation becomes an emerging challenge. The cooperation is necessary in voltage stability and efficient use of energy. The communication technology has been pointed out to be the key to achieve it [3]. For instance, Controller Area Network (CAN) connects distributed elements in a vehicle [4]. The data on CAN includes state of charge of batteries and control signals from electronic control units. This example confirms that the power system is tied to the communication. In this context, ICT aided power management systems have been proposed and studied. The power packet and its dispatching system is one of these proposals.

The concept of a power packet is a unit of power and information [5–8]. When the information is physically attached to the power, their simultaneity is exactly achieved during transmission [7]. The simultaneity is necessary in controlling electric energy at discrete form. Our research group has developed the power packet dispatching system for low to medium voltage DC systems, such as mobile robots and electric vehicles [7,9–11]. In the system, the power packet router (router) receives, holds, and sends power packets in Time Division Multiplexing (TDM) scheme. Therefore, the router is the key component to keep the simultaneity of power and information during the transmission. The router has generated a power packet with a single switch [7,9–11]. The switch confirmed the simultaneity during the transmission in the method. It also decided the capacities of power and information of a unit power packet. However, the power and information have a linked restriction. They cannot avoid a tradeoff between the capacities of power and information. For example, sending data in high data rate (more than 1 Mbps), the payload voltage was less than 11.5 V [12]. In order to extend both capacities of power and information, the power packet generation and the routing method must be improved.

We previously studied [13] that two voltage sources can be combined to generate a single power packet. Based on it, a power packet router is proposed in this brief. The router ensured the simultaneity of power and information during the transmission by its power packet generation method. This method allows collaboratively to combine the switches for power and

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signal to generate a single power packet. The combination of switches contributes to extending capacities of power and information for the router. The proposed router achieved the 100 V power and 1 Mbps data transmission in the experimental verification.

2 Power packet dispatching system

The power packet is a unit of integrated power and information. Fig. 1 shows the concept of a unit power packet and the power packet dispatching system. The concept of power packet was originally proposed in 1990s [5]. In the proposal, the electric power and its information were combined with the accompanied information network. Our group has proposed the physical integration of power and information using wide gap semiconductors [7]. The physical integration ensures the simultaneity of power and its information as a packet during transmission.

A unit power packet consists of the header, payload, and footer. The configuration of power packet is an analogy of the packets in information networks. The header and footer transmit information such as the power source, destination, and control signals of the load. They are sent in voltage waveforms without power. It is an exception that the headers and footers are directly transmitted to loads. It needs and exceptional operation of routers. Here the payload transmits DC power. It implies that current flows during the payload. The length of the payload is set longer than the header and footer. Loads cannot accept power at high frequency. The design of power packet faces to the difficulties due to it.

The power packet dispatching network consists of multiple power sources, storages, loads, power packet

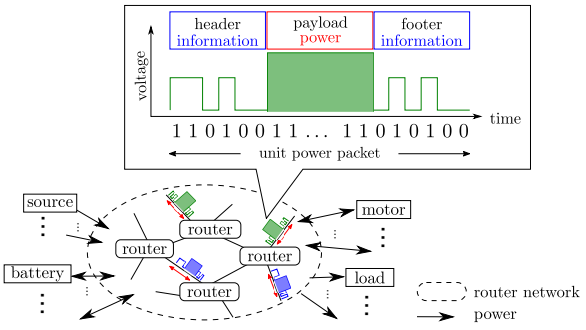

Fig. 1: Concept of power packet and its dispatching system.

mixers (mixers), and routers. The mixer is directly connected to power sources and generates power packets. When a power source is directly connected to a router, it becomes a mixer. Power packets are transmitted in TDM scheme. TDM scheme allows power packets with different profiles to share the same power line without overlapped. Power line sharing will reduce the number of wires for both power and information transmission. That saves the space, weight, and cost of the power system. The feature also makes the network flexible and enables it to distribute electric power in the similar way to the information in the Internet. The network flexibility also contributes to improving the fault tolerance of the power system. These features will suit the applications.

In conventional power systems, the power flow is continuous and described by differential equations. On the other hand, in the power packet dispatching system, the power flow is discrete and can be indicated by the number or density of transmitted power packets in the network [7, 8]. S. Mochiyama *et al.* [14] experimentally verified the motor control by the power packet density modulation. The power balance between sources and loads was described by consensus dynamics [15]. Based on them, the system was modeled by distributed hybrid automata, and numerically studied [16].

3 Power packet router with power and signal switches

The router is the key component in the power packet dispatching network. It is mainly composed of a controller, isolators, switching circuits, and storages. The router reads the information of an input power packet through the attached isolators, which separates the payload and the tag information. Next, it connects the designated storage to the power line and receives the input power packet. After receiving the power at the storage, it re-generates power packets to the neighbors using the switching circuit. They are namely the store and forward operations of power packets. They achieve the routing of power packets. That is to say, the router keeps the relationships between the stored power and its information and takes it forward.

3.1 Preceding studies on developing router

In our project, two types of power packet routers have been proposed [10, 11]. R. Takahashi *et al.* [10] employed unidirectional switches and N. Yoshida *et al.* [11] bidirectional ones. Both switches show both advantages and disadvantages. A unidirectional switch consists of a FET switch and a diode. The diode blocks reverse current through the body diode of the FET. However, the voltage drop of the diode decreases the payload voltage. A bidirectional switch has back-to-back connection of FETs. This configuration can reduce the voltage drop than a unidirectional switch. However, it can become a disadvantage to prevent unintentional current.

As mentioned in Sec. 1, the single switch configuration inherits the tradeoff between the ratings of the power and data rate. To extend the power and data capacities per power packet, the payload voltage and switching frequency must be increased.

3.2 A router with switches for power and signal

This brief proposes a router which aims to ensure the simultaneity of power and information during transmission with multiple types of switches. The router collaboratively manipulates them to generate a single power packet. We employed bi and unidirectional switches for power and for signal, respectively, adopting their advantages. Bidirectional switches generate the payload. They realize multi-directional power switching. We chose unidirectional switches and the same power source as the router to generate the header and footer. The power source of the router is common. Its voltage is low enough to feed the controller. Low voltage power sources are appropriate to generate signals from the viewpoint of data rate. However, back-flow of power to the source should be prohibited. Unidirectional switches suit to avoid it.

Fig. 2 shows the schematic diagram of the proposed bidirectional router. This router is aimed at handling 100 V power and 1 Mbps data transmission. The router consists of a controller, gate drivers, storages, and a switching circuit. The controller is a Field Programmable Gate Array (FPGA) board (Avnet, MiniZed), which contains Zynq SoC chip (Xilinx, XC7Z007S-1CLG225C). The gate driver consists of a digital isolator (Silicon Labs, Si8610BC) and MOSFETs (Rohm, US6M1). The storages are selected to meet the power rating of the router. In the

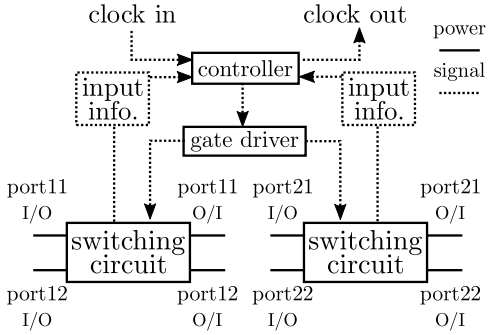

Fig. 2: Schematic diagram of bidirectional power packet router proposed in this brief.

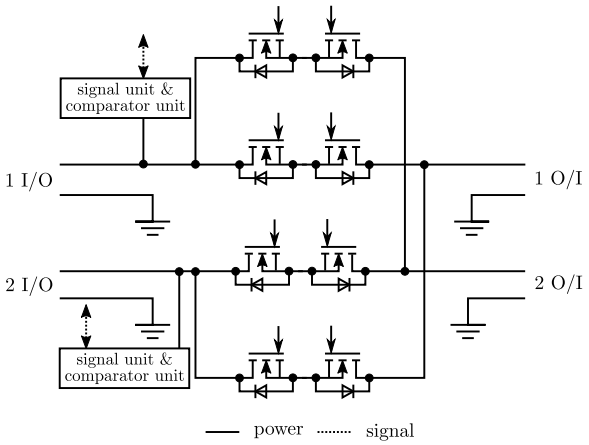

Fig. 3: Switching circuit of proposed router. MOSFETs are SiC MOSFETs (SCT3022AL).

router, capacitors are employed as storages. Storages are connected between two O/I ports (e.g. between port11 O/I and port21 O/I). The router use *clock in* and *clock out* to synchronize with other routers for reading signals. The rating frequency of the clock is set at 1 MHz. The clock synchronization can be achieved by the additional signal before the header of the power packet [17].

Figs. 3 to 5 show the switching circuit and units in it. Fig. 3 shows the schematic diagram of the switching circuit. The bidirectional switches consist of the back-to-back connections of SiC MOSFETs (Rohm, SCT3022AL). We selected their rating voltages to be sufficiently larger than 100 V. Their ratings are tabulated in the appendix. This circuit has the same topology as the bidirectional power packet router proposed in the preceding research [11]. Power from an I/O (O/I) port can be transferred to any O/I (I/O) ports through one switch and the other I/O (O/I)

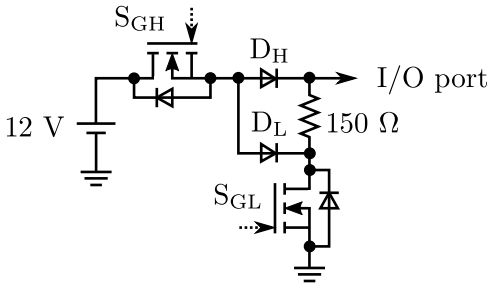

Fig. 4: Schematic diagram of signal unit. FETs are GaN HEMT (EPC2010) and diodes are (MBRS3201T3G). 12.0 V source is the same as the source of the router.

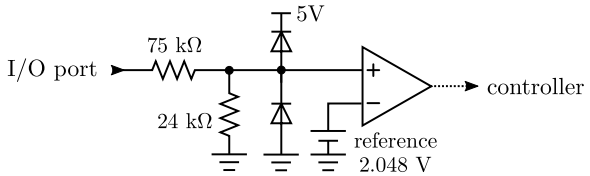

Fig. 5: Schematic diagram of comparator unit. Comparator is LT1713. 5.0 V source is the same as the source of the router.

ports through two switches, respectively.

Fig. 4 shows the schematic diagram of the signal unit. The unidirectional switches consist of the GaN FETs (Efficient Power Conversion, EPC2010) and Si diode (ON Semiconductor, MBRS3201T3G). We chose the rating voltage of S_{GL} and diodes (D_H and D_L) to be larger than 100 V. Because they have to withstand the payload voltage. Their ratings are tabulated in the appendix. S_{GH} generates the "1" of the header and footer using the 12.0 V power source. The 12.0 V power source is the same power source as the router. S_{GL} sends the bit of "0". It lowers the source voltage of S_{GH} through D_L and the power line voltage through 150 Ω resistor. D_H prevents the reverse current to the voltage source. D_L also prevents it and helps decrease the source voltage of the S_{GH}. This topology contributes to both the high-speed signal generation [14] and the protection of S_{GL} from the surge current on the power line. The dead time between S_{GH} and S_{GL} is set at 50 ns. In order to simplify the dead time control, we chose the same GaN FET to S_{GH} as S_{GL}.

Fig. 5 shows the schematic diagram of the comparator unit. The comparator unit consists of voltage divide resistors, voltage clamp diodes (Toshiba, 1SS226), a reference voltage source (Linear Technology, LT6654-2.048), and a comparator (Linear Technology, LT1713). The threshold voltage of the comparator unit is set at 8.5 V. The router reads the signal of '1' when the power line voltage exceeds the threshold. The diodes protect the comparator from the overvoltage.

Tab. 1: Bit assignment of power packet

	Header	Payload	Footer
Length	7 bits	24 bits	3 bits
Bit	1110101	111...11	000

4 Operation verification

This section describes the experimental verification of the proposed router. The routing of power packets is achieved by store and forward. These operations are verified in an experimental system.

4.1 Experimental setup

Fig. 6 shows the experimental circuit with proposed routers. This circuit consists of one source, mixer, router, and load of 430 Ω. Dotted arrows show the connections to the comparator unit. In this circuit, the mixer transmits power packets, and the router receives them and transmits the same power packets to the load. The voltage of the DC source E is set at 100.0 V. Tab. 1 shows the bit assignment of power packets. The header tells the start of a power packet and its destination. The footer does not transmit information. Its duration corresponds to the time to decrease the power line voltage through S_{GL}. The mixer and router send power packets continuously. The duration is set at 1 bit between the mixer starts sending a power packet and the router starts. The clock is set at 1 MHz. The mixer and router are synchronized through the clock line with respect to power packet transmission. We measured the voltage and current of the power line between the mixer and router (V_l, I_l), and the voltages of the storage (V_s) and the load (V_r). V_s was measured with the DC voltage offset of 80 V to reduce the effects of noise.

Practically, a port of a router can be connected to not only one port. Such situations are called multiple access in information networks. The problems which arise from the multiple access are the congestion and the collision of packets. They can make a chance for a

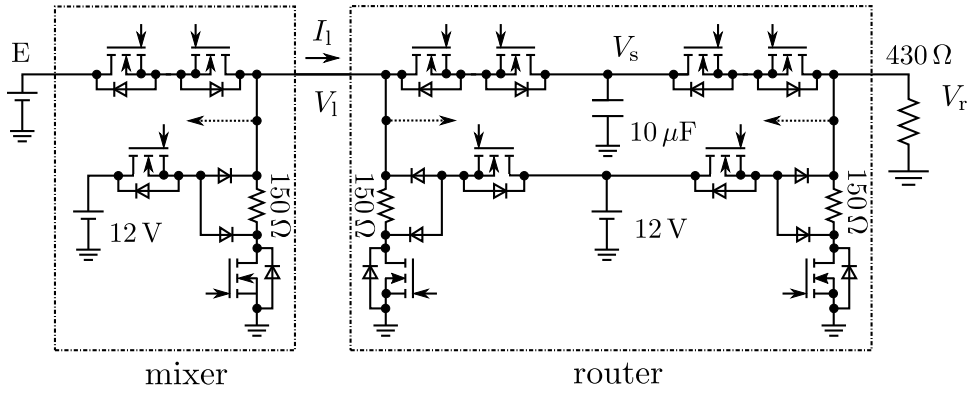

Fig. 6: Experimental circuit configuration with one power source and one load. The source voltage E is set at 100 V. Dotted arrows show the connections to the comparator units.

source or a storage to have an unintentional connection with other sources or storages in power packet dispatching networks. However, they can be solved by the similar ways in information networks [9,13,18]. For instance, N. Fujii *et al.* [9] demonstrated the power packet transmission on a system with a branch on wire. Because these solutions request some additional rules to the controller of the router and do not need any changes to the hardware. This study focuses on the power packet generation method and hardware of the router to achieve it. That is, the experimental system meets the sufficient condition to verify the operation of the router.

4.2 Experimental results

Fig. 7 shows examples of experimental voltage and current waveforms. First, the operations of proposed router are confirmed. V_l shows the logical value of the power packet sent to the router. The header signal starts at -7 μs. The logical value is confirmed as same as the settings shown in Tab. 1. This result is also shown in V_r. Therefore, we can verify that the mixer and the router send the same power packets in the duration of 1 bit. I_l shows that the current starts flowing at 0 μs when the payload starts, except the surge current. This result indicates that the router reads the header signal of the power packet and receives the payload to the storage. These results verify that the proposed router achieves routing of power packets and the simultaneity of power and information is kept during the transmission based on different aims of switches.

Second, we can confirm the values of the measured waveforms. I_l converges to around 230 mA at 25 μs.

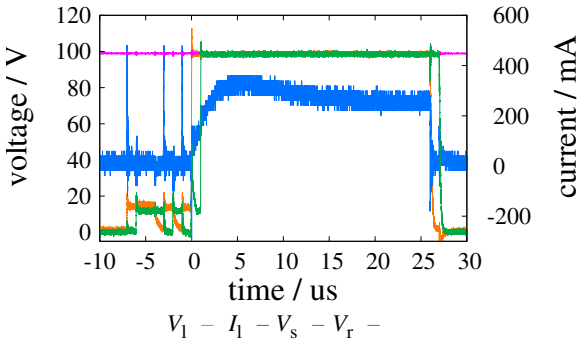

Fig. 7: Example of experimental waveforms. V_l and I_l show the voltage and the current waveforms of the power line between the mixer and the router. V_s and V_r show the voltage waveforms of the storage and the load, respectively. V_s was measured with DC offset of 80 V to reduce the effects of noise.

Considering the experimental circuit, it is derived from the source voltage to the load resistance. V_s is 98.8 V in average. Here, we see the voltage drop across the power switch. The voltage drop limits the number of hops during routing. In order to decrease the voltage fluctuation due to the switching, we took 10 μs to 20 μs. The voltage difference between V_s and V_r is 0.31 V in average. Using unidirectional switches, the voltage drop between the storage and the router output was around 0.6 V even when the current is 90 mA due to the diode [9]. It clearly shows that the voltage drop with the switches are less than the previous studies.

There appears the surge current at -7, -3 and -1 μs. They are caused by the switching of GaN HEMTs.

They do not affect operation of the proposed router in this experiment. Needless to say, they should be suppressed from the viewpoint of EMC and protecting the router hardware. The expected countermeasures include the waveform shaping of power packet [19] and the soft switching technique [20].

The combination of switches used in the experiment is not optimized for generating power packets on the target voltage and data rate. The prototype router must be improved. The appropriate circuit design can improve the ratings of the routers.

5 Conclusion

In this brief, a power packet router is proposed. The router ensures the simultaneity of power and information by introducing the power packet generation method with the switches for power and signal. This topology allows a combination of switches with different ratings to meet the target voltage and data rate. The operation of the router is experimentally verified. The proposed router achieves 100 V power transmission and 1 Mbps data transmission. This router verifies that the simultaneity of power and information is kept by its generation method when different types of switches are employed. The experimental results show that the power and data capacities of the router can be achieved independently.

Further researches are expected for the bidirectional power packet transfer and its transmission protocols to improve power transmission efficiency and to solve the problems which arise from the multiple access. The power flow control in discrete form is also expected for future works. The wave shaping and soft switching techniques are other possibilities. They might lead the flexible power packet network and efficient use of electric energy by the discretized form. The proposed router is a prototype to verify the power packet generation method. For the practical applications, there still remains many challenges to be solved, such as the cost and size. We think downsizing and circuit integration are important. The results of this brief proved that the signal circuit can be optimized separately to the power circuit. It shows the possibility of the integration of the router circuit.

A Ratings of the switches

Absolute maximum ratings of bi and uni-directional switches are shown in Tab. 2. The proposed router is a prototype and its design is not optimized to the target voltage and bit rate. The switches with sufficiently large absolute maximum ratings are employed in this brief.

Acknowledgment

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Tab. 2: Absolute maximum ratings of switches [21–23]

SCT3022AL	Drain - Source voltage	650 V
	Continuous drain current (25 °C)	93 A
	Pulsed drain current	232 A
EPC2010	Drain - Source voltage	200 V
	Continuous drain current	12 A
	Pulsed drain current	60 A
MBRS3201T3G	Peak repetitive reverse voltage	200 V
	Average rectified forward current	3 A

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