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Cross Connected Compact Switched-Capacitor Multilevel Inverter (C^3-SCMLI) Topology with Reduced Switch Count

M. Jagabar Sathik, *Senior Member, IEEE*, N. Sandeep, *Senior Member, IEEE*, Dhafer Almakhles, *Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*

Abstract: In this letter, a new cross-connected compact switched capacitor (C^3SC) cell is introduced for multilevel inverter applications. The proposed CCS cell uses four switches and two diodes for interconnecting the input dc source and floating capacitors (FCs). A nine-level inverter is derived with the proposed C^2SC cell requiring only ten switches and two FCs. The proposed C^3SC cell-based MLI is self-balancing and has a voltage gain of two. All the switches of the proposed topology have a maximum blocking voltage within the input dc voltage (v_{in}) value. The operating principle is detailed, and a simple logic gate based gate pulse generation scheme is presented. Detailed simulations and experimental results obtained from an 850 W prototype with several test cases are presented to validate the operation of the proposed topology. Finally, a detailed comparative assessment is performed with other recent SCMLIs to demonstrate the merits and superiority of the proposed topology.

Index Terms: **multilevel inverter, switched capacitor inverter, voltage boosting, self-voltage balancing**

I. Introduction

The multilevel inverters are widely used in industrial drive applications, power quality devices, and renewable power generation. The main advantage of MLIs is the high-quality output voltage and low voltage stress on switches [1]-[2]. In conventional MLIs such as cascaded h-bridge, neutral point clamped, and flying capacitor type, they require a large number of active switches and clamping devices, which increases the losses, size, and weight. In order to avoid a large number of active switches, a reduced number of active switches with a switched capacitor structure is recommended in [3]-[9]. However, these topologies suffer from high voltage stress on switches, which is equal to the maximum output voltage. To minimize the voltage stress on the switches, various SCMLI topologies are presented for different output voltage levels in [10]-[11]. Further, these topologies do not have the boosting ability, and sensors are required to balance the floating capacitors. In recent years the switched capacitor multilevel inverters (SCMLIs) with voltage boosting is famous due to less number of conversion stages. In order to avoid sensors, the self-voltage balancing topologies are proposed with different switched capacitor cells (SCC) as shown in Fig.1 (a)-(e). In [12], the cross-connected switched capacitor is presented. Two different SCC is presented as (i) Half circuit and (ii) Full circuit. In half circuit, the number of FCs is increasing for the same number of IGBTs.

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M.Jagabar Sathik and Dhafer Almakhles are with the Renewable Energy Lab, Prince Sultan University, Riyadh, 11586 Saudi Arabia, (e-mail: mjsathik@ieee.org and dalmakhles@psu.edu.sa). M.Jagabar Sathik is also with Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Kattankulathur Campus, 603203Chennai, India.
N. Sandeep is with the Department of Electrical Engineering, Malaviya National Institute of Technology, 302017 Jaipur, India
F. Blaabjerg is with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark.

The optimized SCC unit full circuit as shown in Fig.1 (a). This full circuit required six IGBTs with maximum voltage stress of $2v_{in}$. A new SCC module as shown in Fig. 1(b) is proposed for the self-voltage balancing of FCs with voltage boosting ability [13]. This topology is able to configure in both symmetrical and asymmetrical methods. The voltage stress on switch and number of charging and discharging of FC is not equal which resultant bulky size of FC is needed. In [14], two floating capacitors are used with a single dc source. The number of charging and discharging of floating capacitors are equal, and it produces nine-level. Further, by cascading, this topology is extended to the "N" number of levels. Another nine-level inverter topology with a switched capacitor cell is presented in [15].

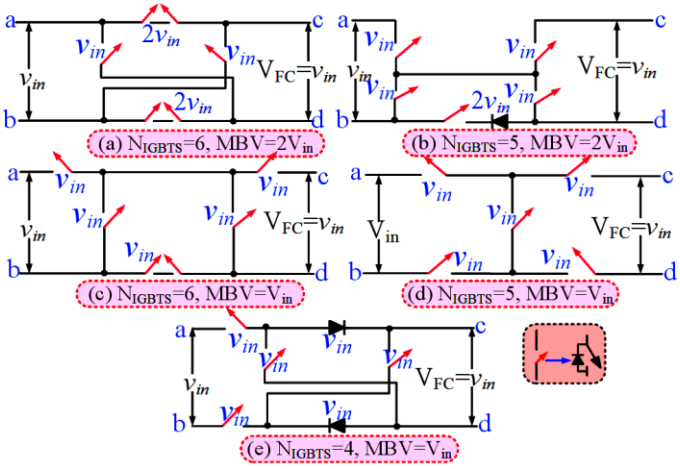

Fig. 1. Different switched capacitor cell (SCC) Modules (a) presented in [12], (b) presented in [13], (c) presented in [15], (d) presented in [16] and (e) Proposed SCC Module

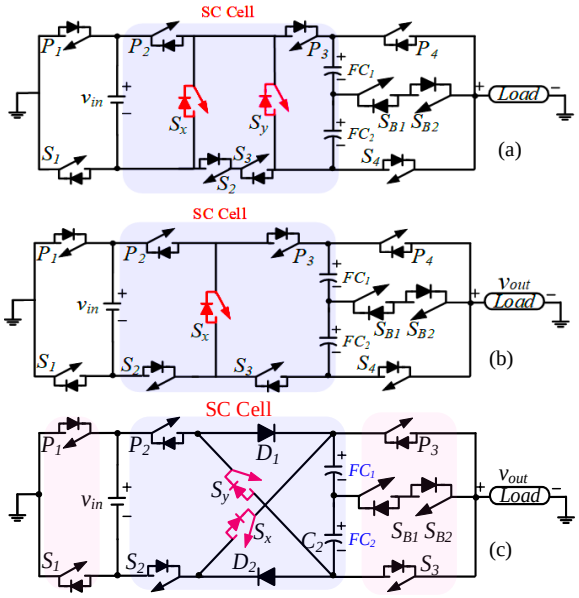

Fig. 2. 9L inverter topologies with different switched capacitor cell (a) presented in [15], (b) presented in [16] and (c) Proposed circuit diagram

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In this topology, the maximum voltage stress on the switch is equal to the input voltage as shown in Fig.1 (c) and the corresponding structure is shown in Fig. 2(a). MLI with quadarable voltage boosting is presented in [16]-[17]. The output voltage is four times higher than the v_{in}. But the voltage stress on the switch is twice the v_{in}. Further to reduce the active switches, a new SCC module is proposed in [18] as shown in Fig. 1 (d) and see Fig. 2 (b). This new compact SCMLI topology is with voltage boosting and one active switch is reduced. In this paper, a new SCC module is proposed as shown in Fig. 1 (e) and the developed topology is shown in Fig. 2 (c). This letter aims to further reduce the required number of switches, gate drivers, and the number of ON state switches while preserving all other benefits of an SCMLI. The article is organized as follows: in section II, the proposed 9L inverter with its operation having different modes is presented with the modulation scheme. Experimental results are presented for various dynamic performance in section III with a detailed comparison among the various 9L inverter topology. The conclusion is discussed in section IV.

II. Structure And Modes Of Operation Of The Proposed 9L Inverter Topology

In Fig. 2 (a), recently reported SC-9L inverter topology is shown, and it consists of 12 switches with a boosting gain of two. The topology in Fig. 2 (b) presented in [13] achieves a reduction of one switch for the same number of output voltage levels and boosting gain. As an extension to [13], this letter proposes a new cross-connected switched cell (refer Fig. 2 (c)) offering a further reduction in the switch count, number of on-state switches, and gate drivers. The advantages of the proposed topology are:

- The total number of the switch is ten.
- The maximum blocking voltage is equal to the input voltage.
- The output voltage is double the input voltage.
- The FC voltages are self-balanced and thus no voltage/current sensors are required.

The proposed topology comprises of a single dc source of magnitude v_{in}, two FCs rated for $v_{in}/2$, and two diodes. The switch pairs (S_1, P_1), (S_3, P_3), (P_2, S_x, S_2) and (P_2, S_y, S_2) should not be turned ON simultaneously to avoid the dc source short-circuiting. The bidirectional switch (S_{B1}, S_{B2}) is connected to the mid-points of the FCs to tap any one of the FC voltage to the load and clamp the FC voltage to $v_{in}/2$.

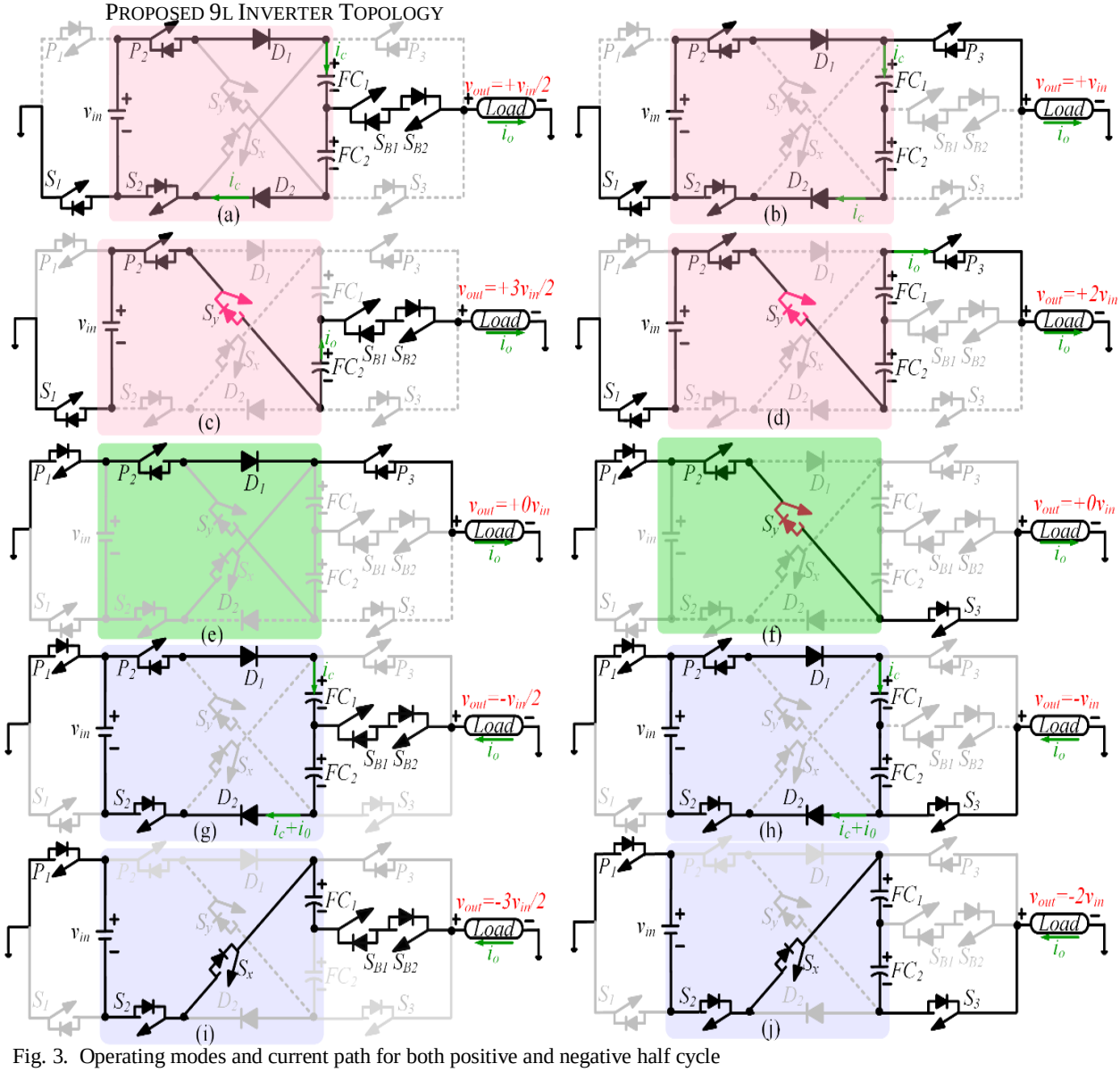

Fig. 3. Operating modes and current path for both positive and negative half cycle

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Further, the switch (S_{B1}, S_{B2}) allows the current to conduct in both directions, and the maximum blocking voltage is $v_{in}/2$. The modes of operation and switching sequence of the proposed topology are shown in Fig. 2 (a)-(f). The number of charging and discharging of both FC is identical. The output equation is given (1)

$$Vout = \left[\begin{array}{l} \left(\frac{S_1+P_1}{2}\right)-\left(\frac{P_2+P_1}{2}\right)+\left(\frac{D_1+D_2}{2}\right)\left(Sx+\frac{1}{2}\right)+\left(\frac{SB_1+SB_2}{2}\right). \\ \left(P_1-\frac{1}{2}\right)+3\left(\frac{S_y+S_x}{2}\right)+\left(\frac{S_3+P_3}{2}\right)\left(\frac{S_x+P_y}{2}\right)+\frac{P_1P_2}{2}(1-S_3)-S_3 \end{array}\right] v_{in} \quad (1)$$

When the corresponding switches are turned ON it should be "1" or else "0".

A. *Modulation Scheme, Switch Voltage and Current Stress Analysis*

The conventional level-shifted Sinusoidal Pulse Width Modulation (SPWM), as shown in Fig. 4 (a) is employed for the modulation of the proposed inverter. Further, as per the switching states sequence in Fig. 3, corresponding logic functions are derived for each of the switches, as shown in Fig. 4 (b). The proposed logic functions can be realized using the logic gates or on any low-cost digital signal processor. Additionally, the switch voltage and current stress of the proposed C^3SC topology is given in Table I.

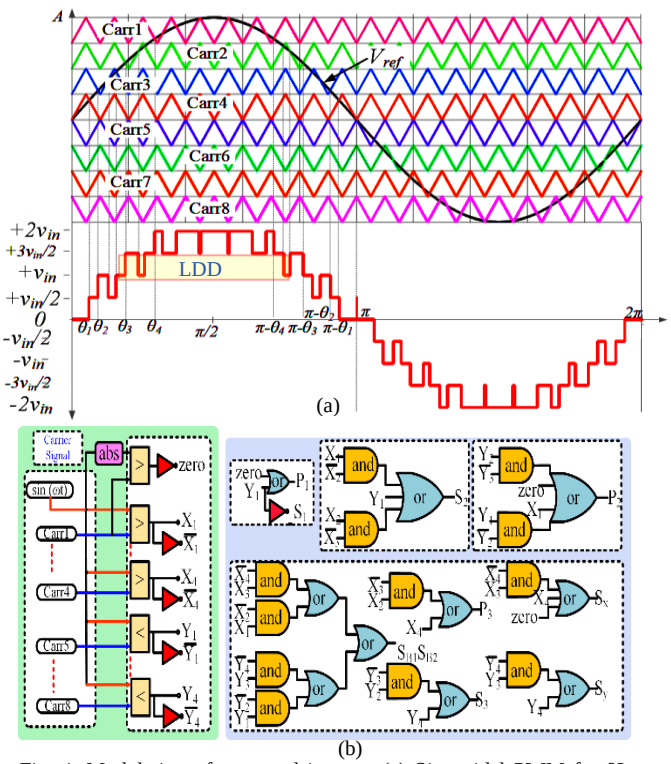

Fig. 4. Modulation of proposed inverter (a) Sinusoidal PWM for 9L inverter (b) PWM logic

TABLE I
VOLTAGE AND CURRENT STRESS OF THE PROPOSED INVERTER

Description	*Switches*								
	S_1	S_2	S_3	$S_{B1}S_{B2}$	S_x	S_y	P_1	P_2	P_3
MBV	v_{in}	v_{in}	v_{in}	$v_{in}/2$	v_{in}	v_{in}	v_{in}	v_{in}	v_{in}
MCS	i_o	i_o+i_c	i_o	i_o	i_o	i_o	i_o	i_o+i_c	i_o

MBV-Maximum blocking voltage on switch, MCS-Maximum current stress in switch

As it can be seen, the proposed topology exhibits a uniform voltage blocking requirement. Further, two out of 10 switches are required to block only half of the maximum voltage. Similar to the other SCMLIs, the current stresses for the switches P_2 and S_2 are high as they also need to carry the FC charging currents. The rest of the switches have uniform current stress which is equal to i_o.

III. SIMULATION AND EXPERIMENTAL RESULTS

Firstly, MATLAB/Simulink simulations are performed to confirm the operability of the proposed topology. Following which, experiments are conducted on an 850 W laboratory prototype as a validation. The selected simulation and experimental parameters are given in Table II.

TABLE II
SIMULATION AND EXPERIMENTAL PARAMETERS

Descriptions	Simulation	Experimental
Input DC Voltage	100 V	
FC Rating	50V/ 1000µF	50V/ 1700µF
R-L Load	100 Ω, 40Ω & 80mH	
Fundamental/ Switching Frequency	50 Hz / 5 kHz	

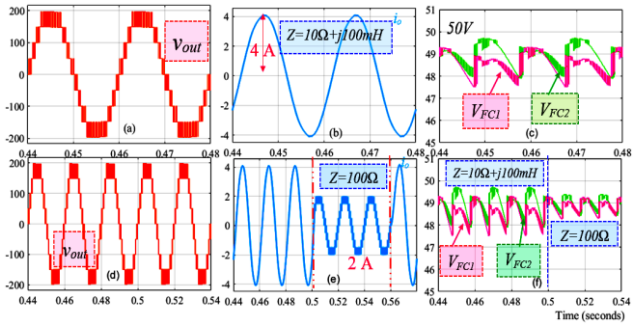

Fig. 5. Simulation results (a) output voltage (v_{out}), (b) load current (i_o), (c) voltages across the FCs (d)-(f) Under load varying condition (see Table III)

The input voltage is set to 100 V, and the chosen fundamental frequency is 50 Hz with a switching frequency of 5 kHz. The TLP 250 driver circuit is providing a dead time of 4 µs drive the IGBTs SKM 75GB063D with a rating of 600 V/75 A. A variable R-L load with a maximum power rating of 0.85 kW is employed as the load. The simulation results of the proposed topology are shown in Fig.5. The output voltage and current for *R= 40* Ω and *L=80 mH* are shown in Fig. 5 (a)-(b), respectively, and the voltage across the FCs is given in Fig. 5 (c) having a maximum ripple voltage of 5% (2.5 V). Further to validate the dynamic performance, the proposed topology is simulated for changing the load from resistive-inductive to resistive and the corresponding waveforms of v_{out}, i_o and V_{FC} are shown in Fig. 5 (d)-(f). It is confirmed that during sudden load changing, the FCs are able to maintain the voltage of 50 V with corresponding ripple voltages.

The experimental prototype model is shown in Fig. 6. Next, the experimental results are shown in Fig. 7 (a)-(j). The inrush current was the big challenge during the experimental validation due to the parallel connection of DC source and switched FC's. In order to limit the inrush current, a small inductor is inserted in circuit loop. The inductor value is chosen based on the ripple voltage, capacitor and inductor

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value. Here worth mentioning that inductor value is chosen as 0.05 *mH*.

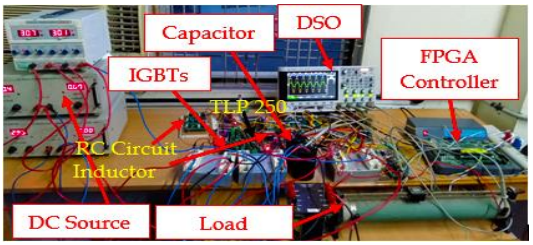


Fig.6. Hardware prototype model

Firstly, the output voltage and current waveform for R= 40 Ω, L=80 *mH* and R= 100 Ω are shown in Fig. 7 (a) and (b), respectively. The dynamic load variation is performed with R=100 Ω to R= 40 Ω, L=80 *mH* and corresponding waveforms are shown in Fig. 7 (c) and (d) with DC and AC coupling mode of FCs voltages. During load changes, the FC maintains the voltage with a small variation of ripple voltage. and the corresponding efficiency is 97.12%. Finally, a comparison of the proposed topology with other recent SCMLI topologies [3]-[20] is given in Table III. The various figures of merit are significantly chosen for assessing the topologies which are shown in Table III. A few topologies use the same or a smaller number of IGBTs than the proposed topology but the voltage stress on switch is high.

The topologies [5], [8] and [19] uses eight switches which significantly reduce the switch count and other supporting components but the maximum voltage stress *i.e* blocking voltage on the switch is equal to the output voltage whereas in our proposed topology has maximum blocking voltage of half of the output voltage which remarkable advantage of proposed topology over other high gain topologies. Since the proposed topology is derived from the [15] and [16], the switch count and losses are reduced with improved efficiency.

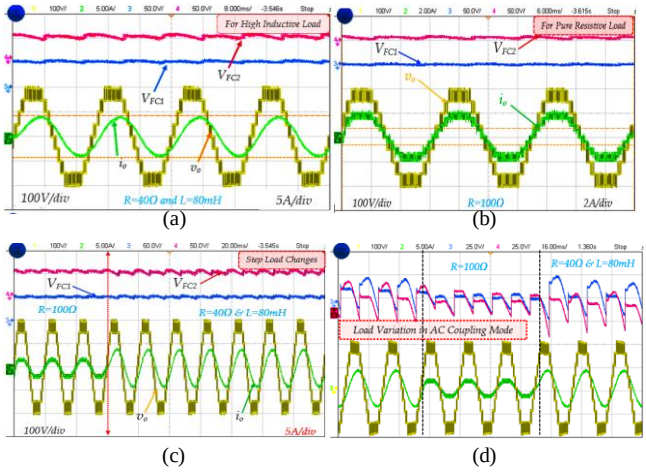
TABLE III
COMPARISON OF PROPOSED 9L INVERTER WITH OTHER RECENT SCMLI TOPOLOGIES

Ref	N_L	N_{SW}	N_{Dio}	N_{DC}	N_{FC}	N_{CP}	V_{FC}	FC_{max}	TSV	MBV	$N_{SD,L}$	$V_{o,max}$	H	G	τ	Efficiency (η)
[3]	9	13	-	1	3	7	v_{in}	1.0	25 v_{in}	4 v_{in}	6	4 v_{in}	1.0	4	3.0	85.9% @ 1 kHz
[4]	9	12	3	1	2	5	v_{in}	NA	24 v_{in}	4 v_{in}	6	4 v_{in}	1.0	4	2.0	NA
[5]	9	8	6	1	3	5	v_{in}	4.7	20 v_{in}	4 v_{in}	7	4 v_{in}	1.0	4	3.0	92.2%@ 0.4 kHz
[6]	9	10	2	2	2	5	v_{in}	1.8	20 v_{in}	4 v_{in}	4	4 v_{in}	1.0	2	1.0	88%@ 50 Hz
[7]	9	11	1	1	1	6	v_{in}	2.2	11 v_{in}	2 v_{in}	4	2 v_{in}	1.0	2	1.0	>96%@ 50 Hz
[8]	9	8	4	1	4	4	2 v_{in}	4.7	16 v_{in}	4 v_{in}	4	4 v_{in}	1.0	4	1.0	95.9 @ 50 Hz
[9]	13	16	2	2	4	7	v_{in}	2.5	33 v_{in}	6 v_{in}	8	6 v_{in}	1.0	6	2.0	92.1%@ 50 Hz
[10]	9	10	-	1	2	4	v_{in}/4	10	6 v_{in}	v_{in}/2	5	v_{in}/2	1.0	0.5	1.0	98.5%@ 50 Hz
[11]	9	12	-	1	1	5	v_{in}	1.0	8 v_{in}	v_{in}	4	v_{in}	1.0	1	1.0	92.3%@ 50 Hz
[12]	5	10	-	1	2	6	v_{in}	0.03	14 v_{in}	2 v_{in}	4	2 v_{in}	1.0	2	1.0	94.0@ 50 Hz
[13]	7	9	1	1	1	4	v_{in}	2.2	16 v_{in}	2 v_{in}	4	1.5 v_{in}	1.33	1.5	2.0	97.29% @50Hz
[14]	9	10	1	1	2	4	v_{in}/2	1.0	24 v_{in}	2 v_{in}	2	2 v_{in}	1.0	2	1.0	95% @ 50Hz
[15]	9	12	-	1	2	7	v_{in}/2	NA	11 v_{in}	v_{in}	4	2 v_{in}	0.5	2	1.0	80.61%@ 50 Hz
[16]	9	11	-	1	2	6	v_{in}/2	4.7	11 v_{in}	v_{in}	4	2 v_{in}	0.5	2	1.0	NA
[17]	9	12	-	1	3	6	2 v_{in}	4.3	24 v_{in}	4 v_{in}	5	4 v_{in}	1.0	4	1.0	96%@ 50 Hz
[18]	9	12	-	1	2	6	2 v_{in}	3.3	21 v_{in}	2 v_{in}	5	4 v_{in}	0.5	4	1.0	NA
[19]	9	8	3	1	3	4	v_{in},2 v_{in}	3.3	23 v_{in}	4 v_{in}	4	4 v_{in}	1.0	4	1.0	>93% @ 50Hz
[20]	9	9	1	1	2	5	v_{in},2 v_{in}	2.2	24 v_{in}	4 v_{in}	4	4 v_{in}	1.0	4	2.0	NA
Proposed	**9**	**10**	**2**	**1**	**2**	**5**	**v_{in}/2**	**1.7**	**9 v_{in}**	**v_{in}**	**4**	**2 v_{in}**	**0.5**	**2**	**1.0**	**97.12@50Hz**

N_L-Number of Level, N_{SW}-Number of switches, N_{Dio}-Number of Diodes, N_{DC}-Number of Sources, N_{FC}-Number of floating capacitors, N_{CP}-Number of switches on conduction path, V_{FC}(V)- voltage rating of FCs, FC_{max} (mF)- Maximum FCs capacitance value, TSV (V)-Total Standing Voltage, MBV (V)-Maximum blocking voltage on switches, $N_{SD,L}$- Number of devices in current loop (including diodes), $V_{o,max}$(V)- maximum output voltage , H= MBV/ $V_{o,max}$ (should be low), G-Voltage gain, τ- Ratio of number of times discharging and charging (should be low) , NA-Not Addressed

The modulation index variation is another important performance evaluation parameter in MLI topologies. The proposed topology is tested in variation modulation index variations form 0.4-0.6-0.8-1.0 and the corresponding waveforms are shown in Fig. 7 (e)-(g). Fig. 7 (h) depicts the sudden input changes from the 50 V to 100 V. It is confirming that the proposed topology is adopted to any load varying condition without affecting the output voltage level. The switch S_2 and P_2 are always high in proposed topology which is the sum of the charging of capacitors current and load current as shown in Fig. 7 (i). Further, the diode blocking voltage is 100 V and this diode is not always conducting during every half-cycle as shown in Fig. 7 (j). The obtained experimental waveforms are having a good agreement with simulation results. Further, the loss evaluation of the proposed topology is performed using the method described in [14]. The total power loss consists of switching, conduction and ripple losses. For unit power factor, with a load of 50 Ω @ 400 W, the maximum power loss is ~8 W in PLECS simulation tool and ~12 W in experiments. The detailed loss breakup is shown in Fig. 8

In proposed topology, two power diodes are additionally required over other topologies and the number of IGBTs is low with equal voltage stress. The diodes having high reliability, low cost and small in size as compared to IGBT. Where it is evident that the proposed topology scores over the other topologies in many aspects and is a promising alternative.



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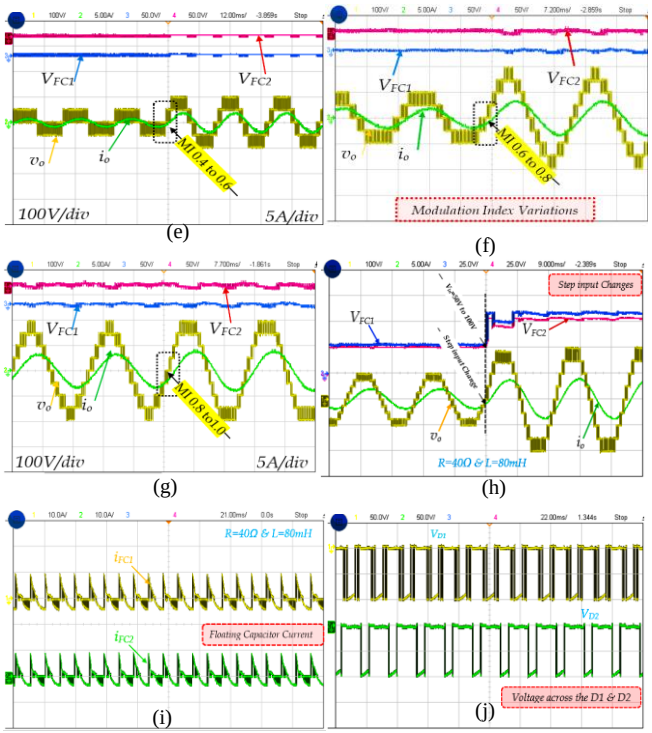

Fig. 7. Experimental Output voltage and current waveforms (a) for Resistive-Inductive load (b) for pure resistive load (c) and (d) Step load changes (e)-(g) Modulation index variations (h) Step input changes (i) FCs current and (j) diode voltage.

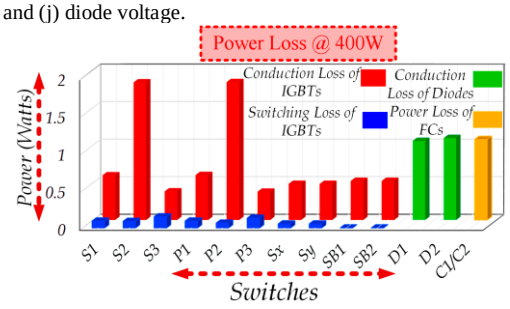

Fig.8. Power loss distribution at 400 W load

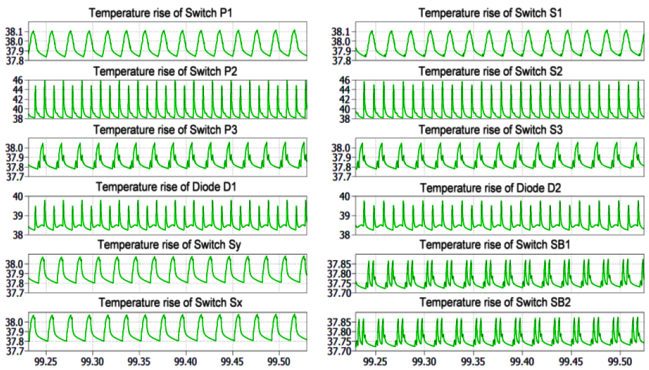

Fig. 9. Simulated thermal profile for each switches and diodes

The simulated thermal profile for each of the switches and diodes are given in Fig.9 and it is supportive to the claim that the P_2 and S_2 have high thermal stress due to their active part in the charging current path.

IV. Conclusion

A novel SCMLI employing the proposed CCS cell with a reduction the number of conducting switches and gate drivers is presented. The maximum blocking voltage of the individual switch is within v_{in}. Further, the number of times of charging and discharging of FCs are equal, giving in least capacitance requirement. The developed simple logic gate based PWM scheme is devoid of any sensors to balance the FCs and thus, makes the proposed topology more cost-effectiveness. The presented simulation and experimental results have validated the principle of operation and demonstrated the capability of the proposed topology in handling a variety of load cases. Finally, the detailed comparative study affirmed the merits of the proposed topology in comparison to recent studies and thus proving its suitability for various applications, especially in grid-interactive photovoltaics. Further, the proposed cell can be applied to other MLI families yielding many other interesting topologies.

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