NoisFre: Noise-Tolerant Memory Fingerprints from Commodity Devices for Security Functions

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Abstract—Building hardware security primitives with on-device memory fingerprints is a compelling proposition given the ubiquity of memory in electronic devices, especially for low-end Internet of Things devices for which cryptographic modules are often unavailable. However, the use of fingerprints in security functions is challenged by the small, but unpredictable variations in fingerprint reproductions from the same device due to measurement noise. Our study formulates a novel and pragmatic approach to achieve highly reliable fingerprints from device memories. We investigate the transformation of raw fingerprints into a noise-tolerant space where the generation of fingerprints is intrinsically highly reliable. We derive formal performance bounds to support practitioners to easily adopt our methods for applications. Subsequently, we demonstrate the expressive power of our formalization by using it to investigate the practicability of extracting noise-tolerant fingerprints from commodity devices. Together with extensive simulations, we have employed 119 chips from five different manufacturers for extensive experimental validations. Our results, including an end-to-end implementation demonstration with a low-cost wearable Bluetooth inertial sensor capable of on-demand and runtime key generation, show that key generators with failure rates less than 10⁻⁶ c an be efficiently obtained with noise-tolerant fingerprints with a single fingerprint snapshot to support ease-of-enrollment.

Index Terms—Hardware Fingerprinting, Memory Fingerprinting, SRAM, Flash, EEPROM, Root Key, Error Reconciliation.

1 INTRODUCTION

Various schemes have investigated fingerprinting commercial-off-the-shelf (COTS) devices to build security applications: verifying the provenance of integrated circuits (IC) to guard against counterfeiting by fingerprinting IC packages [1]; identifying unlawful 3D printed products by fingerprinting unique textures resulting from 3D printers [2]; authenticating smartphones by fingerprinting the Photo-Response Non-Uniformity of a camera image sensor [3]; and identifying commodity mobile devices by fingerprinting on-board sensors [4], [5].

Compared with fingerprinting methods for on-board sensors and other components like central processor units (CPUs) [1], [3]–[11], fingerprinting embedded memories including static random access memory (SRAM) [12]– [14], dynamic random access memory [15], Flash memory [16], [17], and electrically erasable programmable readonly memory (EEPROM)—pervasively embedded in COTS devices is a highly desirable proposition for provisioning security functions, especially in the absence of cryptographic modules. Fingerprinting embedded memory is attractive because: i) memory cells are intrinsic to computing platforms and available in large volumes to obtain many independent

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fingerprints or secret keys; ii) memory biometrics provides a physical source of true randomness; iii) it removes the need for a protected non-volatile memory for secrets (root keys can be generated on-demand and "forgotten" after usage); and iv) imparts no extra hardware costs to existing COTS devices such as medical devices, wireless sensors, credit cards, wearable devices, and a plethora of low-end Internet of Thing (IoT) devices, which are projected to grow to 75.44 billion worldwide by 2025 [18].



Fig. 1: Conventional schemes extract *raw* fingerprints from individual memory cells, such as from the random power-up state of each SRAM cell. However, raw fingerprints \mathbf{f}'_i regenerated at different time instances from the same device can mismatch a reference raw fingerprint template \mathbf{f} due to native bit errors introduced by noise \mathbf{e}_i . The red curves in the *fingerprint symbol* depict errors resulting from noise.

1.1 The Challenge

Whenever a fingerprint is generated from the same device, the digitized fingerprint should be exact for its use in security functions. However, fingerprints generated at different time instances are susceptible to unpredictable noise, such as thermal noise, supply voltage fluctuations, and device aging, and, consequently, differ in some bits. First, the positions of flipped raw bits vary. Second, the number of flipped raw bits varies from time to time. Thus, it is challenging to determine reliable raw bits, and existing memory fingerprinting schemes cannot naturally tolerate noise in the raw, noisy fingerprint space. Therefore, it is often infeasible to regenerate a fingerprint identical to a reference template that is securely stored (e.g., in a server) for directly building security functions between it and devices, as shown in Fig. 1.



Fig. 2: Illustrating the use of noise-tolerant memory fingerprints from commodity devices for security functions. We transform the raw fingerprint from an *n*-dimensional noisy fingerprint space to an *m*-dimensional space, we refer to as the noise-tolerant fingerprint space, where m < n. In the noise-tolerant space, as long as the noise \mathbf{e}_i is less than a bound θ , the regenerated and transformed fingerprint can be correctly projected to the reference transformed fingerprint template \mathbf{F} securely enrolled and stored on the server. Red curves in the *fingerprint symbol* depict errors in the raw fingerprint upon regeneration at time instances t_1 to t_3 . Now, the \mathbf{F} obtained can serve as a root of trust or a root key for a security function.

Until now, using approximate and noisy renditions of biometric fingerprint templates in security functions has been demonstrated to be possible with fuzzy extractor (FE) based methods [19], [20]. The FE employs a generation function to transform "fuzzy" biometrics into private secrets together with helper data used in a subsequent reproduction function to reconcile errors and derive the exact private secret from an approximately close template of the original biometric [21]-[23]. Employing an FE on a device leads to two fundamental problems: i) the computation overhead introduced on a device by FE logic is high [24] and ii) the associated helper data can be actively manipulated, in helper data manipulation (HDM) attacks, to weaken or even compromise the security of the derived fingerprint or private secret [25], [26]. A generic countermeasure against HDM attacks remains an open challenge [26].

Hence, there remains a significant leap between the desire for re-purposing ubiquitously available memory for security functions and the practicability of exploiting memory fingerprints for security.

While the notion of exploiting tiny hardware fabrication variations to generate memory fingerprints is not new, we challenge the traditional method of reliable fingerprint provisioning and pose the following research questions (RQs):

RQ1: How can we extract *intrinsically reliable fingerprints* from device memories?

RQ2: If an approach does exist, is the method *pragmatic* and *usable* for fingerprinting memory resources on pervasive commodity computing devices?

1.2 Our NoisFre Concept

Current memory fingerprinting schemes extract a fingerprint bit from each memory cell. Fingerprinting under this scheme is susceptible to noise. To the best of our knowledge, for commodity memories, existing techniques fail to accurately capture the noise-tolerance degree of each raw bit to formally determine those extremely reliable bits for direct key usage without the problematic error reconciliation.

We recognize that device memories are a cost-free and abundant source of entropy. Attributing to the everdecreasing fabrication costs, the size of memory pervasively embedded within devices has become increasingly large. Hundreds of kilobytes (KiB), even in low-end devices, are common (see the devices we tested in Table 1). Consequently, we envision that the entropy of extracted information may be sacrificed for improved reliability. Therefore, we propose the concept of transforming the raw fingerprint space of high information density into a lower-dimensional space with the attribute of being largely invariant to noise bit flips—observed in the digitized raw fingerprint space or memory biometrics. We refer to this noise-tolerant memory fingerprinting concept as **NoisFre**.

We illustrate our concept in Fig. 2. Building upon a raw memory biometric source that is a noisy fingerprint space, we propose extracting new fingerprints \mathbf{F} in the deliberately transformed noise-tolerant fingerprint space, which can tolerate a desirable noise bound θ . Here, as long as the noise \mathbf{e}_i induced number of raw fingerprint bit errors is less than θ , the regenerated and transformed raw fingerprints are guaranteed to be *projected* to its reference counterpart \mathbf{F} enrolled at the server. More generally, the regenerated and transformed fingerprint \mathbf{F} is insensitive to bit errors (resulting from noise) in the raw fingerprint space. Therefore, it can be directly employed—without error reconciliation—as a root key in a security function, despite the noisy renditions of the raw fingerprints at times t_1 , t_2 , and t_3 .

Significantly, we recognize that the best strategy for fingerprint memory is not always directly from the raw noisy fingerprint space, such as directly treating the power-up state of an SRAM memory of a cell as a fingerprint bit, the foundation for all current memory fingerprinting schemes. We argue for exploiting the freely available, abundant entropy of memories. We do not focus on individual raw fingerprint bits but seek to find an invariant property of a group of raw bits to measure, so we can be less concerned of the complexity about the process generating those bits.

1.3 Contributions and Results

• We *exploit the freely available and abundant* entropy from memories to propose a *new concept*—NoisFre—for highly reliable fingerprinting of commodity device memories. The principle is based on transforming from a noisy raw fingerprint space to a lower dimensional, noise-tolerant fingerprint space capable of reconciling noise inherent across multiple measurements of the same raw fingerprint. To corroborate the proposed No-isFre concept, we have developed two specific transformation methods: i) S-Norm and ii) D-Norm (**RQ1**).

- We formulate analytical models with the expressive power to support the design of security functions and evaluate the transformation methods. We express i) an upper bound for the unreliability of the transformed F bits with respect to the transform function parameters; and ii) the expected fingerprint extraction efficiency—the number of transformed F bits that can be extracted from a given memory size (**RQ2**).
- We conduct elaborate and extensive evaluations with a synthetic chip model to obtain the massive number of repeated fingerprint measurements necessary to validate our formalization of unreliability and extraction efficiency. Billions of repeated measurements were simulated using the synthetic chip model with bitlevel modeling capable of capturing bit-error behavior in SRAM device memories. Our formal models are confirmed to be worst-case bounds in practice (**RQ2**).
- We extensively test: i) 110 SRAM memory devices from three different manufacturers to experimentally validate NoisFre performance. We focus on SRAM memory, as it is the most commonly embedded memory, especially for low-cost IoT devices. Further, we employ: ii) seven Flash memories and iii) two EEPROM memories for validating the *generalizability* of NoisFre (RQ2).
- To demonstrate the expressive power of our formalization, we investigate the derivation of a root key the foundation for realizing various security functions. We demonstrate a 128-bit root key with an extremely low key failure rate of less than 10⁻⁶ can be directly obtained by transformed fingerprints to obviate the need for costly noise reconciliation. Significantly, a fingerprint snapshot or single measurement is sufficient for enrolling a key, a process we follow in all our experiments (**RQ2**).
- As a case study, we *implement a NoisFre key generator* and a security function on a low-end wearable Bluetooth inertial sensor. We extract a root key directly from native SRAM fingerprints transformed into noisetolerant *F* bits for use in a remote attestation primitive. By fundamentally obviating the state-of-the-art method necessary for reconciling noisy key bits, we demonstrate a significant overhead reduction (i.e., 54% compared to reverse FE and 82% compared to FE) and enhanced security. By utilizing the power isolation features, we also demonstrate the realization of *run-time and on-demand generation of robust SRAM fingerprints* F on this low-end device. A video demo is available at https://youtu.be/O5NWZw-swpw (RQ2).
- We release the 100 chip SRAM memory fingerprint dataset that we collected and opensource code artifacts to facilitate future research at https://github.com/AdelaideAuto-IDLab/NoisFre.

2 BACKGROUND

We concisely describe the well-known methods of fingerprinting memories. Then we briefly introduce the commonly accepted (reverse) FE to reconstitute a "fuzzy" secret into cryptographic secrets for security functions.

2.1 Fingerprinting Device Memories

We consider the widely used, specifically in low-end devices, SRAM, Flash, and EEPROM memory fingerprinting. As for the SRAM memory, when SRAM is powered up, each cell exhibits a *favored power-up state*; such an initial state varies from cell to cell and chip to chip. Therefore, each SRAM cell's power-up state is treated as a fingerprint bit. Fingerprinting SRAM is closely related to the SRAM physical unclonable functions [12], [13].

To extract fingerprints from Flash memory [16], [17], all Flash cells on the same page are first erased to "1". Then partial programming is applied. As a result of tiny fabrication variations, some cells will remain in state "1" while others flip to "0". Which cell remains or flips is determined by the random and uncontrollable fabrication process variations. One can treat whether a cell flips as the fingerprint bit—a flip as logic "0", and otherwise "1". The partial programming period is pre-determined to ensure balanced "0"/"1" bits in practice. The same procedure is applicable to fingerprint EEPROM.

2.2 Reliable Secrets with Fuzzy Extractors

A widely accepted method to turn noisy hardware fingerprint bits (key material) into usable cryptographic keys is to use an FE [19], [20]. In general, the FE consists of two procedures: i) a secure sketch and ii) an entropy extraction. The secure sketch reconciles errors in the regenerated bits. The entropy extraction (e.g., a cryptographic hash function) compresses the bits into a uniformly distributed cryptographic key with full bit entropy.



Fig. 3: The fuzzy extractor (FE) and the lightweight state-of-the-art reverse fuzzy extractor (RFE) for reconciling noisy fingerprint responses with the aid of helper data **p**. In an RFE the encoding is embedded in a device and the computationally heavy decoding is offloaded to the server.

The secure sketch construction has a pair of operations, as shown in Fig. 3: i) encoding and ii) decoding. Typically, in the FE setting, the encoding employing an error correction code (ECC) encoder is executed by the server during the fingerprint template enrollment phase to compute helper data p (redundant information). The decoding employing an ECC decoder is performed on the in-field device to recover a reliable fingerprint, sk. By recognizing that the encoding function's computational burden is significantly higher than decoding, it is feasible to place the ECC encoder on the device-side while leaving the computationally complex ECC decoder to the resource-rich server; this method is termed reverse FE (RFE) or reusable FE [19], [27], [28]. More specifically, the encoding function is implemented on the device-side to produce the associated helper data \mathbf{p}' as well as an $\mathbf{s}\mathbf{k}'$ based on on-device fingerprint evaluation \mathbf{f}' , where \mathbf{p}' is now sent to the server to assist the reconstruction of $\mathbf{sk'}$. Now, $\mathbf{p'}$ and $\mathbf{sk'}$ could vary every time as the ondevice fingerprint \mathbf{f}' can differ during each reevaluation. In

contrast to an FE setting, the server uses the enrolled f along with p' for recovering the key sk'.

3 NoisFre Transformation

We provide the impetus for developing NoisFre fingerprinting and its key insights, followed by two specific and *practical* NoisFre transformation methods.

3.1 Our Pragmatic Approach



Fig. 4: NoisFre transformation concept. A group of raw bit vectors exhibiting errors measured at different times can be transformed into the same NoisFre fingerprint bit F (e.g., "0"), attributing to the *invariance of the transform* patterns to: i) *permutations* of raw bit vectors (e.g., at time t = 0 and t = 1) and ii) vectors with different *combinations* of raw bits (e.g., at times t = 2 and t = 3)

In contrast to extracting one fingerprint bit from each memory cell, we propose a many-to-one transformation possessing a *property of invariance* to underlying raw bit patterns: more generally, invariant to the unpredictable, complex and dynamic raw fingerprint generating processes. Our desire is to project all of the fingerprint measurements conducted from the same block of memory at different time instances to the *exact* same transformed bit, $F \in \{0,1\}^1$. The concept is illustrated in Fig. 4. Note that:

- Bit errors leading to permutations of raw bits—where the positions of "1" and "0" values change in a bit vector but the number of "1"s and "0"s do not, as seen at t = 0 and t = 1 in Fig. 4—are projected to the *exact* same transformed bit $F \in \{0, 1\}^1$.
- Bit errors leading to vectors constituting different combinations of "1"s and "0"s (e.g., the fingerprint from the same block of memory at time *t* = 1 with two "1" binary bits and that regenerated at time *t* = 2 with only one "1" binary bit in Fig. 4) are projected to the *exact* same transformed bit *F* ∈ {0,1}¹.

We observe that a transformed bit, F, is able to mitigate the impact from multiple raw fingerprint bit errors manifesting as permutations or combinations of an *n*-bit raw fingerprint, **f**. The concept we propose is surprisingly simple but efficient and practical because of the *important but inadvertent* reality of large memory volumes intrinsic to devices. From a practical consideration, our critical insight is that memory embedded within modern electronics is large and *provides abundant entropy* to be exploited without additional costs for security functions. This fact is the foundation for our NoisFre transformation method: *trade-off entropy for reliability*.

This work proposes two specific NoisFre transformation methods: Single ℓ 1-Norm (S-Norm) and Differential ℓ 1-Norm (D-Norm).

3.2 Single *l*1-Norm Transformation (S-Norm)

The l1-Norm of a vector is the distance of the vector from an all-zero vector—or the Hamming weight of a vector, as described in Definition 1.

Definition 1 (ℓ 1-**Norm**). Let **f** be a binary vector length *n* representing a noisy raw fingerprint where f_j is the j^{th} bit in **f**; then the ℓ 1-Norm of **f** is defined as:

$$\|\mathbf{f}\|_1 \triangleq \sum_{j=1}^n f_j. \tag{1}$$



Fig. 5: NoisFre transformation via S-Norm; the transformed bit F is extracted using the l1-Norm of a group of raw bits. The group size is an odd integer number (e.g. 7 in this illustration) to ensure a balance between zeros and ones in the F bits. We illustrate the regenerated raw fingerprints from two blocks of memory—**Block 1** and **Block 2**—at times t = 0, 1, and 2.

Interestingly, an ℓ 1-Norm of a vector is permutation invariant. Hence, a new bit F can be obtained by applying an ℓ 1-Norm over a raw fingerprint vector \mathbf{f} as $\|\mathbf{f}\|_1$ and as described by the S-Norm below.

Definition 2 (S-Norm). Let the *i*-th raw fingerprint bit vector of *n* bits, where *n* is an odd integer, be \mathbf{f}_i . Then S-Norm transform is defined as:

$$F = \begin{cases} 1, & \|\mathbf{f}_i\|_1 \ge \left[\frac{n}{2}\right] \\ 0, & \|\mathbf{f}_i\|_1 \le \left[\frac{n}{2}\right] \end{cases}$$
(2)

An illustrative example of S-Norm-based transformation is provided in Fig. 5. When $\|\mathbf{f}\|_1 > \frac{n}{2}$, where *n* is an odd integer, the F bit is "1", and otherwise "0". This transform has the first desirable property of being insensitive to bit errors manifesting as permutations of a raw fingerprint f. For example, despite the raw bit errors at time t = 1 for the raw fingerprint from **Block 1** that lead to a permutation in respect to the bit vector referenced at time t = 0, the corresponding ℓ 1-Norm remains invariant; the memory **Block 1** is still projected to F = "0". The transform has the second desirable property of being insensitive to bit errors manifesting as combinations of an *n* raw fingerprint bit vector. Notably, errors that lead to different combinations of raw binary "1" and "0" values can increment or decrement ℓ 1-Norm but these can still be projected to the same transformed F bit. For example, see ℓ 1-Norm values for memory **Block 1** at time t = 1 compared to t = 2 in Fig. 5. Hence, S-Norm achieves the two qualities we desire from a transform expressed in Section 3.1.

In Fig. 5, we can expect the transformed F bit from **Block 2** with ℓ 1-Norms at the decision boundary, defined in equation (2), to more likely be affected by error bits within the raw fingerprint, resulting in different combinations of an *n*-bit raw fingerprint. A resulting combination of *n* bits with a single change in the number of raw binary "1" bits can lead to an ℓ 1-Norm projection that crosses the

decision boundary. We recognize the resulting F bits from such raw fingerprints to effectively display low reliability. Therefore, we propose winnowing raw fingerprints based on treating ℓ 1-Norm as a reliability measure for F bits. For this purpose, we define the S-Norm-based Selection method described in Definition 3 and generalize the approach using a noise tolerance parameter θ to provide an upper bound of tolerance on raw bit errors or the combinations of n-bit patterns; the transform will faithfully project to a specific F bit. Interestingly, the evaluation of ℓ 1-Norm only require a single measurement, while a larger θ can be chosen to facilitate higher noise tolerance. Therefore, we propose selecting based on the ℓ 1-Norm of raw fingerprint vectors obtained from a single measurement defined as being at time t = 0. Notably, this approach facilitates rapid characterization of raw fingerprints from device memories, as ℓ 1-Norms can be acquired in a single measurement. All our experimental and theoretical analyses assume such a characterization.

Definition 3 (S-Norm-based Selection). Let the raw fingerprint in the *i*-th *n*-bit block extracted at time *t* be \mathbf{f}_i^t . Then for a chosen noise tolerance parameter $\theta \in \mathbb{N}^0$, an extracted raw fingerprint vector \mathbf{f}_i^0 is selected at time t = 0 if:

$$\|\mathbf{f}_{i}^{0}\|_{1} \leq \lfloor \frac{n}{2} \rfloor - \theta \quad \text{or} \quad \|\mathbf{f}_{i}^{0}\|_{1} \geq \lceil \frac{n}{2} \rceil + \theta \tag{3}$$

To understand and demonstrate the significant role of the noise tolerance parameter θ in the mitigation of raw bit errors, we consider the distribution of $\|\mathbf{f}^0\|_1$. We used the experimental dataset obtained from Nordic Semiconductor chips detailed in Table 1. Fig. 6 plots the resulting distribution of enrolling measurements (at time t = 0) for two cases of a small and a large θ for an \mathbf{f} of n = 15-bit. As expected, the distribution of $\|\mathbf{f}^0\|_1$ approximates a bell curve.

Consider the groups of \mathbf{f}^0 raw fingerprints (green bar) at the boundary of the selection criteria in equation (3), where $\|\mathbf{f}_i^0\|_1 = \lceil \frac{n}{2} \rceil + \theta$ for the two cases of a small and large θ . These groups represent those closest to the decision boundary, $\|\mathbf{f}_i^0\|_1 = \lceil \frac{n}{2} \rceil$ (green line), consequently representing those most likely to lead to a bit error in a transformed bit F when raw bit errors changes the ℓ 1-Norm of \mathbf{f}^0 . When θ is small ($\theta = 2$), a change in more than two bits in a given pattern can lead to $\|\mathbf{f}\|_1$ crossing the decision boundary $\frac{n}{2}$ in a subsequent raw fingerprint extraction, resulting in a Fbit flip.



Fig. 6: Illustrating the role of the noise tolerance parameter θ in S-Normbased selection. The plots show the ℓ 1-Norm distribution of raw noisy fingerprints. It approximates normal distribution. A larger θ ensures the transformed F bits can tolerate a higher degree of noise.

In contrast, when θ is large, set to 4, the ℓ 1-Norm of the selected fingerprint vectors or $\|\mathbf{f}^0\|_1$ are further away from the decision boundary. Consequently, a change in more than four bits in a \mathbf{f} is needed to flip the corresponding F in a subsequent fingerprint evaluation. Such a probability is

Observation 1: The S-Norm $\|\mathbf{f}\|_1$ yields a representation analogous to the reliability of the new bit F.

Observation 2: The S-Norm transformed bits are invariant to permutations and combinations of raw bit patterns. Further, θ provides a desirable lower bound on raw bit errors tolerated by the transform.

Observation 3: There is an expected trade-off evidence in Fig. 6. While increasing θ increases the noise tolerance of the transform, it reduces the number of noise-tolerant fingerprint bits extractable from a given memory.

3.3 Differential *l***1-Norm Transformation (D-Norm)**

Considering *Observation 3* and the distribution in Fig. 6, we recognize that *a distance measure capable of presenting a bimodal distribution could provide an intrinsic separation of groups of underlying raw fingerprint bits* with the potential to yield higher numbers of noise-tolerant bits. We hypothesize that a differential distance measure may afford such a desirable distribution and propose the D-Norm transform based on a differential distance measure.

Definition 4 (D-Norm). Let the lowest and highest l1-Norm of m groups (each group is an n-bit vector) be l and h, respectively, where:

$$h \triangleq \arg \max_{\mathbf{f}_i \mid i \in \{1,..,m\}} (\|\mathbf{f}_i\|_1) \tag{4}$$

$$l \triangleq \underset{\mathbf{f}_i \mid i \in \{1,..,m\}}{arg \min} \left(\|\mathbf{f}_i\|_1 \right) \tag{5}$$

Now, following the general definition in Section 3.1, the D-Norm transform is defined as:

$$F = \begin{cases} 1, \ h-l \ge 0 & \text{and} & [h] < [l] \\ 0, \ l-h < 0 & \text{and} & [h] > [l] \end{cases}$$
(6)

Here, we denote the spatial index *i* (memory address, in practice) of the vector \mathbf{f}_i chosen for *h* based on equation (4) or *l* based on equation (5) using a square bracket, "[]".

The D-Norm-based transformation is illustrated in Fig. 7. In the illustration, the ℓ 1-Norm of two blocks of m = 3 groups of n = 8 bit vectors are evaluated at time t = 0. In subsequent evaluations of the fingerprint at t = 1:

- In Block 1, we can observe the *permutation invariance property*, similar to the S-Norm. For example, the highest ℓ 1-Norm at t = 0 and t = 1 is h = 5 for the third 8-bit vector despite repeated generation of the raw bits not being exact.
- In **Block 2**, we further observe the difference of h l is 6-1 = 5 at t = 0 and shows an *extreme case* of 3-3 = 0 at t = 1, where F bit of "1" remains invariant. Which reflects the *combination invariance property*.

In both **Block 1** and **Block 2**, the fingerprint bit F remains robust to the raw fingerprint bit error patterns observed at different measurement times. However, a combination of n bits with a single change in the number of



Fig. 7: D-Norm-based NoisFre transform illustration, where n = 8 and m = 3. We show the results of reading out two blocks of memory (**Block 1** and **Block 2**). Here, each block $(n \times m$ bits) is formed by accessing three bytes from a byte-level addressable memory, and each block provides a new bit *F*. Hence, the new bit *F* is a transformation from a block of raw bits with m = 3 groups, where each group is an n = 8 bit vector. The raw bit values are measured at two different time instances, t = 0 and t = 1, from each block to illustrate the manner in which the D-Norm transform is reliable against raw bit error.

raw binary "1" bits can lead a D-Norm projection at the proximity of the decision boundary in equation (6) to cross that boundary. Hence, the resulting F bits from such raw fingerprints effectively display low reliability. Therefore, similar to S-Norm, we propose winnowing raw fingerprints based on their |h - l| projections. We describe the *D-Normbased Selection* method in Definition 5 and generalize the approach using a noise tolerance parameter θ to bound the combinations of bit patterns the transform needs to tolerate, using the differential ℓ 1-Norm of the raw fingerprint vectors measured once (i.e., at t = 0).

Definition 5 (D-Norm-based Selection). From a block of *m* different *n*-bit raw noisy fingerprint vectors \mathbf{f}_i^0 for $i \in \{1, \ldots, m\}$ extracted at t = 0, the block is selected for fingerprinting the device using D-Norm if *h* and *l* as defined in equation (4) and equation (5) satisfy:

$$|h-l| \ge \theta \tag{7}$$

To understand the significance of the D-Norm-based selection method and the role of the noise tolerance parameter θ , we employ the Nordic Semiconductor chip fingerprint dataset used in S-Norm. The resulting distribution of enrolling measurements (at time t = 0) for two cases of a small and a large θ for blocks of $n \times m$ raw fingerprint bits is shown in Fig. 8. Interestingly, the distribution of |h - l|approximates a bimodal distribution; each mode represents those vectors mapping to F = "1" and "0", respectively. *Importantly, the two clear groupings of* $n \times m$ *bit blocks based on the D-Norm distance measure results in an intrinsic separation.*

Now, consider the blocks of h - l raw fingerprint bit vectors (green bar) in blocks at the boundary of the selection criteria, in equation (7), where $|h - l| = \theta$ for the two cases of a small and a large θ . These blocks of bits represent those most likely to lead to a bit error in a transformed bit *F*. When θ is small, e.g. $\theta = 2$, two bit flips in the raw fingerprint in a subsequent measurement is enough to push |h - l| across the h - l = 0 decision boundary, defined in equation (6), and result in a *F* bit flip. In contrast, when θ is large, e.g. $\theta = 4$, at least five raw fingerprint bit changes are required to flip the *F* bit in a subsequent evaluation.

Therefore, we can expect the F bits selected upon a larger θ to be more reliable.

The D-Norm method effectively sacrifices more of the available entropy ($n \times m$ raw bits are transformed into 1-bit F) than S-Norm. However, the differential distance measure h - l is bimodal and, thus, *D-Norm is expected to yield a significantly higher number of noise-tolerant* F bits.

4 FORMALIZING PERFORMANCE MEASURES

We now formulate and derive analytical models to: i) provide an upper bound for the unreliability of noise-tolerant fingerprint bits and ii) evaluate the expected number of noise-tolerant fingerprint bits that can be extracted from each of the transform methods—the *extraction efficiency*. We summarize the analytical formulations from our **detailed derivations differed to Appendix A** for interested readers.

4.1 Reliability

We employ the well-known measure of bit error rate (BER) to quantify the reliability of transformed fingerprint **F**:

$$BER_{\mathbf{F}} = \mathsf{FHD}(\mathbf{F}, \mathbf{F}') \tag{8}$$

where **F** and **F**' are two fingerprint measurements at distinct times from the same physical memory. The function FHD() is the fractional Hamming distance between the (binary) vectors **F** and **F**'. Commonly, **F** is a reference fingerprint template measured at t = 0, and **F**' is the reevaluation under a potentially different device operating condition, such as temperature, and, therefore, is subject to noise. A lower BER_F indicates higher tolerance to noise introduced from the raw fingerprints.

S-Norm Reliability. The expected BER of noise-tolerant fingerprints for the S-Norm transformation BER_F is formulated in equation (9); we defer details of the derivation to **Appendix A.2**:

$$BER_{\mathbf{F}} = \sum_{i=0}^{\lfloor \frac{n}{2} \rfloor - \theta} \left((1 - \mathsf{binocdf}(\theta + i, \lceil \frac{n}{2} \rceil + \theta, BER_{\mathbf{f}})) \times \mathsf{binopdf}(i, \lfloor \frac{n}{2} \rfloor - \theta, BER_{\mathbf{f}}) \right)$$
(9)



Fig. 8: The role of the noise tolerance parameter θ in D-Norm-based selection. The plots depict the differential ℓ 1-Norm distributions—the difference between the *h* and *l*—of raw fingerprints. The distribution of differences leads to a bimodal distribution. Here, n = 16 and m = 32, where $n \times m$ raw bits are transformed into a 1-bit *F*. If [h] has a lower memory address than [l], the D-Norm would be h - l which is positive and plotted on the right half of the x-axis (otherwise, left). The reliability of *F* increases when the ℓ 1-Norm difference between selected groups is away from 0. *Significantly, the proportion of F that tolerates a chosen noise tolerance* θ *is greatly increased under D-Norm compared to the S-Norm.* For example, the uncovered (gray area) for D-Norm is much larger than that of S-Norm in Fig. 6 for the same θ values.

Here, binopdf and binocdf are density and cumulative density functions of a binomial distribution, respectively. The BER_F is a function of θ , n and the BER of the raw noisy fingerprint bits, BER_f. If we select the worst-case BER_f of any memory chip, equation (9) provides a worst-case (upper-bound) assessment of BER_F.

D-Norm Reliability. A D-Norm transform employs a block of *m* groups—each group with *n* raw fingerprint bits—to be transformed into a 1-bit F. The BER_F of D-Norm is expressed in equation (10); we defer the derivation of the formula to **Appendix A.3**:

$$BER_{\mathbf{F}} = \sum_{i=0}^{n-\theta} \left((1 - \mathsf{binocdf}(\theta + i - 1, n + \theta, BER_{\mathbf{f}})) \times \mathsf{binopdf}(i, n - \theta, BER_{\mathbf{f}}) \right)$$
(10)

We can observe the reliability of transformed bits from the D-Norm to be related to θ (the selection criterion), *n* and BER_f. Again, equation (10) provides an upper-bound estimation when the worst-case BER_f is assumed. Notably, the BER_F is independent of the number of groups *m* within the block.

4.2 Extraction Efficiency

We define extraction efficiency η as the number of obtainable transformed bits, F, *subject to a given noise-tolerance* θ , from the total number of available memory bits expressed in KiB.

S-Norm Extraction Efficiency. The extraction efficiency of S-Norm can be expressed as below; the detailed derivation is deferred to **Appendix A.4**:

$$\eta_{\text{SNorm}} = \frac{1}{n} \times (1 - \mathsf{binocdf}(\lfloor \frac{n}{2} \rfloor + \theta, n, 0.5) + \mathsf{binocdf}(\lceil \frac{n}{2} \rceil - \theta - 1, n, 0.5)) \times (1024 \times 8)$$
(11)

Here, the term $1 - \text{binocdf}(\lfloor \frac{n}{2} \rfloor + \theta, n, 0.5)$ expresses the case when the $\ell 1$ -Norm of an *n*-bit **f** is larger than the selection threshold $\lfloor \frac{n}{2} \rfloor + \theta$, assuming that the probability of each bit being "1"/"0" is 50%. While the term $\text{binocdf}(\lceil \frac{n}{2} \rceil - \theta - 1, n, 0.5)$ formulates the alternative case when the $\ell 1$ -Norm of a *n*-bit **f** is less than or equal to $\lceil \frac{n}{2} \rceil - \theta - 1$. Both cases comprise vectors that satisfy the selection criterion in equation (3). We can see that the overall extraction efficiency should be the sum of the above two cases divided by *n*—recall that *n* raw bits transform into a 1-bit *F*. The 1024×8 term expresses the extraction efficiency as bit/KiB—number of selected reliable bits *F* out of 1 KiB memory.

D-Norm Extraction Efficiency. A D-Norm transform obtains a 1-bit F from a block of m, n-bit raw fingerprint vectors. We define the probability that a given block will meet the selection criterion ($|h - l| \ge \theta$) in equation (7) as $P_{\text{DNorm}}^{\text{select}}$ (recall that we refer to the lowest ℓ 1-Norm as l, and the highest ℓ 1-Norm as h, out of all m groups within a block). The direct derivation of $P_{\text{DNorm}}^{\text{select}}$ is non-trivial. Instead, we use a different but equivalent problem and defer the details to **Appendix A.5**. We formulate the extraction efficiency of D-Norm as:

$$\eta_{\rm DNorm} = \frac{1}{n \times m} \times P_{\rm DNorm}^{\rm select} \times (1024 \times 8)$$
(12)

Here, the term of $\frac{1}{n \times m}$ expresses $n \times m$ raw bits producing a single F bit, while the 1024×8 constant facilities express the result in terms of bits/KiB of memory. Given the complexity of formulating η_{DNorm} , the fitness of the formalized expression is further validated through running extensive numerical experiments (defined in Section 5), with the results detailed in Fig. 24 in **Appendix**.

4.3 Summary

Our formulation of *reliability* allows a security practitioner to evaluate, for a given transform, suitable transform parameters (e.g., the number of bits *n* to employ in a raw fingerprint vector **f** and noise tolerance parameter θ) for extracting new fingerprint **F**. The extracted **F** will have an expected worst-case error bound given by BER_F. Then, the η yields the total number of such noise-tolerant bits BER_F that can be extracted from a given memory size.

5 EXPERIMENTAL VALIDATIONS

For comprehensively evaluating NoisFre we used 119 commodity chips consisting of three memory types pervasive in COTS devices, especially in low-end IoT devices and extensive simulation based experiments with billions of bit generations to overcome the practical hurdle of demonstrating extremely low BER and key failure rates with physical chips. In the following:

- We validate our analytical models for *reliability* and *extraction efficiency*.
- We we assess the performance of the noise-tolerant fingerprints by evaluating the uniqueness and uniformity of **F**.

5.1 Evaluation Approaches

We consider three evaluation approaches described below.

Predictions (Analytical model). In this evaluation, we use the analytical models formalized in Section 4 to predict extraction efficiency and the BER_{F} of the transformed fingerprints.

Simulations (Synthetic chip model). To evaluate the reliability of the transformed fingerprint, a massive number of repeated measurements and the management of the data for analysis are required. For example, if we want to validate whether a 128-bit NoisFre enabled key can achieve a failure rate of 10^{-6} as done in Section 6.2, the BER_F needs to be no more than 7.81×10^{-9} . To test this with physical measurements, approximately 10^8 repeated measurements are required from the same chip instance. Such a measurement process would take more than nine years and generates roughly 6 Terabyte (TB) of data-this is merely for one 64-KiB chip. Such a massive testing regime is impractical, as detailed in Measurement (Physical chips). Instead, we employed a synthetic memory chip model (detailed in Appendix A.1). The model follows the physical unclonable function (PUF) response model summarized in [31] and assumes each bit to have a binomial probability of a bit flip across repeated measurements based on employing a worst-case BER measured from a physical SRAM chip (see Table 1) as the binomial probability parameter value for **p**. Using the

TABLE. 1: Memory Datasets.

Manufacturer Model ¹	Abbr	Tech Node	Memory Type	Memory Size	Quantity	Repeat Times	Operating Range ²	Enrolling Condition	Worst Condition	Worst $\operatorname{BER}_{\mathbf{f}}$
Nordic (ours) nRF52832	NORDIC	55 nm	SRAM	64 KiB	$12 + 88^{6}$	100	-15-80°C	25°C	80°C	6.09%
ISSI [29], [30] IS61WV25616BLL	ISSI	110 nm	SRAM	256 KiB	4	30	25-80°C	25°C	80°C	8.29%
IDT [29], [30] IDT71V416S	IDT	130 nm	SRAM	512 KiB	6	50	25-80°C	25°C	80°C	5.42%
Winbond [17] W29N02GV	Flash	46 nm	FLASH	69,696 Bytes/ 256 MiB ³	7	99	0-100,000 P/E Cycles	0th P/E Cycle	after 100,000th P/E Cycles ⁴	16.26%
Microchip (ours) 24LC256	EEPROM	350 nm	EEPROM	2 KiB/ 32 KiB ⁵	2	100	14-80°C	14°C	80°C	16.37%

¹The NORDIC and EEPROM datasets we collected will be released, remaining public datasets are from https://www.trust-hub.org/data.

²Notably these public datasets focus on room temperature and high-temperature evaluations. Other operating corners are incomplete.

³The tested Flash memory size in the public dataset is 69,696 bytes, while the total memory size is 256 MiB.

⁴Experimental studies demonstrate that the BER_f of Flash memory is mainly affected by the programming/erase (P/E) cycles, equivalent to wear-out or aging, but negligibly affected by voltage and temperature [17]. The maximum endurance is 100,000 according to the datasheet. ⁵The EEPROM chip has 32 KiB capacity, while the first 2 KiB memory is evaluated here.

⁶There are 12 chips with three corner measurements $\{-15, 25, 80\}$ °C and 88 chips with a single 25°C corner measurement.

synthetic chip model, for instance, 100 million (10^8) times of simulations can be completed in approximately 53 hours or 2.2 days using a laptop equipped with quad-core Intel Core i7-10510U CPU and 16 Gigabyte (GiB) RAM. The synthetic chip, models bit errors and when applied with the worst-case BER is sufficient for evaluating reliability and extraction efficiency. Therefore, we employ the data from the simulated measurements to determine η and the BER_F.

Measurements (Physical chips). Performing massive testing on physical chips is impractical. For example, obtaining 100 repeated measurements from an nRF52832 physical chip (in the NORDIC dataset) takes four minutes and 45 seconds, and this generates 6.25 Megabyte (MiB) of data (the SRAM memory size of the single chip is 64 KiB). Then, we can estimate that 100 million (10^8) repeated measurements for a single physical chip under a single operating corner will take 3,298.6 days (or nine years) and generate 5.96 TB of data. Therefore, we confirm extraction efficiency and the transformed fingerprints' BER validated using the synthetic chip model with a limited number of *repeated* physical chip measurements. However, we dedicate the physical chip measurements across a large batch of 100 chips to evaluate the quality of the transformed bits because properties such as fingerprint uniformity and uniqueness are affected by fabrication variations not incorporated in the synthetic chip model used for simulations. The datasets we used are described in Physical chips-Fingerprint Datasets below.

Physical chips–Fingerprint Datasets. Specifications of: i) three SRAM; ii) one Flash memory; and iii) one EEPROM datasets are summarized in Table 1 and described in detail in Appendix. C. Each dataset is obtained from chips from a *different manufacturer*. Further, the datasets describe multiple repeated measurements of raw fingerprint bits under *each* operating condition—see the operating range in Table 1.

We use the NORDIC dataset for extensive validations, considering the fact that it is collected with the broadest operating range and highest number of repeated measurements (100 repeated measurements). In addition, we use the remaining datasets to corroborate the generality of our approaches. When we evaluate the BER of transformed bits, BER_F, we report the average from repeated evaluations. Notably, the enrolled reference template is only based on the first *single measurement*.

5.2 Validating Extraction Efficiency and Bit Error Rate

We employ simulations with the synthetic chip model to conduct the necessary massive number of repeated measurements to assess the reliability of transformed fingerprint **F**. To generate the results, for each parameter combination (i.e., n, θ in S-Norm and m, n, and θ in D-Norm) of a NoisFre transform in Fig. 9 for S-Norm and Fig. 10 for D-Norm, we simulated *one million* repeated measurements using a synthetic chip with a memory capacity of up to 16 MiB¹

5.2.1 Using Simulations



Fig. 9: S-Norm BER_F and extraction efficiency η_{SNorm} validation using the synthetic chip model constructed based on the NORDIC chip dataset. The evaluation is conducted for different *n* and noisetolerance parameter θ , where θ ranges from 1 to n/2. Here, *n* raw bits are transformed into one *F* bit.

S-Norm. The evaluation results from S-Norm are detailed in Fig. 9 under various n and θ settings. Based on Fig. 9, we can confirm that the formalization of BER_F in equation (9) provides a conservative estimation of the selected F bits. The results for extraction efficiency are in good agreement with equation (11) used to predict the number of F bits that can be expected from a given chip.

D-Norm. The validation results of D-Norm are shown in Fig. 10. As expected, the BER_F plotted in Fig. 10 reduces substantially as the θ is increased. Again, we can confirm

^{1.} We start with a memory size of 64 KiB, the SRAM capacity of the NORDIC chip, but we double the size when a 128-bit \mathbf{F} cannot be obtained. Thus, for each parameter setting, at least 128 bits are ensured to be produced.

that the formalized BER_F in equation (10) is a conservative estimate because it is always shown to be higher than the synthetic chip model results. Further, the extraction efficiency derived in equation (12) provides an accurate prediction of the number of bits of **F** that can be expected from a given chip under various D-Norm settings (n, m, and θ).



Fig. 10: D-Norm BER_{**F**} and extraction efficiency η_{DNorm} validation on the synthetic chip model constructed based on the NORDIC chip dataset. The evaluation is conducted under different *n* and noisetolerance parameter θ where θ ranges from 1 to *n* and m = 4. Here $n \times m$ raw bits are transformed into one *F* bit.

5.2.2 Using Measurements

Three SRAM datasets (our NORDIC, public ISSI and IDT datasets); one Flash dataset; and our EEPROM dataset are used to validate the generality of the NoisFre approach based on *physical chip measurements*. The results of S-Norm and D-Norm validated on these five datasets are detailed in Fig. 11. In contrast to our simulation-based study in Section 5.2.1, here we use a synthetic chip of identical data capacity and worst-case BER_f matching the physical chip under investigation and simulate 100 repeated measurements in sympathy with the physical measurement regime.² Overall, we can observe from the plots in Fig. 11 that simulations with the synthetic chip model agree well with the measurements for both S-Norm and D-Norm.

Based on our comprehensive experimental validations on SRAM memories from three different manufacturers, Flash memories, and EEPROM memories, we can now conclude that our formalized model of the unreliability, BER_F, and extraction efficiency, η , in Section 4 are indeed reliable measures. Most importantly, the formalized models serve as bounds for BER_F and η in practice; the measurement results and synthetic chip model results are the same or better than those predicted by the analytical models.

5.3 Evaluating Uniformity and Uniqueness

In addition to the two crucial performance measures we formulated, reliability and extraction efficiency, we further consider measures that evaluate other qualities of the transformed bits in terms of *uniqueness* and *uniformity* (see [32] for a definition of these measures). In the following, our

evaluations are based on the measurements obtained from the 100 physical chips in the *augmented NORDIC dataset*.

Uniqueness Evaluation. Essentially, uniqueness measures how different the fingerprints are between devices. However, the formal definition of uniqueness based on fractional Hamming distance ³ [32] cannot be directly applied for **F** fingerprints because the transformed bits are generated from different physical memory blocks from chip to chip, and the number of such bits obtained could also vary from chip to chip. To account for this, we propose evaluating the uniqueness of S-Norm and D-Norm transformed finger-prints based on the following approach:

- Given a set of transformation parameters (such as n, m, and θ for D-Norm), we extract all the F bits for each of the N (i.e., 100) devices.
- 2) Given a pair of devices out of $\binom{N}{2}$, we identify the device which produces the **F** string with the smaller number of F bits within this pair, and truncate the longer bit string to the same length. Then, we calculate the fractional inter-chip Hamming distance for this pair.
- We repeat the process in Step 2) for all the ^N₂ pairs to obtain the uniqueness measurement over the 100-chip dataset.

The uniqueness of raw fingerprints, S-Norm fingerprints, and D-Norm fingerprints is illustrated in Fig. 12. The mean uniqueness of the raw fingerprints is 0.48, with a standard derivation of 0.037. For S-Norm, the mean uniqueness achieves the ideal value of 0.50 under all tested settings, and the largest standard derivation is 0.037 under the setting of $(n = 15 \text{ and } \theta = 7)$ and $(n = 47 \text{ and } \theta = 9)$. The mean uniqueness of the D-Norm fingerprints also exhibits the ideal value of 0.50, except for settings $(n = 32, m = 128, \theta = 16)$, but the mean uniqueness of 0.49 is still nearly the ideal value. In general, as the number of extracted fingerprints in a tested sample decreases, we also observe an increase in standard deviation; this is expected because of the resulting small sample size for statistical analysis.

Uniformity (Bias) Evaluation. Uniformity measures the balance between zeros and ones in a fingerprint vector. The uniformity distribution of raw fingerprints, S-Norm fingerprints and D-Norm fingerprints is illustrated in Fig. 13. The uniformity of the raw fingerprint is very close to the ideal value of 0.5, with a very small standard deviation. The uniformity of S-Norm and D-Norm methods—across the various parameter settings—is close to the ideal value, albeit with a slight bias toward "1". Notably, such slight biases are acceptable for key derivation and can be simply compensated by using a few more fingerprint bits when deriving a key [33].

6 DERIVING CRYPTOGRAPHIC KEYS FOR SECU-RITY FUNCTIONS

We demonstrate the *expressive power of our formalization* by investigating the derivation of root keys from commodity memory chips facilitated by our analytical models. The

^{2.} One hundred measurements are due to the impracticality of conducting the necessary number of repeated measurements with physical chips, as detailed in Section 5.1

^{3.} Fractional Hamming distance (FHD) is a distance measure between two vectors of equal length, defined as the number of positions in the two vectors with different values, normalized by the vector length.



Fig. 11: S-Norm and D-Norm validation on the datasets including three types of SRAM memories from three different manufacturers (NORDIC, ISSI, and IDT), one type of Flash memory, and one type of EEPROM memory with S-Norm setting (n = 63) and D-Norm settings (n = 64, m = 4). Note (1): the number of repeated measurements is finite (see Table 1) and inadequate to demonstrate any errors when the expected BER_F is considerably less than 1/(number of repeated measurements).



Fig. 12: Uniqueness evaluation using physical nRF52832 chips. The plots summarize the mean (μ) and standard deviation (σ) across a subset of S-Norm parameters, S(n, θ), and D-Norm parameters, D(n, m, θ) applied to our large dataset of 100 chips.



Fig. 13: Uniformity evaluation using physical nRF52832 chips. The plots show the mean (μ) and standard deviation (σ) for uniformity across a subset of S-Norm parameters, S(n, θ), and D-Norm parameters, D(n, m, θ) applied to our large dataset of 100 chips.

dynamic and direct generation of cryptographic keys from memory fingerprint transformations into noise-tolerant bits is a basis for building security functions because: i) memory biometrics is a true source of randomness and ii) it removes the need for a protected non-volatile memory—keys can be generated on-demand and *"forgotten"* after usage.

In the following sections, we elaborate on a method for employing the new fingerprint \mathbf{F} obtained from the NoisFre transformation to realize a cryptographic key generator (Section 6.1) and evaluate the practical realization of such a key generator (Section 6.2); we defer the security analysis of the key generation process to Section 8.3.

6.1 A Method for Realizing a NoisFre Key Generator

A typical memory fingerprint-based key generation method involves two steps: i) a one-time secure key enrollment on the server-side and ii) on-demand secure key regeneration on the device-side [22], [24], [34], [35]. Positions of transformed bits F should be provisioned during the key enrollment phase and provided during the key regeneration phase. We refer to these positions using a **mask**. Recall that we have referred to those raw bits that produce a 1-bit F as a block. For the S-Norm, one block has n raw bits, while one block has $n \times m$ raw bits in the D-Norm; for both methods, n raw bits form one ℓ 1-Norm. In the discussion that follows, we consider key generation under two practical settings:

- Devices with write once read many (WORM) memory for storage of the mask defined to select the memory regions to be used in the NoisFre transform prior to deployment.
- Devices without WORM memory where the mask has to be transmitted, for example, through a wireless com-

munication channel.

6.1.1 On-Server Secure Key Enrollment

First, we describe the one-time secure key enrollment process, depicted in Fig. 14. This process is performed in a secure environment by the server.



Fig. 14: NoisFre secure key enrollment process. The raw fingerprints are extracted and used in the NoisFre Transform Selection process (as defined in equations (6) and (7) for D-Norm) to determine the selected memory addresses (**mask**) for subsequent use in security functions. Although we have only focused on the generation of a single mask, several masks may be defined to allow the server to subsequently generate different secret keys on-demand.

Protocol. The one-off on-server secure key enrollment protocol with NoisFre is as follows:

- 1) Fingerprint memory is a memory region from which the raw device memory fingerprint **f** is extracted.
- 2) The raw fingerprint f is processed by the server. The NoisFre Transform Selection process determines a noisetolerant fingerprint vector F and the corresponding mask based on the parameters n, m, and θ determined by a security practitioner. Notably, a practitioner can employ the analytical expressions derived in Section 4 to determine the appropriate parameter values.
- Both F and the mask are stored in the server's secure database (DB, indexed by, for example, the device identification number [id], although not explicitly shown here for simplicity).
- 4) *Optionally,* the **mask** can be stored inside the device's WORM memory.

6.1.2 Dynamic On-Device Secure Key Generation

Now, we consider the realization of on-device secure key generation with a device memory fingerprint biometric. We illustrate the key generation method in Fig. 15.

Protocol. The dynamic on-device secure key generation protocol with NoisFre is as follows:

- 1) If the device implements WORM memory to store the **mask**, as in Fig. 15 (a), the server fetches device-specific information from the **DB**, such as the enrolled **F**.
- 2) If the device does not implement WORM memory, the server fetches device-specific information from the DB, such as the enrolled F and mask, as in Fig. 15 (b). The mask is transferred from the server to the device over a (non-secure) wireless communication channel. To ensure the integrity of the mask, a message authentication code (MAC) tag is computed by the server as tag ← MAC_F(mask) and appended to the mask.

- 3) The device dynamically generates a new noisy raw fingerprint **f**' from the fingerprint memory.
- The device computes F ← NoisFre.Transform(f', mask), where NoisFre.Transform() is a function defined by, for example, the D-Norm transform in equation (6).
- 5) If the device does not implement a WORM memory, then the mask is sent by the server, as shown in Fig. 15 (b); the device computes tag' ← MAC_F(mask). To check the integrity of the mask, the tag' is compared to the tag supplied by the server. If the two values match, output the NoisFre fingerprint F; otherwise, output ⊥.
- 6) Now both the server and the device share the same highly reliable F to be used as a shared secret in a security function.



Fig. 15: On-device NoisFre key generation: (a) the **mask** is stored in a device's WORM memory; (b) the **mask** is supplied by the server over the wireless communication channel, if there is no WORM memory available on-device, for example. Although the illustration shows the production of one **F**-based key using one **mask**, it is possible to enroll and generate several keys if desired.

6.2 Evaluations

We begin our systematic evaluation of cryptographic key generation with the following question and employ the formal models and the physical chip measurements for our evaluations.

What is the reliability of a *k*-bit NoisFre fingerprint **F**?

Transformed fingerprint **F** can be directly utilized as a cryptographic key because they are invariant to a desirably high number of noise-induced bit error patterns—these F bits exhibit a high noise tolerance. The overall failure rate $P_{\mathbf{F}}^{\text{fail}}$ of a *k*-bit noise-tolerant key **F** can be expressed as:

$$P_{\mathbf{F}}^{\text{fail}} = 1 - (1 - \text{BER}_{\mathbf{F}})^k \tag{13}$$

Recall that the formalized BER_F in Section 4.1 is conservative. Therefore, the $P_{\mathbf{F}}^{\text{fail}}$ in equation (13) will also yield a conservative estimation. We expect a key failure rate in practice to be lower than our prediction here. This hypothesis is validated with an extensive simulation-based on a large simulated chip with up to *one billion* repeated noise-tolerant key bit extraction, as illustrated in Fig. 16.



Fig. 16: Validation of equation (13). The simulated chips are based on the worst-case BER_f = 6.09% from the NORDIC chip set. The parameters selected are n = 32, m = 16 and varied D-norm parameter θ from 1,..., 17. We conducted 10 *million* re-evaluations of a 128-bit noise-tolerant fingerprint for each value of $\theta = 1, ..., 16$ and one *billion* evaluations for $\theta = 17$. Our results corroborates equation (10) and equation (13) as an upper bound on the failure rate of a NoisFre fingerprint employed as a cryptographic key. An even lower $P_{\mathbf{F}}^{\text{fail}}$ is achievable if a larger θ is used. We halted our investigation at θ =17 as it answers the question we investigated.

Next, considering a practitioner's desire for a $P_{\mathbf{F}}^{\text{fail}} < 10^{-6}$ performance target ⁴ for typical industrial applications, as highlighted in [36] and recent studies [26], [34], [37]–[40], we investigate the following question.

What is the most efficient transformation method presenting the highest extraction efficiency while ensuring sufficient reliability for **F** to be *direct* use as a 128-bit cryptographic key with a failure rate lower than 10^{-6} under *worst-case* raw fingerprint BER_f?

We employ NORDIC SRAM-based synthetic data to facilitate the massive number of evaluations necessary to address the question. The evaluation process is described below:



Fig. 17: Extraction efficiency comparison between D-Norm and S-Norm. For S-Norm and D-Norm extractions, we have evaluated 16,384 and 8,388,480 parameters combinations, respectively. The θ of D-Norm may take any value in [1, *n*], while in S-Norm, the θ is restricted within [1, *n*/2]. Meanwhile, D-Norm extraction employs the additional parameter, *m*. Therefore, the possible combinations of parameters for D-Norm are magnitudes larger than that of S-Norm.

- 1) We determine the BER_F corresponding to a 128-bit key with a failure rate of 10^{-6} using equation (13). The resulting BER_F is 7.81×10^{-9} .
- 2) For each $n \in \{1, 2, 3, ..., 256\}$, evaluate the minimum θ for the required BER_F (equation (9) for S-Norm and equation (10) for D-Norm) to ensure BER_F < 7.81×10^{-9} . In these equations, we employ the mean of the worst-case BER_f = 6.09% of NORDIC dataset to

4. Notably, there is nothing fundamentally preventing us from aiming for a lower key failure rate. We can see from Fig. 16 that a larger θ will achieve a lower failure probability. compute an upper bound for $BER_{\mathbf{F}}$.

- For S-Norm, the extraction efficiency η is calculated with equation (11) using the n and θ determined in the previous step.
- 4) D-Norm requires us to further determine the *m* value that can provide the highest η . As observed in Fig. 24 in the Appendix, η changes smoothly with respect to *m*. To reduce the search-time overhead, we applied a gridbased search technique: i) evenly select *j* sample points from the entire domain of $m \in \{1, 256\}$. ii) calculate the η for each m = 1, 2, 3, ..., j; iii) find the *m* values corresponding to the highest and the second highest η ; iv) refine the search domain to be between the two points found in step iii); and v) repeat from i) to iv) to locate the *m* that gives the highest η .

The results from our investigation are depicted in Fig. 17; here, we plot the occurrences of extraction efficiency as a function of η from all the combinations of S-Norm parameters (n and θ) and D-Norm parameters(n, θ and m). We can conclude that the D-Norm always affords significantly higher extraction efficiencies conditioned on the 128-bit $P_{\mathbf{F}}^{\text{fail}} < 10^{-6}$ constraint. *Therefore, in the following discussion, we focus on the D-Norm.*

Given: i) different sizes of memories embedded within various COTS electronics and ii) BER_f characteristics of noisy fingerprints from different memory technologies:

What is the *lowest key failure rate* $P_{\mathbf{F}}^{\text{fail}}$ achievable for a 128-bit key **F** from *each* memory technology and manufacturer considered in our study?

This scenario resembles a practical application setting where the computing platform or micro-controller unit, for example, needs to be selected based on meeting security and application requirements. We can assume that inherent (worst-case) BER_f of raw fingerprints are known (i.e., published measurement studies on memory technologies). Thus, we test our suite of memory technologies using the following approach:

- 1) For each memory dataset listed in Table 2, we conduct an exhaustive parameter search using possible combinations of D-Norm parameters $(n, m \in [1, 128])$, and $\theta \in [1, n]$ using our analytical models. This step identifies the (n, m, θ) combination exhibiting the lowest $P_{\mathbf{F}}^{\text{fail}}$ while still providing least 128-bit \mathbf{F} .
- 2) We employ the formulated equation (10) to obtain the BER_F of the extracted **F** using the identified m, n, θ and the mean of BER_f characterized across the chips in a given memory type dataset.
- We use BER_F substituted into equation (13) to determine the best P_F^{fail} of the selected and transformed F with at least 128 bits.

Results are summarized in Table 2. Taking the expected BER_f across the smallest SRAM dataset, the lowest $P_{\mathbf{F}}^{\text{fail}}$ expected from a chip with SRAM capacity of 64 KiB is in the magnitude of 10^{-5} . Notably, $P_{\mathbf{F}}^{\text{fail}}$ reported in Table 2 is conservatively estimated from formulations. In practice, $P_{\mathbf{F}}^{\text{fail}}$ is expected to be much better. Importantly, with more abundant and freely available on-chip SRAM, represented

TABLE. 2: The lowest key failure rate $P_{\mathbf{F}}^{\text{fail}}$ achievable for obtaining a 128-bit key \mathbf{F} for *each* investigated memory dataset using D-Norm. Here Mem. size is the abbreviation for Memory size. Worst case BER_f is the mean of the value calculated across the chips in a given dataset. Notably, as described in Section 6.2 and illustrated in Fig. 16, equation (13) provides a conservative upper bound, the actual key failure rates will be much lower in practice.

Dataset (Type)	worst case BER _f (mean)	Mem. size	n	m	θ	$ P_{\mathbf{F}}^{\text{fail}} $ equation (13)
NORDIC (SRAM)	6.09%	64 KiB	29	65	13	4.04×10^{-5}
ISSI (SRAM)	8.29%	256 KiB	50	128	19	3.56×10^{-5}
IDT (SRAM)	5.42%	512 KiB	83	128	25	5.29×10^{-9}
Winbond (Flash)	16.26%	256 MiB $^{\rm 1}$	120	128	41	2.52×10^{-4}
Microchip (EEPROM)	16.37%	32 KiB 1	14	61	9	4.01×10^{-1}

¹Recall that the tested size of Flash and EEPROM memory are 69 KiB and 2 KiB. When calculating the number of selected noise-tolerant bits, the memory sizes are scaled up by assuming the entire 256 MiB Flash memory and 32 KiB EEPROM memory are available for fingerprinting.

in the IDT dataset, a remarkably low key failure rate of 5.29×10^{-9} is achievable.

As expected, the higher worst-case BER_f of the EEPROM and Flash datasets implies that the techniques in NoisFre are not able to select a 128-bit **F** with a satisfactory $P_{\mathbf{F}}^{\text{fail}}$. However, the Flash memory tested benefits from a high memory capacity (256 MiB compared to 32 KiB for EEPROM) and we can achieve orders-of-magnitude better $P_{\mathbf{F}}^{\text{fail}}$ than EEPROM.

In summary, for SRAM—the most prevalent memory type in IoT devices—a 128-bit key with a key failure rate less than 10^{-6} can be efficiently obtained given an adequate SRAM memory capacity. However, for memory types exhibiting severely high BER_f, for example, EEPROM and Flash, the method itself is insufficient to gain a satisfactory $P_{\mathbf{F}}^{\text{fail}}$. Although, NoisFre does significantly reduce the key failure rate given the higher capacity of Flash memory for selecting bits. Notably, with such high BER_f memory characteristics, even the state-of-the-art, efficient method of RFE-based key generators are unlikely to deliver a computationally tractable solution on resource limited devices. We discuss this limitation further in Section 8.4.

7 SECURITY FUNCTION IMPLEMENTATION FOR COMPARISON

Here, we describe a case study implementing a NoisFrebased key generator followed by performance and implementation overhead comparisons against the lightweight, state-of-the-art (R)FE-based method.

7.1 An Overview

The entities, a Verifier and a Prover, involved in this case study are illustrated in Fig. 18 (a). The Verifier consists of a server and a wireless network gateway (smartphone). The Prover refers to a wireless sensor node (Bluetooth sensor). In this setup, the server functions as a coordinator, holds the enrolled Prover's information in the database, and issues commands to instruct the Prover to perform remote attestation. The gateway bridges the communication between the server and the Prover. The traffic between the server and the



Fig. 18: (a) System overview. (b) Experiment setup: Verifier consists of (1) a laptop as the cloud server and (2) a smartphone as the gateway; device is (3) a commercial widely used nRF52832 Bluetooth-LE sensor. See the demo video for more details https://youtu.be/O5NWZw-swpw.

gateway is assumed to be secure by applying standard security protection mechanisms. The Prover, communicating wirelessly, is deployed in an (insecure) environment. Details of the corresponding attestation protocol are provided in Fig. 19. Our case study aims to:

- Implement a lightweight remote attestation routine suitable for a Prover with a constrained resource by following [41].
- Experimentally demonstrate that *SRAM fingerprints can* be accessed on-demand and at *run-time* by exploiting the low-cost micro controller unit (MCU)'s memory power control features—SRAM regions are arranged in blocks can be individually powered on or off.



Fig. 19: Remote attestation protocol, with mask transmitted from the Verifier, In case the WORM is not supported on the Prover device.

Remote Attestation Mechanism. An overview of the remote attestation mechanism based on a NoisFre key generator is illustrated in: i) Fig. 19, where we assume the Prover has no WORM memory available for storing a **mask** and that it has to be transmitted over the wireless communication channel (the worst-case setting in terms of implementation overhead) and ii) Fig. 20, where we assume the Prover has available WORM memory. We assume the Prover has already undergone the enrollment phase we described in Section 6.1.1. The enrollment is conducted by the Verifier in the current setting.

A remote attestation can be requested anytime. First, the Verifier scans for visible Provers by sending a "hello" message. Once there is a Prover in the horizon responding with its unique identifier id, the Verifier fetches the Prover's information (e.g., F and mask) from the secure database **DB** by using the **id** as an index. Second, if the received **id** matches one of that stored in the Verifier's DB, the Verifier instructs the Prover to perform attestation-by sending the mask and MAC tag for Provers with no WORM memory, as in Fig. 19. In this context, the Prover performs a power cycling of memory banks solely corresponding to the fingerprint zone⁵ and dynamically generates \mathbf{F}_i following the steps described in Section 6.1.2. After confirming a ready acknowledgment from the Prover, the Verifier randomly generates a challenge (a nonce) chal, and sends it to the Prover along with the address addr and the *length* of the target application program (App) code bin in the Prover's memory. The Prover's response resp' is generated using MAC computed with the noise-tolerant fingerprint \mathbf{F} . The Verifier compares the received response **resp** with a locally calculated reference response resp'. The remote attestation is accepted if resp and resp' match and rejected otherwise.



Fig. 20: Remote attestation protocol, with mask stored in Prover's WORM. In the demo, we implement this version.

If the Prover device implements WORM memory for storing a **mask**, the protocol can be simplified as shown in Fig. 20; in our end-to-end demo implementation, we consider this simpler case, and describe the implementation details in Fig. 26 in Appendix. B.

7.2 Overhead Comparisons

Implementation Details. We provide an overview of the system implemented in Fig. 18 (b) and defer details to **Appendix B**. Further, we refer the reader to our open-source code release⁶ for detailed descriptions of our implementation, including dynamic and run-time key generation from SRAM fingerprints. A video demonstration of the end-to-end implementation is available at https://youtu.be/O5NWZw-swpw.

We implemented a D-Norm-based key generator on an nRF52832 chip with the smallest on-chip SRAM capacity and BER_f of 4.93% tested under -15 to 80°C operating range. We used *n*=32, *m*=48, θ =13 for D-Norm parameters determined by equation (10), (12), and (13) to be able to extract a 128-bit NoisFre key capable of a key failure rate below 9.15×10^{-6} .

For comparisons, we implemented the (R)FE-based key generators summarized in Table 3 to achieve a key failure rate to closely match 10^{-6} . As discussed in Section 2.2, in an FE, the device executes the computationally-heavy decoding function, while in an RFE, the device executes the more lightweight encoding function. In our end-toend demonstration, to achieve a comparable failure rate to that of the D-Norm-based NoisFre key generator, the (R)FE implementation needs 13 parallel blocks of (n = 63, k = 10, t = 13) BCH code⁷ to provide a similar key failure rate.

Implementation Overhead. The implementation overhead evaluates the usage of two system resources: random-access memory (for run-time data) and clock cycles (for code executions). Overall, in terms of obtaining a 128-bit reliable key with a key failure rate of 9.15×10^{-6} , the implementation of the D-Norm-based NoisFre method with parameters (n=32, m=48, $\theta=13$) takes 51,044 clock cycles⁸. If the **mask** is provided by the server and transmitted over a wireless channel, an additional 45,622 clock cycles are required for mask integrity checks.

In contrast, the FE-based and the lightweight state-ofthe-art RFE-based method introduces significantly higher overheads to achieve a 128-bit reliable key with a slightly inferior key failure rate of 2.45×10^{-5} . Specifically, as evaluated and shown in Fig. 21, the on-device FE decoding and RFE encoding functions consume 285,311 and 109,850 clock cycles, respectively. Both methods need an additional 60,755 clock cycles for helper data integrity checks. In comparison with the state-of-the-art FE and RFE, for meeting a comparable key failure rate, NoisFre reduces clock overhead by 72% and 43%, respectively, if the mask or helper data is transmitted over the wireless channel requiring helper data integrity checks. However, if the mask or helper data for all of the method are stored on a device's WORM memory, clock cycles required in comparison to NoisFre reduces by 82% (compared to FE) and 54% (compared to RFE).

It is worth ephasizing that we have compared NoisFre with an RFE capable of deriving a key with a failure rate

^{5.} Each memory bank can be individually powered off by exploiting particular power control registers, thus enabling run-time SRAM fingerprinting.

^{6.} See https://github.com/AdelaideAuto-IDLab/NoisFre

^{7.} BCH code is a class of cyclic error-correcting codes, named after its inventors Bose, Chaudhuri, and Hocquenghem, constructed using polynomials over Galois field

^{8.} This was tested with nRF52832 SoC, via J-link EDU V10.1 debugger, with nRF5 SDK Ver. 15.3.0, Keil uvision 5.25.2.0 and ARM CC compiler Ver. 5.06 Update 6. Optimization setting = -O3.



Fig. 21: Comparison of implementation overhead of the proposed NoisFre key derivation against traditional (R)FE-based key derivation. The integrity checks are necessary if the helper data or the mask is transmitted over a wireless channel.

of $P_{\rm F}^{\rm fail}\,\approx\,10^{-6}.$ However, as we show in Table 2, if an IDT chip is used in the implementation, we can obtain a key with a significantly lower key failure rate by exploiting the *free*, abundant memory; now, $P_{\mathbf{F}}^{\text{fail}}$ can be $\approx 5 \times 10^{-9}$. Attempting to achieve such a small $P_{\mathbf{F}}^{\text{fail}}$ using an (R)FE will lead to significantly higher overheads. The (R)FE-based key provisioning method introduces increasing execution overheads if a lower key failure rate is desired as illustrated in Table 3. For example, if an IDT SRAM chip is used as the fingerprinting barometric source instead of the NORDIC chips' internal SRAM, a 128-bit key with failure rate of 1.69×10^{-9} requires 188,487 (3.69 times larger) clock cycles with the REF-based method or 967,599 (18.95 times larger) clock cycles with the FE-based method, compared with 51,044 clock cycles for our NoisFre-based method. Hence, in contrast to (R)FE methods, the on-device computational overhead of the proposed NoisFre key generator remains constant, regardless of the desired key reliability and only depends on the size of the key to be derived.

8 DISCUSSION

8.1 Generality of NoisFre

Although our work focused predominantly on SRAM, considering its *ubiquity in low-end IoT devices and the simplistic nature of fingerprint extraction*, the NoisFre fingerprinting methods presented are applicable for other memories, including Flash and EEPROM memories validated in our study. In principle, it can be applied to other hardware fingerprinting methods [42], [43], given an abundant raw digital fingerprint bit space.

8.2 Provisioning Fingerprints at Run-time

Flash and EEPROM memory fingerprints can be accessed during run-time. However, for SRAM fingerprinting, the TABLE. 3: Implementation overh most common method is to utilize its initialization pattern at power-up as a fingerprint, although there are other means [44]; for example using data retention voltage [44] or intentionally putting SRAM cells under a meta-stable state. Those methods usually require customized peripheral circuitry, which tends to be unavailable in COTS devices. Thus, SRAM fingerprinting generally requires power cycling to read the start-up values. As a matter of fact, some low-end microcontrollers allow direct control over the powering of individual SRAM banks [45] (e.g., the low-end nRF52832 studied in this work). Consequently, by leveraging such a feature, SRAM fingerprint-based root keys can be requested during *run-time*.

8.3 Security Analysis

We have looked at the problem of achieving a pragmatic, on-device key derivation method using noisy memory fingerprints. NoisFre fundamentally obviates the need for computationally intensive on-device ECC logic for the task. It is thus immune to HDM attacks [25], [26] that strategically tamper the helper data associated with the ECC to weaken or compromise the key extracted using the state-of-the-art (R)FE methods. The vulnerability is induced by the usage of ECCs (see Section 2.2). Various ECCs are examined and shown to be vulnerable to HDM attacks [26]. A generic countermeasure against HDM attacks appears to be an open challenge. The NoisFre scheme has sought to remove the necessity for helper data associated with key generation in an RFE and, thus, avoid the HDM attacks that exploit helper data. In the following, we consider the security of our proposed key derivation method in the context of prior methods based on the state-of-the-art (R)FE methods.

8.3.1 Threat Model

Memory fingerprint-based key provisioning studies rarely explicitly define a threat model [33], [39], [46] and operate under the assumption that the key material (i.e., memory fingerprint) cannot be directly accessed. However, studies focusing on incorporating key derivation methods to provide a security function, such as authentication or remote attestation [47]–[50], follow a threat model. Therefore, we follow the threat model reasoned therein, along with the assumption that the key material cannot be directly accessed.

Specifically, we consider that an adversary cannot access the raw fingerprint and temporary data stored in RAM or internal chip registers during key derivation. The attacker can tamper with public information used to assist the key derivation. Notably, in prior work, such information would be the ECC associated helper data in a (R)FE-based reliable key derivation method [26]—in our key derivation approach, we assume the *mask* is public information. The mask is sent to a device over a communication channel together with a method for assessing the integrity of the mask or is stored in WORM.

TABLE. 3: Implementation overhead of R(FE) employing BCH codes.

Fingerprint source						Clock cycles			
(BFR -)	BCH(n,k,t)	Block number	Key failure rate	Key size	Helper data size	Fuzzy Extractor	Reverse Fuzzy	Helper data	
(BERG)						decoding	Extractor encoding	integrity check	
NORDIC (4.93%)	(63,10,13)	13	2.45×10^{-5}	130	689	285,311	109,850	60,755	
IDT (5.42%)	(127,15,27)	9	1.69×10^{-9}	135	1008	967,599	188,487	84,013	

8.3.2 Mask Manipulation Attack

In use cases where the mask is sent to a device over a communication channel, it is possible for an attacker to manipulate the mask. Therefore, we consider *mask manipulation attacks*.

In the context of a NoisFre-based key generator, a MAC **tag** is produced over the mask using the derived **F** to ensure the integrity of the mask—more specifically, **tag** \leftarrow MAC_F(**mask**), with **F** being the reliable secret key, as illustrated in Fig. 15 (b). The **mask** and MAC **tag** can be publicly stored off-chip and/or stored on-chip. Subsequently, the MAC **tag** can be regenerated to validate the integrity of a mask stored on-device or transmitted to the device prior to the use of the key derived on-demand, as illustrated in Fig. 15 (b). Now, the probability of making a modification without being detected is $\frac{1}{2^k}$ with *k* the length of the derived key. It will be $\frac{1}{2^{128}}$ for a typical 128-bit key.

Although we adopted a simple mechanism in this study to ensure mask integrity, other mechanisms have been proposed to ensure the integrity of helper data in the context of state-of-the-art (R)FE methods [25]. Thus, we can also employ these existing methods to ensure the integrity of the mask for NoisFre key derivation method.

8.3.3 Brute-force Attack

For completeness, we also assess the attack complexity of a brute-force attack on a NoisFre-based key derivation method. The attacker may utilize a brute-force attack to determine the derived key. However, this is extremely challenging when the key is appropriately sized. For a brute-force attack, the probability of finding the correct derived key is $\frac{1}{2^k}$, which is computationally infeasible given a reliable key with a typical length of k = 128 bits.

8.3.4 Aging Attack

The data stored in a SRAM cell can gradually affect its startup state. This is called data-dependent aging [51]. Given that the key derivation is based on a physical primitive, we also consider *aging attacks* that may attempt to exploit the small changes in behavior of memory cells that occur as a result of aging the underlying electronic components.

In use cases where a write access protected (e.g., using a memory protection unit [MPU]) memory cannot be allocated for generating fingerprints and where the memory space used for fingerprints must be shared with user application code, an attacker may utilize malicious code on the device to continuously write specific memory patterns to the SRAM used for device fingerprinting. Such an attempt can accelerate aging and can potentially degrade the reliability of a NoisFre key generation method.

In use cases where a dedicated memory cannot be allocated for generating fingerprints, several simple mitigation strategies already exist. First, the aging effect is data dependent. The user can employ an anti-aging method, such as writing reverse data patterns to mitigate the aging effect validated as an efficient approach to counter aging [51]. Second, the SRAM unreliability induced by aging, even over six years, is small—only 2% [51]. Hence, a simple anti-aging method for NoisFre is to allow the server to intentionally assume a higher worst-case BER_f during the enrollment phase to count for or tolerate the aging effect by trading off a slight increase in SRAM volume required to retain the same NoisFre key reliability. If the available memory volume is constrained, a further low-cost anti-aging measure is for the server to adopt the trial-and-error method reported in [52] to recover the least reliable transformed F bits, because the server can ascertain the bit-specific reliability of each F bit. Notably, in this approach, all the computation overhead is offloaded to the server without imparting any overhead to the device.

8.4 Limitations and Future Work

Our study is not without limitations. As shown in Fig. 17, the highest extraction efficiency (i.e., the number of fingerprint bits with a BER_F < 7.81×10^{-9} that can be extracted from a unit-sized memory block) that NoisFre can achieve is 0.62 bits per KiB. Hence, extracting a usable (e.g., 128bit) secure key from a highly resource-limited device with a mere 2 KiB memory space (i.e., the SRAM size of the passively powered computational radio frequency identification (CRFID) device studied in [35]) with NoisFre is not immediately possible.

The investigation of potential methods for improving the performance, in particular enhancing the BER_{F} and/or extraction efficiency η , is left out of scope for our current study focused on developing NoisFre, formalizations, and extensive evaluations. As a potential direction for future work, it will be interesting to consider approaches, for example, to extract more bits from a given memory. Although our formulation for reliability is applicable for such a method, the analytical formulation of extraction efficiency for such new methods will likely require considerable effort to develop. Importantly, the complexity of the task will provide an interesting direction for future work. Therefore, we leave the investigation of potential means for improving the NoisFre performance, in particular enhancing the BER_{F} and/or extraction efficiency η , as potential directions for future research.

9 RELATED WORK

Besides memories, various on-board sensors, such as cameras, accelerometers, gyroscopes, magnetometers, and other components, such as CPU magnetic radiations, are utilized to provide fingerprints [3]–[11]. Other recent works also explore commodity scanners to fingerprint 3D objects to track them [2] and exploit the package variations as fingerprints for anti-counterfeiting [1]. However, to obtain hardware fingerprints, those fingerprint extractions are relatively complicated in comparison with memory, especially SRAM, enabled fingerprints.

Notably, hardware fingerprinting is closely related to the notion of PUFs [34], [53]–[56]. Commodity memory fingerprinting, such as SRAM PUF and Flash PUF, is not new. However, mounting them on low-end IoT devices to derive a usable key for security functions relies on post-error correction to reconcile bits errors, which is cumbersome in terms of both overhead and security in practice. Our simple yet efficient NoisFre memory-fingerprinting approach addresses this gap.

We exploit the idea of a differential measurement in the formulation of the D-Norm method based on the base distance (ℓ 1-Norm) to improve the *extraction efficiency* (number of F bits with a desired noise tolerance) from a given memory. Interestingly, in PUF studies, formulating methods to exploit a differential gap or comparison has been utilized by extrinsic PUFs-implemented with additional hardwaresuch as ring oscillator PUF (RO-PUF) [55]-[58] and arbiter PUF (APUF) [59] to obtain responses with improved reliability. The concept has subsequently been applied in [55], [56] to enhance reliability and address aging of electronic components in RO-PUFs facilitated by the ease with which RO frequency differences are already measured and can be directly used. In our intrinsic memory studies, we exploit a base distance, ℓ 1-Norm, to generate a differential measurement to build the D-Norm transform for memory PUFs intrinsic to COTS devices. As discussed in Section 3.3, we recognized that the differential formulation can yield significantly more reliable bits compared to S-Norm employing (simply, the ℓ 1-Norm base distance). Thus, in our work, we combine these two mathematical concepts (base distance with a differential measure) together to extract more noise-tolerant bits from a memory PUF-a method that can be used with intrinsic memories widely exist in COTS devices.

10 CONCLUSION

By exploiting ubiquitously embedded memory within commodity computing devices, the proposed NoisFre approach constructively extracts transformed memory fingerprints that were embodied with a high tolerance to noise affecting the generation of fingerprints. With a simple, single, oneoff fingerprint enrollment measurement, NoisFre is able to judiciously identify highly reliable transformed fingerprints serving as hardware root key or root of trust to directly support various security functions for a wide range of COTS electronic devices. Besides formalization of two specific S-Norm and D-Norm fingerprint transformation methods and extensive empirical validations on SRAM, Flash, and EEPROM memories using 119 physical chips in total, we have conducted a case study with an end-to-end implementation of a remote attestation security service employing NoisFre fingerprints to significantly reduce the overhead in comparison with the state-of-the-art RFE method for constructing reliable fingerprints for a key generator. We also demonstrate how SRAM fingerprints can be generated at run-time by utilizing individual memory-bank power control features on MCUs. Overall, NoisFre is a simple but practical method, especially for existing low-end commodity electronic devices.

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APPENDIX A

DERIVATION OF PERFORMANCE METRIC MODELS

In this section, we detail the derivation of equations in Section 4, where the following ideal chip model is adopted.

A.1 Synthetic Chip Model

Due to the size limitation of physical chips and difficulty of taking a massive number of repeated measurements from physical chips, we adopt a synthetic chip model to evaluate our analytic predictions. The synthetic chip model used is from [31] and is built under the following settings:

- 1) Each bit has a 50% chance being logic "1" or "0" during the enrollment phase. Each initial bit value is randomly generated during chip initialization.
- 2) Each bit has an equal probability, BER_f, of being flipped during a regeneration.
- 3) The values of bits are independent and identically distributed (iid); hence, we assume no spatial or temporal correlations.

A.2 Unreliability Formalization of S-Norm Transformation

As described in Section 3.2, all possible cases of noise-tolerant S-Norm transformed bit F are shown below.

$$F \leftarrow \mathcal{T}_{\mathrm{SNorm}}(\mathbf{f}^{n \times 1}, \theta) = \begin{cases} 1, & \|\mathbf{f}\|_{1} \ge \left\lceil \frac{n}{2} \right\rceil + \theta \\ 0, & \|\mathbf{f}\|_{1} \le \left\lfloor \frac{n}{2} \right\rfloor - \theta \\ \bot, & \text{Otherwise} \end{cases}$$



Fig. 22: S-Norm-based NoisFre. Two boundary conditions are illustrated: when F = "1" where $\|\mathbf{f}\|_1 = \lceil \frac{n}{2} \rceil + \theta$, and when F = "0" where $\|\mathbf{f}\|_1 = \lfloor \frac{n}{2} \rfloor - \theta$. Here we use F = "1" as an example to demonstrate the influence of flipped raw bits on their transformed 1-bit *F*. The generated $\ell 1$ -Norm is partitioned into two segments: A and B. Consider three representative cases: (1) any single raw bit flip in B will enhance the reliability of the transformed bit *F*; otherwise (2) any single raw bits flip in segment A will deteriorate reliability of the *F*; (3) the *F* will fail/flip if there are θ or more raw bits flipped in segment A.

The formalization is visualized in Fig. 22. Recall that a F bit can be transformed from n raw bits and the ℓ 1-Norm of the F is between [0, n]. To assess the worst-case BER_F, we consider the condition where the selected word's ℓ 1-Norm is exactly equal to $\lceil \frac{n}{2} \rceil + \theta$, as shown in boundary condition F = "1" in Fig. 22. Here, θ is a threshold to select highly reliable F bits.

Each raw bit is with BER_f probability to be flipped under reevaluation. Using boundary condition F = "1" as an example, on the one hand, (1), if there are raw bits of "0" (marked as segment B) flipping, it will increase the tolerance of the number of *raw bits of "1"* that allows being flipped (in segment A) *without influencing* F *bit.* In contrast, (2) flipping raw bits of "1" (marked as segment A) will potentially result in an error to the F bit. Further, (3), supposing that raw bits of "0" (marked as segment B) remain unchanged, if more than θ raw bits of "1" flip, the F will exhibit an error—flipping from "1" to "0". To be precise, the transformed F bit *will not exhibit* error unless more than $\theta + i$ raw bits of "1" flipping.

Overall, bit flipping within raw bits of "0" (marked as segment B) increases the reliability of extracted **F**. In contrast, bit flipping within raw bits of "1" (marked as segment A) decreases the reliability of extracted **F**. The boundary condition F = "0" is logically equivalent to the case F = "1" but, only inverts F's "0"/"1" value rather than its BER_F.

Without losing generality, we focus on one case shown in (1) in Fig. 22. $\|\mathbf{f}_i\|_1 = \lceil \frac{n}{2} \rceil + \theta$, the probability of having exact x error bits in segment A can be expressed as $\Pr_{|x|\in A}^{\text{flip}} = \text{binopdf}(x, \frac{n}{2} + \theta, \text{BER}_f)$, given that each raw bit has a BER_f probability of flipping. Similarly, the probability of y bits in segment B to be flipped is formulated as $\Pr_{|y|\in B}^{\text{flip}} = \text{binopdf}(y, \frac{n}{2} - \theta, \text{BER}_f)$.

Although bit flip could occur in either segment A or B, consequential BER_F of F bits are opposite: flipped bits in segment A reduction in the margin or potentially increases the BER_F (shown as the dashed boundary line in Fig. 22 that moves toward the left). In contrast, flipped bits in segment B increase the margin or potentially decrease BER_F (the boundary moves toward the right). If the boundary crosses the middle point of $\frac{n}{2}$, the $||\mathbf{f}_i||_1$ falls below $\frac{n}{2}$, and consequently, the F bit flipped—exhibiting an error.

Starting from the extreme but straightforward condition—there is no bit flip in segment B (i.e., y = 0). the maximum number of erroneous bits that can be tolerated is θ as discussed above. This can be expressed as $P_{\parallel ||t_i||_1}^{\text{fail}} = \Pr(x - y \ge \theta) = \Pr(x \ge \theta \mid y = 0) = \Pr(x \ge \theta) \times \Pr(y = 0)$, where the term $\Pr(x \ge \theta)$ can be expressed as $1 - \Pr(x < \theta) = 1 - \sum_{x=0}^{\theta} \left(\Pr_{|x| \in A}^{\text{flip}}\right) = 1 - \text{binocdf}|(\theta, \lceil \frac{n}{2} \rceil + \theta, \text{BER}_f)$. By substituting $\Pr_{||y| \in B}^{\text{flip}} = \text{binopdf}(0, \lfloor \frac{n}{2} \rfloor - \theta, \text{BER}_f)$ into the $P_{\parallel ||t_i||_1}^{\text{fail}}$ equation, $P_{\parallel ||t_i||_1}^{\text{fail}}$ is expressed:

$$\begin{split} P^{\text{fail}}_{\|\mathbf{f}_i\|_1} &= \left(1 - \mathsf{binocdf}(\theta, \lceil \frac{n}{2} \rceil + \theta, \text{BER}_{\mathbf{f}})\right) \\ &\times \mathsf{binocdf}(0, \lfloor \frac{n}{2} \rfloor - \theta, \text{BER}_{\mathbf{f}}) \end{split}$$

However, there is more than one case that satisfies $x - y \ge \theta$ for $\{(x, y) : |x| \in A, |y| \in B\}$. Since *A* and *B* are finite sets, the combination of *x* and *y* are numerable. Another property worth mentioning is |A| > |B|. Therefore the total number of combinations is up bounded by $|B| = \lceil \frac{n}{2} \rceil - \theta$ where " $\mid \mid$ " denotes the cardinality or the size of a set. If we enumerate and sum up all possible combinations, we obtain the complete form of equation (9):

$$\begin{split} \mathrm{BER}_{\mathbf{F}} &= \sum_{i=0}^{\lfloor \frac{n}{2} \rfloor - \theta} \bigg(\Big(1 - \mathsf{binocdf}(\theta + i, \lceil \frac{n}{2} \rceil + \theta, \mathrm{BER}_{\mathbf{f}}) \Big) \\ &\times \mathsf{binopdf}(i, \lfloor \frac{n}{2} \rfloor - \theta, \mathrm{BER}_{\mathbf{f}}) \bigg) \end{split}$$



Fig. 23: D-Norm-based NoisFre (a) Two boundary conditions are illustrated: when F = "0" where $(h - l = \theta) \land ([h] > [l])$; and when F = "1" where $(h - l = \theta) \land ([l] > [h])$. (b) Here we use F = "0" as an example to demonstrate the influence of flipped raw bits on their transformed 1-bit F. The two ℓ 1-Norms are firstly reshaped to a single row as shown above to backtrack to the same formulation strategy in S-Norm. The reshaped ℓ 1-Norm is partitioned into two segments: A and B, the size of segment A is $n + \theta$, and the size of B is $n - \theta$ under the boundary condition F = "0". Consider three cases: (1) any single raw bit flip in B will enhance the reliability of transformed F bit; otherwise, (2) any single raw bit flip in segment A will degrade the reliability of **F**. The case of F will fail/flip (3) if there are θ or more raw bits flipped in segment A.

A.3 Unreliability Formalization of D-Norm Transformation

As discussed in Section 3.2. The transformed bit via D-Norm is determined as below:

$$= \left\{ \begin{aligned} & T_{\text{DNorm}}(\mathbf{f}^{n \times m}, \theta) \\ & = \begin{cases} 1, & h-l \geq \theta \ \land \ [h] < [l] \\ 0, & h-l \geq \theta \ \land \ [h] > [l] \\ \bot, & h-l < \theta \end{aligned} \right.$$

where [] indicates the index.

F

To apply the same derivation strategy as the S-Norm, as illustrated in Fig. 23 (b), the two l1-Norms are reshaped into a single row, and four partitions are now rearranged as two segments: A and B. The length of segment A is eventually h + (n - l) by considering the fact $h = l + \theta$, whereas we can see that the length of A is $n + \theta$. The largest number of errors/flips within raw bits **f** that still can not result in error or flip to the transformed F bit is $(n + \theta) - n = \theta$.

The rest of the steps are identical to those in S-Norm. Using (1) as an example, on the one hand, Case (1), if one raw bit in segment B is flipped, it will increase the tolerance of the number of raw bits in segment A which allows being flipped *without influencing* F bit. On the other hand, Case (2) flipping one raw bit in segment A will potentially result in an error to the F bit. Further, for Case (3), supposing that segment B's raw bits remain unchanged, if more than θ raw bits flipped in segment A, the **F** will exhibit an error—flipping from "0" to "1". To be precise, the transformed **F** *will not exhibit* error unless more than $\theta + i$ raw bits in segment A flip.

Now, an extreme condition is considered as a starting point: as shown in the third column in Fig. 23, we have two words, labeled with spatial index the "first" and the "second". We denote the raw bits as $f_{\rm first}$ and $f_{\rm second}$, respectively.

In the exemplified case, $\mathbf{f}_{\text{first}}$ has the lowest ℓ 1-Norm while the $\mathbf{f}_{\text{second}}$ has the highest ℓ 1-Norm in the *m*-word block. (i.e., $\|\mathbf{f}_{\text{first}}\|_1 = l$, $\|\mathbf{f}_{\text{second}}\|_1 = h$). From the diagram, we can write the following equation:

$$\|\mathbf{f}_{\text{second}}\|_{1}^{\mathbf{-}} - \|\mathbf{f}_{\text{first}}\|_{1} = \theta$$

By substituting $\|\mathbf{f}_{second}\|_{1} = h$ and $\|\mathbf{f}_{first}\|_{1} = l$ into the equation above (the case (1) in Fig. 23 (a)), we obtain: $h - l = \theta$

Add n (number of bits in one word/group) to both sides of the equation. We obtain:

$$h + (n - l) = n + \theta$$

If we reshuffle the four partitions in Fig. 23 (b), the error rate of D-Norm can be formalized in a similar manner as the S-Norm (equation (9)). The margin (denoted as a dashed line) reduces and results in an unstable trend if any bit flips in the segment A. Once the margin crosses n (marked as a solid line) from the right to the left, the transformed **F** is therefore erroneous. In contrast, bits flipped in segment B increase the margin and stabilize the **F**.

The probability of x error bits occurring in segment A can be expressed as $\Pr_{|x|\in A}^{\text{flip}} = \text{binopdf}(x, n + \theta, \text{BER}_{f})$. Similarly for y bits in segment B to be flipped can be expressed as $\Pr_{|y|\in B}^{\text{flip}} = \text{binopdf}(y, n - \theta, \text{BER}_{f})$.

Now consider the special case where there is no bit flip in segment B; then the highest number of bits allowed to be flipped in segment A is simply θ . Otherwise, the **F** will exhibit errors. Consequently, the $P_{\text{DNorm}}^{\text{fail}}$ can be expressed as:

$$\begin{split} P_{\mathrm{DNorm}}^{\mathrm{fail}}(y=0) &= \left(1 - \mathsf{binocdf}(\theta-1, n+\theta, \mathrm{BER}_{\mathbf{f}})\right) \\ &\times \mathsf{binopdf}(0, n-\theta, \mathrm{BER}_{\mathbf{f}}) \end{split}$$

If the number of flipped bits in segment B is non-zero, $\Pr_{|y|\in B}^{\text{flip}} = \text{binopdf}(y, n - \theta, \text{BER}_{\mathbf{f}})$, where $y \in [0, |B|]$, $|B| = n - \theta$. In other words, flipped bits in segment B allows more tolerance of error bits in segment A, before F exhibiting error. Therefore, the D-Norm, $\text{BER}_{\mathbf{F}}$, is the summation of $P_{\text{DNorm}}^{\text{fail}}(y)$ for all possible y, finally formulated as in equation:

$$BER_{\mathbf{F}} = \sum_{y=0}^{n-\theta} \left(\left(1 - \mathsf{binocdf}(y+\theta-1, n+\theta, BER_{\mathbf{f}}) \right) \times \mathsf{binopdf}(y, n-\theta, BER_{\mathbf{f}}) \right)$$

A.4 Extraction Efficiency of S-Norm Transformation

For the S-Norm, if one group/word **f** is selected, it must satisfy the selection criteria $\|\mathbf{f}\|_1 \in [0, \lfloor \frac{n}{2} \rfloor - \theta] \cup [\lceil \frac{n}{2} \rceil + \theta, n]$. Hence, the probability of a group being selected can be expressed as:

$$P_{\text{SNorm}}^{\text{select}} = \Pr(\|\mathbf{f}\|_{1} \leq \lfloor \frac{n}{2} \rfloor - \theta) + \Pr(\|\mathbf{f}\|_{1} \geq \lceil \frac{n}{2} \rceil + \theta)$$
$$= \sum_{i=0}^{\lfloor \frac{n}{2} \rfloor - \theta} \left(\Pr(\|\mathbf{f}\|_{1} = i)\right) + \sum_{k=\lceil \frac{n}{2} \rceil + \theta}^{n} \left(\Pr(\|\mathbf{f}\|_{1} = k)\right)$$

By substituting $\Pr(\|\mathbf{f}\|_{1} \le i) = \operatorname{binocdf}(i, n, 0.5)$ and $\Pr(\|\mathbf{f}\|_{1} \ge k) = 1 - \operatorname{binocdf}(k, n, 0.5)$, we get:

$$\begin{split} P^{\text{select}}_{\text{SNorm}} &= \mathsf{binocdf}(\lceil \frac{n}{2} \rceil - \theta - 1, n, 0.5) \\ &+ \left(1 - \mathsf{binocdf}(\lfloor \frac{n}{2} \rfloor + \theta, n, 0.5)\right) \end{split}$$

The $P_{\rm SNorm}^{\rm select}$ formulates the probability that one group is selected under S-Norm. The extraction efficiency $\eta_{\rm SNorm}$ can be directly expressed via $P_{\rm SNorm}^{\rm select}$:

$$\eta_{\text{SNorm}} = \frac{1}{n} \times P_{\text{SNorm}}^{\text{select}} \times (1024 \times 8)$$

Where $\frac{1}{n}$ means that a transformed F bit is from n raw bits, The last term 1024×8 is the conversion factor between bit and KiByte (bit/KiB). By substituting $P_{\text{SNorm}}^{\text{select}}$ into η_{SNorm} , we can finally obtain equation (11).

$$\begin{split} \eta_{\mathrm{SNorm}} &= \frac{1}{n} \times \left(\mathsf{binocdf}(\lceil \frac{n}{2} \rceil - \theta - 1, n, 0.5) \right. \\ &+ \left(1 - \mathsf{binocdf}(\lfloor \frac{n}{2} \rfloor + \theta, n, 0.5) \right) \right) \times (1024 \times 8) \end{split}$$



Fig. 24: Validation on equation (12) (extraction efficiency of D-Norm) using a simulated chip (the **Simulation** test setting in Section 5). Here, n = 32, while *m* and the noise tolerance parameter θ are varied. Overall, the simulation agrees well with the prediction, as two values overlaps.

A.5 Extraction Efficiency of D-Norm Transformation

To estimate the extraction efficiency of D-Norm, what we need to do first is estimate the probability that among *m* groups/words $\mathbf{f}_1, \mathbf{f}_2, \ldots, \mathbf{f}_m$), the minimum ℓ 1-Norm $\|\mathbf{f}_i\|_1$ is any given value *a* from 0 to *n*, and the maximum ℓ 1 norm $\|\mathbf{f}_i\|_1$ is another given value *z* from 0 to *n*:

$$P(a,z) \triangleq \Pr\left(l = a \land h = z\right)$$

Recall that:

$$h \triangleq \arg \max (\|\mathbf{f}_i\|_1)$$
$$\mathbf{f}_i|_{i \in \{1,..,m\}} (\|\mathbf{f}_i\|_1)$$
$$l \triangleq \arg \min (\|\mathbf{f}_i\|_1)$$
$$\mathbf{f}_i|_{i \in \{1,..,m\}} (\|\mathbf{f}_i\|_1)$$

Once we comply with the above principle, the $P_{\text{block}}^{\text{select}}$, that one block to be selected for noise-tolerant fingerprint extraction is simply the sum of all P(a, z) over $z - a \ge \theta$.

$$P_{\text{block}}^{\text{select}} = \sum_{a=1}^{n-\theta} \sum_{z=a+\theta}^{n} P(a,z)$$

P(a, z) is a non-trivial to estimate. Fortunately, we can solve an easier and related problem first:

$$Q(a, z) \triangleq \operatorname{Prob}\left(l \ge a \land h \le z\right) = \left(\sum_{i=a}^{z} \operatorname{binopdf}(i, n, 0.5)\right)^n$$

Another angle to look at Q(a, z) is: What is the probability that among m words in a block with all ℓ 1-Norm are at least a and at most z? That question can be answered because it poses an independent question on each word \mathbf{f}_i : is $a \leq \|\mathbf{f}_i\|_1 \leq z$ or not? The answer must be "yes" for all m words, and it is "yes" for a single word with probability $\sum_{i=a}^{z} \mathsf{binopdf}(i, n, 0.5)$ (the usual formula for the number of $\|\mathbf{f}_i\|_1$ meet θ divided by the number of all m words), and because those events are independent, the probabilities can be consequentially multiplied.

The question becomes: how do we get from Q(a, z) to P(a, z)?

Note that:

$$\begin{split} &\{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m): (l = a \ \land \ h = z)\} \\ &= \{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m): (l \geq a \ \land \ h = z)\} - \{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m): (l \geq a + 1 \ \land \ h = z)\} \end{split}$$

because for the l to be equal to a it is equivalent to ask for the l to be at least a but not to be at least a + 1. In addition, the set we are subtracting is actually a subset of the set we are subtracting from, so we obtain:

$$P(a, z) = \operatorname{Prob}\{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m) : (l = a \land h = z)\} = \operatorname{Pr}\{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m) : (l \ge a \land h = z)\} - \operatorname{Pr}\{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m) : (l \ge a + 1 \land h = z)\}$$

Our two operands are of the same type. We can do the same operation to reduce each probability to something expressible by some Q(r, s):

$$P(a, z) = \{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m) : (l \ge r \land h = z)\}$$

= $\{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m) : (l \ge r \land h \le z)\} - \{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m) : (l \ge r \land h \le z - 1)\}$
And we obtain:
$$\Pr\{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m) : (l \ge r \land h = z)\} =$$

 $\Pr\{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m) : (l \ge r \land h \le z)\} - \Pr\{(\mathbf{f}_1, \mathbf{f}_2, \dots, \mathbf{f}_m) : (l \ge r \land h \le z - 1)\} = Q(r, z) - Q(r, z - 1)$

And finally, for P(a, z), by substituting this in the above formula:

$$P(a,z) = (Q(a,z) - Q(a,z-1)) - (Q(a+1,z) - Q(a+1,z-1))$$



Fig. 25: Showing the relationship between P_{block} and Q terms

The normalized D-Norm extraction efficiency η_{DNorm} is finally given:

$$\eta_{\text{DNorm}} = \frac{1}{n \times m} \times P_{\text{block}}^{\text{select}} \times (1024 \times 8)$$

To be concise, we keep $P^{\rm select}_{\rm block}$, $P_{\rm block}$ and Q(l,h) to be expressed separately. The term of $\frac{1}{n\times m}$ stands for $n\times m$

raw bits producing a 1-bit noise-tolerant bit, per (1024×8) 1 KiB memory. It tends be hard to follow when we substitute all terms and write a huge equation. To be concise, we keep express $P_{\text{DNorm}}^{\text{select}}$, P_{block} and Q(l, h) separately.

APPENDIX B REMOTE ATTESTATION

The following description is based on the setting shown in Fig. 20 where the Prover device implements a secure WORM memory for storing the enrolled mask. During the one-time enrollment conducted by the trusted Verifier, we use a cabled JTAG interface and Segger J-link command-line tool to read out the start-up state (fingerprints) of Prover's (Nordic Semiconductor nRF52832) SRAM. Readout raw fingerprints are saved as binary files and then processed (using Matlab) for performing the D-Norm transform and selection (Section 3). Such a process produces: i) a database entry containing Prover id and selected reliable noise-tolerant F bit and ii) a C language header file containing the mask indicating the memory addresses of raw fingerprint bits to be employed for obtaining F bits to be compiled with the sensor node code. Next, we elaborate on an efficient means for organizing the memory addresses defined by the **mask**.

D-Norm Mask. The **mask** first specify the starting address of the fingerprint zone, which is set to 0x4000, reserving the lower 16 KiB of SRAM space for system run-time operations. To reduce the storage footprint of the **mask**, only the relative offsets between selected memory addresses, rather than the 32-bit absolute addresses are recorded. Once the **mask** is determined, the server computes a MAC **tag** over the **mask** with the derived key **F** for integrity checks.

Implemented System. During the attestation phase, we employ a command-line Verifier tool, (1) shown in Fig. 18 (b), to randomly generate a challenge (nonce). We look up the **DB** according to the Prover's returned id and compute the expected response. To visualize the data exchange for demonstration purposes, we built our Gateway (2) using an Android demo APP based on FastBLE library⁹ and used the smartphone's built-in Bluetooth-LE interface to communicate with the Prover. In practice, the Gateway could be realized by any base station with a Bluetooth-LE transceiver. The Prover (3) in this case study is a representative lowend sensor node equipped with an ARM-Cortex M4-based nRF52832 Bluetooth-LE SOC. The code to be attested on the Prover is statically allocated with a linker Preprocessor command.¹⁰ The noise-tolerant fingerprint regeneration function, the mask, and the immutable bootloader are placed in WORM memory using an ARM MPU.

APPENDIX C MEMORY FINGERPRINT DATASETS

Below we detail the collected NORDIC dataset since the details of the public SRAM datasets are in [29], [30]. In addition to the SRAM datasets, we also employed a public FLASH dataset [17] and collected EEPROM datasets for



Fig. 26: Memory management and data flow for the remote attestation at the Prover. Notably, the total SRAM memory size is 64 KiB. We only use 48 KiB for the fingerprint zone and reserve 16 KiB for system runtime operations.

generalization. The Winbond W29N02GV Flash used in [17] is a single-level cell (SLC) Flash and its partial programming time is set to be 150 us [17]. The BER_f of Flash memory fingerprints are negligibly affected by changes in voltage and temperature but programming cycles impart chip aging. Hence, we only consider aging induced BER_f for Flash memory. Our method for collecting EEPROM data is similar to that employed for Flash [16] based on leveraging partial programming. Different from Flash, EEPROM can only be programmed byte-by-byte. Consequently, partial programming consumes a longer period of time on EEPROM than on Flash. The partial programming latency depends on the temperature, at 25°C, it takes at least 40 ms to evaluate one byte.

NORDIC. We first collected 12 nRF52832 chips under each of the three operating temperatures (see one such chip in Fig. 18). The nRF52832 is a popular RF-enabled MCU, and supports various protocols including Bluetooth 5, Bluetooth mesh, ANT, and NFC. This chip has a 64 KiB SRAM memory. The NORDIC chip is representative of a typical lowcost IoT device MCU. Three temperature corners $\{-15^{\circ}C,$ 25°C, 80°C are evaluated to measure the reliability of raw bits using 100 repeated measurements taken under each operating corner. The worst-case BER_f of 6.09% occurs under 80°C when the reference template is collected at 25°C. We have collected a further 88 nRF52832 chips under room temperature conditions of 25°C to augment the dataset. This extensive dataset of 100 chips (at room temperature) is used to evaluate uniformity and uniqueness as these metrics benefit from a larger sample of chips but are normally insensitive to operating conditions. In our evaluations, unless otherwise stated, we use the 12-chip dataset (with evaluations at three operating corners) when referring to the NORDIC chip dataset.

^{9.} FastBLE is available: https://github.com/Jasonchenlijian/FastBle 10. For example __attribute__((section(".ARM.__at'0x50000"))) in Keil uVision specifies placing the function at memory starting from address 0x50000.