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A System Health Indicator for the Distributed Minority and Majority Voting Based Redundancy Scheme

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***Abstract*—The distributed minority and majority voting-based redundancy (DMMR) scheme was proposed as an efficient alternative to the conventional N-modular redundancy (NMR) scheme for the design of mission and safety-critical circuits and systems. However, only a basic implementation of the DMMR scheme was considered with no provision for indicating any fault or error in the DMMR system when they might occur. In this context, this paper presents the novel design of a generic system health indicator (SHI) for the DMMR scheme. Compared to the basic DMMR system, the DMMR system with the proposed SHI can provide concurrent information about the state of the system, i.e., whether the system is healthy or not. This helps to improve the observability of the DMMR system which could be useful during the online testing and/or troubleshooting of any faulty zones in the system, pre-emptively or during any scheduled maintenance. Example DMMR systems and their corresponding NMR systems without and with SHI have been implemented using a 32/28nm CMOS process and compared. On average, the DMMR systems with the proposed SHI report 6.5× improvement in a normalized figure of merit compared to the corresponding NMR systems incorporating SHI.**

Keywords— Digital circuits; VLSI; Fault tolerance; Redundant design; Standard cells

I. INTRODUCTION

Mission- and safety-critical circuits and systems used in space, aerospace, nuclear, defense, banking, financial, and other sensitive industry applications usually employ redundancy in the design to overcome arbitrary function module (circuit or system) faults or failures whilst providing the correct operation [1]. In this context, the N-modular redundancy (NMR) has been widely used [2] [3]. In the NMR scheme, N identical function modules are used, where N is odd, and a majority (N+1)/2 out of the N function modules is required to operate correctly to guarantee the correct NMR system operation. The NMR scheme can tolerate the faulty or failure state(s) of maximum of (N–1)/2 function modules.

The 3MR or TMR is the basic, 3-tuple version of the NMR scheme which can mask the faulty or failure state of at most one function module. To cope with situations where multiple faults or failures [4 – 6] are likely to occur in modern electronic designs due to radiation or any other phenomena [7 – 11], higher versions of the NMR such as 5MR, 7MR, and 9MR are recommended to be used selectively in the sensitive or critical portions of a circuit or system [12]. The 5MR, 7MR, and 9MR represent the respective 5-tuple, 7-tuple, and 9-tuple versions of the generic NMR system. However, the drawbacks in employing higher versions of the NMR are the exaggerated increases in design metrics, weight, and cost.

To mitigate the exacerbated overheads associated with circuit or system designs which might have to employ higher levels of redundancy, the distributed minority and majority voting-based redundancy (DMMR) scheme was proposed [13], as an alternative to the NMR scheme. It was shown that the DMMR scheme is efficient compared to the NMR scheme in terms of the design metrics, weight, and cost whilst being able to achieve the same degree of fault tolerance but with fewer function modules. However, just a basic implementation of the DMMR scheme was considered in [13] with no provision for indicating any fault or error in a DMMR system when they might occur. It is important to be aware of the operational state of a system, i.e., whether a system is healthy (without or with fault masking) or unhealthy, as this could be useful to promptly initiate appropriate remedial action based on need and/or depending upon a system's safety-criticality. Also, this avoids making any assumption about a system's operation that it is perfect when this may not be true.

A system with high safety ensures that the probability of undetected errors is low [14]. Hence the provision of a dedicated logic to reflect the healthy or the unhealthy state of a system contributes to enhancing the system safety. Further, the provision of continuous information about a system's health through dedicated outputs helps to improve the observability of the system which could be useful during the online testing and/or troubleshooting of any faulty zones in the system, pre-emptively or during any scheduled maintenance. In this context, the word-voter [15] was proposed to enhance the data integrity of TMR systems. The word-voter would issue an error signal when more than one function module becomes faulty or fails in a TMR system owing to disjoint faults affecting the function modules. However, the limitations of the word-voter are: i) it does not provide real-time information about any fault or failure occurrence in the system, and ii) the word-voter is confined to the TMR scheme.

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A generic system health monitor for the NMR scheme was proposed in [16] which could provide continuous information about an NMR system health, i.e., whether an NMR system is healthy or not. If the corresponding output(s) of majority of the function modules comprising an NMR system are contradictory, then a fault warning is issued. On the other hand, if the number of faulty or failed function modules in an NMR system unfortunately attains a majority, an error signal is issued indicating that the NMR system is in error and therefore its output(s) are not dependable, which might necessitate immediate attention. If the NMR system health monitor does not issue fault warning or error signals, it implies that the NMR system operates correctly and is therefore healthy (without or with fault masking). If the NMR system health monitor issues only a fault warning and no error signal, it implies that the NMR system is healthy and its internal fault(s) or failure(s) have been successfully masked.

This paper presents the novel design of a generic system health indicator (SHI) for the DMMR scheme. The DMMR SHI consists of a fault warning logic (FWL) and an error signaling logic (ESL). The FWL of the DMMR SHI would issue a fault warning when any single output of any function module within the DMMR system produces a contradictory output to the rest of the corresponding outputs of the remaining function modules. This could pave the way for initiating appropriate pre-emptive action depending upon a system's safety-criticality. The ESL of the DMMR SHI would generate an error signal if the output of the Boolean majority logic group is 1, and the output of the Boolean minority logic group is 0. No fault warning or error signals issued from the DMMR SHI implies that the DMMR system is healthy without or with fault masking. The issuance of only a fault warning and no error signal by the DMMR SHI implies that the DMMR system is healthy but with fault masking enabled, and hence it is dependable.

In the remainder of this paper, Section 2 discusses the (basic) DMMR system architecture and its operation. Section 3 describes the proposed DMMR SHI and explains the operation of FWL and ESL which constitute the DMMR SHI. Section 4 presents the design metrics of example DMMR system implementations without and with the proposed SHI which are realized using a 32/28nm CMOS process technology. The design metrics such as power dissipation, delay, and area corresponding to the corresponding NMR systems without and with SHI are also presented in this section and are compared with the design metrics of DMMR systems without and with SHI. Finally, Section 5 concludes this paper.

II. DMMR System

The block diagram of the DMMR system [13] is the portion enclosed within the dashed lines at the top of Fig 1. If M identical function modules are used to construct a DMMR system, the M function modules are split into 2 groups as the majority logic group and the minority logic group. The DMMR system is generally specified as a 3-of-M DMMR system, where 3 function modules constitute the majority logic group and the remaining (M–3) function modules constitute the minority logic group.

The majority logic group mandates the correct operation of majority of the function modules, i.e., in Fig 1, at least 2 out of the 3 function modules labelled as 1, 2, and 3 must operate correctly. On the other hand, the minority logic group requires the correct operation of at least 1 out of the (M–3) function modules, i.e., in Fig 1, at least 1 out of the (M–3) function modules labelled as 4 to M should operate correctly. However, there could be exceptions to minority logic group operation depending on the inputs supplied from the outside world, and these will be discussed later. Thus, in the absence of any inputs assumption, the conditions stated for the majority and minority logic groups of a DMMR system should be upheld.

Note that the DMMR system accords higher priority for the majority logic group compared to the minority logic group. The less priority for the latter is because the Boolean minority condition may encompass the Boolean majority condition. For example, given that the Boolean minority condition specifies that at least 1 out of the (M–3) function modules in the minority logic group should operate correctly, and even if all but one of the (M–3) function modules operate correctly, the incorrect operation of a single function module may be erroneously interpreted as Boolean minority. Hence the output of the majority logic group is kept as the reference while considering the output of the minority logic group to determine the DMMR system output. The failure of the majority logic group is therefore not acceptable and may be catastrophic.

It was observed in [13] that for every extra function module introduced into the minority logic group of the DMMR system, its fault tolerance increases by unity. In contrast, 2 function modules should be introduced into an NMR system to enhance its fault tolerance by unity. The 3-of-5 DMMR and 5MR systems can accommodate the faulty or the failure state of maximum of 2 function modules; the 3-of-6 DMMR and 7MR systems can tolerate the faulty or the failure state of up to 3 function modules; and the 3-of-7 DMMR and 9MR systems can withstand the faulty or the failure state of at most 4 function modules. Hence the 3-of-5, 3-of-6, and 3-of-7 DMMR systems form the corresponding redundant counterparts of the 5MR, 7MR, and 9MR systems. Thus, a higher order DMMR system can minimize the design cost, weight, and the design metrics to achieve a required degree of fault tolerance compared to a higher order NMR system.

The DMMR voter, portrayed in Fig 1, consists of a 3-input majority gate that performs majority voting on the outputs of the function modules comprising the majority logic group. The output of the majority gate is labelled *Maj*. The DMMR voter also contains a multi-input OR gate which accepts the outputs of the function modules comprising the minority logic group, performs logical disjunction, and its output is labelled *Min*. The fan-in of the multi-input OR gate is (M–3) for a 3-of-M DMMR system, and this OR gate can be arbitrarily decomposed. The intermediate outputs of the DMMR voter viz. *Maj* and *Min* are combined using a 2-input AND gate to produce the DMMR system output viz. DSO. The logical equations for *Maj*, *Min*, and DSO are given by (1), (2), and (3). F_1 to F_M represent the outputs of the function modules 1 to M, shown in Fig 1. In the equations, + denotes logical sum, and the conjunction of two or more literals represents the logical product.

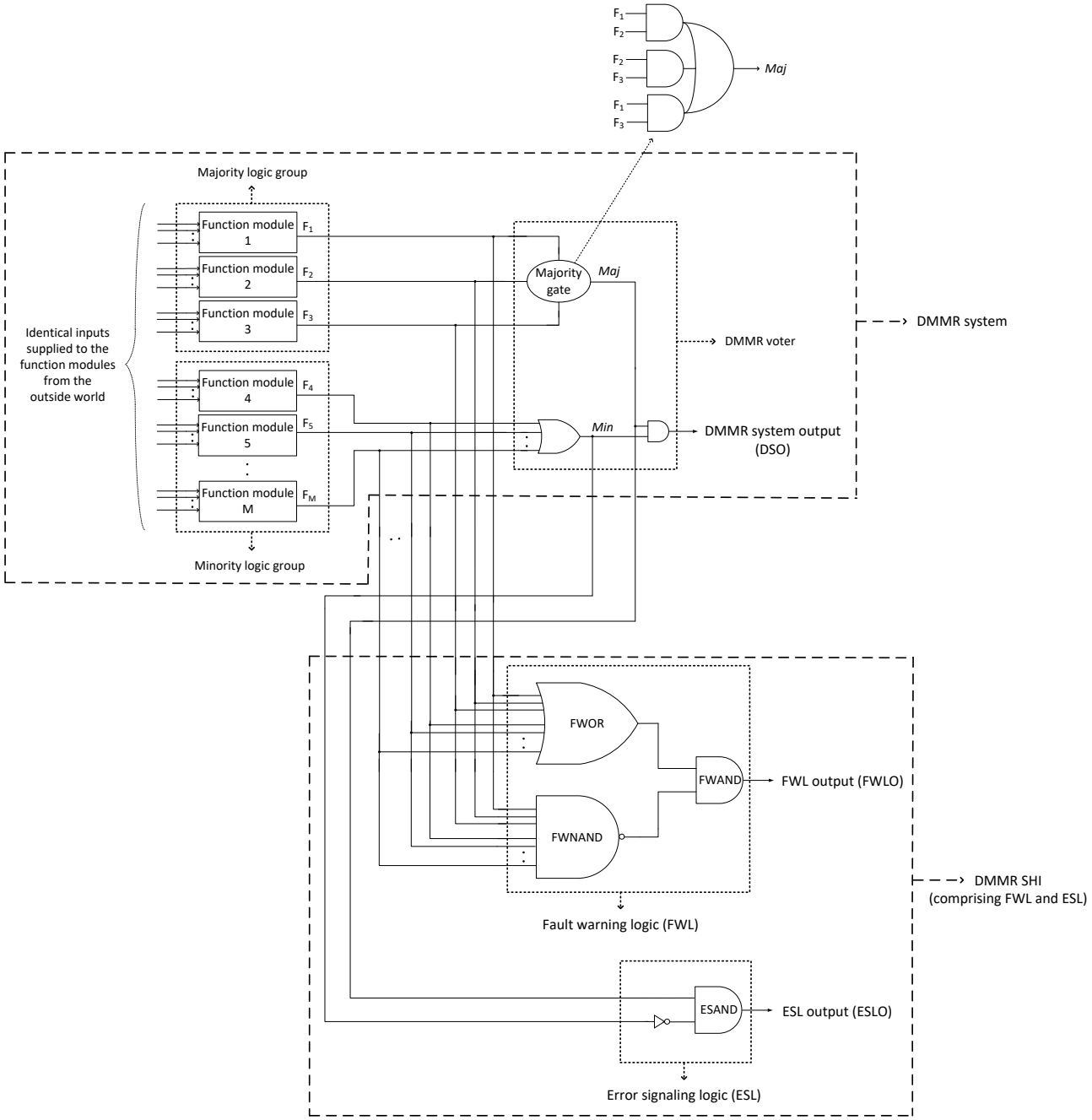

Fig. 1. Block diagram of the (3-of-M) DMMR system, shown in dashed lines at the top; the SHI is shown in dashed lines at the bottom. For function modules with multiple outputs, the FWLO and ESLO signals corresponding to the respective function module outputs would be OR-ed separately to generate the FWLO and ESLO signals for the DMMR SHI. For example, if each function module in a DMMR system has K outputs, then K numbers of FWL circuits and an equal number of ESL circuits would be implemented. The intermediate FWLO and ESLO outputs corresponding to these FWL and ESL circuits would be separately combined through two K-input OR gates to generate the FWLO and ESLO signals of the DMMR SHI.

$$Maj = F_1F_2 + F_2F_3 + F_1F_3 \quad (1)$$

$$Min = F_4 + F_5 + \ldots + F_M \quad (2)$$

$$DSO = (Maj)\,(Min) \quad (3)$$

It was shown in [13] that the voters of the 3-of-5, 3-of-6, and 3-of-7 DMMR systems require just 0.55×, 0.22×, and 0.14× areas of the corresponding majority voters of 5MR, 7MR, and 9MR systems, when implemented using a 32/28nm CMOS digital cell library [17]. This implies that even with an increase in the redundancy, the DMMR voter may be just a

small proportion of the entire DMMR system, and so it may be reasonable to assume the perfect behavior of a DMMR voter.

To discuss the operation of the basic DMMR system which does not have a SHI, as shown in the top of Fig 1, we refer to Table 1 which captures all the distinct input combinations with respect to the majority logic group and a representative set of the possible input combinations corresponding to the minority logic group.

TABLE I
ILLUSTRATION OF (BASIC) DMMR SYSTEM OPERATION

Majority Logic Group			**Minority Logic Group**				**Internal Outputs**		**System Output**	**System State**
F_1	F_2	F_3	F_4	.	.	F_M	*Maj*	*Min*	**DSO**	**(C/E)***
Majority and Minority logic groups are in perfect agreement										
0	0	0	0	.	.	0	0	0	0	C
1	1	1	1	.	.	1	1	1	1	C
***Majority logic group outputs* 0*, and Minority logic group outputs* 0 *or* 1**										
0	0	1	0	.	.	*d*	0	*d*	0	C
0	0	1	1	.	.	*d*	0	1	0	C
0	1	0	0	.	.	*d*	0	*d*	0	C
0	1	0	1	.	.	*d*	0	1	0	C
1	0	0	0	.	.	*d*	0	*d*	0	C
1	0	0	1	.	.	*d*	0	1	0	C
***Majority logic group outputs* 1*, and Minority logic group outputs* 0 *or* 1**										
1	1	0	0	.	.	0	1	0	0	E
1	1	0	1	.	.	*d*	1	1	1	C
1	0	1	0	.	.	0	1	0	0	E
1	0	1	1	.	.	*d*	1	1	1	C
0	1	1	0	.	.	0	1	0	0	E
0	1	1	1	.	.	*d*	1	1	1	C

d – Don't care state (i.e., binary 0 or 1); * C – Correct; E – Error

In Tables 1 and 3, the notations used for the function modules of the minority logic group imply the following: i) 'F_4 . . F_M' given by '0 . . 0' implies F_4 to F_M are 0, ii) 'F_4 . . F_M' given by '1 . . 1' implies F_4 to F_M are 1, iii) 'F_4 . . F_M' given by '0 . . *d*' implies F_4 is 0, and F_5 up to F_M may assume *d*, and iv) 'F_4 . . F_M' given by '1 . . *d*' implies F_4 is 1, and F_5 up to F_M may assume *d*.

There are three broad scenarios which are captured through Table 1. Firstly, when all the function modules comprising the majority and minority logic groups of the DMMR system produce identical outputs, the DMMR system output would be correct. Secondly, when the majority logic group outputs 0, and if the output of one of the function modules in the minority logic group is 1, the minority logic group will output 1. This condition is said to be an exception for the DMMR system architecture although $Maj \neq Min$. This is because the DMMR system output is governed by the logical conjunction of the outputs of majority and minority logic groups, as given by (3). In general, when the majority logic group outputs 0, the DMMR system would output 0, regardless of the correct or the incorrect state of the output of the minority logic group. Thirdly, when the majority logic group outputs 1, and if the minority logic group also outputs 1, the DMMR system output would be correct. However, when the majority logic group outputs 1, and if the minority logic group outputs 0 due to the complete faulty state or the failure of the minority logic group, the DMMR system would produce an erroneous output. Moreover, there is a likelihood for incorrectly interpreting this as a correct operation of the DMMR system. Although the complete faultiness or the failure of the minority logic group is unwarranted, it should be noted that in a basic DMMR system there is no provision to indicate this due to the absence of any SHI. This gives rise to the need for a SHI which would report the correct or the error state of a DMMR system to the outside world.

III. DMMR SHI

In [13], only a basic implementation of the DMMR system was considered with no provision for indicating any fault or error occurrence within the system. In this work, a novel and generic DMMR SHI is presented which is portrayed by the circuit shown within the dashed lines at the bottom portion of Fig 1. The DMMR SHI consists of the FWL and the ESL, whose operations are described next.

A. FWL

The FWL is shown within the dotted region at the top of the DMMR SHI in Fig 1, whose output is FWLO and is expressed by (4). The symbol ' represents logical inversion in the equations which follow.

$$FWLO = (F_1 + F_2 + \ldots + F_M)\,(F_1F_2\ldots.F_M)' \quad (4)$$

As seen in Fig 1, the equivalent outputs of the identical function modules 1 to M, i.e., F_1 to F_M are supplied to the FWOR gate and the FWNAND gate concurrently. If all the function module outputs F_1 to F_M are 0 or 1, one input to the FWAND gate would be 0 and the other would be 1 and hence FWLO would become 0, meaning no fault occurrence within the DMMR system. On the contrary, if one or more of the outputs among F_1 to F_M is 0 or 1 and the others are 1 or 0, both the inputs to the FWAND gate would be 1 and hence FWLO would assume 1 thereby reporting a fault occurrence. The FWL would issue a fault warning when one or more outputs of any function module is different from the rest of the corresponding outputs of the remaining function modules. The FWOR gate and FWAND gate, if they may have a high fan-in, may be decomposed arbitrarily and subsequently realized as a logic tree. Likewise, a high fan-in FWNAND gate may be realized as a tree of AND gates and the tree outputs can be combined using a final NAND gate.

B. ESL

The ESL is shown within the dotted region at the bottom of the DMMR SHI in Fig 1, whose output is specified as ESLO, and is expressed by (5).

$$ESLO = (Maj)\,(Min)' \quad (5)$$

Referring to Fig 1, if the outputs of majority of the function modules in the majority logic group are 0, *Maj* would evaluate to 0, and irrespective of the value of *Min*, ESLO could evaluate to 0, implying no DMMR system error. Supposing if the outputs of majority of the function modules in the majority logic group are 1, *Maj* would be 1. Simultaneously, if the output of at least one function module in the minority logic group is 1 and the rest are different due to faulty or failed function modules, *Min* would also equate to 1. Under this

condition, one input to the ESAND gate would be 1 and the other would be 0 and thus ESLO would evaluate to 0 thus implying no DMMR system error because DSO equals 1. Supposing if F_1 and F_2 are 1, and F_3 up to F_M are all 0s due to the faults or failures of function modules 3 up to M, *Maj* would equate to 1 and *Min* would equate to 0, and as a result ESLO would evaluate to 1 thereby conveying that the DMMR system is in error since DSO = 0 and it does not equal *Maj*.

C. SHI

It may be noted that the values of FWLO and ESLO define the healthy or the unhealthy state of a DMMR system as shown in Table 2.

TABLE II
DMMR SHI OUTPUTS AND INTERPRETATION OF SYSTEM STATUS

FWLO	ESLO	DMMR System Health Status
0	0	Healthy (dependable)
0	1	Indeterminate
1	0	Healthy with fault masking (dependable)
1	1	Unhealthy (not dependable)

To discuss the operation of the DMMR SHI, we refer to Table 3. Table 3, derived from Table 1, showcases the different possible scenarios which are likely to be encountered by a DMMR system, and shows how the DMMR SHI would signal no error or an error through FWLO and ESLO.

TABLE III
ILLUSTRATING THE OPERATION OF DMMR SYSTEM WITH SHI

Majority Logic Group			Minority Logic Group				System Output	System State (C/E)	SHI Outputs	
F_1	F_2	F_3	F_4	.	.	F_M	DSO		FWLO	ESLO
Majority and Minority logic groups are in perfect agreement										
0	0	0	0	.	.	0	0	C	0	0
1	1	1	1	.	.	1	1	C	0	0
***Majority logic group outputs* 0*, and Minority logic group outputs* 0 *or* 1**										
0	0	1	0	.	.	*d*	0	C	*d*	0
0	0	1	1	.	.	*d*	0	C	*d*	0
0	1	0	0	.	.	*d*	0	C	*d*	0
0	1	0	1	.	.	*d*	0	C	*d*	0
1	0	0	0	.	.	*d*	0	C	*d*	0
1	0	0	1	.	.	*d*	0	C	*d*	0
***Majority logic group outputs* 1*, and Minority logic group outputs* 0 *or* 1**										
1	1	0	0	.	.	0	0	E	1	1
1	1	0	1	.	.	*d*	1	C	*d*	0
1	0	1	0	.	.	0	0	E	1	1
1	0	1	1	.	.	*d*	1	C	*d*	0
0	1	1	0	.	.	0	0	E	1	1
0	1	1	1	.	.	*d*	1	C	*d*	0

When the majority and minority logic groups of a DMMR system are in perfect agreement, FWLO = ESLO = 0, which signifies the healthy state of a DMMR system. If the majority logic group would output 0, DSO could assume 0 regardless of the output of the minority logic group. This implies that FWLO may be 0 or 1 (i.e., *d*) and ESLO would be 0. This also represents the healthy state of a DMMR system as depicted in Table 2. When the majority logic group outputs 1 and if the minority logic group fails completely (i.e., F_4 to F_M are all 0s) then DSO = 0, which is erroneous. Under this condition, FWLO = ESLO = 1, conveying that the DMMR system is in error. Hence it is clear from Table 3 that the DMMR SHI duly reports the correct or the error state of a DMMR system which is useful information about the status of the system, making it feasible to initiate appropriate action.

IV. EXAMPLE IMPLEMENTATIONS OF DMMR AND NMR SYSTEMS WITHOUT AND WITH SHI

Example DMMR systems and their corresponding NMR systems without and with SHI were implemented by utilizing a 4×4 array multiplier for the function modules like that of [13] for comparison. The DMMR and the corresponding NMR systems were realized in semi-custom ASIC design style using the standard digital library cells of a 32/28nm CMOS process [17]. The functionalities of the gate level DMMR systems and their corresponding NMR systems, without and with SHI, were verified by performing functional simulations using Synopsys VCS. The switching activity captured through the simulations were subsequently used for estimating average power using Synopsys PrimeTime. The average power was estimated accurately by invoking the time-based power analysis mode of PrimeTime. The simulations were performed by supplying all the distinct input vectors to the (identical) function modules at time intervals of 2.5ns (i.e., 400 MHz) through test benches like that of [13]. This paves the way for a straightforward comparison of the design metrics of different redundant systems post-synthesis. The design metrics viz. average power dissipation, critical path delay, and silicon area estimated for the different DMMR and NMR systems without and with SHI, and they are given in Table 4.

To comprehensively evaluate the design parameters of the DMMR and NMR systems, a figure of merit (FOM) is defined as the inverse product of power, delay, and area. Since power, delay, and area are desirable to be minimized, the maximum FOM indicates the best result. The calculated FOM values were normalized and are also given in Table 4. The DMMR and NMR systems without SHI are referred to as basic DMMR and NMR systems in Table 4 for the ease of referencing.

TABLE IV
DESIGN METRICS AND NORMALIZED FOM OF EXAMPLE DMMR SYSTEMS AND THEIR COUNTERPART NMR SYSTEMS WITHOUT SHI (BASIC) AND WITH SHI, ESTIMATED USING A 32/28NM CMOS PROCESS

Redundant System	Power (μW)	Delay (ns)	Area (μm^2)	Normalized FOM
Fault tolerance of* 2 *function modules				
5MR (Basic)	120.7	0.98	529.64	38.93
3-of-5 DMMR (Basic)	109.3	0.90	480.84	51.56
5MR (with SHI)	184.4	1.32	1037.92	9.66
3-of-5 DMMR (with SHI)	133.4	1.13	619.09	26.15
Fault tolerance of* 3 *function modules				
7MR (Basic)	191.2	1.12	865.11	13.17
3-of-6 DMMR (Basic)	129.4	0.90	567.25	36.93
7MR (with SHI)	302.5	1.45	1804.42	3.07
3-of-6 DMMR (with SHI)	157.7	1.15	709.57	18.95
Fault tolerance of* 4 *function modules				
9MR (Basic)	278.5	1.23	1269.7	5.61
3-of-7 DMMR (Basic)	151.2	0.91	661.79	26.78
9MR (with SHI)	462.8	1.70	3072.62	1
3-of-7 DMMR (with SHI)	183.3	1.19	816.31	13.71

It should be noted that the FWL and ESL portions of the DMMR SHI and the NMR SHI are more sophisticated than the corresponding voting logic of the DMMR and NMR systems.

Hence, more logic gates are utilized for the DMMR and NMR systems with SHI compared to their basic implementations which results in increased area and power dissipation for the former. The critical path of the basic DMMR and NMR systems involves the function module and the voter, whereas the critical path of the DMMR and NMR systems with SHI involves the function module and the SHI. This explains the reason behind the increases in critical path delays for the DMMR and NMR systems with SHI compared to the critical path delays of their basic implementations. As a result, the increases in power dissipation, area occupancy, and critical path delay for the DMMR and NMR systems with SHI are inevitable compared to their basic implementations. Hence the FOM of the former would be inferior to the FOM of the latter. Nevertheless, this is a trade-off which is implicit to ascertain valuable information about the state of the system.

From Table 4 it is calculated that on average the DMMR systems with SHI report a 49% reduction in FOM compared to the FOM of basic DMMR systems, and the NMR systems with SHI report a 76.2% decrease in FOM compared to the FOM of basic NMR systems. Let us compare the FOM of DMMR systems with SHI with the FOM of NMR systems with SHI. The 5MR, 7MR, and 9MR systems with SHI were realized based on [16]. The FWL portions of the DMMR SHI and the NMR SHI may be logically equivalent, but their ESL portions are different. The ESL portion of the NMR SHI substantially increases in size with an increase in the order of the NMR system. In an NMR system, where at least a majority K out of the N identical function modules is expected to maintain the correct operation it gives rise to NC_K distinct majority combinations, where NC_K represents the mathematical combination: $NC_K = [N!/\{K!\times(N - K)!\}]$. For the 5MR, 7MR, and 9MR systems, NC_K evaluates to 10, 35, and 126 respectively. This means that the matching logic forming part of the ESL of the NMR SHI, which is responsible for determining the equality or the non-equality of the corresponding outputs of the NC_K function module(s), would also significantly increase in size. As a result, with an increase in the redundancy order from 5MR to 9MR, the ESL portion of the NMR systems with SHI would feature a substantial increase in the logic complexity. Hence, the higher order NMR systems with SHI would have much more logic consequently leading to more area and power dissipation and encounter greater critical path delay. This explains why the FOM of NMR systems with SHI are less than the rest in Table 4.

From Table 4, it is calculated that the FOM of the 3-of-5, 3-of-6, and 3-of-7 DMMR systems with SHI are greater than the FOM of the 5MR, 7MR, and 9MR systems with SHI by 1.7×, 5.2×, and 12.7× respectively. Thus, on average, the FOM of the DMMR systems with SHI is significantly greater than the FOM of the corresponding NMR systems with SHI by 6.5×.

V. Conclusions

In this paper, the novel design of a generic SHI for the DMMR scheme was presented. The SHI is useful as it could provide continuous and valuable real-time information about a DMMR system's health, i.e., whether the system is healthy or not, thus advancing the system safety and reliability. This avoids making any assumption about the operational state of a DMMR system. Further, the SHI improves the observability of the system and this could be useful when performing online testing and/or troubleshooting of any faulty zones in the system, preemptively or during any scheduled maintenance.

The higher order DMMR systems, i.e., the 3-of-6 and 3-of-7 DMMR systems with SHI report greater FOM than even the basic NMR systems while providing similar degrees of fault tolerance and in addition conveying useful information about the system health. Further, the DMMR systems with SHI feature substantially greater FOM than their corresponding NMR systems incorporating SHI. Hence, we infer that for the design of a redundant system along with SHI, the DMMR scheme is preferable to the conventional NMR scheme.

References

[1] B.W. Johnson, *Design and Analysis of Fault-Tolerant Digital Systems*, Addison-Wesley Publishing Company, USA, 1989.

[2] I. Koren, C. Mani Krishna, *Fault-Tolerant Systems*, Morgan Kaufmann Publishers, CA, USA, 2007.

[3] E. Dubrova, *Fault-Tolerant Design*, Springer, NY, USA, 2013.

[4] N. Miskov-Zivanov, D. Marculescu, "Multiple transient faults in combinational and sequential circuits: a systematic approach," *IEEE Trans. CAD Integr. Circuits Syst.*, vol. 29, pp. 1614-1627, 2010.

[5] N.N. Mahatme *et al*., "Terrestrial SER characterization for nanoscale technologies: a comparative study," *Proc. IEEE International Reliability Physics Symposium*, pp. 4B.4.1-4B.4.7, 2015.

[6] M. Ebrahimi *et al*. "Comprehensive analysis of sequential and combinational soft errors in an embedded processor," *IEEE Trans. CAD Integr. Circuits Syst.*, vol. 34, pp. 1586-1599, 2015.

[7] T. Karnik, P. Hazucha, J. Patel, "Characterization of soft errors caused by single event upsets in CMOS processes," *IEEE Trans. on Dependable and Secure Computing*, vol. 1, pp. 128-143, 2004.

[8] R.C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. on Device and Materials Reliability*, vol. 5, pp. 305-316, 2005.

[9] H. Quinn *et al*., "Radiation-induced multi-bit upsets in SRAM-based FPGAs," *IEEE Trans. Nuclear Science*, vol. 52, pp. 2455-2461, 2005.

[10] N. Seifert *et al*., "Radiation-induced soft error rates of advanced CMOS bulk devices," *Proc. IEEE Intl Reliab. Phys. Symp.*, 217-225, 2006.

[11] D. Rossi *et al*., "Impact of aging phenomena on soft error susceptibility," *Proc. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, pp. 18-24, 2011.

[12] T. Ban, L. Naviner, "Progressive module redundancy for fault-tolerant designs in nanoelectronics," *Microelectronics Reliability*, vol. 51, pp. 1489-1492, 2011.

[13] P. Balasubramanian, D.L. Maskell, "A distributed minority and majority voting based redundancy scheme," *Microelectronics Reliability*, vol. 55, pp. 1373-1378, 2015.

[14] N.H. Vaidya, D.K. Pradhan, "Fault-tolerant design strategies for high reliability and safety," *IEEE Trans. Comput.*, 42, pp. 1195-1206, 1993.

[15] S. Mitra, E.J. McCluskey, "Word-voter: a new voter design for triple modular redundant systems," *Proc. 18th IEEE VLSI Test Symposium*, pp. 465-470, 2000.

[16] P. Balasubramanian, "ASIC-based design of NMR system health monitor for mission/safety-critical applications," *SpringerPlus*, vol. 5:628, pages 16, 2016.

[17] Synopsys SAED32/28_CORE Databook, Revision 1.0.0, 2012.