AUTOMATIC LINEARITY (IP3) TEST WITH BUILT-IN PATTERN GENERATOR AND ANALYZER

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ABSTRACT: We present a Built-In Self-Test (BIST) approach based on direct digital synthesizer (DDS) for functionality testing of analog circuitry in mixed-signal systems. Of particular interest, and a main contribution of this paper, is the BIST-based hardware implementation and measurement of amplifier linearity (IP3) test using DDS. The approach described in this paper has been implemented in Verilog and synthesized into FPGAs where it was used for functional testing and compared to simulation results.

1. INTRODUCTION

Analog functionality testing in a high-speed radio frequency integrated circuit (RFIC) is a time-consuming and costly process based on the current methodology of manual analog testing. It is becoming a substantial barrier to continued RFIC cost reductions because of the additional complexities required by new standards – including multi-band compatibility, higher linearity, lower bit-error rate, and longer battery life. Typical test costs as a percentage of the manufacturing cost are commonly low for digital application specific integrated circuits (ASICs). However, the RFIC test cost can be as high as 50% of the total cost, depending on the complexity of the functionality to be tested. The overall cost of an RF system consists of manufacturing, testing (wafer sort and final testing) and packaging. The DC wafer test for RFICs is mainly digital using cheap testers to prune away defective devices. Typically in this flow, the RF circuitry is bypassed due to the high cost of RF testers. Unfortunately, RF functional faults cannot be tested until the chip is packaged, resulting in a significant loss since RFIC packaging can represent 30% of the overall cost. Current test practices are expensive because of, among other reasons, the required tester infrastructure, long test times, cumbersome test preparation, lack of appropriate defect and fault models, and lack of standardized tests.

It is therefore highly desirable to automate the analog testing process with low cost, built-in test circuitry. Analog test features built into the RF and base-band ASICs could provide not only analog test capability, but also an efficient technique for calibrating and compensating analog circuitry that is sensitive to temperature, supply voltage and process variations. Built-In Self-Test (BIST) and design for testability (DFT) of analog circuits are important and necessary to produce highly reliable mixed-signal systems. Due to the constant increase of analog circuit speed and density, the nature of analog faults, and the embedding of analog functions within large digital systems, the detection and isolation of faults in these circuits is becoming more difficult. At the operating frequencies beyond a few GHz, analog IC testing requires tester electronics close to the device under test, or even better, directly built on-chip. Hence, BIST and other forms of embedded analog testing will come to market in just a matter of time [1].

A few techniques have been suggested to perform on-chip frequency-domain testing of mixed-signal circuits. These approaches normally focus on one or two simple parameter tests such as cut off frequency of a filter and cannot perform rigorous and complete analog tests such as frequency response, linearity, noise and modulation tests. The goal of prior art techniques was to overcome the complexity of integrating a traditional AC characterization approach [2]. Well-defined techniques for reducing the size of the test set while maintaining high fault coverage have been reported [3][4]. Some AC BIST techniques inject optimized digital inputs into a linear device under test and extract a DC signature [5][6]. These approaches are simple, but their precision is limited. On the other hand, Roberts [7] has proposed several methods to make frequency-domain tests using on-chip generated sine waves and analyzing the results with an on-chip digital signal processor (DSP). The approach requires 1-bit sigma–delta digital-to-analog converters with moderate area overhead. The precision of the generated frequency is not fine enough to support some analog tests such as various analog modulation and linearity tests using precise two-tones. Several techniques have been published to generate on-chip linear ramps [8]–[12], but the results either depend largely on the accuracy of the additional components in the test circuitry, or have not been proven experimentally. An on-chip ramp generator can perform monotonicity and histogram tests of analog-to-digital converters (ADCs), yet the linearity of on-chip ramp generator itself needs to be very high.

Analog BIST can be categorized into two types, one is the analog functional test and another is the structural

fault test. The difference between functional testing and structural testing is that the test patterns in structural testing are derived from the circuit implementation rather than from the circuit specification. Given that the transistor count of analog circuits is not typically large, structural testing can benefit from inductive fault analysis techniques. In this way, the test pattern is targeted to a set of realistic faults. Additionally, it is possible to derive figures of merit such as defect and fault coverage to measure the test pattern effectiveness.

Structural testing focuses on the development of DC and transient testing of analog circuits. In transient testing, the circuit under test is excited with a transient test stimulus and the circuit response is sampled at specified times to detect the presence of a fault. The transient waveform can be formed from piecewise linear segments that excite the circuit in such way that the sensitivity of the fault to the specific stimulus is magnified. These waveforms can have a periodic shape, or even arbitrary shapes, or as recently proposed they can have a binary shape with distinct duty cycles. It is also possible to structurally test the circuit by testing its DC conditions, e.g. by inspecting quiescent currents.

Analog functional test is a challenging task even for a manual test by an experienced engineer. It tests the functionality of the integrated circuit against the system specifications. The complexity of the functional test depends on test tasks and the operation frequency. For instance, a base-band amplifier test normally includes its linearity, frequency response, in-band ripple and 3dB cut-off frequency. While for a RF low-noise amplifier (LNA) test, we need to characterize its noise figure (NF), linearity through the 3rd order intercept point test (IP3), frequency response including gain, and return loss that is related to the input matching.

We have been investigating the use of a direct digital synthesizer (DDS) based testing approach, which can generate various modulated waveforms and frequency tones for analog functionality test. The approach is illustrated in Figure 1 for a wireless transceiver RFIC with automatic analog self-test features. For base-band digital test features such as the test waveform generator and output response analyzer, we initially designed and synthesized the functionality in Field Programmable Gate Array (FPGA) technology with the intent to eventually fabricate the design in a CMOS ASIC. We have been investigating and analyzing the DDS-based BIST approach for its ability to detect faults and to assist in characterization and calibration during manufacturing and field testing. The vast majority of the BIST circuitry resides in the digital portion of the mixed-signal system to minimize performance impact on the analog circuitry. The only test circuitry added to the analog domain is the analog multiplexers needed to facilitate the return path for the test signals to the BIST circuitry. The test scheme utilizes the existing digital-to-analog converters (DACs) and ADCs associated with conventional transceiver base-band architectures and thus provides accurate analog testing without adding much extra hardware.

The DDS approach can provide precise frequency tones for many analog tests such as IP3 measurement and can generate various modulated waveforms such as ramp, step, FSK, PSK, MSK, etc. The area penalty associated with a conventional DDS approach is minimized by a novel delta-sigma noise shaping scheme presented in this paper. While measurement of IP3 is straightforward with a spectrum analyzer, another challenge is the development of an efficient output response analyzer (ORA) that can make the IP3 measurement on-chip and, with the DDS-based test pattern generator (TPG), create a BIST architecture. Such a BIST approach can then be modeled in VHDL or Verilog for easy inclusion in any mixed-signal design. Therefore, the development of the ORA is another important focus of this paper.

2. DDS WITH DELTA-SIGMA NOISE SHAPING

DDS is an important frequency synthesis technique that provides low cost synthesis with ultra fine resolution. As shown in Figure 2, a conventional DDS includes a digital accumulator that generates the phase word based on the input frequency word *W*. The synthesizer step size is defined as $f_{clk}/2^n$. Fine resolution can thus be achieved using a large accumulator size. The DDS utilizes a look-up table to convert the phase word to a sinusoidal amplitude word, whose length is normally limited by the finite number of input bits of the DAC. Deglitch filters are added after the DAC to remove the spurious components generated in the data conversion process. While a pure sinusoidal waveform is desired at the DDS output, spurious tones can also occur mainly due to the following two nonlinear processes. First, in order to reduce the look-up table Read Only Memory (ROM) size, the phase word needs to be truncated before being used as the ROM addresses. This truncation process introduces quantization noise, which can be modeled as a linear additive noise to the phase of the sinusoidal wave. Second, the ROM word length is normally limited by the finite number of bits of the available DAC. In other words, the sinusoidal waveform can be expressed only by words with finite length, which intrinsically contains quantization error additive to the output amplitude. Considering the quantization errors due to phase truncation e_p, and amplitude truncation (finite ROM word length) e_A, and assuming the phase quantization error is small relative to the phase, the DDS output can be determined as:

$$A_{out} = A\sin\left(\frac{2\pi Wi}{2^n} + e_p(i)\right) + e_A(i) \approx A\sin\left(\frac{2\pi Wi}{2^n}\right) + Ae_p(i)\cos\left(\frac{2\pi Wi}{2^n}\right) + Ae_A(i) \quad (1)$$

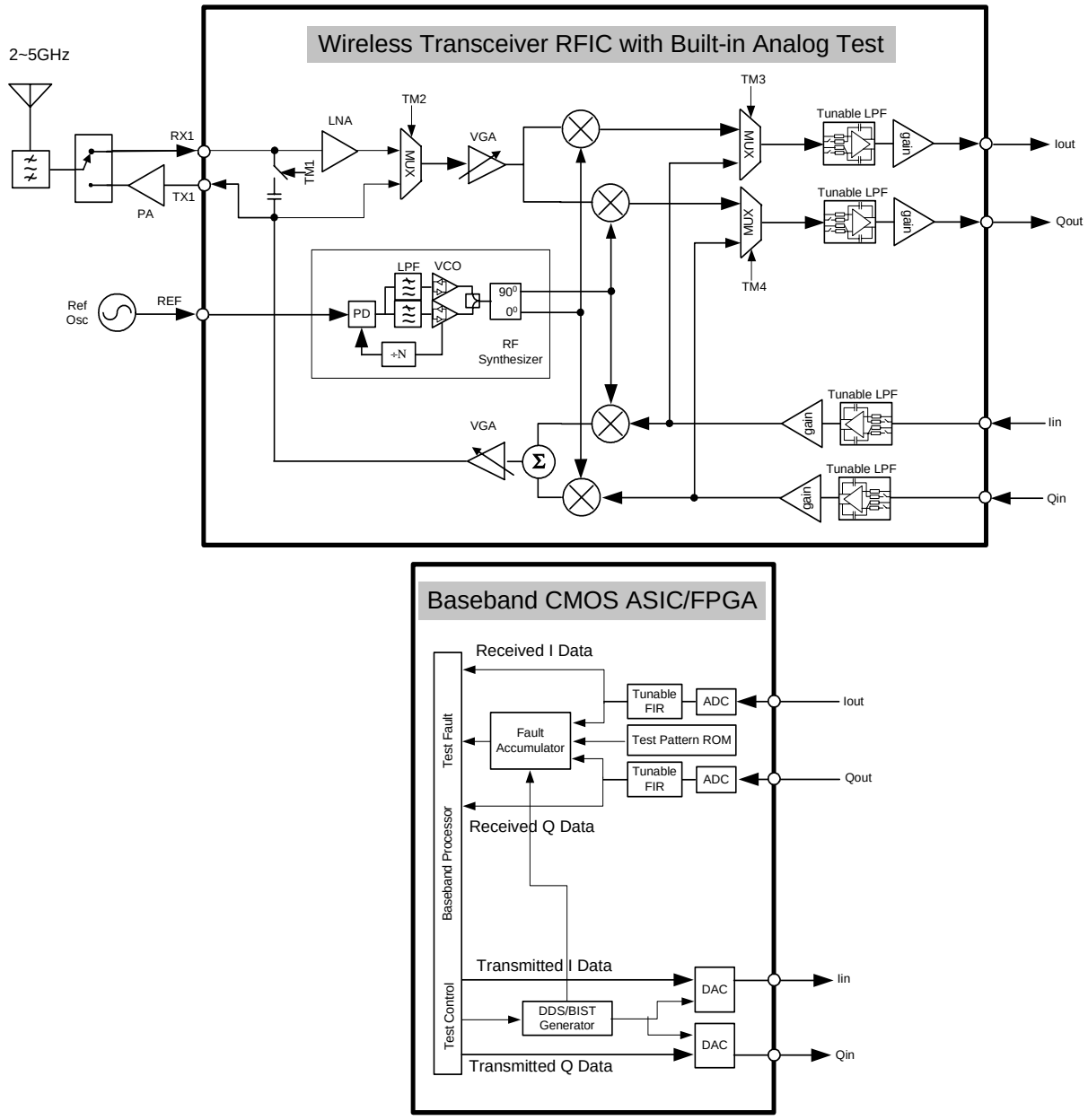


Figure 1. Wireless transceiver architecture with built-in analog test generator and analyzer.

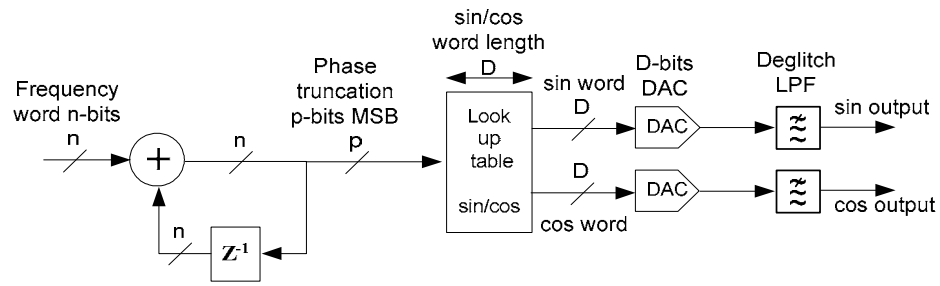


Figure 2. Direct digital synthesizer (DDS) for test signal generation.

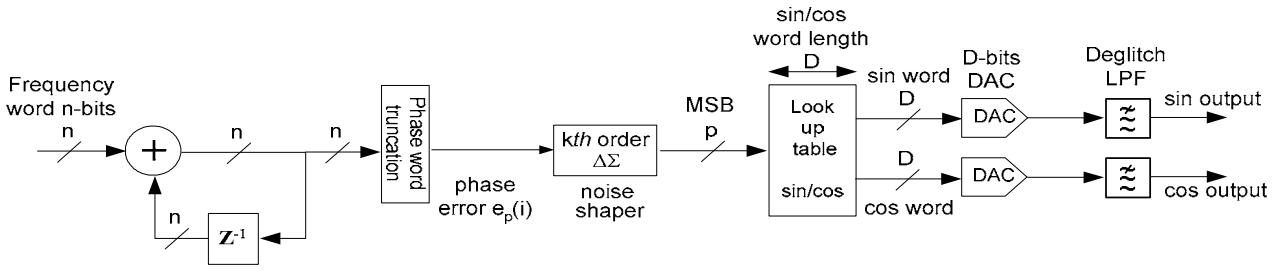


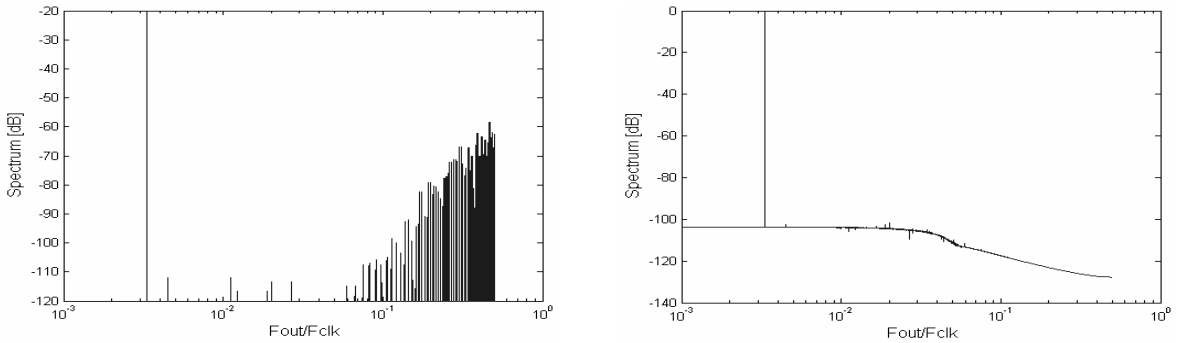
Figure 3. Block diagram of the proposed DDS with a *k*th order delta-sigma noise shaper.

It has been shown that the phase truncation process associated with the conventional DDS architecture introduces quantization error. To avoid aliasing during data conversion, the synthesized frequency is required to be smaller than the DDS clock frequency. Thus, oversampling is always encountered in DDS, allowing noise-shaping techniques to be used to shift the phase quantization error to a higher frequency band, where the noise can be eventually removed by the deglitch filter after the DAC. As shown in Figure 3, a *k*th order delta-sigma noise shaper with unique transfer function is added after the phase truncation. It can be shown that the phase error e_p is high-pass filtered by the sigma-delta interpolator before the amplitude modulation via the look-up table. It greatly reduces the close-in phase noise and de-correlates the phase truncation error. As a result, spurious components at the DDS output are greatly reduced or eliminated. A more ideal sinusoidal waveform with greatly reduced close-in phase noise and spurious components is achieved at the DDS output.

A high-order delta-sigma interpolator can be implemented using pure shifting and adding operations, resulting in little area penalty by avoiding multipliers. In order to prove the concept, we modeled proposed DDS architecture using delta-sigma noise shaper to remove phase truncation error in MATLAB. Figure 4a shows the spectrum for the proposed DDS architecture using a 4th order delta-sigma noise shaper. Figure 4a clearly demonstrates high-pass noise shaping effect of the 4th order delta-sigma interpolator with an 80dB/dec slope. Figure 4b shows the spectrum after the deglitch filter for the DDS architecture using a 4th order delta-sigma noise shaper and shows that the spurs associated with the phase truncation are filtered by the deglitch filter and clean spectrum purity is achieved.

The importance of the delta-sigma DDS architecture lies in the fact that the area associated a ROM look-up table can be greatly reduced compared to the conventional DDS with the same output noise floor. Note that the look-up table takes majority of the DDS area. In order to generate frequency tones with fine step size, the accumulator size *n* has to be large. Thus, the number of phase bits used as the ROM address is large. With the delta-shaping scheme, we can then allow large number of accumulator bits and small number of ROM address bits simultaneously by truncating the phase bits at the accumulator output and removing the truncation error using the delta-sigma interpolator.

The DDS synthesizer/modulator can implement various waveforms such as chirp, ramp, step frequency, MSK, phase modulation, amplitude modulation, QAM and other hybrid modulations, as shown in Figure 5. Thus, it provides a low cost digital approach to frequency, phase and amplitude modulations, eliminating costly analog modulators associated with many analog measurements. The modulated waveform generation is a unique feature of the DDS-based BIST approach. None of the prior art analog testing schemes [1-12] can perform such complete waveform generation as that of the DDS synthesizer/modulator.



a) after the phase truncation b) after the deglitch filter

Figure 4. Spectrum of the proposed DDS using a 4th order delta-sigma noise shaper.

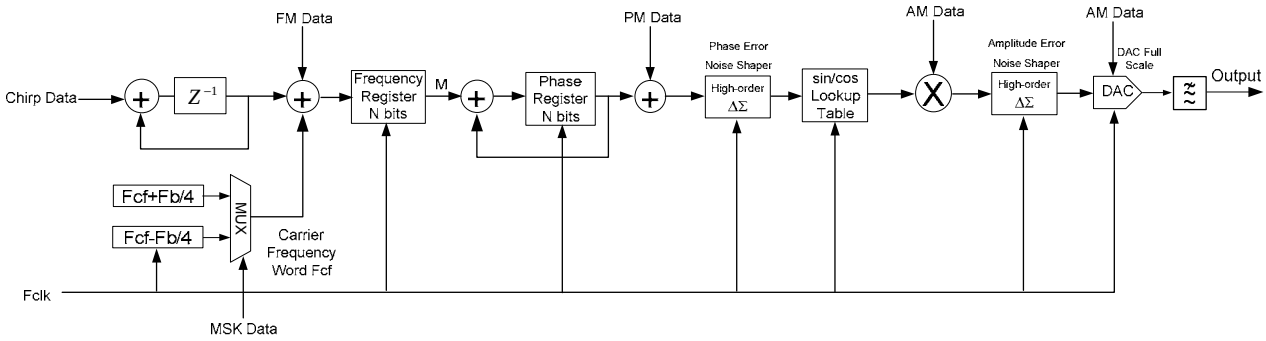


Figure 5. Modulation waveform generation using DDS with delta-sigma noise shaper.

4. ANALOG FUNCTIONALITY TESTS USING DDS

The DDS-based testing approach can provide precise frequency tones for many analog tests such as IP3 measurement and can generate various modulated waveforms, as shown in Figure 5.

Base-band Low Pass Filter (LPF) Test Using DDS: Frequency response (both amplitude and phase response) is the key measure for an integrated LPF. The commonly interested cut-off frequency can be found out by measuring the passband and stopband amplitude response, while the linearity (group delay) can be determined from the phase response. To test the base-band LPF in the transceiver RFIC as shown in Figure 1, the DDS integrated in the base-band ASIC generates a single frequency tone that loops back from transmitter to receiver through multiplexers control by TM3 and TM4 for the I and Q channels, respectively. The DDS generates frequency tones with fine resolution. It can scan the pass and stop bands of the LPF with fine step size and can thus measure the cut-off frequency and passband and stopband ripples of the filter.

One of major problems associated with integrated analog filters is the cutoff frequency variation due to temperature, supply voltage and process variations. If the cut-off frequency can be monitored on the fly during transmission idle periods (e.g., the preamble period in WLAN applications), its variation can be compensated using built-in tunable circuitry in LPF designs.

Base-band Gain Stage Frequency Response Test Using DDS: The frequency response of the base-band gain stage amplifiers can be tested in the same way used to test the base-band LPF frequency response. Basically, the DDS generates frequency tones and scans the pass and stop bands of the amplifier.

Besides production test, the frequency response monitoring can also be used to adjust the gain and bandwidth of the amplifier for multi-band and multi-standard applications. With wireless standards operating in very different frequency bands, market-leading wireless solutions have to offer multi-mode interoperability with transparent worldwide usage. Thus, the base-band gain stage needs to be tunable for different wireless standards. The DDS-based test scheme can be used to calibrate the frequency response of the base-band gain stage and LPF in this connection.

RF Amplifier Test Using DDS: An RF amplifier such as an LNA or an RF variable gain amplifier (VGA) can be tested in a similar way as that of a base-band amplifier with the assistance of existing mixers in the RF transceiver. To test the amplifiers at the RF frequency (2GHz to 5GHz), up-converter and down-converter have to be employed. Again, we use DDS to generate the test tones, namely, scanning tones to test the amplifier frequency response and two-tones to test the amplifier linearity. Those base-band frequency tones can be up-converted to RF frequency by mixing them with the RF carrier frequency generated by RF synthesizer. The RF amplifier output is down-converted to base-band by mixing it with the RF carrier frequency generated by RF synthesizer. The up- and down-converters are image-rejection mixers and thus no image tones will be collected. The up-down-converters and RF synthesizers are the building blocks of every RF transceiver and thus no extra hardware except a few multiplexers is needed to perform automatic analog testing and calibration of RF amplifiers.

To test the VGA, the RF test tones are looped back to VGA input by selecting the multiplexer controls TM2. To test the LNA, the test signal is feed to the LNA input by selecting the controls TM1. To remove the impact of VGA on LNA test, the VGA should also be tested separately with the same input signals and its output response will be subtracted from the LNA test response. Again, since there is a one-to-one mapping between the digitized bit stream and the amplifier output spectrum, the amplifier linearity and frequency response can thus be measured by comparing the digitized bit stream to the pre-calculated golden test output patterns stored in the test pattern ROM.

5. AMPLIFIER LINEARITY (IP3) TEST USING DDS

Linearity is an important measure of any amplifier performance. Amplifier linearity is normally measured by the 3rd order inter-modulation product (IP3) under two-tone test. The DDS can be used to generate two frequency tones required in the two-tone test. When the two-tone test signal passes through an amplifier, both fundamental and 3rd order inter-modulation (IM3) terms will be present at the amplifier output as shown in Fig.6. The input referred IP3 (IIP3) can thus be found by:

$$IIP_3[dBm] = \frac{\Delta P[dB]}{2} + P_{in}[dBm] \tag{2}$$

where ΔP is the difference between fundamental and IM3 terms and P_{in} is the signal power at the amplifier input. To measure the IIP3 based on Eq. (2), a fast Fourier transform (FFT) is required to capture the amplifier output spectrum. Since there is a one-to-one mapping between the digital bit stream (time domain data) and the amplifier output spectrum (spectral domain data), the amplifier linearity can be measured by comparing the digital bit stream of its output to the pre-calculated golden patterns, avoiding FFT computations.

IP3 measurement using FFT requires a large amount of hardware and is not desired for a BIST implementation. As an alternative, we use a multiplier as the down converter to selectively pick the frequency components and down-convert them into a DC signal. The DC level can be further compacted for evaluation by using an accumulator. The following derivation provides a mathematical proof-of-concept for the proposed IIP3 testing technique.

Assume two tones $x(t)=A_1\cos\omega_1 t + A_2\cos\omega_2$ are applied to the input of an amplifier with transfer function expressed as $y(t)=\alpha_0+\alpha_1 x(t)+\alpha_2 x^2(t)+\alpha_3 x^3(t)+\ldots$, where a_j are in general independent of time if the system is time invariant. Inserting the two-tone input into the transfer function, we obtain the amplifier output as:

$$\begin{aligned}
y(t) &= \frac{1}{2}\alpha_2(A_1^2 + A_2^2) \\
&+ \left[\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1(A_1^2 + 2A_2^2)\right]\cos\omega_1 t \\
&+ \left[\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2(2A_1^2 + A_2^2)\right]\cos\omega_2 t \\
&+ \frac{1}{2}\alpha_2\left[A_1^2\cos 2\omega_1 t + A_2^2\cos 2\omega_2 t\right] \\
&+ \alpha_2 A_1 A_2\left[\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t\right] \\
&+ \frac{1}{4}\alpha_3\left[A_1^3\cos 3\omega_1 t + A_2^3\cos 3\omega_2 t\right] \\
&+ \frac{3}{4}\alpha_3\left\{\begin{aligned}&A_1^2 A_2\left[\cos(2\omega_1+\omega_2)t + \cos(2\omega_1-\omega_2)t\right] \\ &+ A_1 A_2^2\left[\cos(2\omega_2+\omega_1)t + \cos(2\omega_2-\omega_1)t\right]\end{aligned}\right\}
\end{aligned} \tag{3}$$

According to Eq. (3), the input referred IP3 (IIP3) and the output referred IP3 (OIP3) can be found as:

$$\begin{aligned}
IIP_3 &\approx \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}\ , \text{if } \alpha_1 >> \frac{9}{4}\alpha_3 A^2 \\
OIP_3 &= \alpha_1 IIP_3
\end{aligned} \tag{4}$$

where the assumption for IIP3 is normally valid when the test tone magnitude is relatively small such that the amplifier is not desensitized.

For IP3 BIST, we use the following technique for the ORA. As can be seen from Figure 6, the closest inter-modulation terms to the fundamental are the IM3 terms with frequencies at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$. First, mixing (multiplying) the amplifier output, Eq. (3), with fundamental tone $A_2\cos\omega_2 t$, produces a DC term:

$$DC_1 = \frac{1}{2}A_2^2\left[\alpha_1 + \frac{3}{4}\alpha_3(2A_1^2 + A_2^2)\right] \approx \frac{1}{2}A_2^2\alpha_1 \tag{5}$$

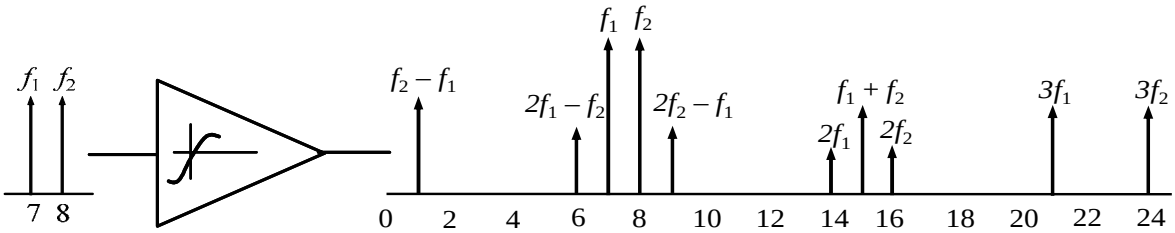
where the second term in Eq. (4) is normally much smaller than the linear gain, α_1, if the input level is small, such that the amplifier is not desensitized. Second, mixing (multiplying) the amplifier output, Eq. (3), with the IM3 tone $A_1\cos(2\omega_2-\omega_1)t$, produces another DC term:

$$DC_2 = \frac{3}{8}A_1^2 A_2^2\alpha_3 \tag{6}$$

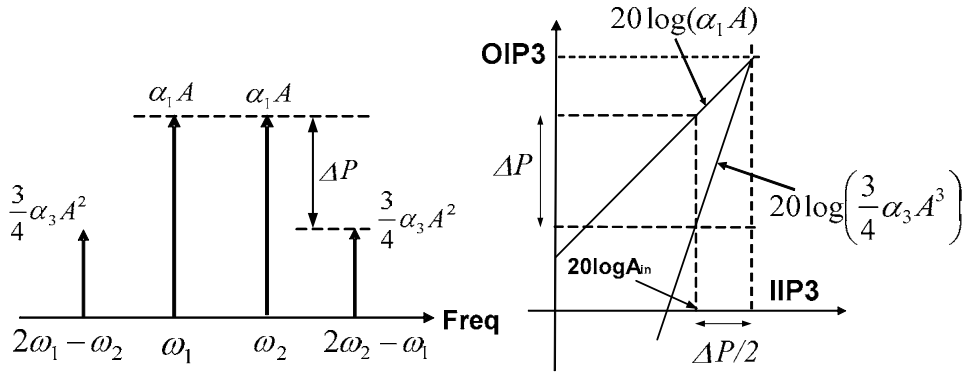
Expressing these two DC terms in dB, we can find the difference ΔP between fundamental and the IM3 and the IIP3 can thus be measured using Eq. (2). Although we can represent dB unit using floating-point format, we don't need to find the actual IP3 value using real hardware in an ORA for a BIST implementation. We may pre-calculate the linear gain requirement to evaluate DC_1 and the IM3 requirement to evaluate DC_2. Then accumulating these values as they exit the multiplier and averaging based on the number of samples, the results can be compared to pre-determined ranges of acceptable values for a pass-fail BIST indication. For characterization of the circuit, the accumulated values can be read and averaged off-chip to perform the IP3 calculation.

The complete linearity test pattern generator (TPG) and output response analyzer (ORA) for our BIST implementation are illustrated in Figure 7. The ORA consists of an N-bit unsigned multiplier (where N is the number of bits from the ADC) and an $2N+M$-bit accumulator (where the number of samples is $<2^M$). A 2's complement transformation is performed on negative numbers entering the accumulator such that subtraction is accomplished by the adder in the accumulator. In addition, the DDS input to the multiplier is converted to a signed magnitude number

while removing DC offset from the DDS output. The sign bit is then used to control the 2's complement transformation at the input to the accumulator.



(a) Output spectrum with two tones at 7 and 8 (MHz).



(b) Calculate IP3 using IM3 and fundamental terms.

Figure 6. Amplifier linearity (IP3) test using two-tones generated by DDS.

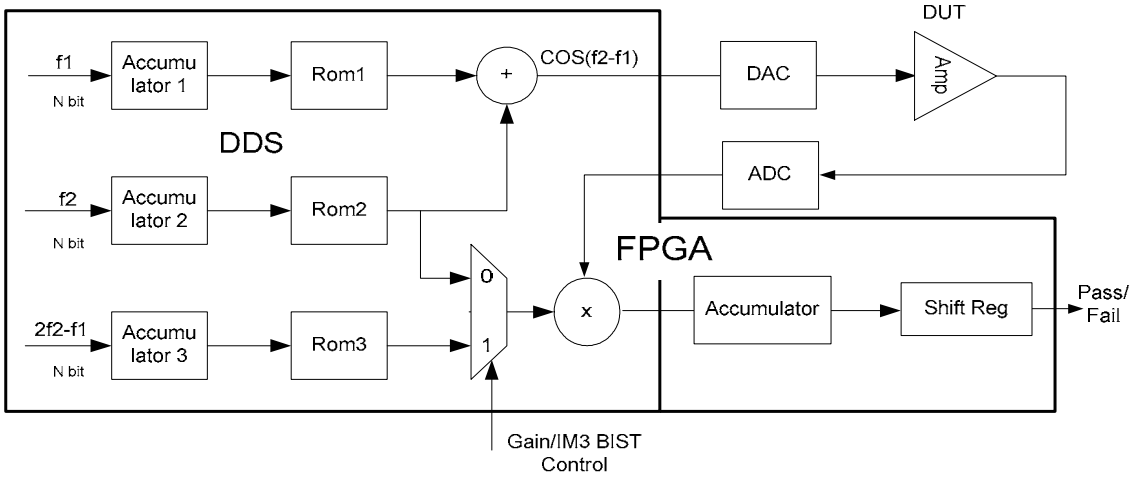


Figure 7. Linearity test generator and analyzer configuration.

6. EXPERIMENTAL RESULTS

Using MATLAB and Verilog, we simulated the proposed amplifier linearity (IP3) BIST scheme for different values of the amplifier third order coefficient α_3. We used test tones with small magnitude such that the amplifier is not desensitized. As an example, the simulated values of the DC_1 accumulator, DC_2 accumulator, and resultant ΔP as a function of the number of clock cycles used to sample the signals are shown in Figure 8, Figure 9, and Figure 10, respectively, for a simulated amplifier with a 20dB ΔP. As can be seen the BIST scheme achieves accurate IIP3

measurements without using any FFT algorithm for spectrum analysis. While an FFT scheme tries to calculate the whole spectrum information with limited number of points, the multiplier-accumulator-based ORA focuses just on the useful spectral information at two frequencies ω_2 and $2\omega_2-\omega_1$ under two-tone test, which is more efficient in terms of area than an FFT implementation.

It is important that the BIST sequence be controlled to run for integer multiple of periods of the lowest frequency tone $\omega_2-\omega_1$, since it's closest tone to DC. The contribution from other tones at higher frequency is relatively small and can be ignored when large number of samples is accumulated. The ripples shown in Fig. 8-10 are of the frequency of $\omega_2-\omega_1$. If we stop the accumulation at the integer multiple of period of $\omega_2-\omega_1$, convergent DC values for DC_1, DC_2 and delta-P can be extracted at the ORA output. Due to the symmetry of sinusoidal waves, other frequency tones cancel out after accumulation through integer multiple periods. The error occurs when we stop the accumulation at non-integer multiple of periods. However, the error is accumulated only for less than one period. Thus, longer accumulation will reduce the impact of residual errors. The need to use a large number of samples for accumulation is apparent in Figure 10 where the ΔP value becomes more accurate with a larger number of samples. As a result, we can trade-off accuracy of the measured ΔP value with the BIST area overhead, which is much smaller than that of a FFT algorithm would take anyway. Thus, the ORA technique provides an efficient means for analog linearity BIST. The BIST scheme can also be used to monitor the linearity variations of analog modules, which is critical for designing automatic linearity compensation circuitry.

We implemented the DDS-based BIST approach in hardware to obtain measurements for comparison with our simulations. An Anadigm AN221E04 Field Programmable Analog Array (FPAA) was configured as a linear amplifier and used as the device under test for our IP3 linearity test configuration. The FPAA amplifier operates around 500 KHz and non-linearity was introduced into the amplifier by lowering its power supply voltage from 5V to about 4V. A 12-bit DAC with low-pass filter and a 12-bit ADC were implemented on a separate printed circuit board with a separate power supply but only the eight most significant bits of the DAC and ADC were used in our system to demonstrate a BIST scheme with small area penalty. The digital BIST circuitry was implemented in a Xilinx Spartan 2S50 FPGA on a Xess XSA50 printed circuit board. The spectrum analyzer measurement of the two-tone test at the output of the amplifier is given Figure 11, where ΔP is measured to be 14dB. The ΔP measured by our BIST hardware is given in Figure 12 as a function of the number of clock cycles used to sample DC_1 and DC_2. As shown, the BIST circuitry measurement also gives a ΔP of 14dB, which agrees very well with the spectrum analyzer measurement.

Using this hardware implementation, we repeated ΔP measurements of 22dB, 28dB, and 30dB with equal accuracy to that shown in Figures 11 and 12. However, once the ΔP goes above 30dB, our BIST circuitry did not track the value measured using the spectrum analyzer due to quantization and board noise. Using an 8-bit DAC, ADC and the multiplier in the ORA, the test bed noise floor is limited by the quantization noise floor of 8 bits, which has an effective number of bits about 5~6 bits as we observed in the test. Thus, our BIST test is limited for cases with ΔP<30dB. Above 30dB, the BIST measured ΔP increases more slowly than the actual ΔP. For example, the BIST circuit reported a 35dB ΔP when the actual measured value from spectrum analyzer was 50dB. This is due to loss of accuracy in the least significant bits of our DAC and ADC in our system. However, the approach does facilitate a threshold measurement in that a BIST ΔP value above 30dB means that the actual ΔP value is greater than that measured while values measured to be below 30dB are accurate with respect to the actual value. Considering the PCB board noise and interface noise between FPAA, FPGA and DAC/ADC boards, we expect lower noise floor and wider measurement range when the whole BIST scheme is integrated in an ASIC.

The DDS-based TPG, test controller, and multiplier-accumulator-based ORA were modeled in Verilog along with an interface to allow PC control of the BIST circuitry and retrieval of the BIST results. The complete Verilog model is approximately 510 lines of non-commented code.

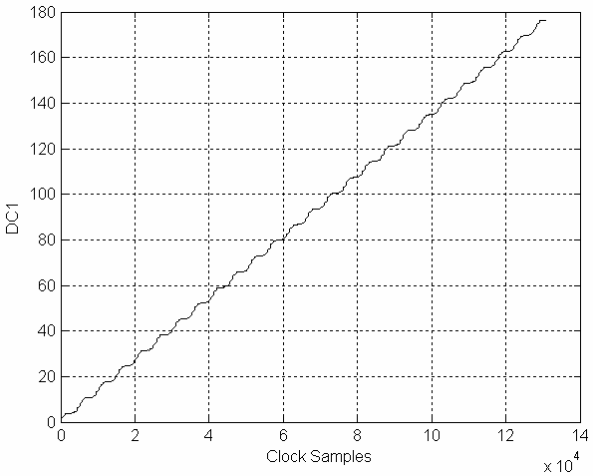


Figure 8. DC_1 accumulator value vs. clock samples.

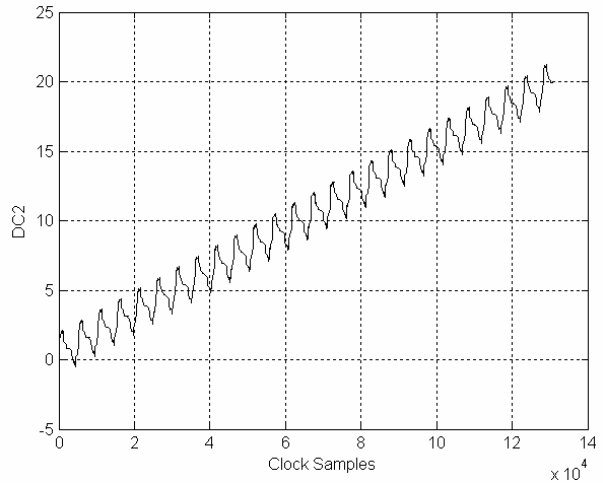


Figure 9. DC_2 accumulator value vs. clock samples.

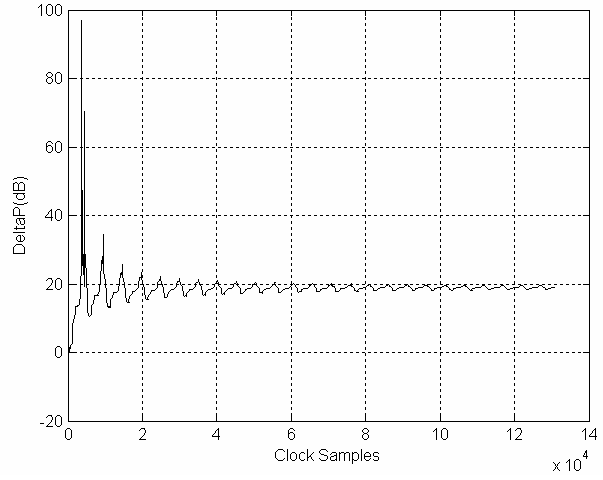


Figure 10. ΔP value vs. clock samples.

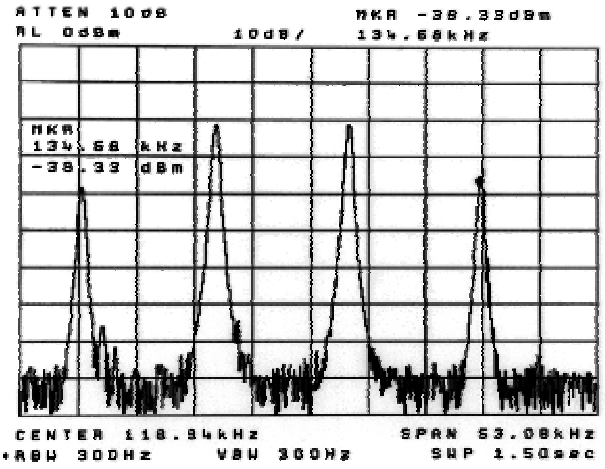


Figure 11. Spectrum analyzer measurement of two-tone test at the amplifier output.

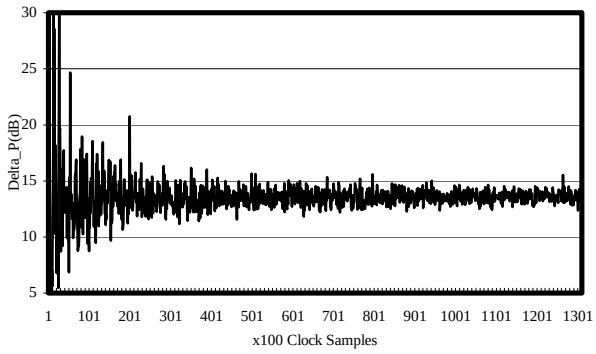


Figure 12. ΔP value vs. clock samples measured by BIST hardware.

The Verilog code can be parameterized to facilitate easy adaptation of the BIST circuitry for different size DAC and ADC for synthesis into standard cell based ASICs or into FPGAs. In our implementation, we worked with an 8-bit DAC and ADC and synthesized the BIST circuitry into a Xilinx Spartan 2S50 FPGA. Table 1 summarizes the synthesis results to give an idea of the area and performance of the complete BIST circuit. The synthesis results are given for two possible implementations. The first implementation includes two multipliers and two accumulators such that DC_1 and DC_2 are obtained simultaneously during the same BIST sequence. The second implementation is the one illustrated in Figure 7 where a single multiplier and accumulator are incorporated with DC_1 and DC_2 obtained during the separate but identical BIST sequences. This increases test time since the BIST sequence must be executed twice to obtain each DC value but it reduces the area overhead of the BIST circuitry by almost 50%. It should be noted that the 2S50 is a mid-sized FPGA in the Spartan II series and is the same size as the smallest Virtex FPGA. However, the 8-bit BIST circuitry will also fit in the smallest Spartan II series, the 2S15. Therefore, the size of the BIST circuitry is reasonably small with the DDS-based TPG accounting for approximately one-third of the total circuitry. Moreover, there are also area penalties for our data capture and monitor purpose, which can be eliminated for actual BIST implementation.

Table 1. Synthesis Results for IP3 BIST Circuit

FPGA Attribute	Total in FPGA	2-mult-accum		1-mult-accum	
		Used by BIST	% Usage	Used by BIST	% Usage
# Slices	768	313	40%	212	27%
# Flip-Flops	1536	218	14%	158	10%
# 4-input LUTs	1536	572	37%	390	25%
Maximum BIST Clock Frequency = 48.5 MHz					

The maximum clock frequency of the BIST circuitry is dominated by delays in the multiplier and accumulator in the ORA and can be increased by simply pipelining the ORA with additional flip-flops at the outputs of the multiplier before entering the accumulator. Since there are many more 4-input LUTs used in the BIST circuitry than flip-flops, pipelining the ORA should cause little if any increase in the FPGA utilization because most flip-flops at LUT outputs are unused in the synthesized implementation.

7. CONCLUSIONS

We have presented a DDS-based BIST approach for analog circuit functional testing including measurement of amplifier linearity. Linearity is an important measure of any amplifier performance and is normally measured by the third order inter-modulation product (IP3) under two-tone test. The DDS can be used to generate two frequency tones required in the two-tone test. And we have shown in this paper how an output response analyzer circuit consisting of a multiplier and accumulator can be used to construct the BIST approach without FFT algorithm in mixed-signal integrated circuits and systems. We have implemented the approach in Verilog which was subsequently synthesized into an FPGA and verified on actual hardware using an FPAA for the implementation of the amplifier used at the device under test. Through actual measurements in an 8-bit sample system, we found that the BIST circuitry accurately measures IP3 below 30dB and that BIST measured values above 30dB imply that the actual value is even greater. This loss of accuracy above 30dB is not a serious problem since one is typically more concerned with lower values where the amplifier is more non-linear for fault detection, manufacturing or in-system circuit characterization, and on-chip automatic compensation.

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