Built-in Self-Calibration of On-chip DAC and ADC

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***Abstract*—Linearity measurements are significant for assessing the performance of a modern mixed-signal system-on-chip. In this paper a new built-in self-test (BIST) scheme is presented for testing and calibration of on-chip high-resolution digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) for better linearity using sigma-delta modulator and low-resolution dithering DAC. Ramp signals are used as testing stimuli and responses of DAC-under-test (DUT) are measured by a first-order 1-bit sigma-delta modulator with high oversampling rate (OSR) and a low-pass digital filter for noise cancellation. A polynomial fit algorithm is used to characterize DAC and to obtain calibrating coefficients that determine whether the DUT passes or fails the test. DUT output error is compensated for by a dithering DAC with dynamic element matching (DEM) technique, which is controlled by the calibrating coefficients, to reduce the integral non-linearity (INL) error. Simulation results show that a sigma-delta modulator with effective number of bits (ENOB) equivalent to 17-bit ADC and a 6-bit low-cost dithering DAC are sufficient to calibrate a 14-bit high-resolution on-chip DAC such that the maximum INL error is reduced from 3 LSB to approximate 0.25 LSB. Testing and calibration of on-chip ADC using the same scheme is also discussed.**

***Index Terms*—BIST, Self-Calibration, Mixed-Signal Circuits, Sigma-Delta Modulator, ADC, DAC, SoC**

I. Introduction

With the rapid advancement in semiconductor technologies, system-on-a-chip (SoC) is widely used in integrated-circuit (IC) industry. The new technologies make it possible to build complicated but low cost devices with lower power consumption and higher density of gates than before. Growing functions and gate density also require single IC to handle not only digital logic but also analog signals that were conventionally kept on stand-alone chips. According to a recent report [10], global shipments of analog and mixed-signal ICs were $31.7 billion in 2005, increased to $37 billion in 2006, and may hit $67.8 billion by 2011.

Design-for-testability (DFT) architectures in mixed-signal systems are widely studied. Sometimes, techniques for digital components can be used to test the analog components [5], [9], [16], [17]. High-resolution ADCs and DACs are among the most basic parts on a mixed-signal chip and usually their accuracy could determine the overall performance of the entire system. Analog signals are transformed into digital signals before being fed to digital components and processors. Therefore, linearity and other characteristics of DAC become a bottleneck for system performance and precision.

While design-for-testability (DFT) studies for digital circuit are progressing, similar techniques for analog components are still challenging and expensive to implement and to apply for production manufacturing, especially for high-speed devices. Automatic test equipment (ATE) for mixed-signal ICs is limited and costly, time for test is lengthy and test process is inefficient partly because limited access and test capability is provided by the external equipment. As mixed-signal components play more and more important roles in digital SoC, testing for analog circuits becomes much more difficult. Built-in-self-test (BIST) has been adopted to test digital circuits for a long time and many recent studies show that BIST is also an ideal solution to test these converters.

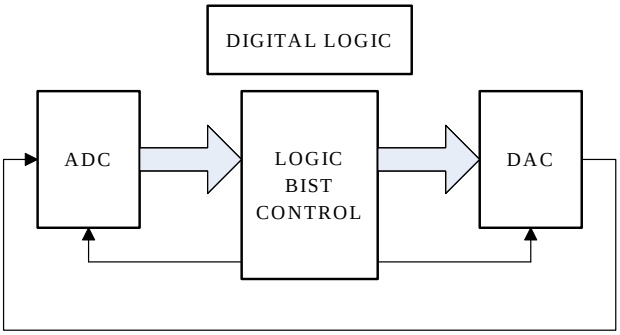

Fig. 1. A typical BIST architecture for SoC with DAC and ADC.

The major challenge in developing a BIST scheme for a mixed-signal design is generation of accurate stimulus and measurement of response from CUT. BIST must be capable of on-chip stimulus generation and usually higher-resolution devices are required to measure results. BIST circuitry has to be more accurate and faster than CUT and these factors increase difficulties in implementation. To keep controllability and observability of CUT, BIST must also work in various environments and applications.

Sigma-delta modulators [13] have high-linearity and require only a low-resolution DAC to achieve much higher precision by oversampling and noise-shaping techniques. They are easy to design and implement and require little efforts to fine tune for high linearity and resolution. With digital stimulus generation, sigma-delta technique is a promising solution for testing high-resolution on-chip DAC at low cost and overhead.

II. BIST Solutions

There were many well-studied BIST approaches proposed for mixed-signal circuits, typically shown as in Figure. 1. A

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sigma-delta modulation based BIST scheme was presented for mixed-signal circuits in [4]. Oversampling sigma-delta modulation was employed for both stimulus generation and response analysis to achieve high-quality stimuli and measurement without stringent hardware requirement. This approach also requires higher-resolution stimuli generator and multi-bit digital streams to measure the function (approximately 6dB per bit). A software based multi-bit sigma-delta encoder is used to compensate for DAC imperfections. The approach depends on software to complete the BIST and compensation and its performance is a concern. The existence of multiple sigma-delta modulator in this approach is another concern, which may increase the design complexity and overhead of BIST circuit.

Lee *et al.* [8] proposed a sigma-delta modulation based BIST scheme to concurrently generate analog sinusoidal test stimuli and digital sinusoidal reference signals. CUT is supplied the analog stimuli and then four key parameters of ADC, namely, *offset error*, *gain error*, *integral nonlinearity error* and *differential nonlinearity error*, are measured against digital reference based on sinusoidal histogram of ADC output. This approach can provide high accuracy and low chip area overhead for 8-bit ADCs. But for testing higher-resolution ADC, it may be difficult to produce analog and digital signals simultaneously and sigma-delta modulator would require more clock cycles leading to a reduce overall performance. The histogram method used in the scheme also requires much larger overhead for additional memory space for storing data. Ong *et al.* [12] give a second-order delta-sigma modulator based mixed-signal BIST architecture capable of testing/characterizing itself using all digital stimulus. Test time of the architecture is shorter than the static linear ramp testing. However, it heavily depends on DSP processor for generating digital stimulus, filtering the results from delta-sigma modulator, performing fast Fourier transform (FFT) and characterizing the modulator.

Histogram methods are also often used in some BIST schemes for DAC/ADC. Wang *et al.* [18] present a low-cost BIST based on linear histogram for testing on-chip ADC with parallel time decomposition technique to minimize area overhead and test time. Several authors [7], [19] use dithering techniques to obtain precise analog signals for high quality stimuli generation.

As some previous papers indicate, an interdependence deadlock exists in BIST schemes for DAC/ADC pair. On-chip BIST circuitry has to generate two stimuli, one of which is a digital signal for DAC and the other is an analog waveform for ADC. Output response produced by DAC requires verification from ADC, and vice versa for ADC output response. Both DAC and ADC need to be tested and verified by each other without additional components or external ATE devices, and thus the results are unreliable. To break the deadlock while keeping the design cost low, additional on-chip components to generate precise stimuli and to analyze the responses must exist.

In this paper, we propose a sigma-delta modulator based BIST scheme in which we introduce an additional low-cost low-resolution dithering DAC to test and calibrate on-chip high-resolution DAC, and then use the calibrated high-linearity DAC to test and calibrate the on-chip high-resolution ADC. Such testing method is an efficient approach [20] to test both on-chip DAC and ADC.

The test and calibration processes begin with on-chip DAC, as soon as the chip is powered up. When BIST is done the two converters have been fine-tuned to achieve high-linearity. Only digital stimuli are required in the BIST process and responses from DAC are converted to digital form by a sigma-delta modulator before being analyzed and characterized. The same digital stimuli are used to generate linear ramp signals in analog waveform by on-chip DAC, which has been calibrated in the previous step, for testing on-chip ADC and the response of ADC is then analyzed and characterized as well. Thus, expensive analog signal generation and analysis are avoided by the use of the digital BIST circuitry, which is easier to design and manufacture. The loop-back link connecting internal DAC and ADC only exists during BIST process. The overall overhead is minimal because major components of the BIST scheme are a first-order 1-bit sigma-delta modulator, a low-resolution dithering DAC and a few binary computational units.

III. Background

A. Linearity of Converters

For both DAC and ADC, the minimum measurement unit is least significant bit (LSB) that is the average voltage increment for each digital code recognized by the converters. An LSB for N-bit converter is defined as

$$LSB = \frac{v_{2^N-1} - v_0}{2^N - 1} \tag{1}$$

where $n = 2^N - 1$ is the number of such increments in total, v_0 and v_{2^N-1} are the two boundary analog value produced by the converters.

High linearity is required by both DAC and ADC to produce high-resolution and accurate outputs. The linearity can be measured and characterized by specifications like differential non-linearity (DNL) and integral non-linearity (INL) [1]. For each DAC input k, DNL is the incremental error between two consecutive codes k and $k+1$, and INL is the difference between linear fit line and actual DAC output. From these definitions, DNL and INL for code k are as follows:

$$DNL_k = \frac{v_{k+1} - v_k}{LSB} - 1 \tag{2}$$

$$INL_k = \frac{v_k - v_0}{LSB} - k \tag{3}$$

where v_k is the analog value associated with code k. INL_0 and INL_{n-1} are both 0 as defined in (3). The overall DNL and INL are the maximum values of DNL and INL for each code k,

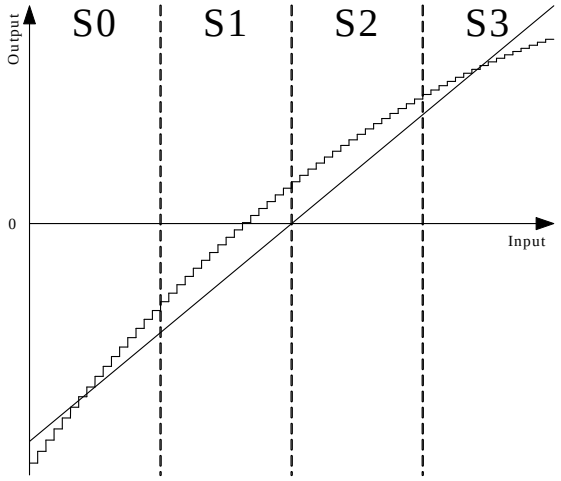

Fig. 2. A typical best fit curve for transfer function of DAC.

defined as

$$DNL = \max_k \{|DNL_k|\} \tag{4}$$

$$INL = \max_k \{|INL_k|\} \tag{5}$$

DNL and *INL* are usually calculated from the output of DAC as in (2) and (3). Because DNL_k can always be obtained by differentiating the INL_k, only *INL* measurements will be discussed in the following section.

B. Third-Order Fitting Algorithm

When histogram methods are used to test DAC and ADC to obtain *DNL* and *INL* figures, we require a huge amount of memory for storing results in such BIST schemes. Sunter and Nagi [15] proposed a simplified 3^{rd}-order polynomial-fitting algorithm for DAC and ADC BIST. Another paper [14] employed an algorithm to build a high accuracy stimulus generator for ADC BIST. It is shown in these papers that the four coefficients of a third-order polynomial that best fits the transfer function of DAC/ADC are mathematically related to four key performance parameters, namely, offset, gain, and second and third order harmonic distortions. This solution, claimed to be general, can be applied to various DAC/ADC devices, such as flash converters, delta-sigma converters and other analog circuits between DAC and ADC. Being mathematically equivalent to the least-square fit it can produce the best unbiased (linear) estimates for the coefficients by feeding converter with a linear ramp test stimulus covering the full range of conversion. The converter may work at full speed to traverse the ramp stimulus and the output results are sampled by a measuring device. The full range of conversion is divided into four equal interval segments, as shown in Figure 2. The samples at each segment are accumulated and the four sums are S_0, S_1, S_2, and S_3. The general third-order polynomial equation to fit converters is

$$y = b_0 + b_1 x + b_2 x^2 + b_3 x^3 \tag{6}$$

The input x is assumed to be a cosine waveform to relate the four coefficients to harmonic distortion,

$$x = A \cdot \cos(\omega t) \tag{7}$$

$$y = c_0 + c_1 \cos(\omega t) + c_2 \cos(2\omega t) + c_3 \cos(3\omega t) \tag{8}$$

where c_0, c_1, c_2, and c_3 represent DC offset, gain, and 2^{nd} and 3^{rd} harmonic distortions, respectively.

We assume the following four syndromes from combination of sums:

$$B_0 = S_3 + S_2 + S_1 + S_0 \tag{9}$$

$$B_1 = S_3 + S_2 - S_1 - S_0 \tag{10}$$

$$B_2 = S_3 - S_2 - S_1 + S_0 \tag{11}$$

$$B_3 = S_3 - 3S_2 + 3S_1 - S_0 \tag{12}$$

One can derive [15] four coefficients for the best fit polynomial from the syndromes:

$$b_0 = \frac{1}{N}\left(B_0 - \frac{4}{3}B_2\right) \tag{13}$$

$$b_1 = \frac{4}{N \cdot n}\left(B_1 - \frac{4}{3}B_3\right) \tag{14}$$

$$b_2 = \frac{16}{N \cdot n^2} \cdot B_2 \tag{15}$$

$$b_3 = \frac{128}{3 \cdot N \cdot n^3} \cdot B_3 \tag{16}$$

The characteristics of converters are derived from the syndromes as well:

$$c_0 \approx \frac{B_0}{n} \quad \text{Offset} \tag{17}$$

$$c_1 \approx \frac{4B_1}{N \cdot n} \quad \text{Gain} \tag{18}$$

$$c_2 \approx \frac{B_2}{B_1} \quad 2^{nd}\text{harmonic} \tag{19}$$

$$c_3 \approx \frac{2B_3}{3B_1} \quad 3^{rd}\text{harmonic} \tag{20}$$

where N is the total number of samples and n is the range of the converter ($A = n/2$, $n = 2^N$). The approximated equations are accurate if the number of samples is large enough (typically greater than 1000, i.e., equals or exceeds 10 bits).

This solution is important because it provides a simple method to determine the characteristics of converters and to estimate the analog value for each code by a best-fitting 3^{rd}-order polynomial equation. By evaluation the harmonic coefficients that are calculated by accumulating samples of each segment, this technique allow us to quickly identify *INL* figures and determine whether or not the converter fails the test. Furthermore, the coefficients give us a general idea of actual linearity of the converter-under-test.

In this paper, we apply a similar 3^{rd}-order polynomial algorithm to evaluate INL_k, the difference between linear ideal value and the actual measurement for code k, rather than analyzing output measurement. Thus *INL* value for each digital code can be asserted immediately using the polynomial.

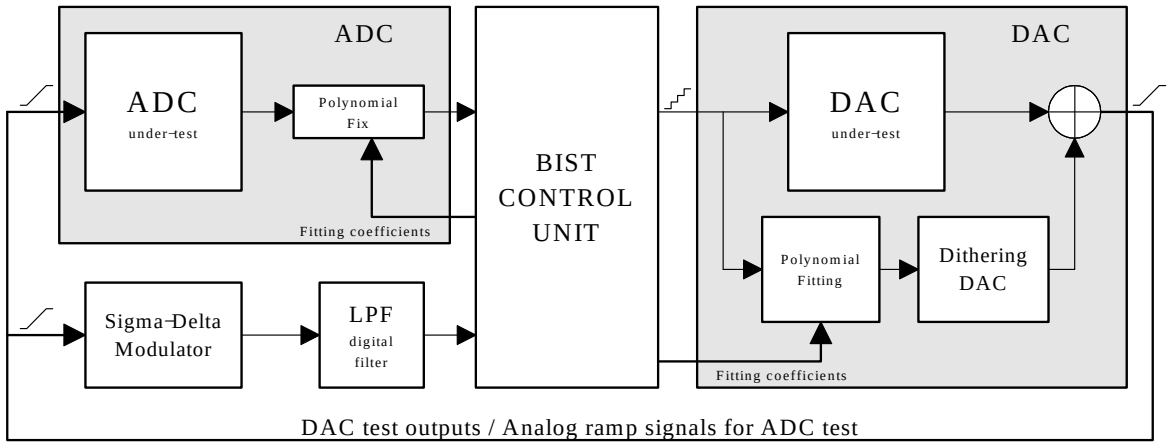

Fig. 3. Proposed BIST scheme for test and calibration of DAC and ADC.

The limited range of *INL* magnitude makes it possible to employ a low-resolution DAC to recover the *INL* value and compensate for such error in a high-resolution on-chip DAC.

IV. Overview of Proposed BIST Scheme

Requirements for on-chip DAC and ADC in mixed-signal SoC usually include resolution, linearity, and converting speed at reasonable cost of design and manufacture. Converters with higher performance may sharply increase the cost of production, which depends on the design and process technology. The proposed BIST scheme, as depicted in Figure 3, demonstrates a feasible solution to achieve improved linearity using dynamic compensation by a low-cost DAC without penalty on the speed of operation. The BIST circuitry includes a measuring ADC built from 1^{st}-order 1-bit sigma-delta modulator, a low-resolution dithering DAC, and some simple 3^{rd}-order digital function logic. A DSP-based BIST control logic provides the core functionality of the scheme that generates test stimuli for both on-chip DAC and ADC, gathers response from ADCs, determines status of conversion and configures the dithering DAC to calibrate the on-chip conversion to achieve higher linearity.

The sigma-delta modulator, shown in Figure 4 can achieve very high linearity through oversampling and noise shaping techniques and it is inexpensive to design and manufacture [13]. The noise figure of this sigma-delta modulator is basically 1-bit random quantization error that occurs during conversion of analog signals to digital signals. By oversampling and filtering, the signal-to-noise ratio (SNR) of such a modulator is increased to achieve a lower noise floor and wider dynamic range. Noise-shaping acts as a high-pass filter for the quantization noise and thus further reduces the noise figure in the lower band, up to half of sampling frequency (Nyquist frequency), further improving the SNR.

The cost of the scheme is minimal, because only major overheads to the system are the sigma-delta modulator and

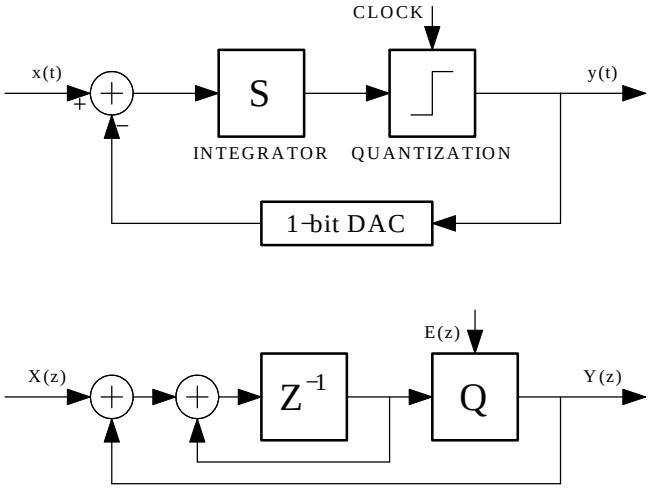

Fig. 4. Principle of sigma-delta modulator and transfer function in z-domain.

low-resolution DAC that do not have strict performance requirements and therefore are easy to design and occupy small chip area. The BIST circuitry itself is more fault-tolerant than other mixed-signal parts due to less stringent requirements on its operational performance.

Sometime following the system power up, the BIST circuitry for DAC/ADC starts the test and calibration procedures. This can begin immediately upon completion of digital BIST which would have tested the digital components of the mixed-signal chip. Loop-back interconnection between output of on-chip DAC and input of two ADCs is established once the procedure begins and we keep the connection until the test is completed.

The on-chip DAC is tested first by test stimulus generated by BIST control unit as consecutive digital codes covering the full operating range with 2^N codes for N-bit DAC. The output response of DAC is sampled and converted by the sigma-delta

ADC to a digital code. Then, according to the least-square fitting algorithm described above, the characteristics of DAC is be obtained by calculating the four coefficients from an accumulation of the digitalized responses. The four computed coefficients are compared to the pre-stored references in order to determine whether DAC passes or fails in terms of linearity. A pass for DAC here means that the characteristics of the DAC is in the predefined range within which a dithering DAC can be used to compensate its output for linearity. A fail for DAC means that the DAC cannot meet design requirements according to the comparison results and is beyond the compensating ability of the dithering DAC. If DAC passes the test, a fitting curve of *INL* error using the calculated coefficients can be obtained and DAC output can be determined as well as the quantization error for each code introduced by DAC. The *INL* and parameters for the quantization error are stored into dithering DAC to generate proper compensation signal that will be added into the output of the on-chip DAC to eliminate the non-linearity. Since the value range of quantization error is much narrower than the full range of DAC output, we can use *INL* as the reference voltage for the dithering DAC to generate compensation signals with very fine granularity although the dithering DAC itself has low-resolution. For given on-chip DAC and maximum *INL* error tolerance, the parameters of the sigma-delta modulator and resolution of dithering DAC are determined. Typically, a 17-bit measuring ADC and a 6-bit dithering DAC are sufficient to calibrate a 14-bit DAC with maximum 3 LSB *INL* error.

After on-chip DAC is tested and calibrated, BIST circuitry then uses the calibrated DAC to test the on-chip ADC by again feeding the same consecutive digital codes into DAC, transmitting analog signal output into the ADC input and, finally, reading conversion results from ADC. ADC is characterized using the same fitting algorithm shown above and another set of four coefficients is obtained to determine whether the ADC passes or fails the test by comparing them to prespecified coefficients. A 3^{rd}-order best-fit curve can be obtained if *INL* figures fall within the prespecified operational range. Then, *INL* error can be evaluated by the curve and removed from ADC outputs to fix final digital codes.

If both DAC and ADC pass tests and get calibrated by their respective polynomial fit algorithms, the BIST procedure is completed and therefore the internal connection between the output of the DAC and the input of ADC is eliminated and the sigma-delta modulator is disabled. The two sets of coefficients calculated during BIST procedures are saved for fitting polynomials to compensate the outputs in the normal operation. This compensation remains in effect until the circuit is powered down. On subsequent power up the test and calibration are again initiated.

V. Test and Calibration of DAC

This section describes details of the proposed BIST scheme to generate digital stimulus, to measure DAC outputs and to calculate parameters that determine the performance of DAC and control the dithering DAC for calibration. To test on-chip DAC, as shown in Figure 5, BIST control unit generates a series of consecutive digital codes (corresponding analog voltage v_k) from the lowest value (v_0) to the highest value (v_{n-1}) and uses sigma-delta modulator to sample the output of DAC ($\hat{v}_k$).

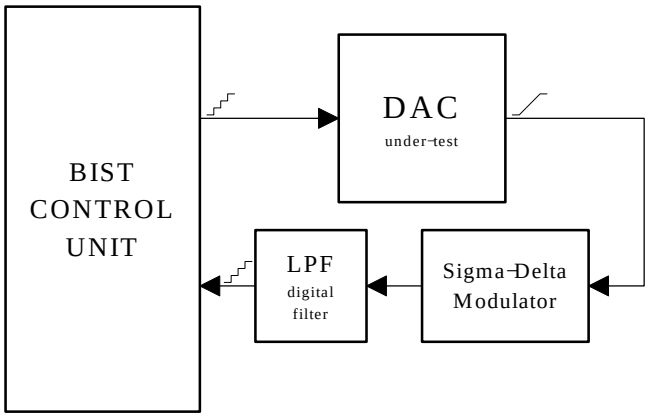

Fig. 5. Test circuitry of DAC.

$$\hat{v}_k = v_k + q_k + \hat{q}_k \tag{21}$$

where q_k is the quantization error of the on-chip DAC and $\hat{q}_k$ that of sigma-delta ADC. $\hat{k}$ is captured at the output of the sampling sigma-delta ADC for each input code k. For an accurate measurement, $\hat{k}$ must contain more effective number of bits (ENOB) than that in k. The ENOB of *hatk* is determined by the oversampling ratio K, and requires higher K to obtain larger ENOB and better resolution. Thus, the total quantization error for each code k is

$$\varepsilon_k = \hat{v}_k - v_k = q_k + \hat{q}_k \tag{22}$$

$\hat{q}_k$ is small enough to be ignored with high oversampling ratio K and thus the quantization error is mainly from the on-chip DAC. The dithering DAC will then eliminate ε_k from the DAC output for normal operation and output linearity can be further improved by employing a dynamic element mismatching (DEM) technique. Because of large number of ε_k for each code k, (2^N in total for N-bit DAC), it requires a huge amount of memory to store the compensation data for every code, thus the 3^{rd}-order best fit algorithm shown above is used to reduce memory consumption. On the other hand, the quantization error ε_k for each code k also satisfies the requirements for the polynomial fitting algorithm. Applying the fitting algorithm to *INL* error ε_k, rather than result $\hat{v}_k$ obtained from sigma-delta modulator as [15] proposed, will make it easier for dithering DAC to generate compensation signals. The consecutive codes from v_0 to v_{n-1} are divided into four equal-size segments and quantization errors ε_k in each segment are summed up to get four fundamental sum

values:

$$S_0 = \sum_{k=0}^{n/4-1} \varepsilon_k = \sum_{k=0}^{n/4-1} (\hat{v}_k - v_k) \quad (23)$$

$$S_1 = \sum_{k=n/4}^{n/2-1} \varepsilon_k = \sum_{k=n/4}^{n/2-1} (\hat{v}_k - v_k) \quad (24)$$

$$S_2 = \sum_{k=n/2}^{3n/4-1} \varepsilon_k = \sum_{k=n/2}^{3n/4-1} (\hat{v}_k - v_k) \quad (25)$$

$$S_3 = \sum_{k=3n/4}^{n-1} \varepsilon_k = \sum_{k=3n/4}^{n-1} (\hat{v}_k - v_k) \quad (26)$$

where $n = 2^N$ is the total value range for the N-bit on-chip DAC. The syndromes and coefficients of the best fit polynomial for ramp signal are calculate from these four sum values using (9) through (12) and (13) through (16), respectively. With these coefficients, representing offset, gain, and 2^{nd} and 3^{rd}-order harmonic distortions by calculating quantization error, we can construct a best fitting curve that has least square error. We use (6) and (8) to replace the actual quantization errors by both DAC and sigma-delta ADC. To achieve even higher linearity of ε_k, the ENOB of sigma-delta ADC shall be larger than number of bits in the DAC, usually at least 3 more effective bits, though test time would be slightly longer. The reference voltage of the dithering DAC can be the maximum *INL* error for the on-chip DAC in theory and usually 3 LSB is used for this dithering range to guarantee the full compensation for a low quality on-chip DAC. Because of spurious factor introduced by the dithering DAC to the final result of on-chip DAC, a low-pass filter must be used to filter out any high frequency noise.

A. Test Preparation

Digital components of SoC have their own BIST architecture and all those parts are assume to have passed their tests before the proposed mixed-signal BIST scheme takes effect because the test and self-calibration procedures require digital control logic to generate digital code as test stimuli, measure ADC outputs and calculate parameters for the dithering DAC. The digital BIST architecture is beyond the discussion of this paper and may be found elsewhere [1]. After digital BIST is done, the proposed mixed-signal BIST scheme generates codes for the on-chip DAC inputs in the form of a digitized ramp test signal. Meanwhile, the dithering DAC is disabled and produces no compensation signal for the on-chip DAC whose output is measured by the 1^{st}-order 1-bit sigma-delta modulator. Any output from the on-chip ADC is not considered at this time because it will be tested only after the DAC test.

B. Sigma-Delta Modulator

A 1^{st}-order 1-bit sigma-delta modulator is now used to sample the on-chip DAC output. This provides a low-cost measuring method with high linearity. As shown in Figure 4, the first order sigma-delta modulator consists of a integrator, a quantizer and a 1-bit DAC. Although higher order or multi-bit sigma-delta modulators are faster and achieve higher resolution, 1^{st}-order 1-bit sigma-delta modulator is more stable and has better linearity [11]. Signal-noise-ratio (SNR) of conventional N-bit DAC/ADC is calculated by:

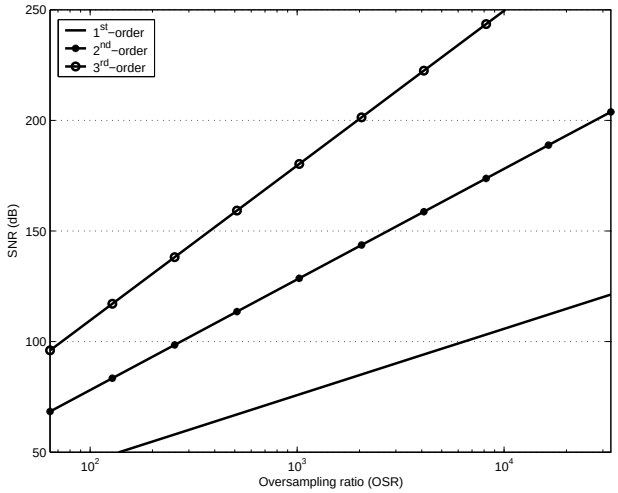

Fig. 6. SNR vs. oversampling ratio (OSR) for sigma-delta modulator.

$$\begin{aligned} \text{SNR} &= 20\log\left(\frac{\text{RMS Signal}}{\text{RMS Noise}}\right) \\ &= 6.02N + 1.76 \end{aligned} \quad (27)$$

The SNR is about 86dB for a 14-bit on-chip DAC and the measuring ADC must be of higher resolution to attain precision.

Since sigma-delta modulator has only 1-bit quantizer, the signal to 1-bit quantization noise ratio is about 7.78dB as given by (27). Oversampling improves the overall SNR by using a much higher sampling frequency f_s and distributing the white noise power over the range of the Nyquist frequency $f_s/2$. Doubling the sampling frequency will decrease the in-band quantization noise figure by 9dB for the first-order sigma-delta modulator [2], i.e., 9dB per octave improvement for SNR. So we can estimate SNR of 1^{st}-order 1-bit sigma-delta modulator by its sampling frequency f_s:

$$SNR = 7.78 + 30\log_{10}\frac{f_s/2}{f_0} \quad (28)$$

where f_0 is the upper frequency or bandwidth of the input signal and f_s/f_0 is defined as the oversampling ratio (OSR), as shown in Figure 6. If sampling frequency f_s is much greater than f_0, the total quantization noise will still be the same but will be spread over a wider spectrum so that quantization noise in signal band is significantly reduced.

The integrator in the sigma-delta modulator is also called noise-shaping filter because it moves much of the quantization noise to a higher band of frequencies such that a very low noise figure is obtained in the band of interest. We can perform a

z-domain analysis as shown in Figure 4:

$$Y(z) = z^{-1}U(z) + (1-z^{-1})E(z) \tag{29}$$

where $E(z)$ is the z-domain transfer function of the quantization error $e(k)$ introduced by 1-bit quantizer for code k. Equation (29) shows that the sigma-delta modulator acts as a low-pass filter for the input signal and high-pass filter for quantization error. Thus, the noise figure of the modulator is shifted upwards to higher frequencies while the signals remains at lower frequency. The sigma-delta modulator outputs a bit stream of 0s and 1s that contains all necessary information from the on-chip DAC but needs filtering to eliminate high frequency noise and then conversion to digital data that could be processed and analyzed by the BIST control logic.

C. Digital Filters

Since the oversampling technique distributes the overall quantization noise from bandwidth of f_0 to $f_s/2$ by the oversampling ratio f_s/f_0 and noise-shaping acts as a high-pass filter for the quantization noise most which fall outside the signal passband, the digital filter is actually a low-pass filter that eliminates the high frequency noise and keeps the low frequency signals.

One simple method to implement the low-pass filter to extract signals is to use an accumulator that sums up the output bit-stream of the sigma-delta modulator. This accumulator acts like a $1^{st} - order$ low-pass filter with a z-domain transfer function:

$$Y(z) = \frac{1}{1-z^{-1}}Y(z) \tag{30}$$

$$= \frac{z^{-1}}{1-z^{-1}}U(z) + E(z) \tag{31}$$

Examining (31), we find that the signals in the bit-stream are extracted by the accumulator and the high frequency noise shaped by sigma-delta modulator is very low in the band of interest and therefore almost eliminated. The remaining noise in the accumulator output is only due to the 1-bit quantization error (1 LSB) while the signal is reinforced during accumulation to achieve much higher SNR.

The bit-stream generated by the sigma-delta modulator requires a smoothing process called *decimation* that eliminates redundant output data by down-sampling the bit-stream to reconstruct the input signal without distortion. A down-sampling reduction ratio M means that the sampling rate of the bit-stream is reduced by a factor M, equivalent to picking up one of every M samples from the stream to reconstruct the input signal and discard the rest of the samples. No signal information will be lost during the down-sampling process provided that decimation data rate is more than twice the signal band width f_0. Digital filter using decimation will minimize the requirements for a high speed parallel multiplier and a large memory to store every bit of the lengthy stream. A common implementation of such decimation is comb filter, or sometimes called *sinc* filter that will also eliminate the unnecessary high frequency portions of the bit-stream. Ong *et al.* [12] give an efficient implementation of a comb filter by cascading K stages of accumulators operating at the sampling rate of the sigma-delta modulator, followed by K stages of cascaded differentiators operating at the down-sampled rate. The transfer function of the sinc filter with K stages and a down-sample ratio M has the form:

$$H(z) = \left(\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right)^K \tag{32}$$

with a frequency response:

$$\left|H\left(e^{j\omega}\right)\right| = \left(\frac{1}{M}\frac{\sin(\omega M/2)}{\sin(\omega/2)}\right)^K \tag{33}$$

The desired frequency components should be contained within the first peak of the frequency response. We also observe that larger K yields larger attenuation to frequency response and larger M yields more and thinner peaks so proper K and M should be chosen carefully to filter the desired frequency components to reconstruct the signal.

D. Dithering DAC

A deterministic dynamic element matching (DDEM) DAC is used to calibrate the on-chip DAC for even better linearity because the DEM approach is able to provide high-resolution DAC output using a low-resolution DAC, i.e., DDEM DAC provides higher ENOB than its actual number of bits. The outputs of both on-chip DAC and this dithering DAC are combined together and serve as the final DAC output for each input code of the normal operation. To eliminate the unexpected spurious frequencies generated from the dynamic matching mechanism, a low-pass filter must be used to process the combined DAC outputs and to remove aliasing distortion before transmitting the analog signal off chip. The calibration method with dithering DAC is illustrated in Figure 3, which consists of four major parts: digital 3^{rd}-order function generator for calculating dithering code from input code and four fitting coefficients, DDEM DAC for converting dithering code to analog dithering signal, and LPF to filter the final combined signal.

The input code k to digital 3^{rd}-order function generator comes from the BIST control unit during self-testing step or normal DAC operation after test with N-bit width same as the code to the on-chip DAC. The function generator calculates and outputs code k' with N'-bit width for DDEM DAC which will in turn generate corresponding analog compensation signal to code k' according to the four coefficients obtained from results of DAC BIST step using the best fitting algorithm discussed earlier. From equation (6), we get:

$$k' = \left(b_0 + b_1 k + b_2 k^2 + b_3 k^3\right)\frac{2^{N'}}{2^N} \tag{34}$$

The newly generated compensation code k' goes to DDEM DAC that consists of a total of $2^{N'}$ current sources for N' bit

DAC [6]. N' is much less than N and thus the N'-bit DAC is a low resolution converter. Let us define p as the DDEM iteration number, which represents the number of samples to be generated for each DAC code k', and $q = N/p$ as the source element distance factor. A cyclic DDEM switching scheme could be applied to the elements that DAC generates, i.e., p samples of output for each input code k', by selecting and switching k' current sources such that the distance from each other is q. DAC rotates the switches that control current sources for one element clockwise after outputting each sample, so for each input code all current sources are used in certain output sample while always keeping k' switched sources to generate the desired total current. The output analog signal is obtained in a load resistor driven by the total current from k' rotating current sources. If the NOB of a DAC is N, by this dynamic element matching scheme the DDEM DAC can achieve the performance comparable to an ideal DAC with $(N + \log_2 p)$-bit resolution and the element mismatch is quite tolerable so that minimum sized current elements are used and the cost of manufacture is reduced.

The reference voltage $V_{ref}^{'}$ for the DDEM DAC is not necessarily same as that of N-bit on-chip DAC V_{ref}. In fact, $V_{ref}^{'}$ is much less than V_{ref} for a fine compensation of the DAC output for better linearity. We have,

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{35}$$

$$V_{ref}^{'} = \pm\alpha \cdot \frac{V_{LSB}}{2} \tag{36}$$

where 2^N is the total number of digital codes and α is a fault tolerance factor. α determines the maximum allowable INL error in the on-chip DAC, i.e., the maximum deviation from an ideal linear DAC output. A DAC with INL error no more than $\alpha/2$-LSB will be considered "good" for calibration, otherwise, the DAC will fail the test. Different values of α could be assigned for different applications and to different SoCs to satisfy varying requirements of fault tolerance. Greater fault tolerance factor α gives more tolerance to on-chip DAC but results in degraded linearity for the calibrated DAC.

For a specified application and the corresponding factor α, we make a tradeoff between the resolution of dithering DAC and the OSR of sigma-delta modulator, as shown in Figure 7. Higher the resolution of the dithering DAC, more complex will be the design. However, a low-resolution dithering DAC requires more SNR for the sigma-delta modulator and higher OSR, which takes more clock cycles to sample the DAC output. Considering the tolerance factor α, LSB for N-bit on-chip DAC and N'-bit dithering DAC, the minimum ENOB of sigma-delta modulator is:

$$\hat{N} = N + N^{'} - \alpha \tag{37}$$

VI. Test and Calibration of ADC

After the DAC is tested and calibrated, it can be used as a precise analog test signal generator to generate a highly linear ramp signal for ADC test. During on-chip ADC test, the sigma-delta ADC is disabled and the BIST control unit feeds ramp signals v_k generated by DAC for consecutive codes k into the ADC and obtain conversion results $\hat{v}_k$ at the ADC output. Using a similar scheme as described in the previous section, the best fit algorithm is used to process the quantization error $\hat{v}_k - v_k$ and four coefficients are calculated from the sum of four equally divided segments of all ramp codes. A digital function generator is used with these four coefficients to calculate corrective number $k - \hat{k}$ to fix the quantization error for each ADC output code $\hat{k}$ corresponding to the analog signal $\hat{v}_k$.

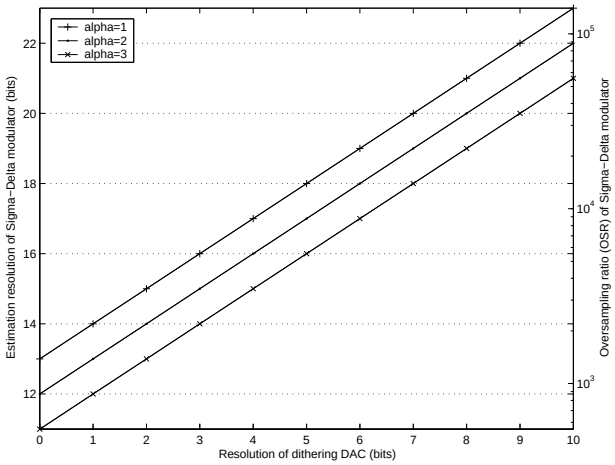

Fig. 7. Minimum oversampling ratio (OSR) of first-order sigma-delta modulator, determined by resolution of dithering DAC, for a 14-bit on-chip DAC with various fault tolerance factors, (α).

VII. Simulation Results

The proposed testing and calibration approach is verified by simulation in Matlab with a 14-bit on-chip DAC and ADC model with various quantization noise levels. A 6-bit low-cost dithering DAC model is used in the simulation to generate the compensating analog signal for DAC calibration. The fault tolerance factor is chosen 3 LSB, which is suitable for most kinds of DACs.

To measure 14-bit DAC with 3 LSB fault tolerance and to require 0.25 LSB maximum INL error in the calibrated output, the sigma-delta modulator must have 17 bits of resolution according to (37). From (27), SNR of this 17-bit ENOB sigma-delta modulator is [3]:

$$SNR = 6.02ENOB + 1.76 = 104.1dB \tag{38}$$

We assume that the oversampling rate (OSR) for the modulator is M,

$$M = \frac{f_s/2}{f_0} = \frac{f_s}{2f_0} \tag{39}$$

where f_s is the sampling frequency of the modulator and f_0 is the upper signal frequency of the input signal. The SNR for

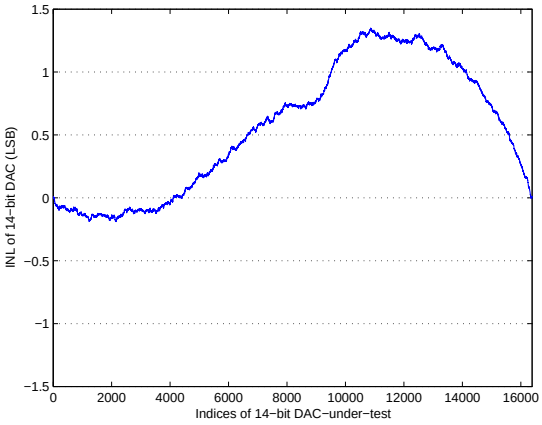

Fig. 8. *INL* of simulated 14-bit DAC-under-test.

TABLE I
THIRD-ORDER POLYNOMIAL FIT FOR *INL* OF FIGURE 8.

Sums	Syndromes	Coefficients
$S_0 = -0.4436 \times 10^3$	$B_0 = 9.0472 \times 10^3$	$b_0 = 0.7958$
$S_1 = 1.5446 \times 10^2$	$B_1 = 6.8453 \times 10^3$	$b_1 = 1.9897 \times 10^{-4}$
$S_2 = 4.4760 \times 10^3$	$B_2 = -2.9938 \times 10^3$	$b_2 = -1.0892 \times 10^{-8}$
$S_3 = 3.4703 \times 10^3$	$B_3 = -4.8803 \times 10^3$	$b_3 = -2.8897 \times 10^{-12}$

the 1^{st}-order sigma-delta modulator can be obtained as [13]:

$$n_0 = e_{rms} \frac{\pi}{\sqrt{3}} \left(\frac{1}{M}\right)^{3/2} \tag{40}$$

$$SNR = \frac{1}{n_0 \cdot 2\sqrt{2}} \tag{41}$$

$$\approx \frac{\sqrt{3}M^{3/2}}{2\sqrt{2}\pi} \tag{42}$$

Assuming $e_{rms} = 1$, the input signal RMS value is $1/(2\sqrt{2})$. We get,

$$M = \left(\frac{2\sqrt{2}\pi \cdot SNR}{\sqrt{3}}\right)^{2/3} \approx 8779 \tag{43}$$

Thus we select $2^{14} = 16384$ as the OSR used in the sigma-delta modulator, which is the closest value to satisfy 2^n. $OSR = 16384$ is sufficient for the sampled data to be recovered from the 17-bit digital output and the quantization error of the modulator can be omitted as compared to that of the on-chip DAC and dithering DAC.

Figure 8 depicts *INL* of a 14-bit DAC with maximum 1.4 LSB quantization error from simulation. The maximum *INL* magnitude is within a pre-defined range, e.g., 3 LSB in this case, so that this on-chip DAC could be calibrated. Otherwise, if any INL_k falls outside the specified range, the on-chip DAC would fail the test.

By dividing the *INL* figure into four segments of equal sizes, we obtain sums of elements for each segment: S_0, S_1, S_2 and S_3 (shown in Table I). We then calculate four syndromes: B_0, B_1, B_2, and B_4 from the sums. Finally, four coefficients, b_0, b_1, b_2, and b_3, are obtained for the polynomial fitting curve in Figure 9(a). Figure 9(b) shows about -39.3dB estimation error for the fitting algorithm.

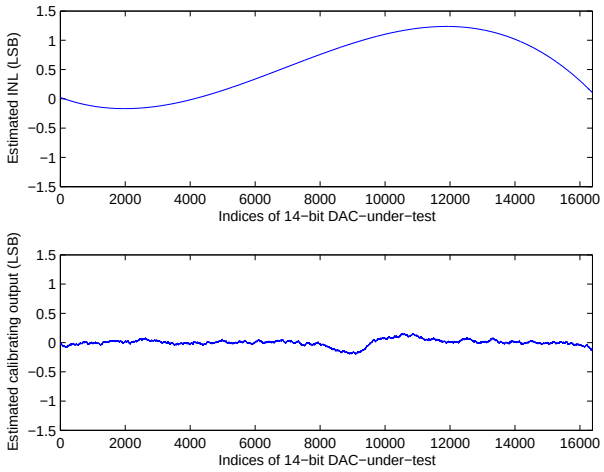

Fig. 9. Least mean-square fit for third-order polynomial (top) and estimation error (bottom) for DAC-under-test *INL* data of Figure 8.

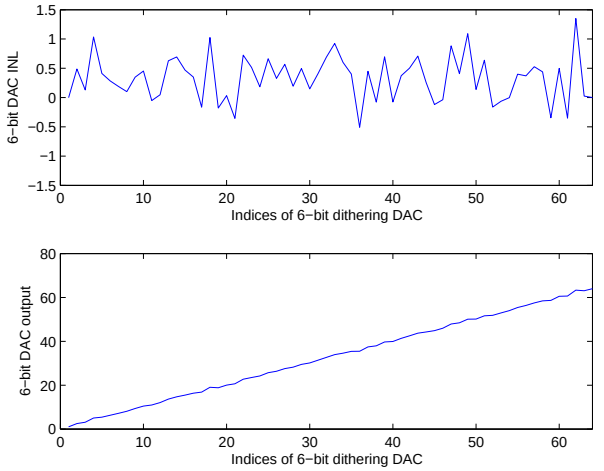

Fig. 10. *INL* (top) of simulated 6-bit dithering DAC, and DAC outputs (bottom).

Characteristics of a low-quality 6-bit dithering DAC are shown in Figure 10. The reference voltage of DAC is $\alpha/2$, typically, 1.5 LSB of DAC-under-test. Using a higher α, larger than 3 LSB, will provide large range of calibration and therefore better fault-tolerance but less calibrating precision and worse linearity. On the other hand, using an α less than 3 LSB will provide better calibration precision and better linearity of outputs but worse fault-tolerance of DAC.

The final calibrated output of the 14-bit DAC-under-test using polynomial fitting curve is shown in Figure 11. Calibrating signal is not as ideal as shown in Figure 9 and the estimation

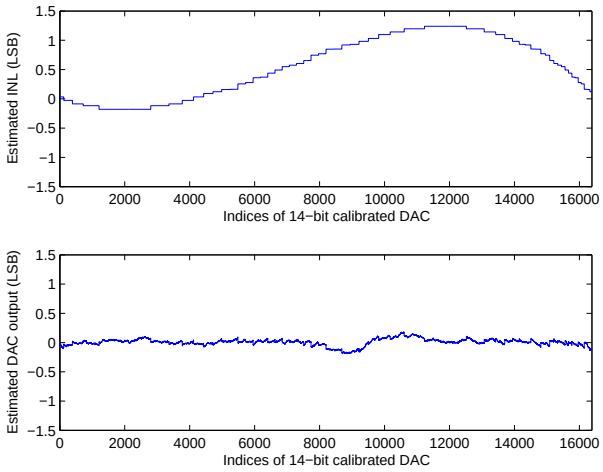

Fig. 11. *INL* (top) of calibrated 14-bit DAC-under-test using third-order polynomial fit and 6-bit dithering DAC, and the corresponding estimated *INL* error (bottom).

error is about -38.0dB. The *INL* of the calibrated DAC is not larger than 0.25 LSB compared to an ideal DAC and is reduced from a maximum of 1.5 LSB in non-calibrated output.

VIII. Conclusion

A BIST scheme for testing and calibration of on-chip DAC/ADC with a low-cost sigma-delta modulator and dithering DEM DAC is presented in this paper. A sigma-delta modulator with sufficient OSR for three or more bits of resolution is used to sample the DAC output and a third-order polynomial-fit algorithm is employed to characterize the DAC with four polynomial coefficients. Characteristics such as offset, gain, and second-order and third-order harmonic distortions are thus determined. The analog output of DAC is calibrated for higher linearity by compensation signals from dithering DAC. Similar algorithm is also used to test and calibrate the ADC for better linearity. The calibration method has been verified by simulation, which shows that with the use of a dithering DAC we can achieve improved linearity for an on-chip DAC output.

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