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Guest Editors Introduction: Special Section on Emerging Technologies in Computer Design

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The IEEE International Conference on Computer Design (ICCD) invited, for the first time in 2016, the highest ranked papers to be included in this special section of *IEEE Transactions on Emerging Technologies in Computing* (*TETC*). These papers describe original work on practical and theoretical work covering system and computer architecture, test, verification and security, design and technology, and tools and methodologies. Papers were submitted and reviewed under five tracks in ICCD 2016:

1. Computer Systems and Applications: Advanced architectures for general and application-specific enhancement; Software design for embedded, mobile, general-purpose, cloud, and high-performance platforms; IP and platform-based designs; HW/SW co-design; Modeling and performance analysis; Support for security, languages and operating systems; Hardware/software techniques for embedded systems; Application-specific and embedded software optimization; Compiler support for multithreaded and multi-core designs; Memory system and network system optimization; On-chip and system-area networks; Support for communication and synchronization.
2. Processor Architecture: Microarchitecture design techniques for uni- and multi-core processors: instruction-level parallelism, pipelining, caching, branch prediction, multithreading; Techniques for low-power, secure, and reliable processors; Embedded, network, graphic, system-on-chip, application-specific and digital signal processor design; Hardware support for processor virtualization; Real-life design challenges: case studies, tradeoffs, post-mortems.
3. Logic and Circuit Design: Circuits and design techniques for digital, memory, analog and mixed-signal systems; Circuits and design techniques for high performance and low power; Circuits and design techniques for robustness under process variability and radiation; Design techniques for emerging process technologies (MEMs, spintronics, nano, quantum, etc.); Asynchronous circuits; Signal processing, graphic processor and arithmetic circuits.
4. Electronic Design Automation: High-level, logic and physical synthesis; Physical planning, design and early estimation for large circuits; Automatic analysis and optimization of timing, power and noise; Tools for multiple-clock domains, asynchronous and mixed timing methodologies; CAD support for FPGAs, ASSPs, structured ASICs, platform-based design and NOC; DFM and OPC methodologies; System-level design and synthesis; Tools and design methods for emerging technologies (MEMs, spintronics, nano, quantum).
5. Test, Verification and Security: Design error debug and diagnosis; Fault modeling; Fault simulation and ATPG; Analog/RF Testing; Statistical Test Methods; Large volume yield Analysis and Learning; Fault tolerance; DFT and BIST; Functional, transaction-level, RTL, and gate-level modeling and verification of hardware designs; Equivalence checking, property checking, and theorem proving; Constrained-random test generation; High-level design and SoC validation. Hardware security primitives; Side channel analysis; Logic and micro-architectural countermeasures; Hardware security for IoT; Interaction between VLSI test and trust.

Upon the completion of the paper reviews by the conference technical program committee, the highest ranked papers from the regular submissions were invited to this special section for publication; these selected papers replaced publication in the ICCD proceedings. The authors presented their paper at the conference, and improved their paper based on the feedback they obtained from the paper review process and the conference audience.

It is our great pleasure to publish this special section on the highest ranked papers of ICCD 2016. This special section contains the following seven high-quality papers on diverse topics relevant to the five tracks of ICCD:

- *"Printability Enhancement with Color Balancing for Multiple Patterning Lithography," by Chen and Fang*
- *"Surviving Information Leakage Hardware Trojan Attacks Using Hardware Isolation," by Hu et al.*
- *"Cache Bypassing and Checkpointing to Circumvent Data Security Attacks on STTRAM," by Motaman et al.*
- *"Resistive CAM Acceleration for Tunable Approximate Computing," by Imani et al.*
- *"EE-SPFAL: A Novel Energy-Efficient Secure Positive Feedback Adiabatic Logic for DPA Resistant RFID and Smart Card," by Kumar et al.*

- *"A Novel Nondestructive Bit-Line Discharging Scheme for Deep Submicrometer STT-RAMs," by Zeinali et al.*
- *"Wire Length Characteristics of Multi-Tier Gate-Level Monolithic 3D ICs," by Lin and Kim*

We sincerely hope that you enjoy reading this special section, and would like to thank all authors and ICCD reviewers for their tremendous efforts and contributions in producing these high-quality articles. We also take this opportunity to thank the *TETC* Editor-in-Chief (EIC), Paolo Montuschi, Associate Editor Ramesh Karri, the editorial board, and the entire editorial staff for their guidance, encouragement and assistance in delivering this special section.

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OZGUR SINANOGLU received the BS degree in electrical and electronics engineering, and another BS degree in computer engineering, both from Bogazici University, Turkey, in 1999, he received the MS and PhD degrees in computer science and engineering from the University of California, San Diego, in 2001 and 2004, respectively. He is a professor of electrical and computer engineering at New York University Abu Dhabi. He has industry experience at TI, IBM and Qualcomm, and has been with NYU Abu Dhabi since 2010. During his PhD, he won the IBM PhD fellowship award twice. He is also the recipient of the best paper awards at IEEE VLSI Test Symposium 2011 and ACM Conference on Computer and Communication Security 2013.

Prof. Sinanoglu's research interests include design-for-test, design-for-security and design-for-trust for VLSI circuits, where he has more than 180 conference and journal papers, and 20 issued and pending US Patents. He has given more than a dozen tutorials on hardware security and trust in leading CAD and test conferences, such as DAC, DATE, ITC, VTS, ETS, ICCD, ISQED, etc. He is serving or has served as track/topic chair or technical program committee member in about 15 conferences, and as (guest) associate editor for *IEEE Transactions on Information Forensics and Security*, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *ACM Journal on Emerging Technologies in Computing*, *IEEE Transactions on Emerging Topics in Computing*, *Elsevier Microelectronics Journal*, *Journal of Electronic Testing: Theory and Applications*, and *IET Computers & Digital Techniques* journals. He is the director of the Design-for-Excellence Lab at NYU Abu Dhabi. His recent research in hardware security and trust is being funded by US National Science Foundation, US Department of Defense, Semiconductor Research Corporation, Intel Corp and Mubadala Technology.

OMER KHAN received the PhD in electrical and computer engineering from the University of Massachusetts Amherst. He is an associate professor of electrical and computer engineering at the University of Connecticut (UConn). Prior to joining UConn, he was a postdoctoral research scientist at Massachusetts Institute of Technology. He has nearly 20 years of computer architecture experience in academia and industry. At UConn, Omer leads the Computer Architecture Group, where he is developing cross-layer methods and system interfaces to improve the performance, security, and resiliency of future multicore processors. He is a member of the ACM and IEEE.