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Guest Editorial: Special Section on Emerging and Impacting Trends on Computer Arithmetic

MIOARA JOLDES, FABRIZIO LAMBERTI, (Senior Member, IEEE),
AND ALBERTO NANNARELLI, (Senior Member, IEEE)

The Computer Arithmetic field encompasses the definition and standardization of arithmetic systems for computers. It also deals with issues pertaining to hardware and software implementations, testing, and verification. Researchers and practitioners of this field also work on challenges associated with using Computer Arithmetic to perform scientific and engineering calculations. As such, Computer Arithmetic can be regarded as a truly multi-disciplinary field, which builds upon mathematics, computer science and electrical engineering. Thus, the range of topics addressed by Computer Arithmetic is generally very broad, spanning from highly theoretical to extremely practical contributions. Computer Arithmetic has been an active research field since the advent of computers, and it is progressively evolving following continuously advancements in technology.

To acknowledge the above richness, this Special Session called for submissions in a number of emerging domains of Computer Arithmetic, including innovative number systems, floating point units and algorithms, high-level language and compiler impact on arithmetic systems, approaches to test, verification, formal proof, computer aided design (CAD) automation and fault/error-tolerance for arithmetic architectures, paradigms for FPGA's or configurable logic, inexact and stochastic arithmetic, as well as efficient, low-power and novel implementations. Submissions related to new arithmetic paradigms and architectures for specific application domains such as cryptography, security, neural networks, deep learning, signal processing, computer graphics, multimedia, computer vision, distributed and parallel computing (e.g., HPC), and finance, among others, were also solicited.

The Special Section was launched jointly with the 28th IEEE International Symposium on Computer Arithmetic (ARITH 2021). Since 1969, ARITH is the premier international event for Computer Arithmetic research. For the first time, ARITH 2021 featured two categories of submissions: Journal Papers (JPs), which were scheduled to appear in this Special Session according to the publication framework known as J1C2 (Journal 1st, Conference 2nd), and Conference Papers (CPs). The two categories had separate submission, review and publication processes, and all accepted JP submissions also included an oral presentation in a regular session at ARITH 2021, like CP submissions.

The Special Section received 19 submissions, which were prescreened and reviewed by experts in the field. Five papers were ultimately accepted for publication.

The paper titled "Algorithms for stochastically rounded elementary arithmetic operations in IEEE 754 Floating-Point arithmetic" by Massimiliano Fasi and Mantas Mikaitis presents algorithms for performing the five elementary operations in floating point arithmetic with stochastic rounding, showing their value in several application domains. The proposed approach consists in emulating stochastic rounding when the underlying hardware does not support it, thus allowing for the behavior and benefits of this rounding mode to be estimated before such hardware actually becomes available. In their experiments, the authors were able to demonstrate that designed algorithms are approximately up to 20 times faster than implementations that simulate extended precision using the GNU MPFR library.

Through the work reported in the paper titled "Custom-precision mathematical library explorations for code profiling and optimization", David Defour, Pablo de Oliveira Castro, Matei Istoan, and Eric Petit aimed to study the effects and benefits of user-defined floating-point formats and target accuracies in computations that involve mathematical functions. In fact, library and hardware designers are progressively leaving the one-size-fits-all, fixed-precision approach in favor of custom-precision approaches with the aim of better coping with the increasing energy consumption and throughput requirements of scientific applications. To support this trend, the authors propose a tool that collects input data profiles in user applications and explores lower precisions for each mathematical function call in an iterative way. They demonstrate the capabilities of the devised tool on a satellite tracking application, showing how profiling data could be valuable for specializing and fine-tuning mathematic function implementations for a given application, e.g., to determine whether variable-precision designs would be actually helpful.

The authors of the paper titled "Sum propagate adders", Giorgios Dimitrakopoulos, Kleanthis Papachatzopoulos, and Vassilis Paliouras explore a new way to design binary adders. More specifically, while the basic approach still relies on the well-known carry-propagation algorithm, the authors

explore a different design that consists in performing the addition by directly propagating the sum bits of previous bit positions rather than the carries. The authors explore the design space of parallel-prefix structures that follows such a sum-propagation paradigm, and demonstrate that worst-case delay of sum-propagate adders is lower than that of carry-propagate adders due to the reduced standard deviation of maximum delay, which compensates their occasionally larger maximum delay.

In their paper titled "XpulpNN: Enabling energy efficient and flexible Inference of Quantized Neural Networks on RISC-V based IoT end nodes", Angelo Garofalo, Giuseppe Tagliavini, Francesco Conti, Luca Benini, and Davide Rossi present a multi-precision arithmetic unit integrated into a RISC-V processor for boosting the efficiency of heavily Quantized Neural Network (QNN) inference, which is getting commonplace in the deployment of Convolutional Neural Networks (CNNs) on limited-memory, low-power IoT end nodes. The authors show that their implementation can provide at least two order of magnitude improvements in performance and energy efficiency compared to state-of-the-art hardware and software solutions based on ARM Cortex-M cores, opening the way to software programmable QNN inference on the edge with ASIC-like efficiency but with higher flexibility.

Lastly, the focus of paper titled "Efficient word size modular arithmetic" by Thomas Plantard is on modular multiplication, which is used nowadays in a number of applications. While existing solutions for modular multiplication often consider large size moduli (which are especially needed in cryptography), many applications like, e.g., Residue Number System (RNS) or polynomial factorization work on moduli smaller than 32 or 64 bits. To deal with this mismatch, the author proposes a new modular multiplication schema designed to be computed on a one-word size only. The author shows that, in the majority of cases, the devised schema outperforms other existing solutions including generalist ones, like Montgomery's and Barrett's modular multiplication, as well as classes of moduli such as Mersenne, Pseudo-Mersenne, Montgomery-Friendly and Generalized Mersenne.

The topics tackled by these papers clearly show how rich and diverse Computer Arithmetic can be, hopefully indicating to interested readers possible directions for further research in this field.

On behalf of every reader of this Special Session, the Guest Editors would like to thank all the authors who submitted their papers and worked hard to respond to Reviewers' requests in due time, all the anonymous reviewers who participated in the review process providing helpful suggestions, as well as the Editor in Chief and the entire staff of IEEE Transactions on Emerging Topics in Computing who oversaw the whole process.

MIOARA JOLDES received the PhD degree from the École Normale Supérieure de Lyon, in 2011, and the habilitation degree from Toulouse III Paul Sabatier University. Since 2013, she is a permanent CNRS researcher with the Laboratory for Analysis and Architecture of Systems (LAAS-CNRS), in Toulouse, France. Her research interests include computer arithmetic, validated computing, and computer algebra. Her work received the Distinguished Paper Award at the 2019 ACM International Symposium on Symbolic and Algebraic Computation (ISSAC), the Best Paper Award at the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) in 2020 and the CNRS Bronze medal in 2021. She served as program committee member of the ACM ISSAC Symposium and of the IEEE International Symposium on Computer Arithmetic. For more information, please visit https://homepages.laas.fr/mmjoldes/

FABRIZIO LAMBERTI (Senior Member, IEEE) received the MSc and PhD degrees in computer engineering from Politecnico di Torino University, Italy, in 2000 and 2005, respectively. He is a full professor with the Dipartimento di Automatica e Informatica at Politecnico di Torino. He co-authored more than 200 technical papers in the areas of computer arithmetic, human-machine interaction, computer graphics and vision, intelligent computing and educational technologies. He is currently serving as associate editor of the *IEEE Transactions on Computers*, *IEEE Transactions on Consumer Electronics*, and *IEEE Transactions on Learning Technologies*. He is also a senior associate editor of the *IEEE Consumer Electronics Magazine* and associate editor of the *International Journal of Human-Computer Studies*. He is a member of the Board of Governors and vice-president of Technical Activities of IEEE Consumer Technology Society, as well as the vice-chair of the IEEE Computer Society's Italy Chapter. For more information, please visit http://staff.polito.it/fabrizio.lamberti/

ALBERTO NANNARELLI (Senior Member, IEEE) received the graduate degree in electrical engineering from the University of Roma "La Sapienza", Roma, Italy, in 1988, and the MS and PhD degrees in electrical and computer engineering from the University of California at Irvine, CA, USA, in 1995 and 1999, respectively. He is an associate professor with the Technical University of Denmark, Lyngby, Denmark. He worked for SGS-Thomson Microelectronics and for Ericsson Telecom as a design engineer and for Rockwell Semiconductor Systems as a summer intern. From 1999 to 2003, he was with the Department of Electical Engineering, University of Roma "Tor Vergata", Italy, as a postdoctoral researcher. His research interests include computer arithmetic, computer architecture, and VLSI design.